MC14512B

8-Channel Data Selector

The MC14512B is an 8−channel data selector constructed with MOS P−channel and N−channel enhancement mode devices in a single monolithic structure. This data selector finds primary application in signal multiplexing functions. It may also be used for data routing, digital signal switching, signal gating, and number sequence generation.

Features

- Diode Protection on All Inputs
- Single Supply Operation
- 3−State Output (Logic "1", Logic "0", High Impedance)
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low−power TTL Loads or One Low−power Schottky TTL Load Over the Rated Temperature Range
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- This Device is Pb−Free and is RoHS Compliant

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Parameter	Symbol	Value	Unit
DC Supply Voltage Range	V_{DD}	−0.5 to +18.0	V
Input or Output Voltage Range (DC or Transient)	V_{in}, V_{out}	−0.5 to V_{DD} + 0.5	V
Input or Output Current (DC or Transient) per Pin	I_{in}, I_{out}	±10	mA
Power Dissipation, Per Package (Note 1)	P_D	500	mW
Ambient Temperature Range	T_A	−55 to +125	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Lead Temperature (8−Second Soldering)	T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Temperature Derating: "D/DW" Package: −7.0 mW/°C From 65°C To 125°C
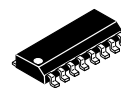
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

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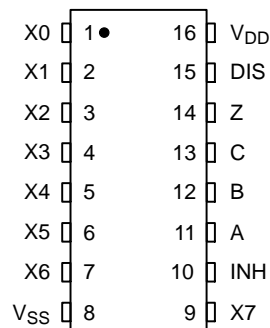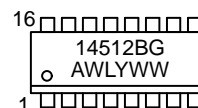**D SUFFIX**
CASE 751B

PIN ASSIGNMENT

X0	1 ●	16	V_{DD}
X1	2	15	DIS
X2	3	14	Z
X3	4	13	C
X4	5	12	B
X5	6	11	A
X6	7	10	INH
V_{SS}	8	9	X7

MARKING DIAGRAM

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14512BG
AWLYWW

1

A	= Assembly Location
WL	= Wafer Lot
YY, Y	= Year
WW	= Work Week
G	= Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

MC14512B

TRUTH TABLE

C	B	A	Inhibit	Disable	Z
0	0	0	0	0	X0
0	0	1	0	0	X1
0	1	0	0	0	X2
0	1	1	0	0	X3
1	0	0	0	0	X4
1	0	1	0	0	X5
1	1	0	0	0	X6
1	1	1	0	0	X7
X	X	X	1	0	0
X	X	X	X	1	High Impedance

NOTE: X = Don't Care

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic		Symbol	V_{DD} Vdc	−55°C Min	−55°C Max	25°C Min	25°C Typ (Note 2)	25°C Max	125°C Min	125°C Max	Unit
Output Voltage "0" Level V_{in} = V_{DD} or 0		V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
			10	–	0.05	–	0	0.05	–	0.05	
			15	–	0.05	–	0	0.05	–	0.05	
"1" Level V_{in} = 0 or V_{DD}		V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
			10	9.95	–	9.95	10	–	9.95	–	
			15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)		V_{IL}	5.0	–	1.5	–	2.25	1.5	–	1.5	Vdc
			10	–	3.0	–	4.50	3.0	–	3.0	
			15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level (V_O = 0.5 or 4.5 Vdc) (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)		V_{IH}	5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
			10	7.0	–	7.0	5.50	–	7.0	–	
			15	11	–	11	8.25	–	11	–	
Output Drive Current (V_{OH} = 2.5 Vdc) (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	Source	I_{OH}	5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	mAdc
			5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
			10	−1.6	–	−1.3	−2.25	–	−0.9	–	
			15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
			10	1.6	–	1.3	2.25	–	0.9	–	
			15	4.2	–	3.4	8.8	–	2.4	–	
Input Current		I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)		C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (Per Package)		I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
			10	–	10	–	0.010	10	–	300	
			15	–	20	–	0.015	20	–	600	
Total Supply Current (Note 3) (Note 4) (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)		I_T	5.0	$I_T = (0.8\ \mu A/kHz)\ f + I_{DD}$								μAdc
			10	$I_T = (1.6\ \mu A/kHz)\ f + I_{DD}$								
			15	$I_T = (2.4\ \mu A/kHz)\ f + I_{DD}$								
3−State Leakage Current		I_{TL}	15	–	±0.1	–	±0.0001	±0.1	–	±3.0	μAdc

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
3. The formulas given are for the typical characteristics only at 25°C.
4. To calculate total supply current at loads other than 50 pF: $I_T(C_L) = I_T(50\ pF) + (C_L − 50)$ Vfk where: I_T is in μA (per package), C_L in pF, V = ($V_{DD} − V_{SS}$) in volts, f in kHz is input frequency, and k = 0.001.

SWITCHING CHARACTERISTICS (Note 5) (C_L = 50 pF, T_A = 25°C, See Figure 1)

Characteristic	Symbol	V_{DD}	All Types		Unit
			Typ (Note 6)	Max	
Output Rise and Fall Time t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns	t_{TLH}, t_{THL}	5.0 10 15	100 50 40	200 100 80	ns
Propagation Delay Time (Figure 2) Inhibit, Control, or Data to Z	t_{PLH}	5.0 10 15	330 125 85	650 250 170	ns
Propagation Delay Time (Figure 2) Inhibit, Control, or Data to Z	t_{PHL}	5.0 10 15	330 125 85	650 250 170	ns
3–State Output Delay Times (Figure 3) "1" or "0" to High Z, and High Z to "1" or "0"	t_{PHZ}, t_{PLZ}, t_{PZH}, t_{PZL}	5.0 10 15	60 35 30	150 100 75	ns

5. The formulas given are for the typical characteristics only at 25°C.
6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

ORDERING INFORMATION

Device	Package	Shipping†
MC14512BDG	SOIC−16 (Pb−Free)	48 Units / Rail
NLV14512BDG*	SOIC−16 (Pb−Free)	48 Units / Rail
MC14512BDR2G	SOIC−16 (Pb−Free)	2500 / Tape & Reel
NLV14512BDR2G*	SOIC−16 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

MC14512B
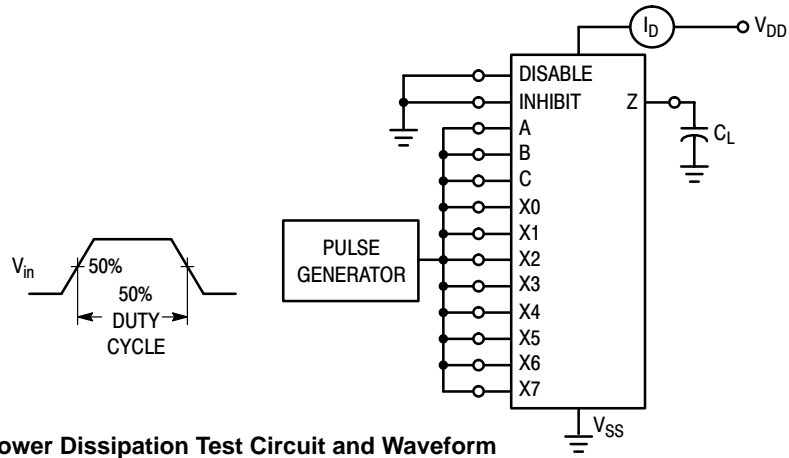
Figure 1. Power Dissipation Test Circuit and Waveform

Parameter	Test Conditions
Inhibit to Z	A, B, C = V_{SS}, X_O = V_{DD}
A, B, C to Z	Inh = V_{SS}, X_O = V_{DD}
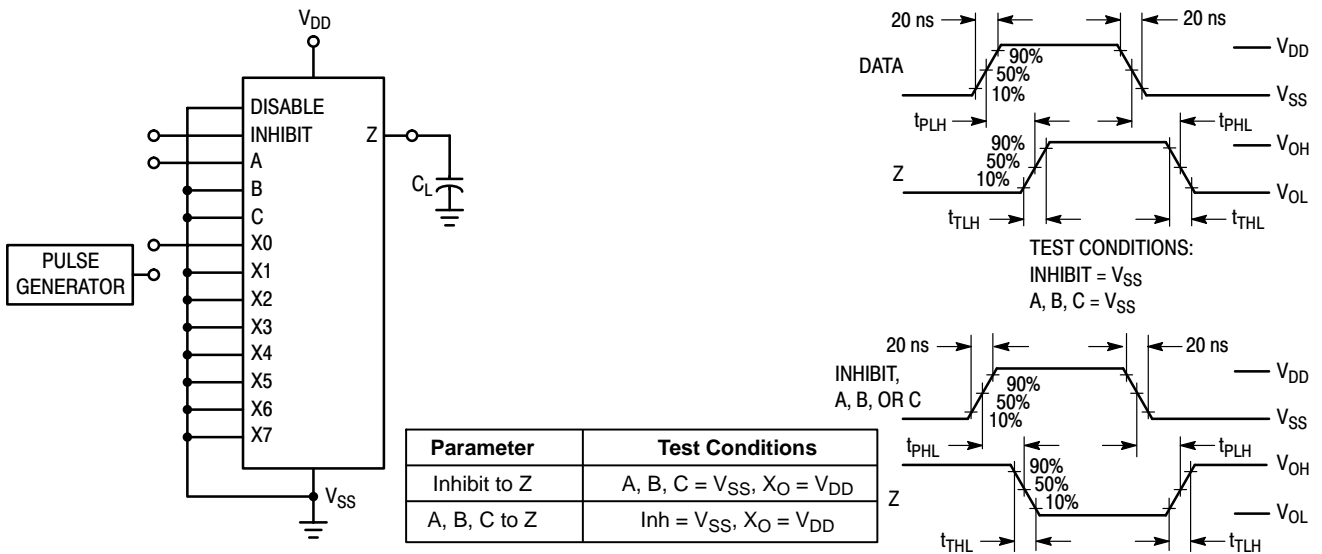
Figure 2. AC Test Circuit and Waveforms

Switch Positions for 3−State Test

Test	S1	S2	S3	S4
t_{PHZ}	Open	Closed	Closed	Open
t_{PLZ}	Closed	Open	Open	Closed
t_{PZL}	Closed	Open	Open	Closed
t_{PZH}	Open	Closed	Closed	Open
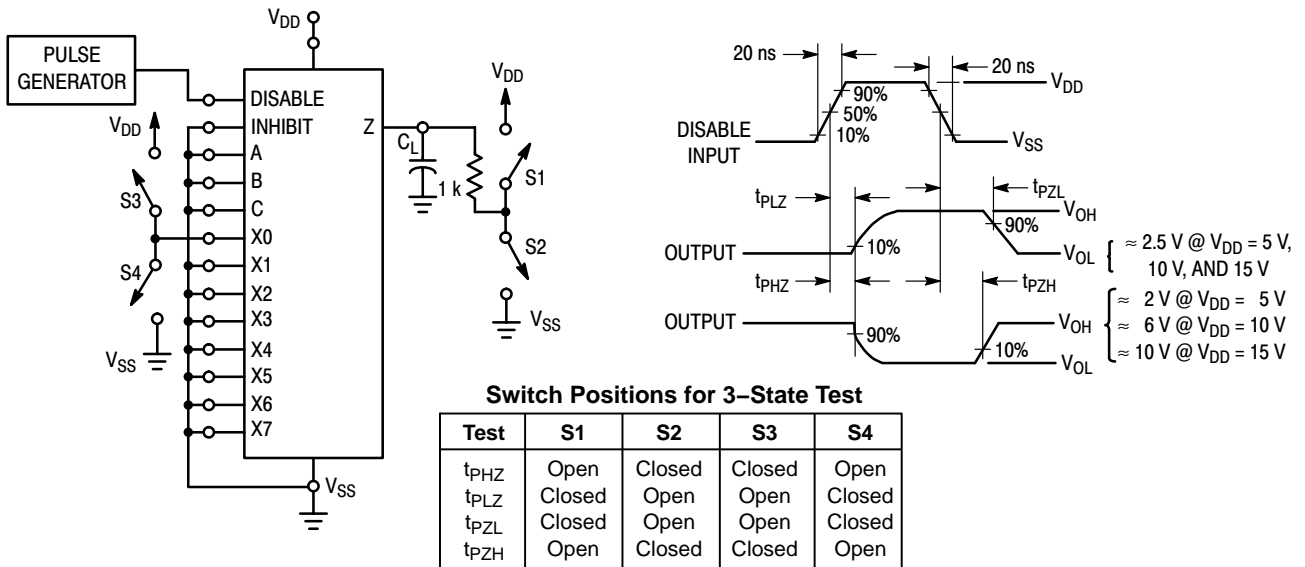
Figure 3. 3−State AC Test Circuit and Waveform

MC14512B

LOGIC DIAGRAM
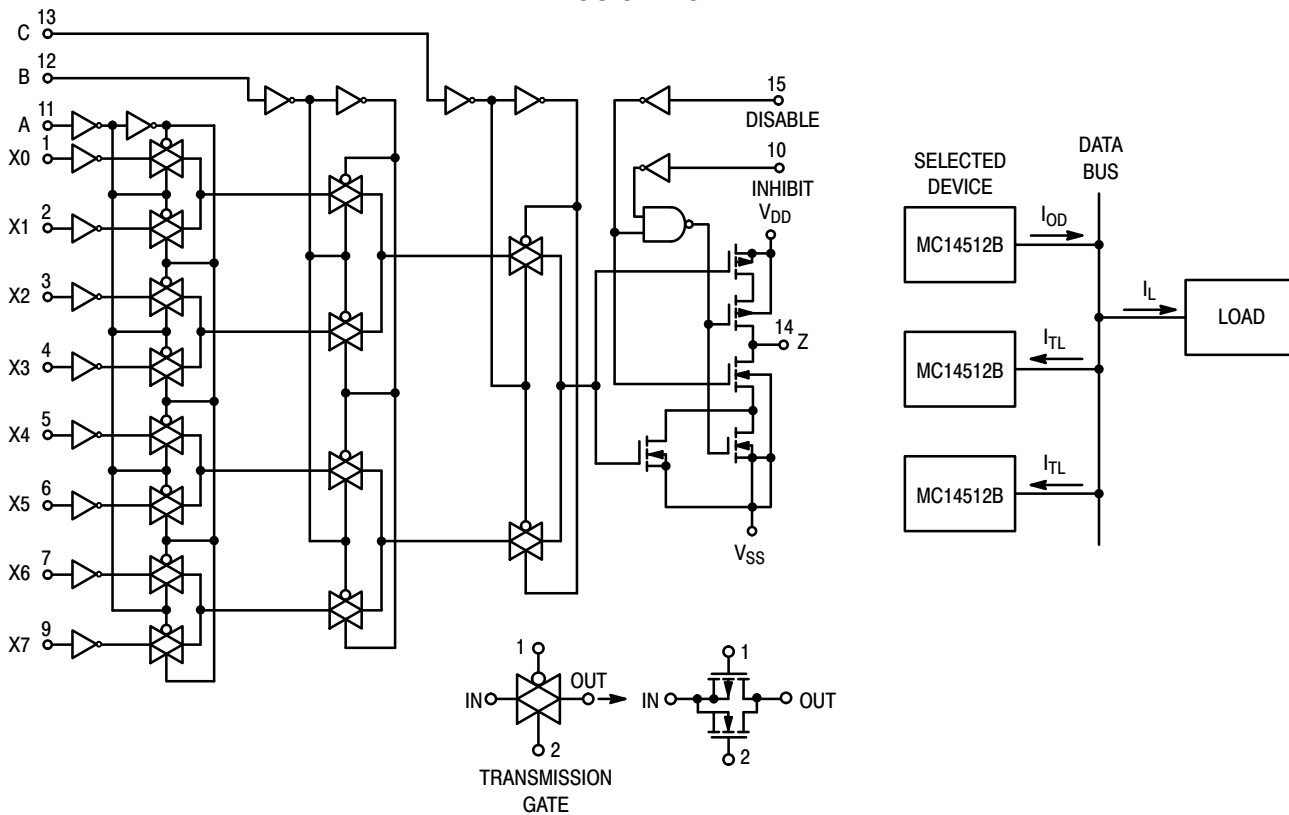
3−STATE MODE OF OPERATION

Output terminals of several MC14512B 8−Bit Data Selectors can be connected to a single date bus as shown. One MC14512B is selected by the 3−state control, and the remaining devices are disabled into a high−impedance "off" state. The number of 8−bit data selectors, N, that may be connected to a bus line is determined from the output drive current, I_{OD}, 3−state or disable output leakage current, I_{TL}, and the load current, I_L, required to drive the bus line (including fanout to other device inputs), and can be calculated by:

$$N = \frac{I_{OD} - I_L}{I_{TL}} + 1$$

N must be calculated for both high and low logic state of the bus line.
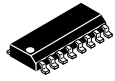
SOIC−16
CASE 751B−05
ISSUE K

SCALE 1:1

DATE 29 DEC 2006
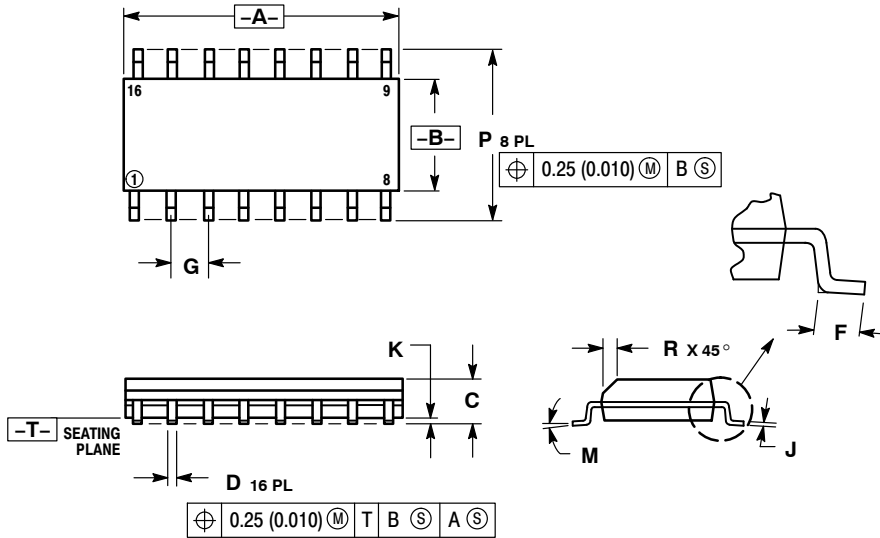
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

−A−

16   9
① ⃝   8

−B− P 8 PL

⊕ | 0.25 (0.010) Ⓜ | B Ⓢ

G

K

C

−T− SEATING PLANE

D 16 PL

⊕ | 0.25 (0.010) Ⓜ | T | B Ⓢ | A Ⓢ

R X 45°

F

M   J

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

STYLE 1:
PIN 1. COLLECTOR
    2. BASE
    3. EMITTER
    4. NO CONNECTION
    5. EMITTER
    6. BASE
    7. COLLECTOR
    8. COLLECTOR
    9. BASE
    10. EMITTER
    11. NO CONNECTION
    12. EMITTER
    13. BASE
    14. COLLECTOR
    15. EMITTER
    16. COLLECTOR

STYLE 2:
PIN 1. CATHODE
    2. ANODE
    3. NO CONNECTION
    4. CATHODE
    5. CATHODE
    6. NO CONNECTION
    7. ANODE
    8. CATHODE
    9. CATHODE
    10. ANODE
    11. NO CONNECTION
    12. CATHODE
    13. CATHODE
    14. NO CONNECTION
    15. ANODE
    16. CATHODE

STYLE 3:
PIN 1. COLLECTOR, DYE #1
    2. BASE, #1
    3. EMITTER, #1
    4. COLLECTOR, #1
    5. COLLECTOR, #2
    6. BASE, #2
    7. EMITTER, #2
    8. COLLECTOR, #2
    9. COLLECTOR, #3
    10. BASE, #3
    11. EMITTER, #3
    12. COLLECTOR, #3
    13. COLLECTOR, #4
    14. BASE, #4
    15. EMITTER, #4
    16. COLLECTOR, #4

STYLE 4:
PIN 1. COLLECTOR, DYE #1
    2. COLLECTOR, #1
    3. COLLECTOR, #2
    4. COLLECTOR, #2
    5. COLLECTOR, #3
    6. COLLECTOR, #3
    7. COLLECTOR, #4
    8. COLLECTOR, #4
    9. BASE, #4
    10. EMITTER, #4
    11. BASE, #3
    12. EMITTER, #3
    13. BASE, #2
    14. EMITTER, #2
    15. BASE, #1
    16. EMITTER, #1

STYLE 5:
PIN 1. DRAIN, DYE #1
    2. DRAIN, #1
    3. DRAIN, #2
    4. DRAIN, #2
    5. DRAIN, #3
    6. DRAIN, #3
    7. DRAIN, #4
    8. DRAIN, #4
    9. GATE, #4
    10. SOURCE, #4
    11. GATE, #3
    12. SOURCE, #3
    13. GATE, #2
    14. SOURCE, #2
    15. GATE, #1
    16. SOURCE, #1

STYLE 6:
PIN 1. CATHODE
    2. CATHODE
    3. CATHODE
    4. CATHODE
    5. CATHODE
    6. CATHODE
    7. CATHODE
    8. CATHODE
    9. ANODE
    10. ANODE
    11. ANODE
    12. ANODE
    13. ANODE
    14. ANODE
    15. ANODE
    16. ANODE

STYLE 7:
PIN 1. SOURCE N-CH
    2. COMMON DRAIN (OUTPUT)
    3. COMMON DRAIN (OUTPUT)
    4. GATE P-CH
    5. COMMON DRAIN (OUTPUT)
    6. COMMON DRAIN (OUTPUT)
    7. COMMON DRAIN (OUTPUT)
    8. SOURCE P-CH
    9. SOURCE P-CH
    10. COMMON DRAIN (OUTPUT)
    11. COMMON DRAIN (OUTPUT)
    12. COMMON DRAIN (OUTPUT)
    13. GATE N-CH
    14. COMMON DRAIN (OUTPUT)
    15. COMMON DRAIN (OUTPUT)
    16. SOURCE N-CH

SOLDERING FOOTPRINT

8X
6.40

16X 1.12

1   16

16X
0.58

1.27
PITCH

8   9
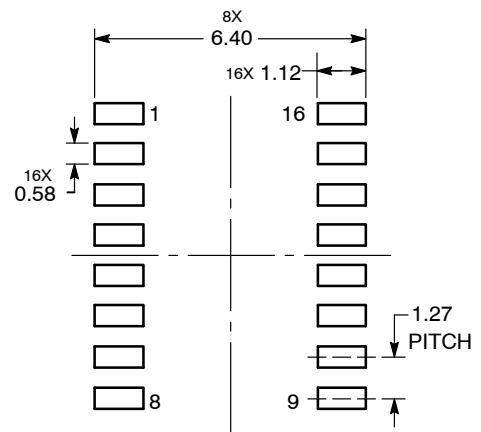
DIMENSIONS: MILLIMETERS

DOCUMENT NUMBER:	98ASB42566B	
DESCRIPTION:	SOIC−16	**PAGE 1 OF 1**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales

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