

NUP45V6P5

ESD Protection Diode Array, Quad, Low Capacitance

This integrated surge protection is designed for applications requiring transient overvoltage protection. It is intended to be used in sensitive equipment such as wireless headsets, PDAs, digital cameras, computers, printers, communication systems, and other applications. The integrated design provides very effective and reliable protection for four separate lines using only one package. This device is ideal for situations where board space is at a premium.

Features

- ESD Protection: IEC61000-4-2: Level 4
- Four Separate Unidirectional Configurations for Protection
- Low Leakage Current < 1 μ A @ 3 V
- Small SOT-953 SMT Package
- Low Capacitance
- These are Pb-Free Devices

Benefits

- Provides Protection for ESD Industry Standards: IEC 61000, HBM
- Protects Four Lines Against Transient Voltage Conditions
- Minimize Power Consumption of the System
- Minimize PCB Board Space

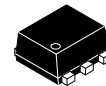
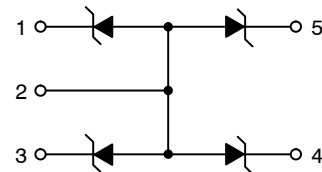
Typical Applications

- Cellular and Portable Electronics
- Serial and Parallel Ports
- Microprocessor Based Equipment
- Notebooks, Desktops, Servers



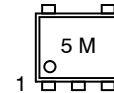
ON Semiconductor®

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SOT-953
CASE 526AE

MARKING DIAGRAM



5 = Specific Device Code
M = Date & Assembly Code

ORDERING INFORMATION

| Device | Package | Shipping† |
|--------------|----------------------|-----------------------|
| NUP45V6P5T5G | SOT-953 (Pb-Free) | 8000 / Tape & Reel |

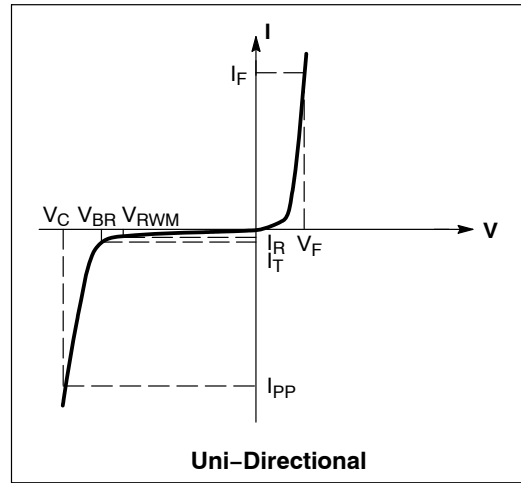
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NUP45V6P5

ELECTRICAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

| Symbol | Parameter |
|-----------------|---|
| I_{PP} | Maximum Reverse Peak Pulse Current |
| V_C | Clamping Voltage @ I_{PP} |
| V_{RWM} | Working Peak Reverse Voltage |
| I_R | Maximum Reverse Leakage Current @ V_{RWM} |
| V_{BR} | Breakdown Voltage @ I_T |
| I_T | Test Current |
| ΘV_{BR} | Maximum Temperature Coefficient of V_{BR} |
| I_F | Forward Current |
| V_F | Forward Voltage @ I_F |
| Z_{ZT} | Maximum Zener Impedance @ I_{ZT} |
| I_{ZK} | Reverse Current |
| Z_{ZK} | Maximum Zener Impedance @ I_{ZK} |



MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

| Characteristic | Symbol | Value | Unit |
|---|-----------------|-------------|----------------------------|
| Thermal Resistance Junction-to-Ambient Above 25°C , Derate | $R_{\theta JA}$ | 560 | $^\circ\text{C}/\text{W}$ |
| | | 4.5 | $\text{mW}/^\circ\text{C}$ |
| Maximum Junction Temperature | T_{Jmax} | 150 | $^\circ\text{C}$ |
| Operating Junction and Storage Temperature Range | $T_J T_{stg}$ | -55 to +150 | $^\circ\text{C}$ |
| Lead Solder Temperature (10 seconds duration) | T_L | 260 | $^\circ\text{C}$ |
| Human Body Model (HBM) Machine Model (MM) | ESD | 8000 | V |
| | | 400 | |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$)

| Device | Device Marking | Breakdown Voltage V_{BR} @ 1 mA (Volts) | | | Leakage Current I_{RM} @ V_{RM} | | Typ Capacitance @ 0 V Bias (pF) (Note 1) | | Typ Capacitance @ 3 V Bias (pF) (Note 1) | | V_C (V) @ $I_{PP} = 1$ A (Note 2) |
|-----------|----------------|---|-----|-----|-------------------------------------|-----------------------------|--|-----|--|------|-------------------------------------|
| | | Min | Nom | Max | V_{RWM} | I_{RWM} (μA) | Typ | Max | Typ | Max | Max |
| NUP45V6P5 | 5 | 5.3 | 5.6 | 5.9 | 3.0 | 1.0 | 13 | 17 | 7.0 | 11.5 | 10.5 |

1. Capacitance of one diode at $f = 1$ MHz, $T_A = 25^\circ\text{C}$.
2. Surge current waveform per Figure 3.

NUP45V6P5

TYPICAL ELECTRICAL CHARACTERISTICS

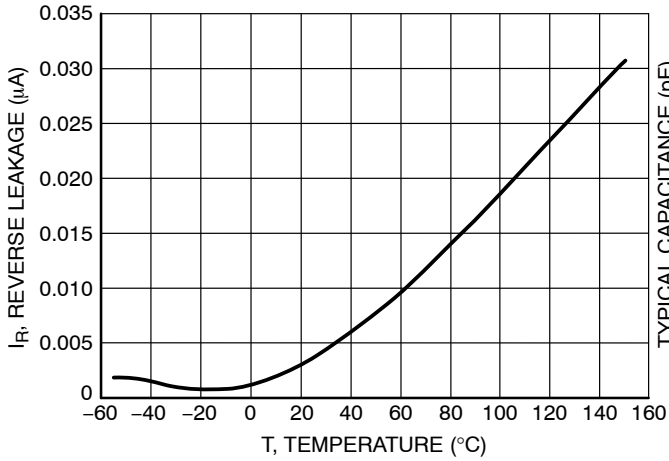


Figure 1. Reverse Leakage Current versus Temperature

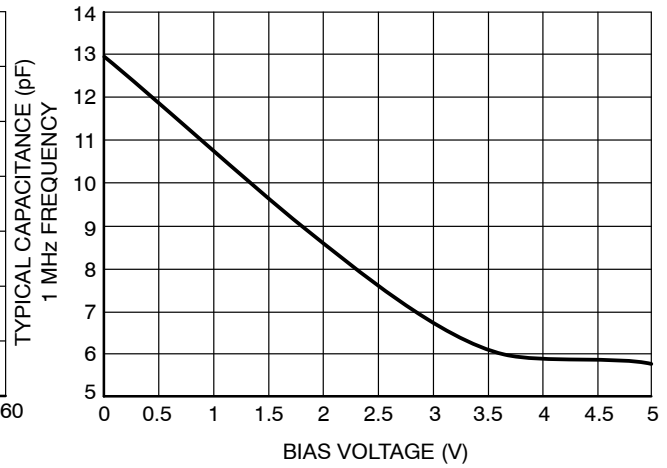


Figure 2. Capacitance

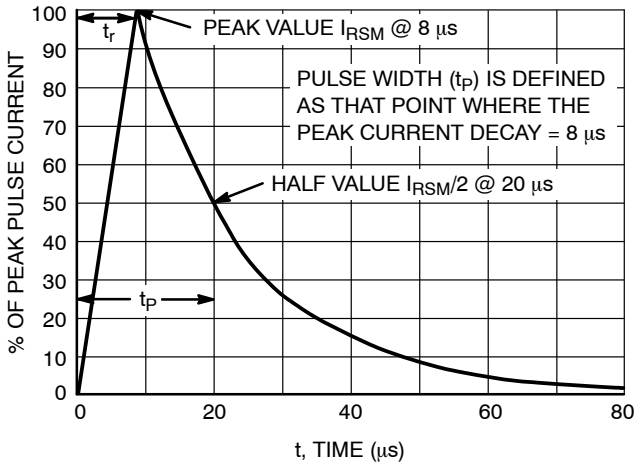


Figure 3. 8 × 20 µs Pulse Waveform

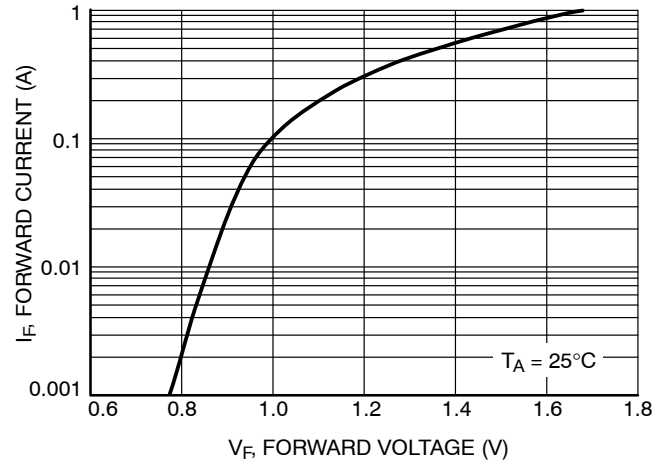


Figure 4. Forward Voltage

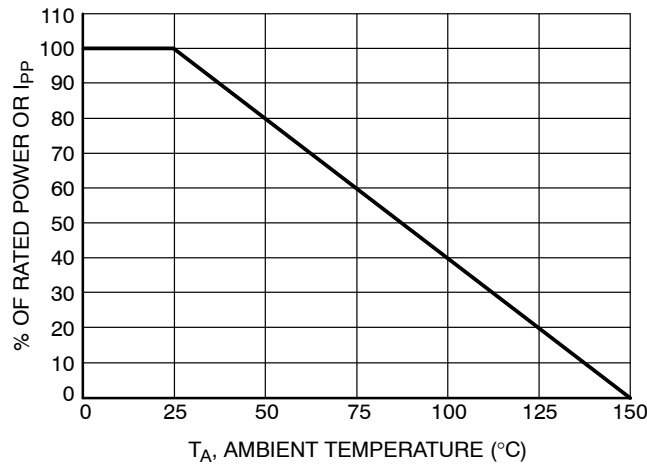


Figure 5. Power Derating Curve

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

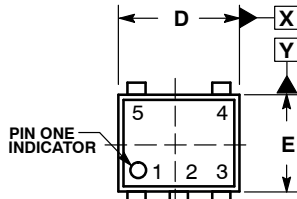
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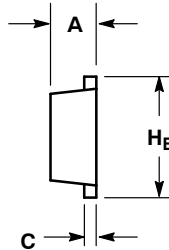
SCALE 4:1

SOT-953
CASE 527AE
ISSUE E

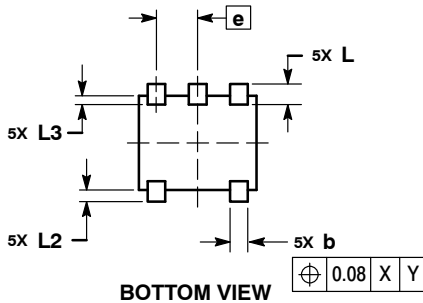
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TOP VIEW



SIDE VIEW



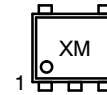
BOTTOM VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

| DIM | MILLIMETERS | | |
|----------------|-------------|------|------|
| | MIN | NOM | MAX |
| A | 0.34 | 0.37 | 0.40 |
| b | 0.10 | 0.15 | 0.20 |
| C | 0.07 | 0.12 | 0.17 |
| D | 0.95 | 1.00 | 1.05 |
| E | 0.75 | 0.80 | 0.85 |
| e | 0.35 BSC | | |
| H _E | 0.95 | 1.00 | 1.05 |
| L | 0.175 REF | | |
| L2 | 0.05 | 0.10 | 0.15 |
| L3 | --- | --- | 0.15 |

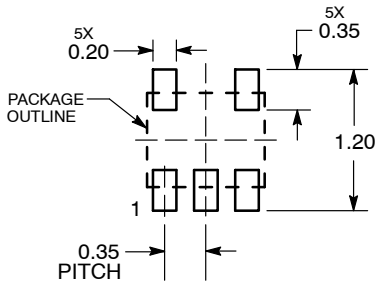
GENERIC MARKING DIAGRAM*



X = Specific Device Code
M = Month Code

*This information is generic. Please refer to device data sheet for actual part marking.
Pb-Free indicator, "G" or microdot "▪", may or may not be present.

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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