TPS65680 18-Channel Pattern-Programmable Level Shifter with Overcurrent Protection

1 Features

- Programmable Output Pattern
  - Same Hardware can Support Different Displays
  - Ideal for Nonstandard / Small-Volume Applications
  - Pattern Changes During Development are Easy to Implement
- Simple 2-Wire Interface Between Level Shifter and TCON
  - Uses Fewer TCON I/O Resources / Allows Smaller TCON Package
  - Simplifies PCB Layout
  - Same 2-Wire Interface can be Shared by Multiple Level Shifter Devices Operating in Parallel
- 12 High-Voltage Clock Outputs
- 6 High-Voltage Control Outputs
- Advanced Functionality
  - Gate-Voltage Shaping
  - Charge-Sharing
  - Low-Frequency ODD / EVEN Output Generation
  - Panel Discharge During Shutdown
  - Output Overcurrent Protection
  - Overtemperature Protection
- Wide Supply Voltage Range
  - V_{IN} Supplies from 2.7 V to 5.5 V
  - V_{GH} Supplies from 9 V to 40 V
  - V_{GL} Supplies from –4 V to –18 V
- 4-mm × 4-mm, 32-Pin QFN Package

2 Applications

- LCD Panels Using GIP / GOA / ASG Technology
  - TVs
  - Monitors
  - Notebook / Tablet PCs
  - Industrial Equipment
  - Public Signage

3 Description

The TPS65680 device is a fully programmable high-voltage level shifter solution for LCD panels. It supports up to twelve high-voltage clock outputs in either charge-sharing or gate-voltage shaping configuration and six high-voltage control outputs for generating start, clear/reset, low-frequency ODD / EVEN signals and panel discharge. The output timing is generated by the level shifter itself, based on a user-programmable pattern sequence and requires only two connections to the timing controller: a line clock and a start pulse that indicates the start of a new frame. These two signals can be shared between multiple TPS65680 devices in applications that require a higher number of output channels than one device can generate.

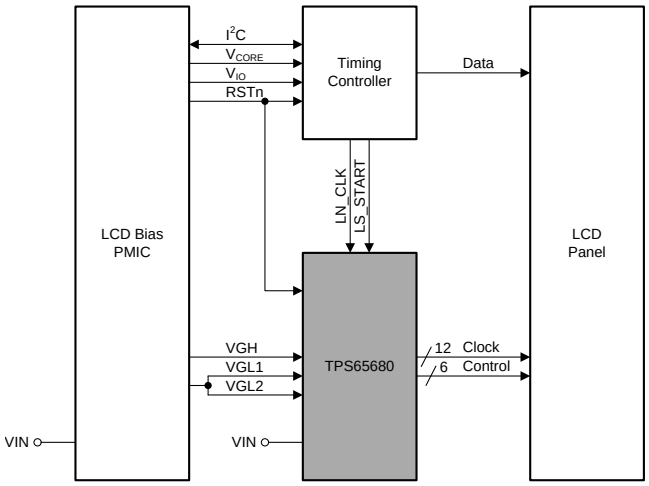
Customer-defined patterns and configuration settings can be stored in an on-chip nonvolatile memory to be used as the default settings after power up. Alternatively, this data can be written to the device after power up, using the I^2C interface. The programmability of the TPS65680 device lets you change the output pattern without reprogramming or changing the TCON. Thus one PCB can support many different panels, which simplifies the system design, shortens the design cycle and enables economies of scale.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS65680	WQFN (32)	4.0 mm × 4.0 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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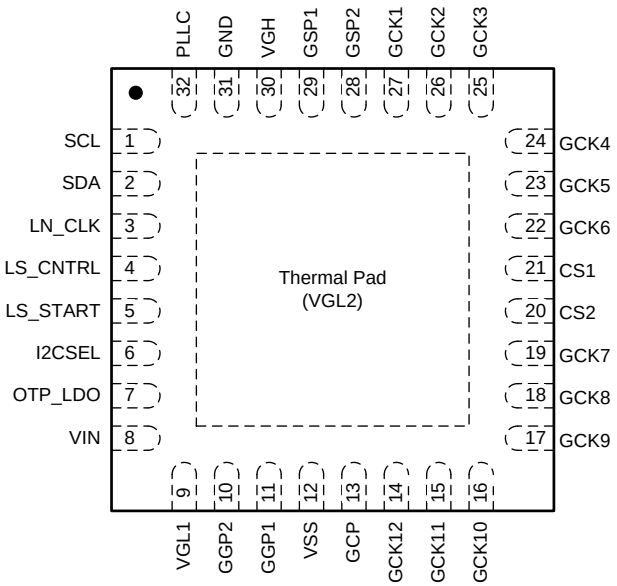
4 Revision History

DATE	REVISION	NOTES
November 2017	*	Advance Information release.
January 2018	A	Production Data release

5 Pin Configuration and Functions

RSN Package
32-Pin (WQFN)
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
CS1	21	ANALOG	Charge sharing / gate voltage shaping pin for GCK1, 2, 3, 4, 5, 6. Leave floating if not used.
CS2	20	ANALOG	Charge sharing / gate voltage shaping pin for GCK7, 8, 9, 10, 11, 12. Leave floating if not used.
GCK1	27	O	Analog, high-voltage clock output with charge sharing / gate voltage shaping connected to CS1. Outputs default to V_{GL2} and should left floating if not used.
GCK2	26	O	
GCK3	25	O	
GCK4	24	O	
GCK5	23	O	Analog, high-voltage clock output with charge sharing / gate voltage shaping connected to CS1. Outputs default to V_{GL2} and should left floating if not used.
GCK6	22	O	
GCK7	19	O	Analog, high-voltage clock output with charge sharing / gate voltage shaping connected to CS2. Outputs default to V_{GL1} and should left floating if not used.
GCK8	18	O	
GCK9	17	O	Analog, high-voltage clock output with charge sharing / gate voltage shaping connected to CS2. Outputs default to V_{GL2} and should left floating if not used.
GCK10	16	O	
GCK11	15	O	
GCK12	14	O	
GCP	13	O	Analog, high-voltage gate-clear-pulse output. Outputs default to V_{GL2} and should left floating if not used.
GGP1	11	O	Analog, high-voltage general-purpose output. Outputs default to V_{GL2} and should left floating if not used.
GGP2	10	O	
GND	31	GND	Ground.
GSP1	29	O	Analog, high-voltage gate-start-pulse output. Outputs default to V_{GL2} and should left floating if not used.
GSP2	28	O	
I2CSEL	6	I	I^2C slave address selection pin.
LN_CLK	3	I	PLL input clock (line-clock from TCON).
LS_CNTRL	4	I	Enable and panel discharge pin. Enables toggling of level shifter outputs when pulled high and initiates panel discharge sequence when pulled low.
LS_START	5	I	Pattern start. Pattern address pointer is reset to start address when pulled high. See functional description for details.
OTP_LDO	7	POWER	OTP LDO regulator output pin. Connect directly to filter capacitor.

Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NAME	NO.		
PLLC	32	I	PLL loop filter input. Connect directly to filter capacitor.
SCL	1	I	I^2C interface clock line.
SDA	2	I/O	I^2C interface data line.
VGH	30	POWER	VGH supply pin.
VGL1	9	POWER	Negative input supply pin for GCK7 and GCK8 outputs.
VGL2	Pad	POWER	Connect the thermal pad to the most negative supply (VGL2). If no second negative supply is used, connect to VGL1. Do not tie thermal pad to GND.
VIN	8	POWER	Supply pin for digital core.
VSS	12	O	Analog, high-voltage panel discharge output signal / low-side supply connected to V_{GL2}.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Supply voltage range	V_{IN}	–0.3	6	V
	V_{GH}	–0.3	42	V
	V_{GL1}, V_{GL2}	–20	0.3	V
	(V_{GH} - V_{GL1}), (V_{GH} - V_{GL2})		55	V
	(V_{GL2} - V_{GL1})	–0.3	0.3	V
	OTP_LDO	–0.3	8.4 (2)	V
Input voltage range	LS_START, LN_CLK	–0.3	V_{IN} + 0.3 (3)	V
	LS_CNTRL, SCL, SDA, I2CSEL	–0.3	6	V
Output voltage range	GCK1-12, CS1-2, GSP1-2, GCP, GGP1-2, VSS	–20	42	V
	PLLC	–0.3	2	V
Output current range	SCL, SDA		30	mA
	GCK1-12, CS1-2	–1000	1000	mA
	GSP1-2, GCP, GGP1-2, VSS	–600	600	mA
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) External programming voltage at OTP_LDO pin should be only applied for a maximum duration of 1 hour.
(3) But not to exceed 6 V.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible if necessary precautions are taken.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V HBM is possible if necessary precautions are taken.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage range	V_{IN}	2.8		5.5	V
	V_{GH}	9		40	V
	V_{GL1} (must be equal to V_{GL2})	–18		–4	V
	V_{GL2} (must be equal to V_{GL1})	–18		–4	V
	OTP_LDO	7.6	8.0	8.2	V
Input voltage range	LS_START, LS_CNTRL, LN_CLK, SCL, SDA, I2CSEL	0		3.3	V
Operating free-air temperature range, T_A		–40		85	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS65680 RSN 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	35.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	25.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	13.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	13.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.4	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

V_{IN} = 3.3 V, V_{GH} = 14 V, V_{GL1} = –15 V, V_{GL2} = –15 V, T_J = – 40°C to +125°C, typical values at T_J = 25°C (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
UNDERVOLTAGE LOCKOUT AND POWER-GOOD COMPARATORS					
Undervoltage lockout threshold (VIN)	V_{IN} rising	2.55	2.6	2.8	V
	V_{IN} falling	2.45	2.525	2.55	V
	Hysteresis	50		250	mV
Power-good threshold (VGH)	V_{GH} rising	6	7	8	V
	V_{GH} falling	3.8	4.0	4.2	V
	Hysteresis	2			V
	Deglitch time		1.1		ms
Power-good threshold (VGL1, VGL2)	$V_{GL1/2}$ rising	–3	–2.5	–2	V
	$V_{GL1/2}$ falling	–4	–3.5	–3	V
	Hysteresis	0.9			V
	Deglitch time		1.1		ms
Power-good threshold (OTP LDO)	$V_{(OTP\_LDO)}$ rising	92	95	98	%
	$V_{(OTP\_LDO)}$ falling	92	95	98	%
	Hysteresis	0			%
VDET					
V_{DET} threshold	Adjustable through I^2C interface in 100-mV steps.	2.7		4.1	V
SUPPLY CURRENTS					
Supply current (VIN)	V_{IN} = 2.0 V, (V_{IN} rising); device still in UVLO			700	µA

Electrical Characteristics (continued)

V_{IN} = 3.3 V, V_{GH} = 14 V, V_{GL1} = –15 V, V_{GL2} = –15 V, T_J = – 40°C to +125°C, typical values at T_J = 25°C (unless otherwise noted).

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Supply current (VIN)	Device in STANDBY mode; outputs unloaded				1.2	mA
Supply current (VGH)					250	µA
Supply current (VGL1)			–150			µA
Supply current (VGL2)			–150			µA
OTP LDO						
Output voltage	V_{GH} = 10 V			8.0		V
HIGH VOLTAGE CLOCK OUTPUTS (GCKx)						
Switch ON resistance	High-side, I_O = 10 mA (sourcing)			6	15	Ω
	Low-side, I_O = -10 mA (sinking)			5	15	
Propagation delay	LS_CLK to GCKx, 50% level; C_L = 1 nF; PLL bypassed.	Output rising			100	ns
		Output falling			100	
CHARGE SHARING SWITCH (CSx)						
Switch ON resistance	10 mA (sourcing); measured from GCKx to corresponding CSx pin			65	130	Ω
Propagation delay	LS_CLK to CSx, 90% level; C_L = 1 nF.	Output rising			150	ns
		Output falling			150	
HIGH VOLTAGE CONTROL OUTPUTS (GSPx, GCP, GGPx)						
Switch ON resistance	High-side, I_O = 10 mA (sourcing)			12	25	Ω
	Low-side, I_O = -10 mA (sinking)			11	25	
Propagation delay	LS_CLK to GSPx/GCP/GGPx, 50% level; C_L = 1 nF; PLL bypassed	Output rising			200	ns
		Output falling			200	
SWITCHED LOW-SIDE SUPPLY (VSS)						
Switch ON resistance	High-side, I_O = 10 mA (sourcing)			12	25	Ω
	Low-side, I_O = -10 mA (sinking)			11	25	
Propagation delay	LS_CLK to VSS, 50% level; C_L = 1 nF; PLL bypassed	Output rising			200	ns
		Output falling			200	
VGH OUTPUT DISCHARGE						
Pulldown current	V_{GH} ≥ 2.0 V		8			mA
OVER-CURRENT PROTECTION						
OCP threshold range	Adjustable through I^2C interface in 20-mA steps		20		320	mA
OCP threshold accuracy	Nominal threshold = 200 mA		–35		15	%
Comparator analog delay time				0.75	1	µs
I/O LEVELS						
Low-level input voltage (LS_START, LN_CLK, LS_CNTRL, SCL, SDA, I2CSEL)					0.55	V
High-level input voltage (LS_START, LN_CLK, LS_CNTRL, SCL, SDA, I2CSEL)			1.25			V
Input bias current (LS_START, LN_CLK)			–1		1	µA
Low level output voltage (SDA, SCL)	I_O = 3 mA (sinking)				0.4	V

Electrical Characteristics (continued)

V_{IN} = 3.3 V, V_{GH} = 14 V, V_{GL1} = –15 V, V_{GL2} = –15 V, T_J = – 40°C to +125°C, typical values at T_J = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	High level output current (leakage) (SCL, SDA)	V_O = 3.3 V			1	µA
	Internal pull-up resistor (LS_CNTRL)			500		kΩ
	Enable delay	Programmable through I^2C in 2-ms steps.	0		510	ms
PLL						
	Maximum output frequency		15			MHz
	Minimum output frequency				3	MHz
	Output frequency range		2		15	MHz
	PLL lock time	Frequency error < 450 ppm; LN_CLK = 40 kHz			8	ms
INTERNAL OSCILLATOR						
	Frequency			2.00		MHz
I2C ADDRESS						
	7-bit slave address for sequencer configuration and pattern memory	I2CSEL = low		0x42		
		I2CSEL = high		0x43		
NONVOLATILE MEMORY						
	Minimum number of write cycles		3			
	Maximum number of write cycles				9	
	Write time				80	ms
	Time-out		100		120	ms
	Data retention	T_J ≤ 85°C	10			y
MISCELLANEOUS TIMING PARAMETERS						
	Boot time	Measured from V_{IN} > UVLO to ready to accept I^2C data			1.5	ms
THERMAL SHUTDOWN						
	Thermal shutdown threshold		130		150	°C

6.6 Timing Requirements

			MIN	TYP	MAX	UNIT
LN_CLK (see Figure 1)						
f	Input frequency range	PLL active	40		500	kHz
		PLL bypassed	0		15	MHz
t_w	High-level pulse width	PLL active	25			ns
$t_{w(1)}$	Low-level pulse width	PLL active	25			ns
$t_{r(1)}$	Rise time	PLL active			25	ns
		PLL bypassed			(1/2f) - 27	
$t_{f(1)}$	Fall time	PLL active			25	ns
		PLL bypassed			(1/2f) - 27	
	Duty cycle ($t_{w(2)}$ × f)		40		60	%
LS_START (see Figure 2)						
$t_{w(3)}$	High-level pulse width		15		500	µs
t_{su}	Setup time (PLL bypass mode only)		50		450	ns
t_h	Hold time (PLL bypass mode only)		50			ns
t_{21}	Delay between rising edge of LN_CTRL & EN_DLY and LS_START.		72			µs

Timing Requirements (continued)

			MIN	TYP	MAX	UNIT
I2C-INTERFACE (see Figure 3)						
f_{SCL}	SCL clock frequency	Standard-mode			100	kHz
		Fast-mode			400	
		Fast-mode Plus			1000	
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated	Standard-mode	4.0			µs
		Fast-mode	0.6			
		Fast-mode Plus	0.26			
t_{LOW}	LOW period of the SCL clock	Standard-mode	4.7			µs
		Fast-mode	1.3			
		Fast-mode Plus	0.5			
t_{HIGH}	HIGH period of the SCL clock	Standard-mode	4.0			µs
		Fast-mode	0.6			
		Fast-mode Plus	0.26			
$t_{SU;STA}$	Set-up time for a repeated START condition	Standard-mode	4.7			µs
		Fast-mode	0.6			
		Fast-mode Plus	0.26			
$t_{HD;DAT}$	Data hold time	Standard-mode	0.05			µs
		Fast-mode	0.05			
		Fast-mode Plus	0.05			
$t_{SU;DAT}$	Data set-up time	Standard-mode	250			ns
		Fast-mode	100			
		Fast-mode Plus	50			
t_r	Rise time of both SDA and SCL signals	Standard-mode			1000	ns
		Fast-mode	20 + 0.1 C_b (1)		300	
		Fast-mode Plus			120	
t_f	Fall time of both SDA and SCL signals	Standard-mode			300	ns
		Fast-mode	20 + 0.1 C_b (1)		300	
		Fast-mode Plus			120	
t_{SP}	Pulse width of spikes that are suppressed by the input filter	Standard-mode	0		50	ns
		Fast-mode	0		50	
		Fast-mode Plus	0		50	
$t_{SU;STO}$	Set-up time for STOP condition	Standard-mode	4.0			µs
		Fast-mode	0.6			
		Fast-mode Plus	0.26			
t_{BUF}	Bus Free Time Between Stop and Start Condition	Standard-mode	4.7			µs
		Fast-mode	1.3			
		Fast-mode Plus	0.5			
C_b	Capacitive load for each bus line	Standard-mode			400	pF
		Fast-mode			400	
		Fast-mode Plus			550	

(1) C_b = total capacitance of one bus line in pF.

6.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Time between successive GSP channels				511	SEQ_CLK cycles
Time between successive GCK channels				255	SEQ_CLK cycles
Time between LS_START rising edge and GSP1 toggling		5			SEQ_CLK cycles
Time between LS_START rising edge and GCK1 toggling		7			SEQ_CLK cycles

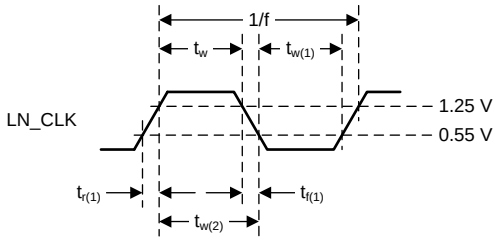


Figure 1. LN_CLK Timing Requirements

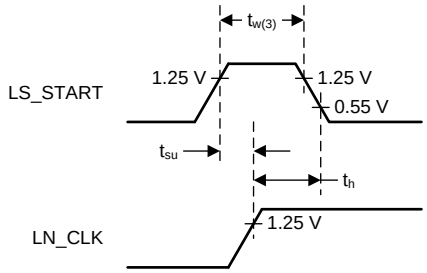


Figure 2. LS_START Timing Requirements

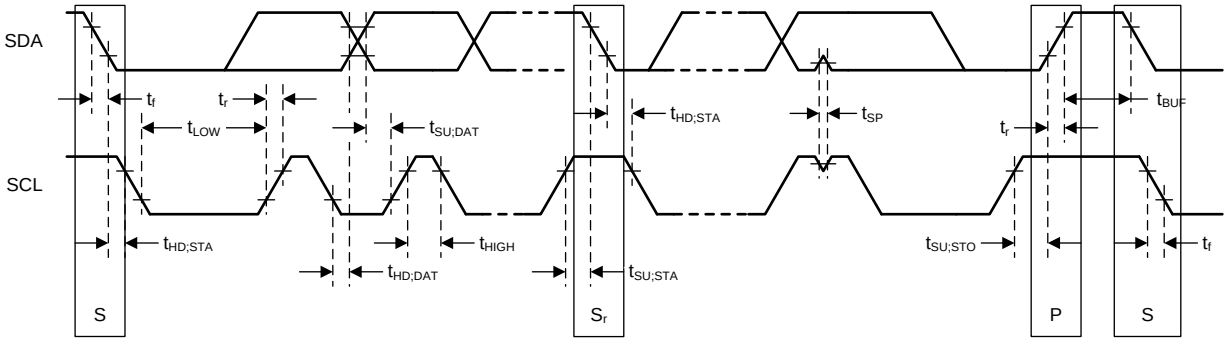


Figure 3. I^2C Data Transmission Timing

6.8 Typical Characteristics

V_{IN} = 3.3 V, V_{GH} = 14 V, V_{GL1} = V_{GL2} = –15 V, T_J = 25°C otherwise noted.

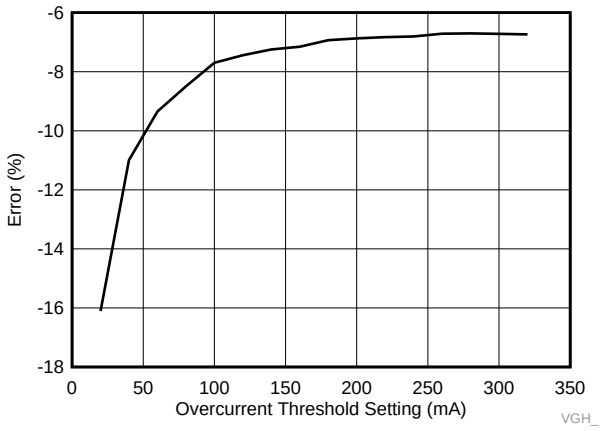


Figure 4. V_{GH} Overcurrent Protection Threshold Error

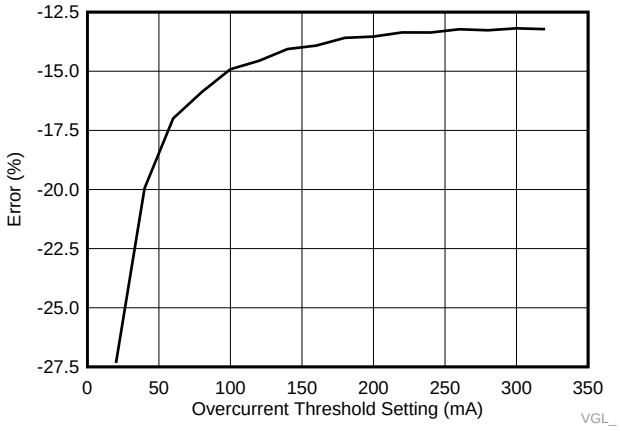


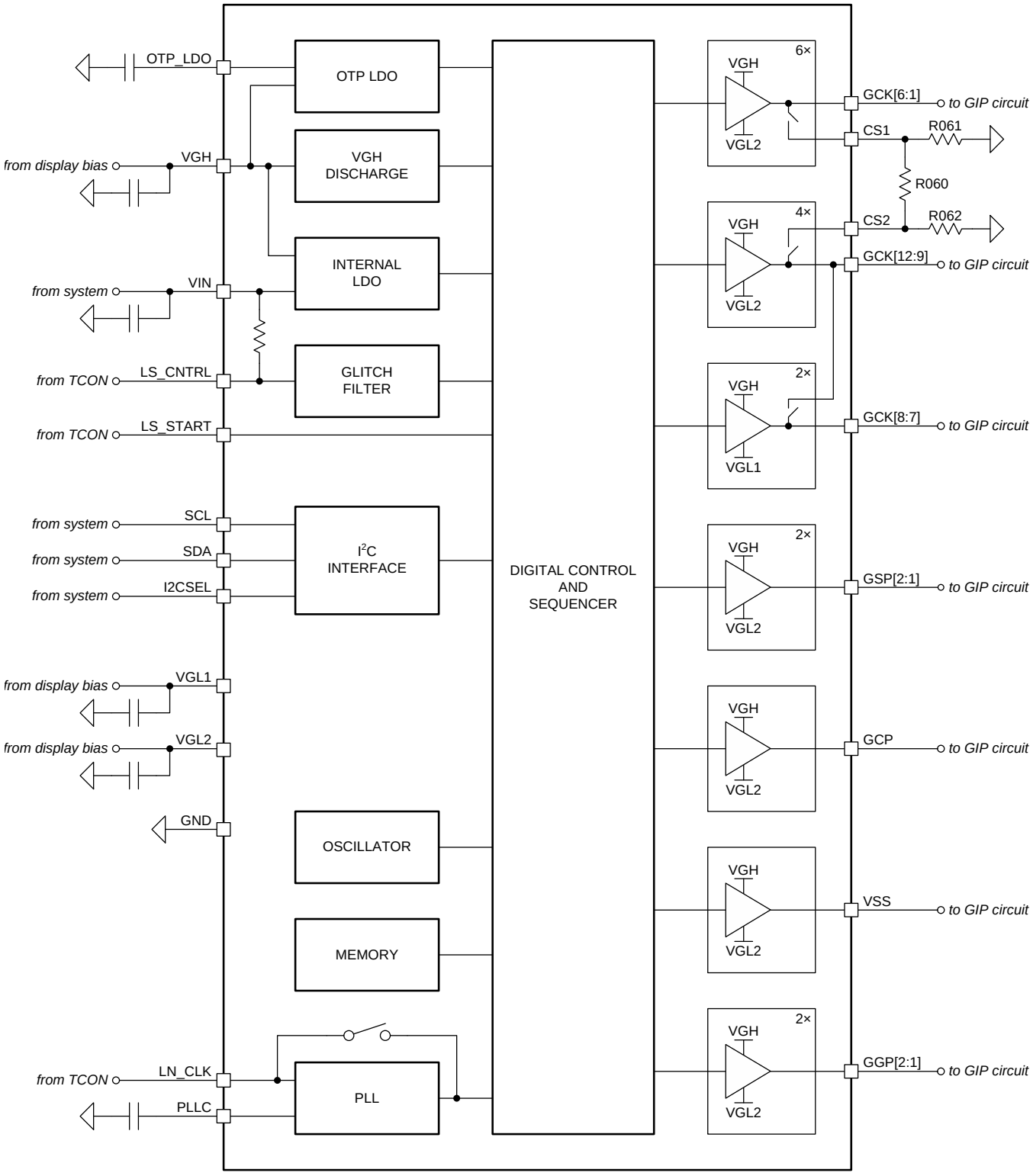
Figure 5. $V_{GL1/2}$ Overcurrent Protection Threshold Error

7 Detailed Description

7.1 Overview

The TPS65680 is a fully programmable level-shifter primarily designed for unipolar and bipolar LCD displays using GIP / GOA technology. It provides twelve high-voltage clock and six high-voltage control outputs to drive the GIP/GOA circuitry in addition to one switchable VSS supply for the LCD panel. Timing is controlled by a user-defined pattern sequence stored in non-volatile memory and two digital input signals driven by the timing controller.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Power-Up / Power-Down Sequencing

The TPS65680 requires a low-voltage input supply VIN (typical 3.7V) and high and low gate driver supplies VGH and VGL1 and VGL2. VGL2 (power pad) may be connected to a dedicated most negative gate driver supply or it must be connected to the VGL1 pin. Supplies may be applied in any order during power-up. The typical power-up and power-down sequence is shown in Figure 6. The first voltage rail to be applied to the device is typically battery voltage or a pre-regulated 3.3V supply, VIN. The second rail is the negative gate driver supply VGL2, followed by VGL1, and finally VGH.

The power-down and panel discharge sequence is triggered by a falling edge on the LS_CNTRL pin. After a delay of D1, active discharge of the VGH supply is enabled. At this point, all external rails can be powered down, typically by disabling them simultaneously.

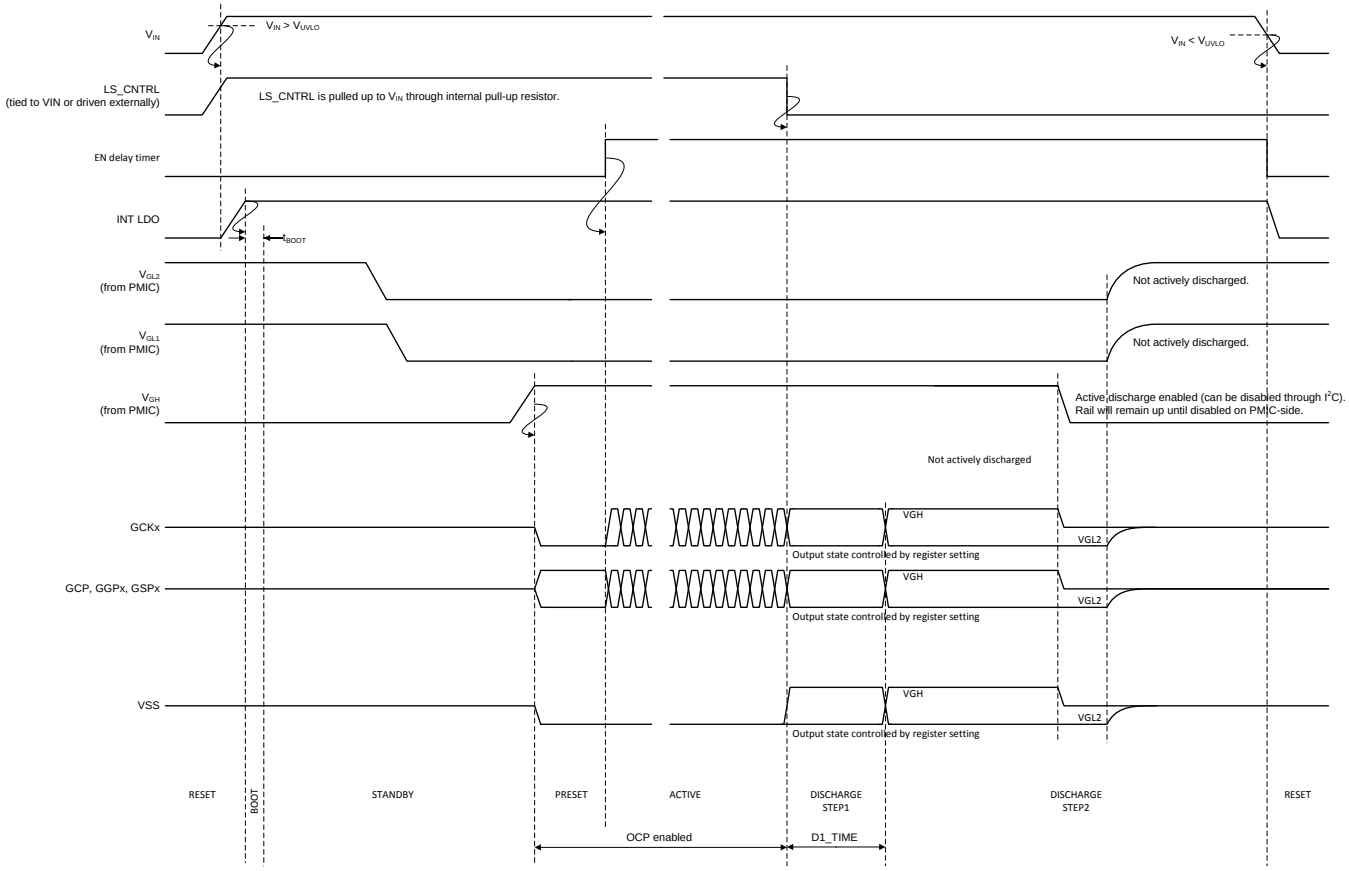


Figure 6. Power-Up / Power-Down Sequence

7.3.2 The EN_DLY Timer

The purpose of the EN_DLY timer is to delay entering ACTIVE state after power-up, in case the LS_CNTRL pin is permanently tied high. This allows to enable and preset all level shifter outputs before the level shifter starts toggling its outputs. The EN_DLY timer is re-started when the device is sitting in WAIT CNTRL HIGH state and the LS_CNTRL pit is pulled high. This allows the VGH rail to recover in case the active discharge function was turned ON during DISCHARGE STEP2 and / or WAIT CNTRL HIGH. The EN_DLY time constant is set in the EN_DLY register and should be only updated while the LS_CNTRL pin is low and the device is in STANDBY or WAIT CNTRL HIGHstate.

Feature Description (continued)

7.3.3 Panel Discharge

The two-step power-down sequence is triggered by a falling edge on the LS_CNTRL pin as shown in Figure 6. The state of the level shifter outputs for each functional group (GCK, GSP, GCP, GGP, VSS) is programmable for each discharge phase (*PNL_DCH1* and *PNL_DCH2* registers) as well as the duration of DISCHARGE STEP1, and the status of the VGH discharge function. DISCHARGE STEP1 duration is set by the D1_TIME constant defined in the CONFIG2 register. D1_TIME must not be changed while the timer is running, i.e. the CONFIG2 register must not be updated while in DISCHARGE STEP1. DISCHARGE STEP2 lasts for as long as VIN remains present, or until the LS_CNTRL pin toggles from low to high.

A typical discharge sequence begins with the LS_CNTRL pin being pulled low. All level shifter outputs are driven low with the exception of the CLEAR channels (GCKx) which are driven high. After 2 ms, the CLOCK (GCKx) and START (GSPx) channels are driven high together with VSS to complete the discharge sequence.

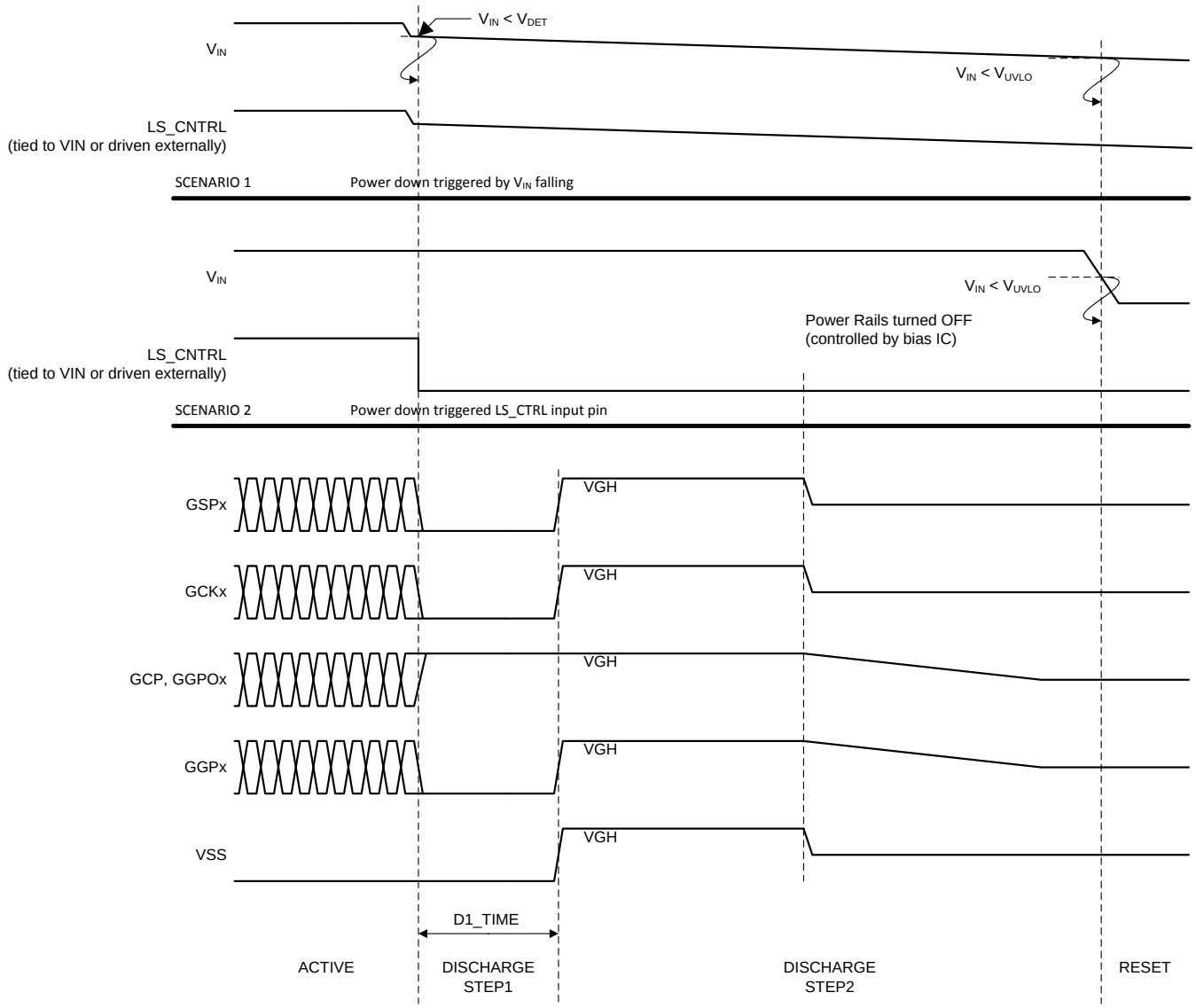


Figure 7. Typical Panel-Discharge Sequence

Feature Description (continued)

7.3.4 Level Shifter Supply Voltage Supervision and Power-Good (LSPG)

VGH, VGL1 and VGL2 input supplies are monitored and validated against a fixed threshold. Only if all three supplies are valid, the internal level-shifter power-good (LSPG) signal is asserted and the level-shifter output stages can be enabled. If any of the rails encounters a fault during normal operation (ACTIVE mode), the sequencer is stopped and the panel discharge sequence is initiated to prevent damage to the panel. Note that the monitoring circuits cannot be disabled. If only one VGL supply is used, VGL1 and VGL2 inputs must be shorted together.

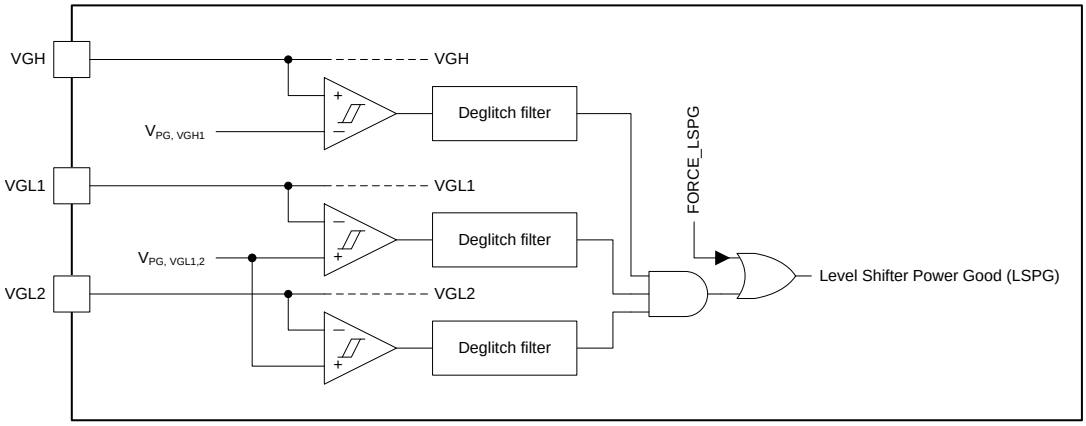


Figure 8. Level Shifter Power-Good

7.3.5 Level-shifter Overcurrent Protection

The TPS65680 device protects its high-voltage output channels against overcurrent conditions in the PRESET and ACTIVE states. When an output channel switches, the device monitors the current flowing in the corresponding input supply pin (VGH, VGL1 or VGL2). If the current exceeds the user-programmed threshold, the device detects an overcurrent event.

When the TPS65680 device powers up it enters the PRESET state and enables each output channel one after the other. If an OCP event is detected, the device stops the output enable sequence, sets all the outputs to HiZ and enters the FAULT state.

In the ACTIVE state, the TPS65680 device counts OCP events in two counters: ALARM1 for clock channel OCP events and ALARM2 for control channel OCP events. If the number of events in either of these counters reaches the programmed maximum value, the device sets all the outputs to HiZ and enters the FAULT state. The ALARM1 and ALARM2 counters are reset at the start of each frame.

The OCP_FAULT1 and OCP_FAULT2 bits in the FAULT register indicate if the OCP event was caused by a clock channel or a control channel. To recover normal operation after an OCP event, you must apply a power cycle to the device.

A number of user-programmable registers control the OCP function. You can:

- Use the CONFIG2 register to enable and disable the OCP function for each supply pin
- Use the OCP_CH_SEL1, OCP_CH_SEL2 and OCP_CH_SEL3 registers to enable and disable the OCP function for each high-voltage output
- Use the OCP_SNS_DLY1 and OCP_SNS_DLY2 registers to set the current sense delay
- Use the OCP_CH_SEL3 register to program the OCP threshold
- Use the OCP_CH_SEL3 register to select how the device reacts to an OCP condition
- Use the OCP_ALARM1 and OCP_ALARM2 registers to select how many OCP events must occur before the device disables its outputs

Feature Description (continued)

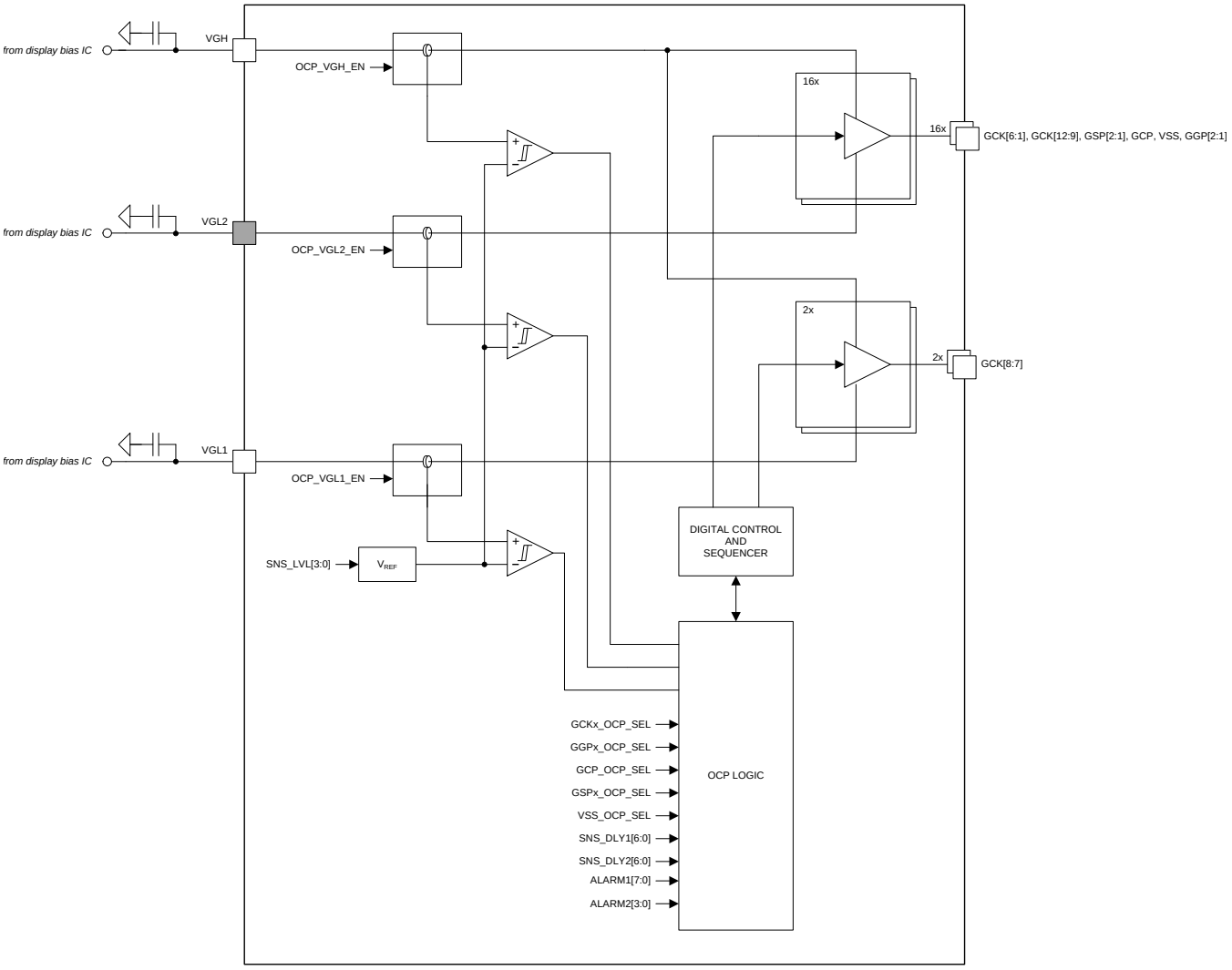


Figure 9. Overcurrent Sensing

7.3.6 I2CSEL Pin

The I2CSEL pin lets you select one of two slave possible addresses, so that you can use two TPS65680 devices in the same application and address each of them separately. This can be necessary, for example, if your application needs more than 12 clock outputs.

- If a low level is applied to the I2CSEL pin, the slave address is 0x42
- If a high level is applied to the I2CSEL pin, the slave address is 0x43

7.3.7 Internal LDO and Biasing System

Internal power for the logic core and analog reference system is primarily sourced from the VIN pin but can be also sourced from VGH after the IC has powered up. When $V_{(VIN)}$ rises above the under-voltage lockout threshold, the reference system and internal LDO are powered up, allowing the IC to boot and enter STANDBY mode. Once powered up, an internal power-path is enabled, sourcing power for the reference system and INT_LDO from either VIN or VGH, allowing the IC to remain functional for as long as either supply is available. Note that the order in which VIN and VGH are supplied to the IC is irrelevant but the IC does not power up without VIN being present. In particular, the IC does not power up if VGH is supplied but VIN is below the UVLO threshold.

Feature Description (continued)

7.3.8 VGH

VGH is the high-side input supply for the VSS, GCKx, GGPx and GSPx level shifter outputs.

7.3.9 VGH Discharge

A 10 mA current sink connected to the VGH pin can be enabled during DISCHARGE1 and DISCHARGE2 phase to discharge the VGH input pin to ground.

7.3.10 OTP LDO

The OTP LDO may be used to generate the programing voltage for the non-volatile memory from the VGH supply input. Alternatively, the OTP LDO may be disabled and the programming voltage applied directly to the OTP_LDO output. If not used, the OTP_LDO pin may be left floating and no output capacitor is needed.

7.3.11 High-Voltage Gate-Clock Outputs (GCKx)

TPS65680 provides two groups of four GCP outputs intended for driving the high voltage clock inputs of the row driver circuitry. All GCP outputs are parametrically identical; Outputs 1-6 share a common charge sharing pin CS1, outputs 7-12 share a common charge sharing pin CS2. Each output supports high (VGH), low (VGL2), charge-sharing (output connected to CS1, CS2), and HiZ state. Gate-voltage shaping is accomplished by connecting the CSx pins individually through resistors to GND or any other suitable potential. Alternatively both CS pins can be shorted together and connected through a common resistor to GND or any other suitable potential.

By design, charge sharing is supported between channels of different groups only, i.e. GCK1-6 can charge share with any channel from group GCK7-12 but not with any other channel from the same group GCK1-6. Charge sharing is accomplished by connecting CS1 to CS2 through a single resistor. Figure 10 shows a common charge sharing scheme for 12 clocks. Channel assignment is determined by the pattern sequence programed into the part.

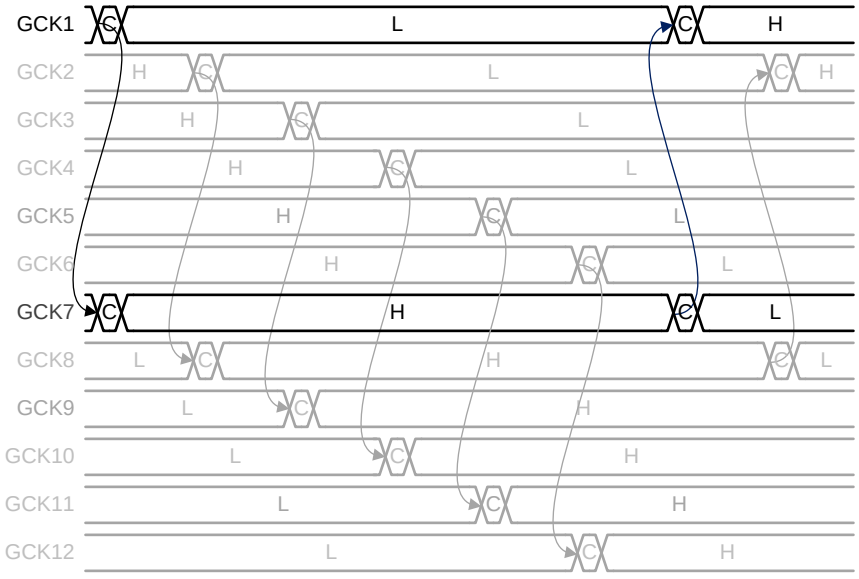


Figure 10. Typical Charge Sharing Scheme.

Feature Description (continued)

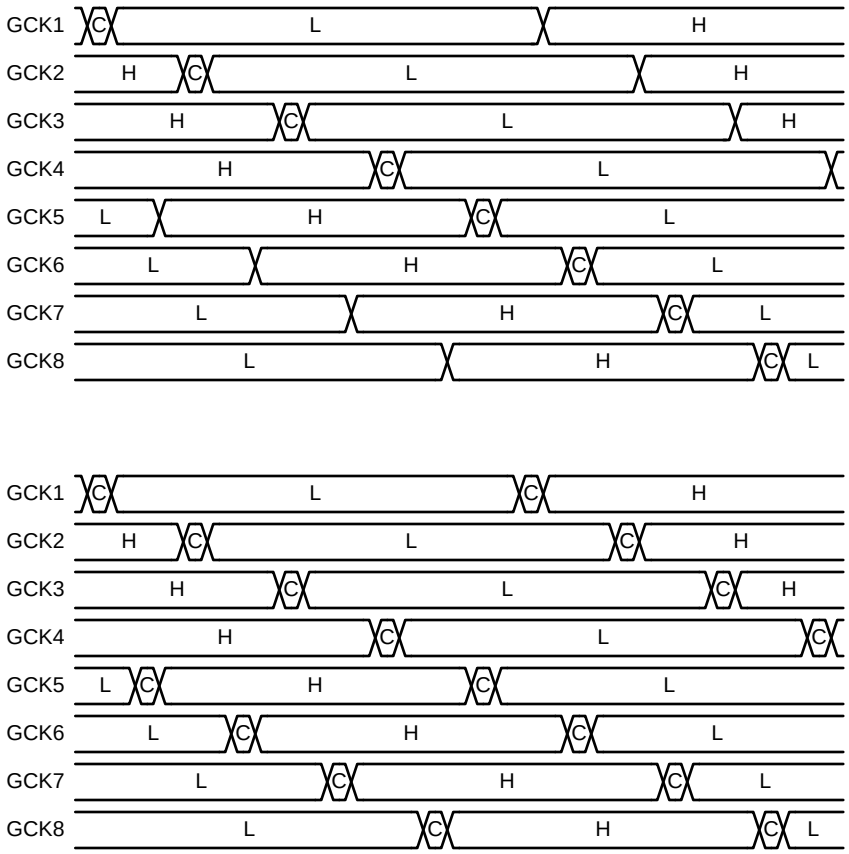


Figure 11. Typical Gate-Voltage Shaping Schemes. Falling Edge Only (Top) or Falling and Rising Edge (Bottom).

At power-up all GCK outputs are in HiZ state and remain in this state until VGH, VGL1 and VGL2 are powered up. Then the outputs are released to the programmed output state as defined in PRESET1 and PRESET2 registers and remain in this state until the sequencer takes control after the programmable EN_DLY timer in EN_DLY register expired. During panel-discharge, the GCK outputs can be configured to be in Low, or High state separately for *DISCHARGE STEP1* and *DISCHARGE STEP2* using the GCK1_D1 and GCK_D2 bits of the *PNL_DCH1* and *PNL_DCH2* registers.

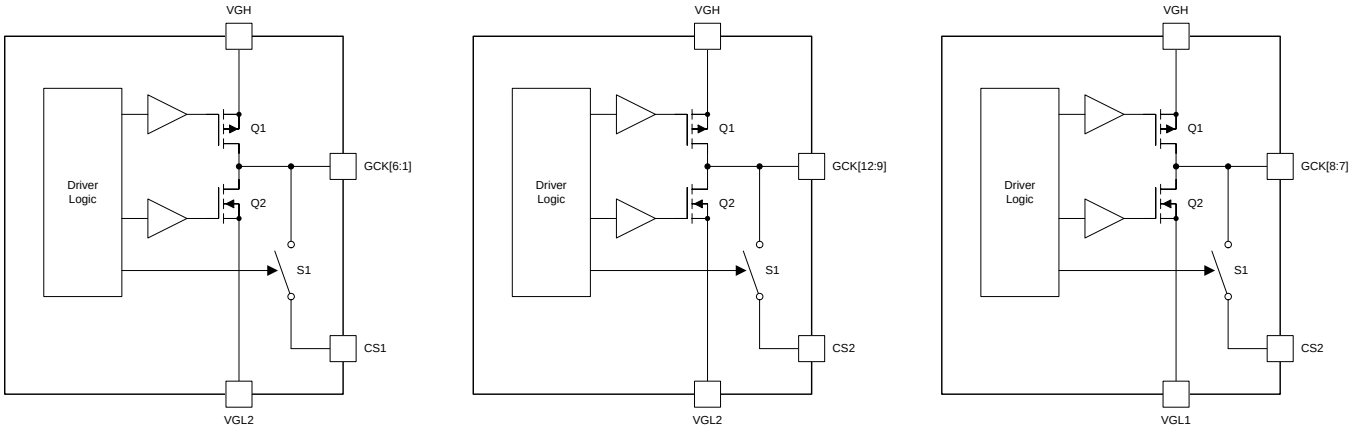


Figure 12. GCKx Output Stages

Feature Description (continued)

7.3.12 High-Voltage Control Outputs (GSP, GCP, GGP)

TPS65680 provides two GSP (Gate Start Pulse), one GCP (Gate Clear Pulse), and two GGP (General Purpose) high-voltage outputs intended for driving control signals of the GIP circuitry. All outputs are parametrically identical. GSP channels drive to VGH and VGL2. GCP and GGP channels drive to VGH and VGL2. All channels support High, Low, and HiZ state.

At power-up, all HV outputs are in HiZ state and remain in this state until VGH, VGL1 and VGL2 are powered up. Then the outputs are released to the programmed output state as defined in PRESET2 register and remain in this state until the sequencer takes control after the programmable EN_DLY timer in EN_DLY register expired. During panel-discharge, the outputs can be configured to be in Low or High state, separately for *DISCHARGE STEP1* and *DISCHARGE STEP2* using the respective bits of the *PNL_DCH1* and *PNL_DCH2* registers.

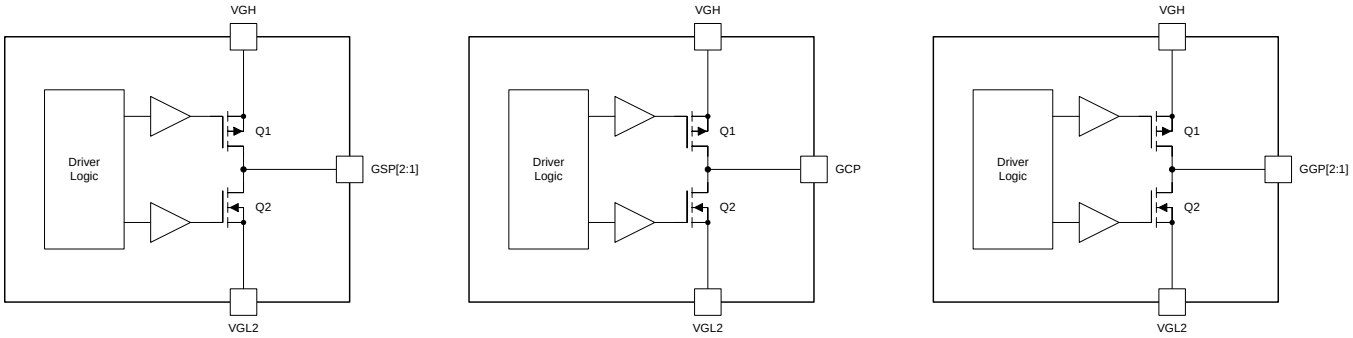


Figure 13. GSPx, GCP, and GGPx Output Stages

7.3.13 High-Voltage Gate Driver Low-Side Supplies (VSS)

The VSS output is a switched Gate-Driver Low-Side Supply and supports High and Low state only.

At power-up, the VSS output is in HiZ state and remains in this state until VGH, VGL1 and VGL2 are powered up. Then the output is released to the programmed output state as defined in PRESET2 register and remains in this state until the sequencer takes control after the programmable EN_DLY timer in EN_DLY register expired. During panel discharge, the output can be configured to be in Low or High state, separately for *DISCHARGE STEP1* and *DISCHARGE STEP2* using the respective bits of the *PNL_DCH1* and *PNL_DCH2* registers.

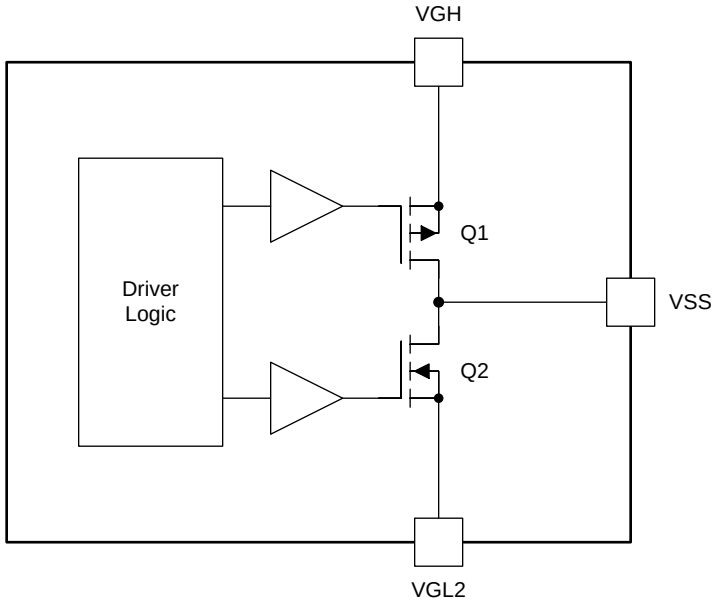


Figure 14. VSS Output Stage

Feature Description (continued)

7.3.14 Programmable Pattern Sequencer

The programmable pattern sequencer governs the level shifter outputs during the frame active and blanking time. It requires only two inputs from the TCON, a line-clock (LN_CLK) and a start pulse (LS_START) that indicates the start of a new frame. The sequencer consists of two main parts, a signal generator that calculates the output state for each analog output, and a channel selector / output gate that determines if the signal is actually applied to the output. The signal generator is explained in detail under *Signal Generator Architecture and Instruction Set*, output gating under *Channel Selection and Output Gating*.

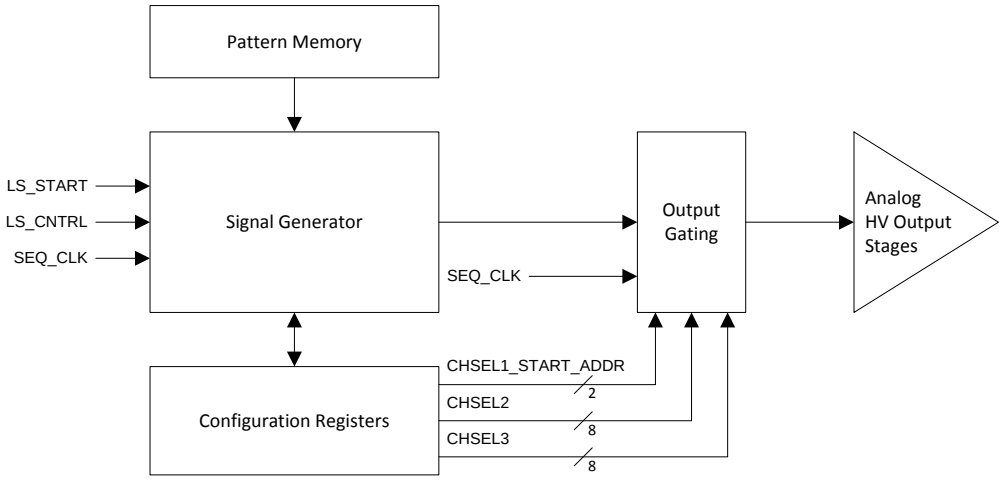


Figure 15. High-Level Sequencer Block Diagram.

The information from which the signal generator calculates the output states is stored as a series of consecutive instructions in pattern memory. Pattern memory holds up to 54 instructions (logical address 0 to 53) that can be used to store a single sequence or may be divided into multiple sections containing different sequences. The start address of a sequence is stored in register *CHSEL1_START_ADDR*.

Level shifter operation is gated by the following conditions:

- The internal EN_DLY counter must have expired,
- LS_CNTRL pin must be high, and
- All rails must indicate power-good

Sequence execution starts on the rising edge of LS_START terminates when the END instruction is reached. Detailed start / stop timing is shown in section Preset and START. The signal generator distinguishes between Master and Slave channels. Master channels are controlled directly by the control bits of an CXE instruction. Slave channels follow one of the master channels with a programmable separation count. See *CLOCK Execute Instruction (CXE) and DATA Execute Instruction (DXE)* for details.

To remain in lock-step with the source-driver data, the sequencer clock (SEQ_CLK) is derived from a reference clock provided by the TCON and connected to the LN_CLK pin. Typically this will be the line clock but can be an integer multiple or fraction of the line clock as long as he frequency is within the valid input frequency range for the PLL.

The pattern sequencer is configured via a set of registers, some of which can be dynamically modified by the sequencer during run time. Registers are addressed by their logical address rather than I^2C address and the mapping is shown in *Table 1*.

Table 1. Logical Address Mapping of Sequencer Configuration Registers.

REGISTER	LOGICAL ADDRESS	SEQUENCER ACCESS
C1256_SEP	N/A	READ
C34_SEP	N/A	READ
D1_SEP	N/A	READ

Feature Description (continued)

Table 1. Logical Address Mapping of Sequencer Configuration Registers. (continued)

REGISTER	LOGICAL ADDRESS	SEQUENCER ACCESS
D2_SEP	N/A	READ
MUX1	0x0	READ / WRITE
MUX2	0x1	READ / WRITE
MUX3	0x2	READ / WRITE
MUX4	0x3	READ / WRITE
CHSEL1_START_ADDR	0x4	READ / WRITE
CHSEL2	0x5	READ / WRITE
CHSEL3	0x6	READ / WRITE
PRESET1	0x7	READ / WRITE
PRESET2	0x8	READ / WRITE
DATA1	0x9	READ / WRITE
DATA2	0xA	READ / WRITE
DATA3	0xB	READ / WRITE
DATA4	0xC	READ / WRITE
DATA5	0xD	READ / WRITE

7.3.14.1 Signal Generator Architecture and Instruction Set

This section describes in detail the instructions available for coding pattern sequences. The data structure of each instruction is shown in Figure 16. Each instruction is 24 bits wide. The 3 MSBs indicate the instruction type, the remaining 21 bits are used to pass data to the sequencer. A 24-bit wide logical instruction is mapped to physical memory as shown in .

DATA WORD

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

INVALID INSTRUCTIONs (INV)

INSTR	NOT USED
0x0	

CLOCK EXECUTE AND IDLE (CXE)

INSTR	C6	C5	C4	C3	C2	C1	IDLE COUNT
0x1	0	0	0	0	0	0	0x00

LOOP (LOP)

INSTR	NOT USED	LINE COUNT	LOOP COUNT
0x2		0x02	0x1F

JUMP (JMP)

INSTR	NOT USED	JUMP ADDRESS
0x3		0x00

END (END)

INSTR	NOT USED	LV	REG ADDR	SET VALUE
0x4		0	0x00	0x00

LOAD DATA REGISTER (LDR)

INSTR	NOT USED	REG ADDR	SET VALUE
0x5		0x00	0xFF

INCREMENT (INC)

INSTR	NOT USED	REG ADDR	INCREMENT VALUE
0x6		0x00	0x00

EXECUTE IF EQUAL (EEQ)

INSTR	NOT USED	LINE COUNT	REG ADDR	COMPARE VALUE
0x7		0x01	0x00	0xFF

DATA EXECUTE AND IDLE (DXE)

INSTR	D3	D2	D1	IDLE COUNT
0x08	0	0	0	0x00

SWAP (SWP)

INSTR	OVERLAP COUNT	REG ADDR	CMP VALUE
0x09	0x00	0x00	0x00

Figure 16. Instruction Set and Bit Coding

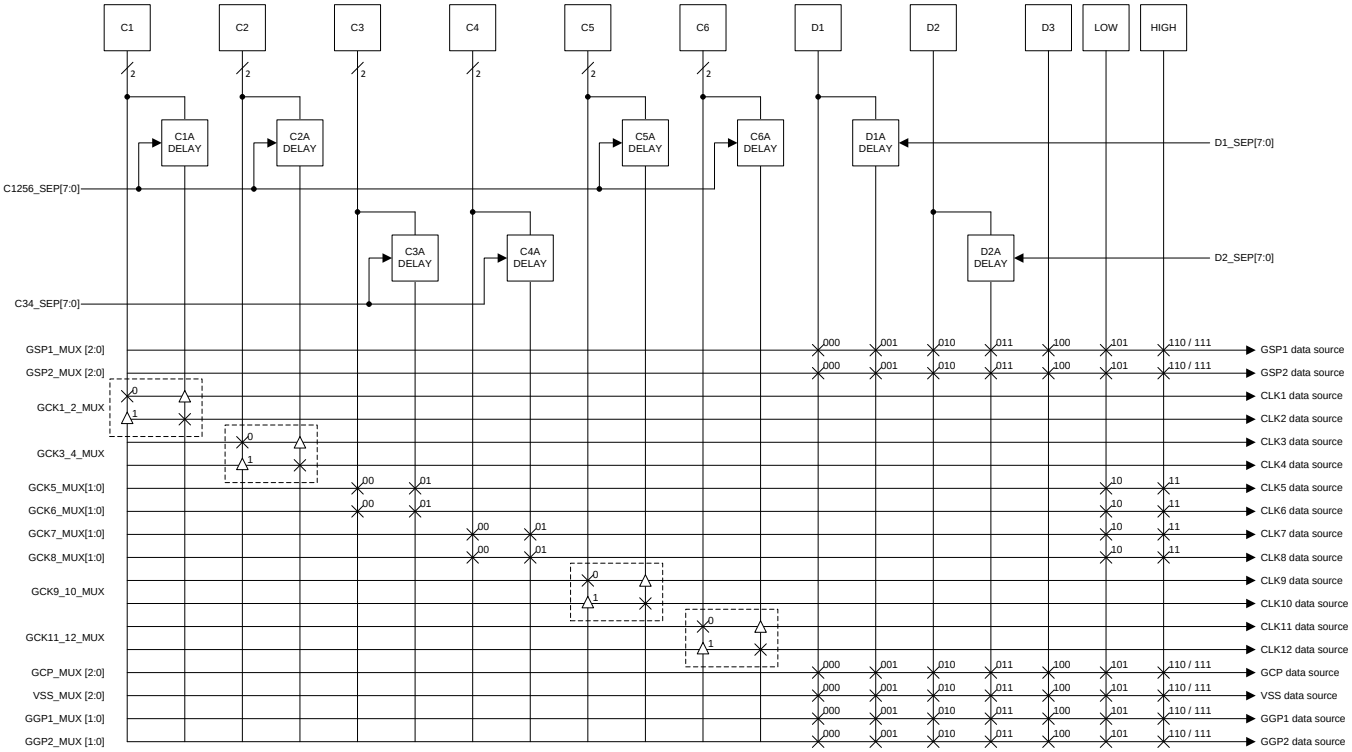


Figure 17. Source Data Multiplexing Matrix for GCKx Outputs (Top) and GSP/GCP/GGP Outputs (Bottom). Numbers Indicate Multiplexer Setting for Individual Channels

7.3.14.2 CLOCK Execute Instruction (CXE) and DATA Execute Instruction (DXE)

This instruction is used to modify the state of the level shifter outputs. C1, C2, C3, C4, C5 and C6 are 2-bit values dedicated to the master high-voltage output clocks GCK1-2, GCK3-4, GCK5, GCK6, GCK7, GCK8, GCK9-10 and GCK11-12. D1, D2 and D3 are 1-bit values used to control GSP1-2, GCP, VSS and GGP1-2 outputs. The coding for each channel is described in its corresponding channel description section above.

High-voltage clock outputs GCK2, CCK4, GCK6, GCK8, GCK10 and GCK12 are not directly controlled by the EXE instruction but trail their respective master channels with a programmable delay equal to an integer number of logic clock cycles as shown in Figure 17. A C1256_SEP setting of 1 delays each slave channel by one logic clock cycle against its preceding channel. A C1256_SEP setting of 2 delays each slave channel by two logic-clock cycles, up to a maximum delay of 255. A C1256_SEP setting of 0 yields no delay, such that the slave output signals are identical, non-shifted copies of the master channel. The clock separation is set in the *C1256_SEP* and C34_SEP registers and the same setting applies to all slave clocks, regardless of their master channel. Note that the master channel must not have more than 4 state transitions within the separation window for the signal to be reproduced properly on a slave output.

The idle count is used to extend the dwell time of an execute instruction. With an idle count of 0, the defined states are applied to the outputs and kept steady for one clock cycle before the sequencer advances to the next instruction. The dwell time may be increased by up to 255 clock cycles by increasing the idle count. The resulting dwell time equals the idle count plus one clock cycle.

Control bits D1 through D3 are dedicated to the control of the GSP1-2, GCP, VSS and GGP1-2 outputs. Different from the C1, C2, C3, C4, C5 and C6 bits, there is no fixed channel assignment, although in a typical use case the channels are used as follows:

- D1 controls GSP1, GSP2
- D2 is not used or controls GGP1, GGP2
- D3 controls GCP, VSS

In most use cases GSP2 and GCP2 level shifter outputs are not directly controlled by D1/D3 control bits but rather by one of the delayed signals, D1A, and D2A. The 8-bit separation settings for D1A and D2A are independently programmable through the and *D1_SEP* and *D2_SEP* registers, respectively. Channel assignment is controlled by the *MUX1-3* registers and the available assignment options are shown in *Figure 17*. Channel assignment may be dynamically changed during run time by modifying the register settings through a LDR instruction.

D1, D2, and D3 are single bit only. If a channel is assigned to a single-bit control, only the high and low drive options are available. See coding tables under *High-Voltage Control Outputs (GSP, GCP, GGP)* for details.

The idle count is used to extend the dwell time of an execute instruction.

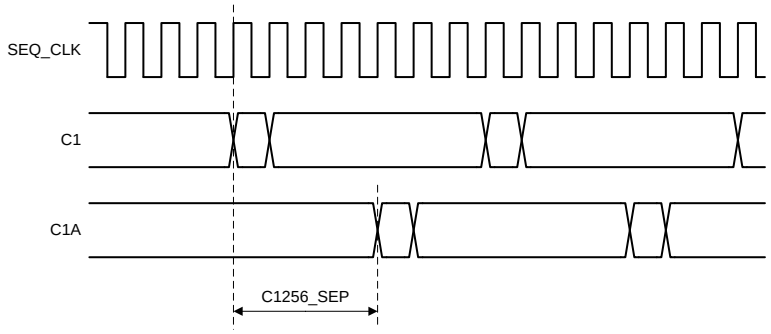


Figure 18. Clock Separation.

7.3.14.3 Loop Instruction (LOP)

The loop instruction allows executing of a section of code a defined number of times. The <Line count> number of instruction immediately following the LOP command are executed <Loop Count> number of times. The minimum number of instructions allowed inside a loop is two (2) and the minimum loop count is one (1). A LOP instruction must not be followed immediately by a JMP command, although jumps are allowed inside of loops in general. Nesting of loops is not supported, i.e. the body of a loop must not contain another LOP instruction. The loop start address plus <Line count> must not exceed the maximum allowed logical address of 53, otherwise the pattern sequence terminates immediately, similarly to executing an END instruction.

Processing of the LOP instruction requires one clock cycle. Within the sequence, the level shifter output state preceding the LOP instruction is extended by one clock cycle while processing the LOP instruction as shown in the example below.

```
ADDR    INST         CLK  OUTPUT STATE
1       CXE<1>         1   <1>
2       CXE<2>         2   <2>
3       LOP(2, 3)      3   <2>  <-- Loop next 2 lines 3x
4       CXE<3>         4   <3>
5       CXE<4>         5   <4>
                       6   <3>
                       7   <4>
                       8   <3>
                       9   <4>
6       CXE<5>        10   <5>
```

7.3.14.4 Jump Instruction (JMP)

This instruction advances the sequencer to <JUMP ADDRESS>. It is most commonly used in conjunction with an EEQ instruction to implement conditional execution of a section of code. Addressing is absolute, i.e. <JUMP ADDRESS> denotes a specific location inside the pattern memory that is independent of the position of the JMP instruction itself. Jumps can be performed in either direction and multiple JMP commands can be executed back-to-back. A JMP instruction must not reflect on itself, i.e. <JUMP ADDRESS> must be different from the address of the issuing JMP instruction itself. Also, a LOP command must not be followed directly by a JMP instruction. See *Loop Instruction (LOP)* for details. If the Jump address exceeds the maximum allowed logical address of 53, the pattern sequence terminates immediately, similarly to executing an END instruction.

Processing a JMP instruction requires two clock cycles. Within the sequence, the level shifter output state preceding the JMP instruction is extended by two clock cycles while processing the JMP instruction as shown in the example below.

```
ADDR    INST        CLK    OUTPUT STATE
1       CXE<1>      1      <1>
2       CXE<2>      2      <2>
3       JMP(5)      3      <2>  <-- Jump to ADDR 5
                    4      <2>
4       CXE<3>                 <-- Line is skipped by JMP instruction
5       CXE<4>      5      <4>
```

7.3.14.5 End Instruction (END)

The END instruction indicates the end of a sequence and stops the advancement of the address counter. Master channels, i.e. such level shifter outputs directly controlled by one of the C1-6 or D1-3 control bits keep their last state whereas slave channels (those controlled by C1A, C2A, C3A, C4A, C5A, C6A, D1A, D2A) may continue to toggle until the respective delays have been consumed. The sequence re-starts at the *CHSEL1_START_ADDR* when the next LS_START pulse is detected.

If the LV bit is set to 1, <SET VALUE> is copied to register <REG ADDR> as the sequence is terminated. This is useful for changing the start address for the next frame. If the LV bit is set to 0, <SET VALUE> and <REG ADDR> are ignored. <REG ADDR> denotes the logical address listed in Table 1 and is specified as a four-bit value. The use of non-specified addresses is legal but not recommended.

Use of the END instruction is optional and not required for proper pattern execution. If the END instruction is omitted, the sequencer continues to the maximum pattern address and stops.

7.3.14.6 Load Data Register Instruction (LDR)

This instruction is used to write data to a register during run-time. It is most commonly used to

- Preset or reset data registers *DATA1*, *DATA2*, *DATA3*, DATA4. DATA5
- Change the pattern start address by modifying the *CHSEL1_START_ADDR* register,
- Modifying the channel assignment through the *MUX1*, *MUX2*, *MUX3* or MUX4 registers,
- Enabling and disabling channels through the CHSEL1_START_ADDR, CHSEL2 and CHSEL3 register, and
- Changing the preset values in the *PRESET1* and *PRESET2* registers.

<REG ADDR> denotes the logical address listed in Table 1 and is specified as a four-bit value. The use of non-specified addresses is legal but not recommended. Processing of the LDR instruction requires one clock cycle. Within the sequence, the level shifter output state preceding the LDR instruction is extended by one clock cycle while processing the LDR instruction as shown in the example below.

```
ADDR    INST        CLK    OUTPUT STATE
 1      CXE<1>      1      <1>
 2      CXE<2>      2      <2>
 3      LDR(5,FF)   3      <2>  <-- Load Reg 0x05 with data 0xFF
 4      CXE<3>      4      <3>
```

7.3.14.7 Increment Instruction (INC)

An increment instruction is used to add an arbitrary 8-bit value to register <REG_ADDR>. Overflow is supported. <REG ADDR> denotes the logical address listed in *Table 1* and is specified as a four-bit value. The use of non-specified addresses is legal but not recommended. Processing an INC instruction requires one clock cycle. Within the sequence, the level shifter output state preceding the INC instruction is extended by one clock cycle while processing the INC instruction as shown in the example below.

```
ADDR    INST        CLK    OUTPUT STATE
 1      CXE<1>      1      <1>
 2      LDR(5,FF)   2      <1>  <-- Load Reg 0x05 with data 0xFF
 3      CXE<2>      3      <2>
 4      INC(5,1)    4      <2>  <-- increment Reg 0x05 by 1
 5      CXE<3>      5      <3>      Reg 0x05 now contains value 0x00.
```

7.3.14.8 Execute If Equal Instruction (EEQ)

The EEQ instruction executes the following <LINE COUNT> number of commands if the content of the <REG ADDR> register matches <COMPARE VALUE>. Otherwise the next <LINE COUNT> number of instructions are skipped and execution resumes at the current address + <LINE COUNT> + 1. If the resulting target address exceeds the maximum allowed logical address of 53, the pattern sequence terminates immediately, similarly to executing an END instruction. <REG ADDR> denotes the logical address listed in Table 1 and is specified as a four-bit value. The use of non-specified addresses is legal but not recommended.

A typical use case for the EEQ instruction is a if-then-else construct consisting of a EEQ and a JMP instruction. In the example below, lines 4 and 5 are executed if register 0x15 equals 0xFF, else line 6 is executed. Lines 1, 2, and 7 are executed in either case.

Processing a EEQ instruction requires two clock cycles. Within the sequence, the level shifter output state preceding the EEQ instruction is extended by two clock cycles while processing the EEQ instruction as shown in the example below.

```
ADDR    INST         CLK     OUTPUT STATE
1       CXE<1>       1       <1>
2       CXE<2>       2       <2>
3       EEQ(2,5,FF)  3       <2>   <-- Execute next 2 lines if Reg 0x05 equals 0xFF
                     4       <2>       For this example Reg 0x05 is assumed to contain 0xFF
4       CXE<3>       5       <3>
5       JMP(7)       6       <3>
                     7       <3>
6       CXE<4>                     <-- Line is skipped by JMP instruction
7       CXE<5>       8       <5>
```

7.3.14.9 SWAP Instruction (SWP)

The SWP instruction compares the <CMP VALUE> to the content of DATA5 register. If the value does not match then DATA5 register is increment by 1 and the instruction is completed.

Otherwise DATA5 register is reset to 0x00 and the content of the <REG ADDR> is temporarily stored. If <OVERLAP COUNT> is > 0, then DATA1 register content is copied to <REG ADDR> and sequencer waits for <OVERLAP COUNT> + 3 clock cycles, else this step is skipped . Finally DATA2 register content is copied to <REG ADDR> register and the temporarily stored value is stored in DATA2 register.

A typical use case for the SWP instruction is to control the very low frequency ODD and EVEN output signals (GGP1 and GGP2) which toggle at the same time or with an overlap defined in <OVERLAP COUNT>. The <CMP VALUE> defines the toggle frequency. ODD and EVEN outputs can be controlled by MUX3 register. The sequencer can address this register by its local address as shown in Table 1.The default setting of MUX3 register (addressed by logic register address <REG ADDR>) defines the output level of the ODD and EVEN signals when the sequencer starts the pattern by entering the ACTIVE state. The default setting of register DATA2 defines the inverted output level of both signals. When DATA5 register got incremented to the value of <CMP VALUE> then actual <REG ADDR> is swapped with DATA2 register content and ODD and EVEN signals are toggled.

Processing a SWP instruction requires 11 + <OVERLAP COUNT> clock cycles.

7.3.14.10 INVALID Instructions (INV)

If the sequencer reads an invalid instruction, then the advancement of the address counter is stopped. Master channels, i.e. such level shifter outputs directly controlled by one of the C1-6 or D1-3 control bits keep their last state whereas slave channels (those controlled by C1A, C2A, C3A, C4A, C5A, C6A, D1A, D2A) may continue to toggle until the respective delays have been consumed. The sequence re-starts at the *CHSEL1_START_ADDR* when the next LS_START pulse is detected.

7.3.14.11 Instruction Execution Time

Each instruction takes one clock cycle to execute with the exception of JMP and EEQ which require two clock cycles. The SWP instructions takes at least 9 clock cycles. With the exceptions of the CXE and DXE commands, the level shifter outputs remain unchanged during the execution time, i.e. the current pattern state is extended by the number of clock cycles shown Table 2 in while a given instruction is being executed. There is a 2 clock cycle time delay between incrementing the address counter and a HV output toggling as shown in Figure 19.

Table 2. Instruction Execution Time

Instruction	Instruction Code	Execution time [SEQ_CLK cycles]
CXE	1	1
LOP	2	1
JMP	3	2
END	4	1
LDR	5	1
INC	6	1
EEQ	7	2
DXE	8	1
SWP	9	9 + <OVERLAP COUNT> + 2

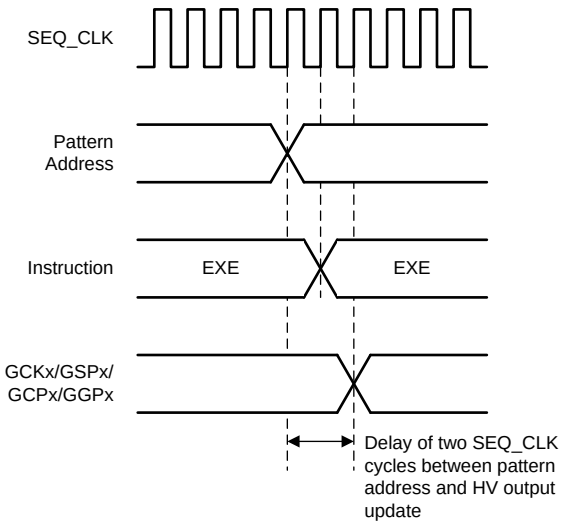


Figure 19. Level Shifter Output Latency

7.3.14.12 INIT Address and Pattern Address Overflow.

The pattern memory holds up to 54 instructions with logical addresses from 0 to 53. Upon detection a rising edge of the LS_START signal, the pattern start address is reset to the START_ADDR in the *CHSEL1_START_ADDR* register. If, however, START_ADDR is greater than 53, the pattern sequence terminates immediately, similar to executing an END instruction. If during normal operation the logical address should overflow, the address counter remains set to 53 and is not further incremented. Any instruction stored at address 53 may be executed multiple times until the next LS_START pulse is detected and the address counter is reset to the START_ADDR value. An exception to this rule is the JMP and EEQ instruction which terminate the sequence immediately if the target address is >53. See respective instruction description for detail.

7.3.14.13 Preset and START

The address counter of the pattern sequencer is reset to the value stored in the CHSEL1_START_ADDR register on every rising edge of LS_START. At the same time, the signal generator is preset to the values defined in the *PRESET1* and *PRESET2* registers. Note that the preset registers contain values for master channels only and the same values are applied to master and slave channels.

The first level shifter output may toggle as soon as the seventh rising edge of SEQ_CLK after LS_START is high.

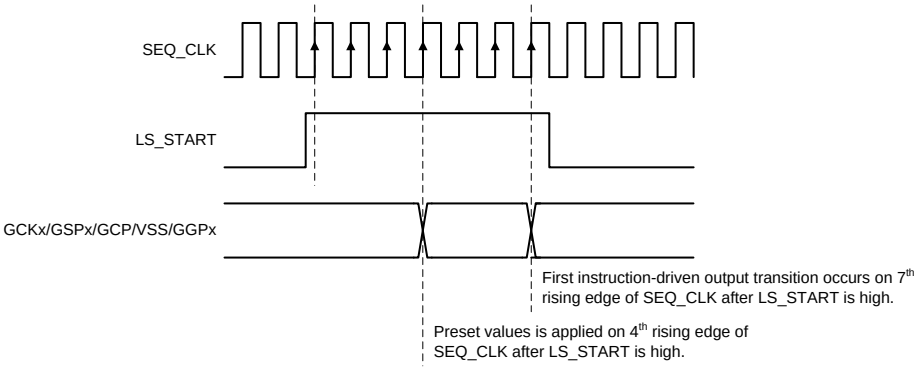


Figure 20. Sequence Start Timing.

7.3.14.14 Channel Selection and Output Gating

Each level shifter output can be selected or deselected prior pattern execution start or dynamically during run-time. If a channel is deselected prior to pattern execution start, it remains in its power-up default state, which is HiZ. If a channel is deselected during run-time, it holds its current state, i.e. the output is frozen and stops toggling. When a deselected channel is selected, it resumes toggling on the next clock cycle. Channel selection bits are located in the *CHSEL1_START_ADDR* register for GCK7-8, *CHSEL2* register for GCK12-9 and GCK4-1 and CHSEL3 all other channels. Note that channel selection settings have no impact on succeeding channels, i.e. a master channel may be disabled without impacting a slave channel.

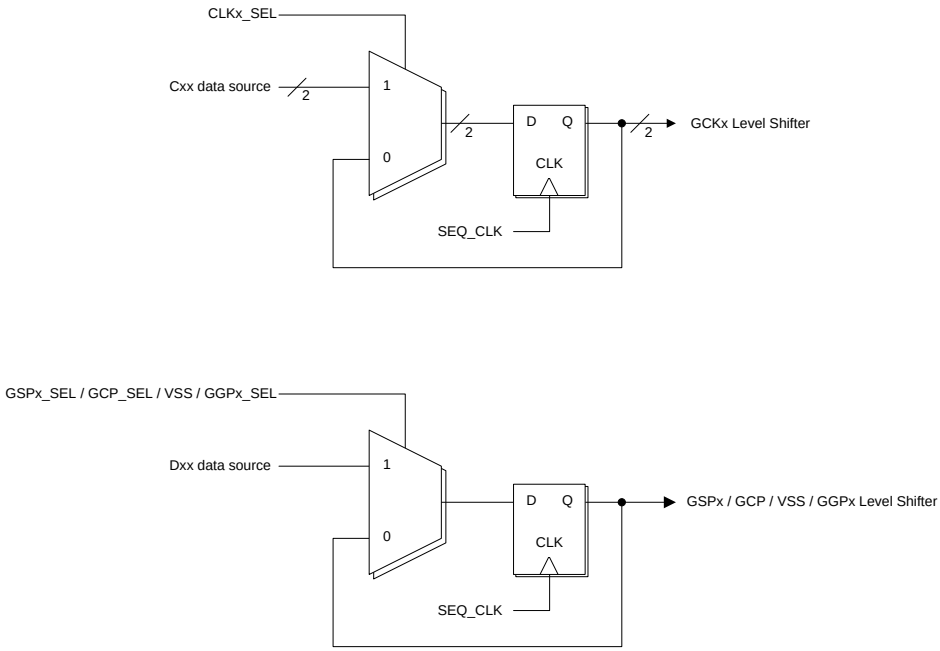


Figure 21. Channel Logic for GCKx Outputs (Top) and GSPx/GCP/GGPx Outputs (Bottom)

7.3.15 Loading Pattern Memory

A pattern sequence consists of up to 54 24-bit wide instructions with logical addresses 0 to 53. A single logical 24-bit wide instruction is mapped to three physical and consecutive 8-bit wide registers. See in for details. Loading a single instruction requires writing to three registers, an entire sequence requires writing up to 162 registers (54 instructions x 3 registers). An instruction or sequence may be updated in whole or in part. Error or syntax checking is not performed. To load a sequence into volatile memory:

1. Apply VIN while keeping the LS_CNTRL pin low.
2. Wait for 1ms.

3. Optional: Read the STATUS register to verify the device is in STANDBY state.
4. Write register data via the I^2C interface.

At this point the device is ready to execute a sequence. Apply the level shifter voltages, VGH, VGL1, VGL2 and pull the LS_CNTRL pin high to enter ACTIVE state and start the sequence.

For loading a pattern sequence into non-volatile memory, please refer to *Programming* section.

7.3.16 PLL

To stay in sync with the source driver data, a reference clock must be provided to the level shifter. This reference clock is typically the line clock, provided by the timing controller. The pattern sequencer, however, needs to run at a higher frequency to provide enough timing resolution to time the charge sharing or gate voltage shaping period, which is typically a fraction of the line time. This higher frequency is generated by the internal PLL. The PLL output frequency equals the input clock (LN_CLK) times the multiplication factor (MPL[2:0]). The multiplication factor is set by the MPL[2:0] bits of the *CONFIG1* register and recommended settings are shown below.

Table 3. Recommended PLL Multiplier Settings

DISPLAY LINE COUNT	REFRESH RATE [Hz]	LINE FREQUENCY [kHz]	LINE TIME [µs]	PLL MULTIPLIER	PLL OUTPUT FREQUENCY [MHz]	TIMING RESOLUTION [ns]
720	60	43.2	23.1	160	6.9	144
768	60	46.1	21.7		7.4	135
800	60	48.0	20.8		7.7	130
1050	60	63.0	15.9	128	8.1	124
1080	60	64.8	15.4		8.3	120
1200	60	72.0	13.9		9.2	108
1440	60	86.4	11.6	96	8.3	120
1600	60	96.0	10.4		9.2	108
2160	60	129.6	7.7	64	8.3	120
720	120	86.4	11.6	80	6.9	144
768	120	92.2	10.9		7.4	135
800	120	96.0	10.4		7.7	130
1050	120	126	7.9	64	8.1	124
1080	120	129.6	7.7		8.3	120
1200	120	144.0	6.9		9.2	108
1440	120	172.8	5.8	48	8.3	120
1600	120	192.0	5.2		9.2	108
2160	120	259.2	3.9	32	8.3	120

7.4 Device Functional Modes

This section describes the different modes of operation. The current state of the main state machine can be polled any time by reading the STATUS1 register.

Device Functional Modes (continued)

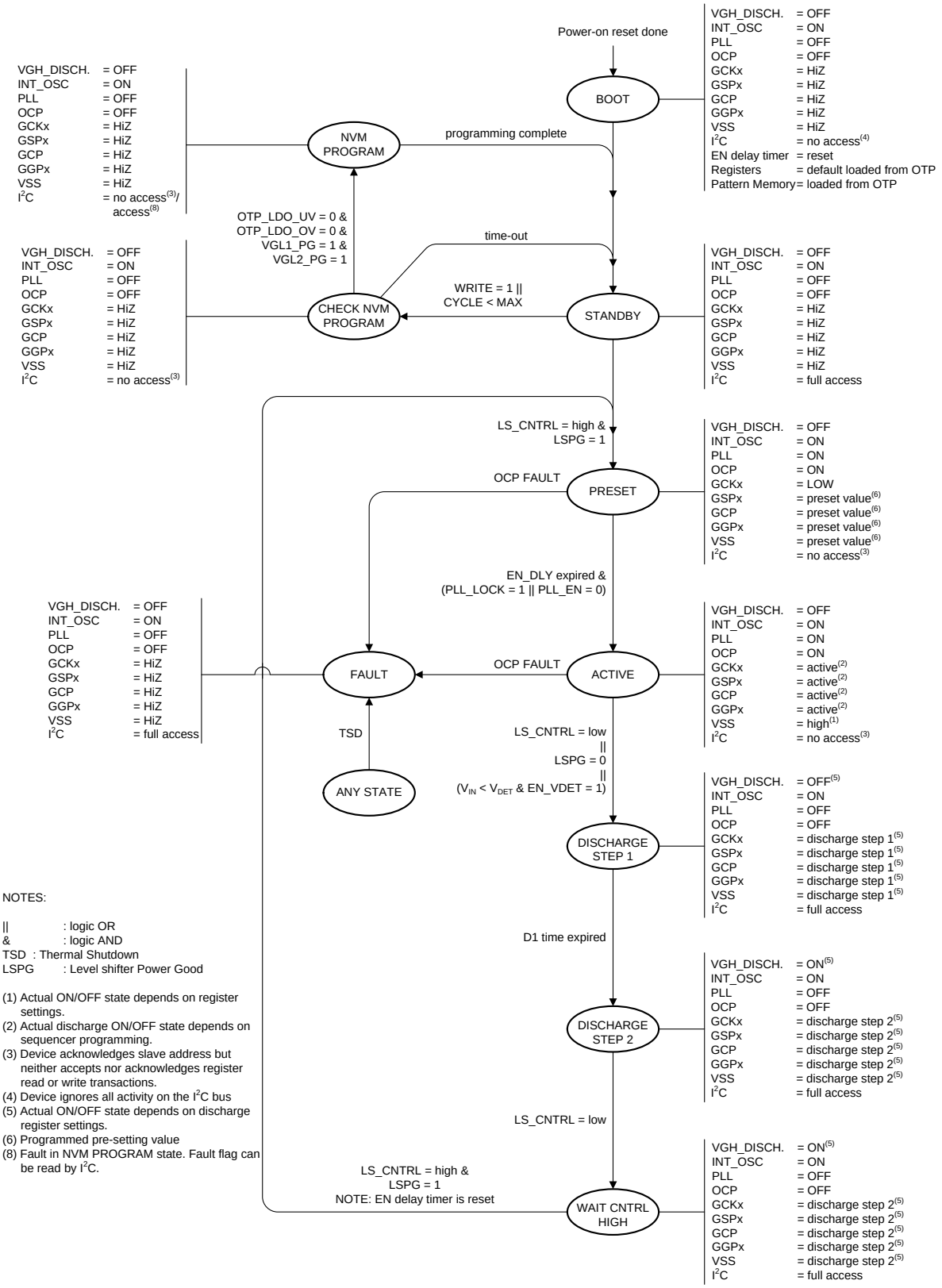


Figure 22. Functional State Diagram

Device Functional Modes (continued)

7.4.1 BOOT State

In BOOT state the logic core is reset and default values are loaded from non-volatile memory. BOOT state is entered upon V_{IN} rising above the $UVLO_{DVDD}$ threshold. No other input voltages are required at this stage. The I^2C interface is not responsive, i.e. it does not send an ACK when addressed while in BOOT state. After the boot phase is completed, the state machine advances to STANDBY state.

7.4.2 STANDBY State

In STANDBY state all level shifter output stages are in a HiZ state. All functions, including the sequencer program memory, can be configured via the I^2C interface. The device remains in STANDBY state as long as the LS_CNTRL pin is low, VGH, VGL1 and VGL2 are not powered up and the WRITE bit to program the non-volatile memory has not been set.

7.4.3 PRESET State

The device enters PRESET state when the LS_CNTRL pin is high and VGH, VGL1 and VGL2 level shifter supplies are in a valid operating range. All outputs change are enabled in a sequence by changing from HiZ state to the preset output level as defined in PRESET1 and PRESET2 registers. In PRESET, the I2C interface is not responsive, i.e. the device does accept any data and does not acknowledge any I^2C transaction even when address properly.

7.4.4 ACTIVE State

The device enters ACTIVE state when the LS_CNTRL pin is high, the EN_DLY counter has expired, and all level shifter supplies are in a valid operating range. The pattern sequencer is now operational and is driving the level shifter output stages according to the programmed pattern sequence. In ACTIVE, the I2C interface is not responsive, i.e. the device does accept any data and does not acknowledge any I^2C transaction even when address properly. Once in ACTIVE state, the device cannot return to STANDBY state but only advance to *DISCHARGE STEP1*.

7.4.5 DISCHARGE STEP1 State

The panel discharge sequence is triggered either by pulling the LS_CNTRL pin low, VIN dropping below the V_{DET} threshold, or one of the input signals dropping below its power-good threshold (LSPG = 0). The device enters DISCHARGE STEP1, the D1 timer is started, and all level shifter outputs, including VSS1, VSS2, and VGH active discharge are driven to the states defined by the *PNL_DCHx* registers. D1 time is set in *CONFIG2* register. After the D1 timer expires, the device enters *DISCHARGE STEP2* state.

7.4.6 DISCHARGE STEP2 State

This is the second and final panel-discharge state. All level shifter outputs, including VSS and VGH active discharge are driven to the states defined by the *PNL_DCH2* registers. The device remains in DISCHARGE STEP2 state until LS_CNTRL is pulled low at which point the device enters WAIT_CNTRL_HIGH state.

7.4.7 WAIT CNTRL HIGH State

The WAIT CNTRL HIGH state is functionally identical to DISCHARGE STEP2. When LS_CNTRL is pulled high, the EN_DLY counter is reset and the device returns to PRESET state. From there it will advance to ACTIVE state after the EN_DLY counter has expired. This allows to restart the sequence.

7.5 Programming

The TPS65680 contains one-time-programmable (OTP), non-volatile memory for storing configuration settings and pattern sequence. The device supports a minimum of three and a maximum of nine programming cycles, depending on the size of the pattern sequence. The programming voltage is generated by the internal OTP LDO which is supplied by VGH, therefore VGH must be applied to the IC prior to initiating the programming sequence.

Programming is initiated by setting the WRITE bit of the *NVM_CONTROL* register to 1. The OTP LDO is automatically enabled before the content of the register space is copied into non-volatile memory. After programing is complete, the OTP LDO is disabled, the WRITE bit is reset to 0, and the device returns to STANDBY state. If the OTP LDO fails to reach the desired programming voltage window within 100 ms of the WRITE bit being set, the device times out and returns to the STANDBY state without modifying the NVM. This case may occur if the OTP_LDO voltage is forced externally, VGH is not supplied, or VGH is below 10V.

To program the NVM:

1. Apply VIN and VGL1,2 while keeping the LS_CNTRL pin low.
2. Wait for 1ms.
3. Optional: Read the *STATUS1* register to verify the device is in STANDBY state.
4. Set the OTPLDO_EN bit of the *CONFIG2* register to 1 to enable the OTP LDO.
5. Write register data via the I^2C interface.
6. Apply VGH (>10V) if not already applied.
7. Set the WRITE bit of the *NVM_CONTROL* register to 1 to commit the configuration to NVM.
8. Wait for 100 ms.
9. Optional: Read the *STATUS1* register to verify the device is in STANDBY state.
10. Optional: Reset the OTPLDO_EN bit of the *CONFIG2* register to 0 to disable the OTP LDO.
11. Optional: Remove VGH.
12. Optional Power-cycle VIN
13. Optional: Wait 1ms.
14. Optional: Verify register content by reading all registers via I^2C.

Prior to initiating the programming sequence, a check is performed to ensure enough memory is available to hold the new settings, and the device has been programmed less than 9 times. In addition, the OTP_LDO output voltage is monitored to make sure it is within a defined range. If not enough memory is available, no programing cycle is left, or the programming voltage is incorrect, the device returns to STANDBY mode without changing the memory content, and the OTP_FAULT bit is set in the STATUS2 register.

7.5.1 I^2C Bus Operation

The I^2C bus is a communications link between a master and a series of slave devices. The link is established using a two-wired bus consisting of a serial clock signal (SCL) and a serial data signal (SDA). The serial clock is sourced from the master in all cases where the serial data line is bi-directional for data communication between the master and the slave terminals. Each device has an open-drain output to transmit data on the serial data line (SDA). An external pull-up resistor must be placed on the serial data line to pull the drain output high during data transmission. The TPS65680 has an I^2C slave interface that supports standard-mode (100 kbit/s), fast-mode (400 kbit/s) and fast-mode plus (1 Mbit/s), and auto-increment addressing compatible with the I^2C standard 3.0.

Data transmission is initiated with a start bit from the controller as shown in Figure 23. The start condition is recognized when the SDA line transitions from high to low during the high portion of the SCL signal. Upon reception of a start bit, the device will receive serial data on the SDA input and check for valid address and control information. If the slave address bits are set for the device, then the device issues an acknowledge pulse and prepares the receive of register address and data. Data transmission is completed by either the reception of a stop condition or the reception of the data word sent to the device. A stop condition is recognized as a low to high transition of the SDA input during the high portion of the SCL signal. All other transitions of the SDA line must occur during the low portion of the SCL signal. An acknowledge is issued after the reception of valid address, sub-address and data words. The I^2C interfaces will auto-sequence through register addresses, so that multiple data words can be sent for a given I^2C transmission.

Programming (continued)

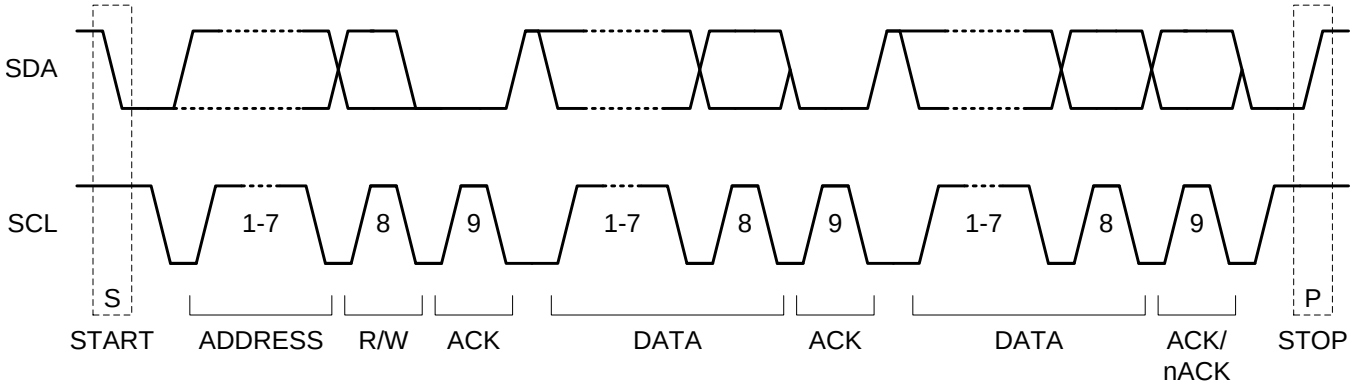


Figure 23. I²C START / STOP / ACKNOWLEDGE Protocol

7.5.1.1 Clock Stretching

Clock stretching pauses a transaction by holding the SCL line LOW. The transaction cannot continue until the line is released HIGH again. Clock stretching occurs under the following conditions:

- The device is addressed (read or write) while programming the internal non-volatile memory. The SCA pin in actively pulled low until programming is completed or the programming cycles times out.
- The internal clock frequency is set to 1MHz and the I²C bus operates in fast-mode plus at 1MHz clock frequency. The device is be able to receive bytes of data at a fast rate, but may need more time to store a received byte or prepare another byte to be transmitted. The slaves can then hold the SCL line LOW after reception and acknowledgment of a byte to force the master into a wait state until the slave is ready for the next byte transfer in a type of handshake procedure.

7.5.1.2 Data Transfer Formats

TPS65680 supports six different read/write operations:

- Single read from a defined register address.
- Sequential read starting from a defined register address.
- Single write to a defined register address.
- Sequential write starting from a defined register address.

All six transactions are described in detail below.

7.5.1.2.1 Single READ from a Defined Register Address

Figure 24 shows the format of a single read from a defined register address. First, the master issues a start condition followed by a seven-bit I²C address. Next, the master writes a zero to signify that it conducts a write operation. Upon receiving an acknowledge from the slave, the master sends the eight-bit register address across the bus. Following a second acknowledge TPS65680 sets the internal I²C register number to the defined value. Then the master issues a repeat start condition and the seven-bit I²C address followed by a one to signify that it conducts a read operation. Upon receiving a third acknowledge, the master releases the bus to the TPS65680. The TPS65680 then returns the eight-bit data value from the register on the bus. The master does not acknowledge (nACK) and issues a stop condition. This action concludes the register read.

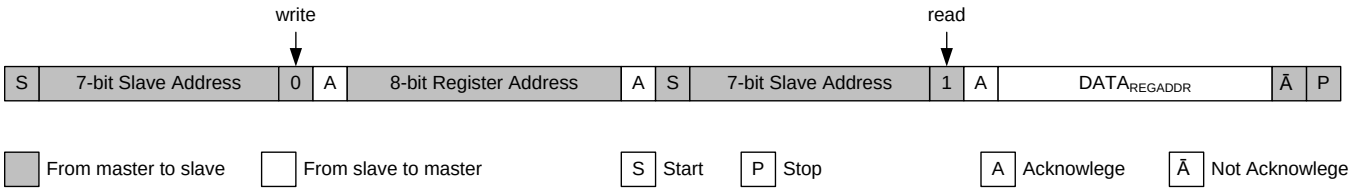


Figure 24. Single READ from a Defined Register Address.

Programming (continued)

7.5.1.2.2 Sequential READ, Starting from a Defined Register Address

A sequential read operation is an extension of the single read protocol and shown in Figure 25. The master acknowledges the reception of a data byte, TPS65680 auto increments the register address, and returns the data from the next register. The data transfer is stopped by the master not acknowledging the last data byte and sending a stop condition.

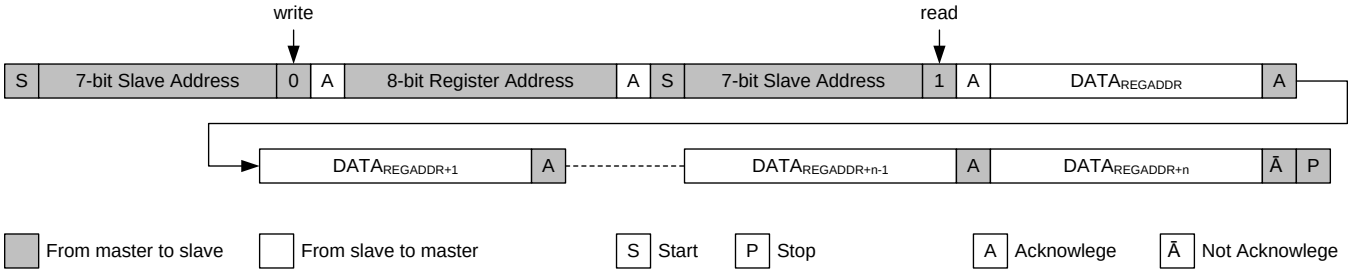


Figure 25. Sequential READ, Starting from a Defined Register Address.

7.5.1.2.3 Single WRITE to a Defined Register Address

Figure 26 shows the format of a single write to a defined register address. First, the master issues a start condition, followed by a seven-bit I^2C address. Next, the master writes a zero to signify that it wishes to conduct a write operation. Upon receiving an acknowledge from the slave, the master sends the eight-bit register address across the bus. Following a second acknowledge, TPS65680 sets the I^2C register address to the defined value and the master writes the eight-bit data value. Upon receiving a third acknowledge, TPS65680 auto increments the I^2C register address by one and the master issues a stop condition. This action concludes the register write.

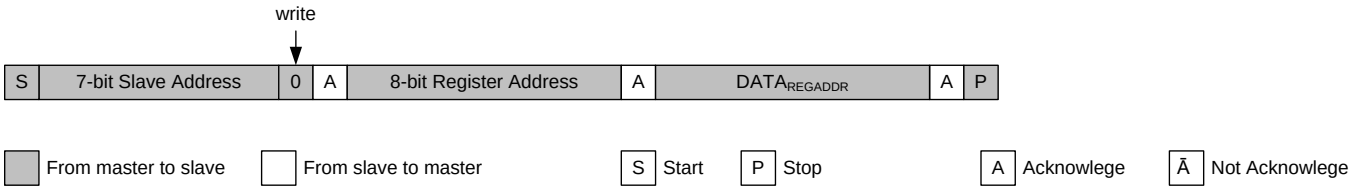


Figure 26. Single WRITE to Defined Register Address.

7.5.1.2.4 Sequential WRITE, Starting from a Defined Register Address

A sequential write operation is an extension of the single write protocol and shown in Figure 27. If the master doesn't send a stop condition after TPS65680 has issued an ACK, TPS65680 auto increments the register address by one and the master can write to the next register.

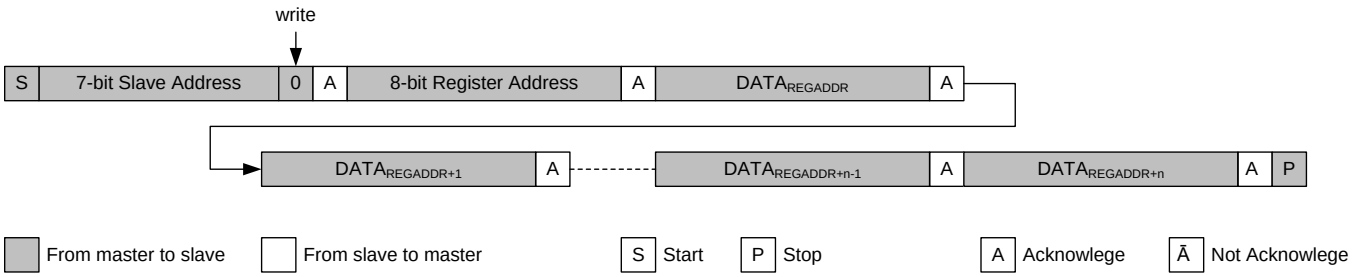


Figure 27. Sequential WRITE, Starting from a Defined Register Address.

7.6 Register Map

7.6.1 Register Description

7.6.1.1 Register Map

SLAVE ADDRESS	REGISTER ADDRESS	REGISTER NAME	FACTORY DEFAULT	DESCRIPTION
0b100001x	0x00	STATUS1	0x00	Read out status of main state machine
0b100001x	0x01	STATUS2	0x00	Read out status of main state machine
0b100001x	0x02	FAULT	0x00	Read out status of main state machine
0b100001x	0x03	CONFIG1	0x00	General device configuration bits
0b100001x	0x04	CONFIG2	0x00	General device configuration bits
0b100001x	0x05	OCP_SNS_DLY1	0x00	OCP configuration bits
0b100001x	0x06	OCP_SNS_DLY2	0x00	OCP configuration bits
0b100001x	0x07	OCP_CH_SEL1	0xFF	Contains OCP channel selection bits for GCK1-4 and GCK9-12
0b100001x	0x08	OCP_CH_SEL2	0xFF	OCP Channel select for GCK5-8, GCP, VSS and GGP1-2
0b100001x	0x09	OCP_CH_SEL3	0x03	OCP Channel select for GSP1-2 outputs. Configuration for SNS_LVL and RCVRY_CNT
0b100001x	0x0A	OCP_ALARM1	0x00	Contains the OCP alarm settings for the GCK1-12 channels
0b100001x	0x0B	OCP_ALARM2	0x00	Contains the OCP alarm settings for Control Channels
0b100001x	0x0C	EN_DLY	0x00	Internal LS enable delay counter
0b100001x	0x0D	FWID	0x00	Contains Firmware identification code.
0b100001x	0x0E	PNL_DCH1	0x00	Panel discharge step 1 definition
0b100001x	0x0F	PNL_DCH2	0x00	Panel discharge step 2 definition
0b100001x	0x10	C1256_SEP	0x00	C1, C2, C5, C6 separation setting.
0b100001x	0x11	C34_SEP	0x00	C3, C4 separation setting.
0b100001x	0x12	D1_SEP	0x00	D1 separation setting.
0b100001x	0x13	D2_SEP	0x00	D2 separation setting.
0b100001x	0x14	SPARE1	0x00	
0b100001x	0x15	SPARE2	0x00	
0b100001x	0x30	MUX1	0x00	Data source MUX for GGPx
0b100001x	0x31	MUX2	0x00	Data source MUX for GGPx
0b100001x	0x32	MUX3	0x00	Data source MUX for GGPx
0b100001x	0x33	MUX4	0x00	Data source MUX for GGPx
0b100001x	0x34	CHSEL1_START_ADDR	0x00	Contains channel selection bits fir GCK7-8 and pattern start address
0b100001x	0x35	CHSEL2	0x00	Contains channel selection bits for GCK1-4 and GCK9-12
0b100001x	0x36	CHSEL3	0x00	Channel select for GSP, GCP, GGP, and GCK5-6 outputs
0b100001x	0x37	PRESET1	0x00	Preset values for clock channels
0b100001x	0x38	PRESET2	0x00	Preset values for control channels
0b100001x	0x39	DATA1	0x00	Data register that can be updated by sequencer, with programmable default.
0b100001x	0x3A	DATA2	0x00	Data register that can be updated by sequencer, with programmable default.
0b100001x	0x3B	DATA3	0x00	Data register that can be updated by sequencer.
0b100001x	0x3C	DATA4	0x00	Data register that can be updated by sequencer.
0b100001x	0x3D	DATA5	0x00	Data register that can be updated by sequencer.
0b100001x	0x40	INSTRUCTION_0_0	0x00	Instruction_0 word

Register Map (continued)

SLAVE ADDRESS	REGISTER ADDRESS	REGISTER NAME	FACTORY DEFAULT	DESCRIPTION
0b100001x	0x41	INSTRUCTION_0_1	0x00	Instruction_0 word
0b100001x	0x42	INSTRUCTION_0_2	0x00	Instruction_0 word
0b100001x	0x43	INSTRUCTION_1_0	0x00	Instruction_1 word
0b100001x	0x44	INSTRUCTION_1_1	0x00	Instruction_1 word
0b100001x	0x45	INSTRUCTION_1_2	0x00	Instruction_1 word
0b100001x	0x46	INSTRUCTION_2_0	0x00	Instruction_2 word
0b100001x	0x47	INSTRUCTION_2_1	0x00	Instruction_2 word
0b100001x	0x48	INSTRUCTION_2_2	0x00	Instruction_2 word
0b100001x	0x49	INSTRUCTION_3_0	0x00	Instruction_3 word
0b100001x	0x4A	INSTRUCTION_3_1	0x00	Instruction_3 word
0b100001x	0x4B	INSTRUCTION_3_2	0x00	Instruction_3 word
0b100001x	0x4C	INSTRUCTION_4_0	0x00	Instruction_4 word
0b100001x	0x4D	INSTRUCTION_4_1	0x00	Instruction_4 word
0b100001x	0x4E	INSTRUCTION_4_2	0x00	Instruction_4 word
0b100001x	0x4F	INSTRUCTION_5_0	0x00	Instruction_5 word
0b100001x	0x50	INSTRUCTION_5_1	0x00	Instruction_5 word
0b100001x	0x51	INSTRUCTION_5_2	0x00	Instruction_5 word
0b100001x	0x52	INSTRUCTION_6_0	0x00	Instruction_6 word
0b100001x	0x53	INSTRUCTION_6_1	0x00	Instruction_6 word
0b100001x	0x54	INSTRUCTION_6_2	0x00	Instruction_6 word
0b100001x	0x55	INSTRUCTION_7_0	0x00	Instruction_7 word
0b100001x	0x56	INSTRUCTION_7_1	0x00	Instruction_7 word
0b100001x	0x57	INSTRUCTION_7_2	0x00	Instruction_7 word
0b100001x	0x58	INSTRUCTION_8_0	0x00	Instruction_8 word
0b100001x	0x59	INSTRUCTION_8_1	0x00	Instruction_8 word
0b100001x	0x5A	INSTRUCTION_8_2	0x00	Instruction_8 word
0b100001x	0x5B	INSTRUCTION_9_0	0x00	Instruction_9 word
0b100001x	0x5C	INSTRUCTION_9_1	0x00	Instruction_9 word
0b100001x	0x5D	INSTRUCTION_9_2	0x00	Instruction_9 word
0b100001x	0x5E	INSTRUCTION_10_0	0x00	Instruction_10 word
0b100001x	0x5F	INSTRUCTION_10_1	0x00	Instruction_10 word
0b100001x	0x60	INSTRUCTION_10_2	0x00	Instruction_10 word
0b100001x	0x61	INSTRUCTION_11_0	0x00	Instruction_11 word
0b100001x	0x62	INSTRUCTION_11_1	0x00	Instruction_11 word
0b100001x	0x63	INSTRUCTION_11_2	0x00	Instruction_11 word
0b100001x	0x64	INSTRUCTION_12_0	0x00	Instruction_12 word
0b100001x	0x65	INSTRUCTION_12_1	0x00	Instruction_12 word
0b100001x	0x66	INSTRUCTION_12_2	0x00	Instruction_12 word
0b100001x	0x67	INSTRUCTION_13_0	0x00	Instruction_13 word
0b100001x	0x68	INSTRUCTION_13_1	0x00	Instruction_13 word
0b100001x	0x69	INSTRUCTION_13_2	0x00	Instruction_13 word
0b100001x	0x6A	INSTRUCTION_14_0	0x00	Instruction_14 word
0b100001x	0x6B	INSTRUCTION_14_1	0x00	Instruction_14 word
0b100001x	0x6C	INSTRUCTION_14_2	0x00	Instruction_14 word
0b100001x	0x6D	INSTRUCTION_15_0	0x00	Instruction_15 word
0b100001x	0x6E	INSTRUCTION_15_1	0x00	Instruction_15 word

Register Map (continued)

SLAVE ADDRESS	REGISTER ADDRESS	REGISTER NAME	FACTORY DEFAULT	DESCRIPTION
0b100001x	0x6F	INSTRUCTION_15_2	0x00	Instruction_15 word
0b100001x	0x70	INSTRUCTION_16_0	0x00	Instruction_16 word
0b100001x	0x71	INSTRUCTION_16_1	0x00	Instruction_16 word
0b100001x	0x72	INSTRUCTION_16_2	0x00	Instruction_16 word
0b100001x	0x73	INSTRUCTION_17_0	0x00	Instruction_17 word
0b100001x	0x74	INSTRUCTION_17_1	0x00	Instruction_17 word
0b100001x	0x75	INSTRUCTION_17_2	0x00	Instruction_17 word
0b100001x	0x76	INSTRUCTION_18_0	0x00	Instruction_18 word
0b100001x	0x77	INSTRUCTION_18_1	0x00	Instruction_18 word
0b100001x	0x78	INSTRUCTION_18_2	0x00	Instruction_18 word
0b100001x	0x79	INSTRUCTION_19_0	0x00	Instruction_19 word
0b100001x	0x7A	INSTRUCTION_19_1	0x00	Instruction_19 word
0b100001x	0x7B	INSTRUCTION_19_2	0x00	Instruction_19 word
0b100001x	0x7C	INSTRUCTION_20_0	0x00	Instruction_20 word
0b100001x	0x7D	INSTRUCTION_20_1	0x00	Instruction_20 word
0b100001x	0x7E	INSTRUCTION_20_2	0x00	Instruction_20 word
0b100001x	0x7F	INSTRUCTION_21_0	0x00	Instruction_21 word
0b100001x	0x80	INSTRUCTION_21_1	0x00	Instruction_21 word
0b100001x	0x81	INSTRUCTION_21_2	0x00	Instruction_21 word
0b100001x	0x82	INSTRUCTION_22_0	0x00	Instruction_22 word
0b100001x	0x83	INSTRUCTION_22_1	0x00	Instruction_22 word
0b100001x	0x84	INSTRUCTION_22_2	0x00	Instruction_22 word
0b100001x	0x85	INSTRUCTION_23_0	0x00	Instruction_23 word
0b100001x	0x86	INSTRUCTION_23_1	0x00	Instruction_23 word
0b100001x	0x87	INSTRUCTION_23_2	0x00	Instruction_23 word
0b100001x	0x88	INSTRUCTION_24_0	0x00	Instruction_24 word
0b100001x	0x89	INSTRUCTION_24_1	0x00	Instruction_24 word
0b100001x	0x8A	INSTRUCTION_24_2	0x00	Instruction_24 word
0b100001x	0x8B	INSTRUCTION_25_0	0x00	Instruction_25 word
0b100001x	0x8C	INSTRUCTION_25_1	0x00	Instruction_25 word
0b100001x	0x8D	INSTRUCTION_25_2	0x00	Instruction_25 word
0b100001x	0x8E	INSTRUCTION_26_0	0x00	Instruction_26 word
0b100001x	0x8F	INSTRUCTION_26_1	0x00	Instruction_26 word
0b100001x	0x90	INSTRUCTION_26_2	0x00	Instruction_26 word
0b100001x	0x91	INSTRUCTION_27_0	0x00	Instruction_27 word
0b100001x	0x92	INSTRUCTION_27_1	0x00	Instruction_27 word
0b100001x	0x93	INSTRUCTION_27_2	0x00	Instruction_27 word
0b100001x	0x94	INSTRUCTION_28_0	0x00	Instruction_28 word
0b100001x	0x95	INSTRUCTION_28_1	0x00	Instruction_28 word
0b100001x	0x96	INSTRUCTION_28_2	0x00	Instruction_28 word
0b100001x	0x97	INSTRUCTION_29_0	0x00	Instruction_29 word
0b100001x	0x98	INSTRUCTION_29_1	0x00	Instruction_29 word
0b100001x	0x99	INSTRUCTION_29_2	0x00	Instruction_29 word
0b100001x	0x9A	INSTRUCTION_30_0	0x00	Instruction_30 word
0b100001x	0x9B	INSTRUCTION_30_1	0x00	Instruction_30 word
0b100001x	0x9C	INSTRUCTION_30_2	0x00	Instruction_30 word

Register Map (continued)

SLAVE ADDRESS	REGISTER ADDRESS	REGISTER NAME	FACTORY DEFAULT	DESCRIPTION
0b100001x	0x9D	INSTRUCTION_31_0	0x00	Instruction_31 word
0b100001x	0x9E	INSTRUCTION_31_1	0x00	Instruction_31 word
0b100001x	0x9F	INSTRUCTION_31_2	0x00	Instruction_31 word
0b100001x	0xA0	INSTRUCTION_32_0	0x00	Instruction_32 word
0b100001x	0xA1	INSTRUCTION_32_1	0x00	Instruction_32 word
0b100001x	0xA2	INSTRUCTION_32_2	0x00	Instruction_32 word
0b100001x	0xA3	INSTRUCTION_33_0	0x00	Instruction_33 word
0b100001x	0xA4	INSTRUCTION_33_1	0x00	Instruction_33 word
0b100001x	0xA5	INSTRUCTION_33_2	0x00	Instruction_33 word
0b100001x	0xA6	INSTRUCTION_34_0	0x00	Instruction_34 word
0b100001x	0xA7	INSTRUCTION_34_1	0x00	Instruction_34 word
0b100001x	0xA8	INSTRUCTION_34_2	0x00	Instruction_34 word
0b100001x	0xA9	INSTRUCTION_35_0	0x00	Instruction_35 word
0b100001x	0xAA	INSTRUCTION_35_1	0x00	Instruction_35 word
0b100001x	0xAB	INSTRUCTION_35_2	0x00	Instruction_35 word
0b100001x	0xAC	INSTRUCTION_36_0	0x00	Instruction_36 word
0b100001x	0xAD	INSTRUCTION_36_1	0x00	Instruction_36 word
0b100001x	0xAE	INSTRUCTION_36_2	0x00	Instruction_36 word
0b100001x	0xAF	INSTRUCTION_37_0	0x00	Instruction_37 word
0b100001x	0xB0	INSTRUCTION_37_1	0x00	Instruction_37 word
0b100001x	0xB1	INSTRUCTION_37_2	0x00	Instruction_37 word
0b100001x	0xB2	INSTRUCTION_38_0	0x00	Instruction_38 word
0b100001x	0xB3	INSTRUCTION_38_1	0x00	Instruction_38 word
0b100001x	0xB4	INSTRUCTION_38_2	0x00	Instruction_38 word
0b100001x	0xB5	INSTRUCTION_39_0	0x00	Instruction_39 word
0b100001x	0xB6	INSTRUCTION_39_1	0x00	Instruction_39 word
0b100001x	0xB7	INSTRUCTION_39_2	0x00	Instruction_39 word
0b100001x	0xB8	INSTRUCTION_40_0	0x00	Instruction_40 word
0b100001x	0xB9	INSTRUCTION_40_1	0x00	Instruction_40 word
0b100001x	0xBA	INSTRUCTION_40_2	0x00	Instruction_40 word
0b100001x	0xBB	INSTRUCTION_41_0	0x00	Instruction_41 word
0b100001x	0xBC	INSTRUCTION_41_1	0x00	Instruction_41 word
0b100001x	0xBD	INSTRUCTION_41_2	0x00	Instruction_41 word
0b100001x	0xBE	INSTRUCTION_42_0	0x00	Instruction_42 word
0b100001x	0xBF	INSTRUCTION_42_1	0x00	Instruction_42 word
0b100001x	0xC0	INSTRUCTION_42_2	0x00	Instruction_42 word
0b100001x	0xC1	INSTRUCTION_43_0	0x00	Instruction_43 word
0b100001x	0xC2	INSTRUCTION_43_1	0x00	Instruction_43 word
0b100001x	0xC3	INSTRUCTION_43_2	0x00	Instruction_43 word
0b100001x	0xC4	INSTRUCTION_44_0	0x00	Instruction_44 word
0b100001x	0xC5	INSTRUCTION_44_1	0x00	Instruction_44 word
0b100001x	0xC6	INSTRUCTION_44_2	0x00	Instruction_44 word
0b100001x	0xC7	INSTRUCTION_45_0	0x00	Instruction_45 word
0b100001x	0xC8	INSTRUCTION_45_1	0x00	Instruction_45 word
0b100001x	0xC9	INSTRUCTION_45_2	0x00	Instruction_45 word
0b100001x	0xCA	INSTRUCTION_46_0	0x00	Instruction_46 word

Register Map (continued)

SLAVE ADDRESS	REGISTER ADDRESS	REGISTER NAME	FACTORY DEFAULT	DESCRIPTION
0b100001x	0xCB	INSTRUCTION_46_1	0x00	Instruction_46 word
0b100001x	0xCC	INSTRUCTION_46_2	0x00	Instruction_46 word
0b100001x	0xCD	INSTRUCTION_47_0	0x00	Instruction_47 word
0b100001x	0xCE	INSTRUCTION_47_1	0x00	Instruction_47 word
0b100001x	0xCF	INSTRUCTION_47_2	0x00	Instruction_47 word
0b100001x	0xD0	INSTRUCTION_48_0	0x00	Instruction_48 word
0b100001x	0xD1	INSTRUCTION_48_1	0x00	Instruction_48 word
0b100001x	0xD2	INSTRUCTION_48_2	0x00	Instruction_48 word
0b100001x	0xD3	INSTRUCTION_49_0	0x00	Instruction_49 word
0b100001x	0xD4	INSTRUCTION_49_1	0x00	Instruction_49 word
0b100001x	0xD5	INSTRUCTION_49_2	0x00	Instruction_49 word
0b100001x	0xD6	INSTRUCTION_50_0	0x00	Instruction_50 word
0b100001x	0xD7	INSTRUCTION_50_1	0x00	Instruction_50 word
0b100001x	0xD8	INSTRUCTION_50_2	0x00	Instruction_50 word
0b100001x	0xD9	INSTRUCTION_51_0	0x00	Instruction_51 word
0b100001x	0xDA	INSTRUCTION_51_1	0x00	Instruction_51 word
0b100001x	0xDB	INSTRUCTION_51_2	0x00	Instruction_51 word
0b100001x	0xDC	INSTRUCTION_52_0	0x00	Instruction_52 word
0b100001x	0xDD	INSTRUCTION_52_1	0x00	Instruction_52 word
0b100001x	0xDE	INSTRUCTION_52_2	0x00	Instruction_52 word
0b100001x	0xDF	INSTRUCTION_53_0	0x00	Instruction_53 word
0b100001x	0xE0	INSTRUCTION_53_1	0x00	Instruction_53 word
0b100001x	0xE1	INSTRUCTION_53_2	0x00	Instruction_53 word
0b100001x	0xF0	PMICID	0x65	Contains PMIC identification code.
0b100001x	0xF1	REVID	0x01	Revision identification code
0b100001x	0xF2	NVM_COUNT1	0x00	NVM byte count, programming cycle 1
0b100001x	0xF3	NVM_COUNT2	0x00	NVM byte count, programming cycle 2
0b100001x	0xF4	NVM_COUNT3	0x00	NVM byte count, programming cycle 3
0b100001x	0xF5	NVM_COUNT4	0x00	NVM byte count, programming cycle 4
0b100001x	0xF6	NVM_COUNT5	0x00	NVM byte count, programming cycle 5
0b100001x	0xF7	NVM_COUNT6	0x00	NVM byte count, programming cycle 6
0b100001x	0xF8	NVM_COUNT7	0x00	NVM byte count, programming cycle 7
0b100001x	0xF9	NVM_COUNT8	0x00	NVM byte count, programming cycle 8
0b100001x	0xFA	NVM_COUNT9	0x00	NVM byte count, programming cycle 9
0b100001x	0xFF	NVM_CONTROL	0x00	NVM programming control

7.6.1.2 Register STATUS1 (slave address: 0b100001x; register address: 0x00; default: 0x00)

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Figure 28. Register STATUS1 Format

7	6	5	4	3	2	1	0
NIL	WAIT_CNTRL_HIGH	FAULT	DISCHARGE2	DISCHARGE1	ACTIVE	PRESET	STANDBY
R	R	R	R	R	R	R	R
--	--	--	--	--	--	--	--

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 4. Register STATUS1 Field Descriptions

Bit	Field	Type	Reset	Description
7	NIL	R	0	This bit is not implemented in hardware. During write operations data for this bit is ignored. During read operations 0 is returned.
6	WAIT_CNTRL_HIGH	R	0	Is "1" if main state machine is in WAIT_EN state
5	FAULT	R	0	Is "1" if main state machine is in FAULT state
4	DISCHARGE2	R	0	Is "1" if main state machine is in DISCHARGE2 state
3	DISCHARGE1	R	0	Is "1" if main state machine is in DISCHARGE1 state
2	ACTIVE	R	0	Is "1" if main state machine is in ACTIVE state
1	PRESET	R	0	Is "1" if main state machine is in PRESET state
0	STANDBY	R	0	Is "1" if main state machine is in STANDBY state

7.6.1.3 Register STATUS2 (slave address: 0b100001x; register address: 0x01; default: 0x00)

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Figure 29. Register STATUS2 Format

7	6	5	4	3	2	1	0
NIL[3:0]				OTP_FLAG3	OTP_FLAG2	OTP_FLAG1	OTP_FLAG0
R				R	R	R	R
--				--	--	--	--

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 5. Register STATUS2 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	NIL[3:0]	R	0000	This bit is not implemented in hardware. During write operations data for this bit is ignored. During read operations 0 is returned.
3	OTP_FLAG3	R	0	OTP Flag 3 **0 : Device is functioning normal** 1 : During programming the OTP power good has dropped
2	OTP_FLAG2	R	0	OTP Flag 2 **0 : Device is functioning normal** 1 : Device reached max number of programming cycles (max = 9 times)
1	OTP_FLAG1	R	0	OTP Flag 1 **0 : Device is functioning normal** 1 : Not enough memory to execute programming cycle
0	OTP_FLAG0	R	0	OTP Flag 0 **0 : Device is functioning normal** 1 : OTP LDO has not reached desired programming voltage window

7.6.1.4 Register FAULT (slave address: 0b100001x; register address: 0x02; default: 0x00)

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Figure 30. Register FAULT Format

7	6	5	4	3	2	1	0
NIL[4:0]					OCP_FAULT2	OCP_FAULT1	TSD_FAULT
R					R	R	R
--					--	--	--

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 6. Register FAULT Field Descriptions

Bit	Field	Type	Reset	Description
7:3	NIL[4:0]	R	00000	This bit is not implemented in hardware. During write operations data for this bit is ignored. During read operations 0 is returned.
2	OCP_FAULT2	R	0	OCP fault detected in GSP1-2, GCP, VSS and GGP1-2 channels **0 : Device is functioning normal** 1 : Device detected over-current condition (OCP)
1	OCP_FAULT1	R	0	OCP fault detected in GCK1-12 channels **0 : Device is functioning normal** 1 : Device detected over-current condition (OCP)
0	TSD_FAULT	R	0	Thermal-shutdown indication bit **0 : Device is functioning normal** 1 : Device is in thermal shutdown

7.6.1.5 Register CONFIG1 (slave address: 0b100001x; register address: 0x03; default: 0x00)

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Figure 31. Register CONFIG1 Format

7	6	5	4	3	2	1	0
PLL_BYPSS	MPL[2:0]			VDET[3:0]			
R/W	R/W			R/W			
OTP	OTP			OTP			

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 7. Register CONFIG1 Field Descriptions

Bit	Field	Type	Reset	Description
7	PLL_BYPSS	R/W	0	PLL can be bypassed if sequencer clock is provided at LN_CLK input. **0 : PLL is enabled** 1 : PLL is disabled and bypassed
6:4	MPL[2:0]	R/W	000	PLL Multiplication factor **000 : 16x** 001 : 32x 010 : 48x 011 : 64x 100 : 80x 101 : 96x 110 : 128x 111 : 160x
3:0	VDET[3:0]	R/W	0000	These bits configure the VIN voltage threshold for discharge step 1. **0000 : disabled** 0001 : 2.7V 0010 : 2.8V 0011 : 2.9V 0100 : 3.0V 0101 : 3.1V 0110 : 3.2V 0111 : 3.3V 1000 : 3.4V 1001 : 3.5V 1010 : 3.6V 1011 : 3.7V 1100 : 3.8V 1101 : 3.9V 1110 : 4.0V 1111 : 4.1V

7.6.1.6 Register CONFIG2 (slave address: 0b100001x; register address: 0x04; default: 0x00)

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Figure 32. Register CONFIG2 Format

7	6	5	4	3	2	1	0
OTPLDO_EN	OCP_VGL2	OCP_VGL1	OCP_VGH	FORCE_LSPG	D1_TIME[2:0]		
R/W	R/W	R/W	R/W	R/W	R/W		
OTP	OTP	OTP	OTP	OTP	OTP		

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 8. Register CONFIG2 Field Descriptions

Bit	Field	Type	Reset	Description
7	OTPLDO_EN	R/W	0	Enables OTP LDO **0 : disabled** 1 : enabled
6	OCP_VGL2	R/W	0	Enables OCP for VGL2 supply pin input. **0 : Over current sensing from VGL2 is disabled** 1 : Over current sensing from VGL2 is active
5	OCP_VGL1	R/W	0	Enables OCP for VGL1 supply pin input. **0 : Over current sensing from VGL1 is disabled** 1 : Over current sensing from VGL1 is active
4	OCP_VGH	R/W	0	Enables OCP for VGH supply pin input. **0 : Over current sensing from VGH is disabled** 1 : Over current sensing from VGH is active
3	FORCE_LSPG	R/W	0	Overrides input power-good detection. When enabled, LSPG signal is forced high independent of actual input voltage level. **0 : disabled** 1 : enabled
2:0	D1_TIME[2:0]	R/W	000	Defines the duration of panel discharge step 1. **000 : 1 ms** 001 : 2 ms 010 : 4 ms 011 : 8 ms 100 : 16 ms 101 : 32 ms 110 : 64 ms 111 : 128 ms

7.6.1.7 Register OCP_SNS_DLY1 (slave address: 0b100001x; register address: 0x05; default: 0x00)

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Figure 33. Register OCP_SNS_DLY1 Format

7	6	5	4	3	2	1	0
NIL	SNS_DLY1[6:0]						
R	R/W						
--	OTP						

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 9. Register OCP_SNS_DLY1 Field Descriptions

Bit	Field	Type	Reset	Description			
7	NIL	R	0	This bit is not implemented in hardware. During write operations data for this bit is ignored. During read operations 0 is returned.			
6:0	SNS_DLY1[6:0]	R/W	0000000	Current sensing delay in number of PLL output clock cycles (LS_CLOCK) after a GCKx clock channel switched			
				0000000 : 1 CLK 0000001 : 2 CLK 0000010 : 3 CLK 0000011 : 4 CLK 0000100 : 5 CLK 0000101 : 6 CLK 0000110 : 7 CLK 0000111 : 8 CLK 0001000 : 9 CLK 0001001 : 10 CLK 0001010 : 11 CLK 0001011 : 12 CLK 0001100 : 13 CLK 0001101 : 14 CLK 0001110 : 15 CLK 0001111 : 16 CLK 0010000 : 17 CLK 0010001 : 18 CLK 0010010 : 19 CLK 0010011 : 20 CLK 0010100 : 21 CLK 0010101 : 22 CLK 0010110 : 23 CLK 0010111 : 24 CLK 0011000 : 25 CLK 0011001 : 26 CLK 0011010 : 27 CLK 0011011 : 28 CLK 0011100 : 29 CLK 0011101 : 30 CLK 0011110 : 31 CLK 0011111 : 32 CLK	0100000 : 33 CLK 0100001 : 34 CLK 0100010 : 35 CLK 0100011 : 36 CLK 0100100 : 37 CLK 0100101 : 38 CLK 0100110 : 39 CLK 0100111 : 40 CLK 0101000 : 41 CLK 0101001 : 42 CLK 0101010 : 43 CLK 0101011 : 44 CLK 0101100 : 45 CLK 0101101 : 46 CLK 0101110 : 47 CLK 0101111 : 48 CLK 0110000 : 49 CLK 0110001 : 50 CLK 0110010 : 51 CLK 0110011 : 52 CLK 0110100 : 53 CLK 0110101 : 54 CLK 0110110 : 55 CLK 0110111 : 56 CLK 0111000 : 57 CLK 0111001 : 58 CLK 0111010 : 59 CLK 0111011 : 60 CLK 0111100 : 61 CLK 0111101 : 62 CLK 0111110 : 63 CLK 0111111 : 64 CLK	1000000 : 65 CLK 1000001 : 66 CLK 1000010 : 67 CLK 1000011 : 68 CLK 1000100 : 69 CLK 1000101 : 70 CLK 1000110 : 71 CLK 1000111 : 72 CLK 1001000 : 73 CLK 1001001 : 74 CLK 1001010 : 75 CLK 1001011 : 76 CLK 1001100 : 77 CLK 1001101 : 78 CLK 1001110 : 79 CLK 1001111 : 80 CLK 1010000 : 81 CLK 1010001 : 82 CLK 1010010 : 83 CLK 1010011 : 84 CLK 1010100 : 85 CLK 1010101 : 86 CLK 1010110 : 87 CLK 1010111 : 88 CLK 1011000 : 89 CLK 1011001 : 90 CLK 1011010 : 91 CLK 1011011 : 92 CLK 1011100 : 93 CLK 1011101 : 94 CLK 1011110 : 95 CLK 1011111 : 96 CLK	1100000 : 97 CLK 1100001 : 98 CLK 1100010 : 99 CLK 1100011 : 100 CLK 1100100 : 101 CLK 1100101 : 102 CLK 1100110 : 103 CLK 1100111 : 104 CLK 1101000 : 105 CLK 1101001 : 106 CLK 1101010 : 107 CLK 1101011 : 108 CLK 1101100 : 109 CLK 1101101 : 110 CLK 1101110 : 111 CLK 1101111 : 112 CLK 1110000 : 113 CLK 1110001 : 114 CLK 1110010 : 115 CLK 1110011 : 116 CLK 1110100 : 117 CLK 1110101 : 118 CLK 1110110 : 119 CLK 1110111 : 120 CLK 1111000 : 121 CLK 1111001 : 122 CLK 1111010 : 123 CLK 1111011 : 124 CLK 1111100 : 125 CLK 1111101 : 126 CLK 1111110 : 127 CLK 1111111 : 128 CLK

7.6.1.8 Register OCP_SNS_DLY2 (slave address: 0b100001x; register address: 0x06; default: 0x00)

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Figure 34. Register OCP_SNS_DLY2 Format

7	6	5	4	3	2	1	0
NIL	SNS_DLY2[6:0]						
R	R/W						
--	OTP						

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 10. Register OCP_SNS_DLY2 Field Descriptions

Bit	Field	Type	Reset	Description			
7	NIL	R	0	This bit is not implemented in hardware. During write operations data for this bit is ignored. During read operations 0 is returned.			
6:0	SNS_DLY2[6:0]	R/W	0000000	Current sensing delay in number of PLL output clock cycles (LS_CLOCK) after a GGPx, VSS, GCP or GGPx clock channel switched			
				0000000 : 1 CLK 0000001 : 2 CLK 0000010 : 3 CLK 0000011 : 4 CLK 0000100 : 5 CLK 0000101 : 6 CLK 0000110 : 7 CLK 0000111 : 8 CLK 0001000 : 9 CLK 0001001 : 10 CLK 0001010 : 11 CLK 0001011 : 12 CLK 0001100 : 13 CLK 0001101 : 14 CLK 0001110 : 15 CLK 0001111 : 16 CLK 0010000 : 17 CLK 0010001 : 18 CLK 0010010 : 19 CLK 0010011 : 20 CLK 0010100 : 21 CLK 0010101 : 22 CLK 0010110 : 23 CLK 0010111 : 24 CLK 0011000 : 25 CLK 0011001 : 26 CLK 0011010 : 27 CLK 0011011 : 28 CLK 0011100 : 29 CLK 0011101 : 30 CLK 0011110 : 31 CLK 0011111 : 32 CLK	0100000 : 33 CLK 0100001 : 34 CLK 0100010 : 35 CLK 0100011 : 36 CLK 0100100 : 37 CLK 0100101 : 38 CLK 0100110 : 39 CLK 0100111 : 40 CLK 0101000 : 41 CLK 0101001 : 42 CLK 0101010 : 43 CLK 0101011 : 44 CLK 0101100 : 45 CLK 0101101 : 46 CLK 0101110 : 47 CLK 0101111 : 48 CLK 0110000 : 49 CLK 0110001 : 50 CLK 0110010 : 51 CLK 0110011 : 52 CLK 0110100 : 53 CLK 0110101 : 54 CLK 0110110 : 55 CLK 0110111 : 56 CLK 0111000 : 57 CLK 0111001 : 58 CLK 0111010 : 59 CLK 0111011 : 60 CLK 0111100 : 61 CLK 0111101 : 62 CLK 0111110 : 63 CLK 0111111 : 64 CLK	1000000 : 65 CLK 1000001 : 66 CLK 1000010 : 67 CLK 1000011 : 68 CLK 1000100 : 69 CLK 1000101 : 70 CLK 1000110 : 71 CLK 1000111 : 72 CLK 1001000 : 73 CLK 1001001 : 74 CLK 1001010 : 75 CLK 1001011 : 76 CLK 1001100 : 77 CLK 1001101 : 78 CLK 1001110 : 79 CLK 1001111 : 80 CLK 1010000 : 81 CLK 1010001 : 82 CLK 1010010 : 83 CLK 1010011 : 84 CLK 1010100 : 85 CLK 1010101 : 86 CLK 1010110 : 87 CLK 1010111 : 88 CLK 1011000 : 89 CLK 1011001 : 90 CLK 1011010 : 91 CLK 1011011 : 92 CLK 1011100 : 93 CLK 1011101 : 94 CLK 1011110 : 95 CLK 1011111 : 96 CLK	1100000 : 97 CLK 1100001 : 98 CLK 1100010 : 99 CLK 1100011 : 100 CLK 1100100 : 101 CLK 1100101 : 102 CLK 1100110 : 103 CLK 1100111 : 104 CLK 1101000 : 105 CLK 1101001 : 106 CLK 1101010 : 107 CLK 1101011 : 108 CLK 1101100 : 109 CLK 1101101 : 110 CLK 1101110 : 111 CLK 1101111 : 112 CLK 1110000 : 113 CLK 1110001 : 114 CLK 1110010 : 115 CLK 1110011 : 116 CLK 1110100 : 117 CLK 1110101 : 118 CLK 1110110 : 119 CLK 1110111 : 120 CLK 1111000 : 121 CLK 1111001 : 122 CLK 1111010 : 123 CLK 1111011 : 124 CLK 1111100 : 125 CLK 1111101 : 126 CLK 1111110 : 127 CLK 1111111 : 128 CLK

7.6.1.9 Register OCP_CH_SEL1 (slave address: 0b100001x; register address: 0x07; default: 0xFF)

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Figure 35. Register OCP_CH_SEL1 Format

7	6	5	4	3	2	1	0
GCK12_OCP_SEL	GCK11_OCP_SEL	GCK10_OCP_SEL	GCK9_OCP_SEL	GCK4_OCP_SEL	GCK3_OCP_SEL	GCK2_OCP_SEL	GCK1_OCP_SEL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
OTP	OTP	OTP	OTP	OTP	OTP	OTP	OTP

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 11. Register OCP_CH_SEL1 Field Descriptions

Bit	Field	Type	Reset	Description
7	GCK12_OCP_SEL	R/W	1	GCK12 channel select 0 : Over current sensing is disabled **1 : Over current sensing is active**
6	GCK11_OCP_SEL	R/W	1	GCK11 channel select 0 : Over current sensing is disabled **1 : Over current sensing is active**
5	GCK10_OCP_SEL	R/W	1	GCK10 channel select 0 : Over current sensing is disabled **1 : Over current sensing is active**
4	GCK9_OCP_SEL	R/W	1	GCK9 channel select 0 : Over current sensing is disabled **1 : Over current sensing is active**
3	GCK4_OCP_SEL	R/W	1	GCK4 channel select 0 : Over current sensing is disabled **1 : Over current sensing is active**
2	GCK3_OCP_SEL	R/W	1	GCK3 channel select 0 : Over current sensing is disabled **1 : Over current sensing is active**
1	GCK2_OCP_SEL	R/W	1	GCK2 channel select 0 : Over current sensing is disabled **1 : Over current sensing is active**
0	GCK1_OCP_SEL	R/W	1	GCK1 channel select 0 : Over current sensing is disabled **1 : Over current sensing is active**

7.6.1.10 Register OCP_CH_SEL2 (slave address: 0b100001x; register address: 0x08; default: 0xFF)

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Figure 36. Register OCP_CH_SEL2 Format

7	6	5	4	3	2	1	0
GGP2_OCP_SEL	GGP1_OCP_SEL	VSS_OCP_SEL	GCP_OCP_SEL	GCK8_OCP_SEL	GCK7_OCP_SEL	GCK6_OCP_SEL	GCK5_OCP_SEL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
OTP	OTP	OTP	OTP	OTP	OTP	OTP	OTP

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 12. Register OCP_CH_SEL2 Field Descriptions

Bit	Field	Type	Reset	Description
7	GGP2_OCP_SEL	R/W	1	GGP2 channel select 0 : Over current sensing is disabled **1 : Over current sensing is active**
6	GGP1_OCP_SEL	R/W	1	GGP1 channel select 0 : Over current sensing is disabled **1 : Over current sensing is active**
5	VSS_OCP_SEL	R/W	1	VSS channel select 0 : Over current sensing is disabled **1 : Over current sensing is active**
4	GCP_OCP_SEL	R/W	1	GCP channel select 0 : Over current sensing is disabled **1 : Over current sensing is active**
3	GCK8_OCP_SEL	R/W	1	GCK8 channel select 0 : Over current sensing is disabled **1 : Over current sensing is active**
2	GCK7_OCP_SEL	R/W	1	GCK7 channel select 0 : Over current sensing is disabled **1 : Over current sensing is active**
1	GCK6_OCP_SEL	R/W	1	GCK6 channel select 0 : Over current sensing is disabled **1 : Over current sensing is active**
0	GCK5_OCP_SEL	R/W	1	GCK5 channel select 0 : Over current sensing is disabled **1 : Over current sensing is active**

7.6.1.11 Register OCP_CH_SEL3 (slave address: 0b100001x; register address: 0x09; default: 0x03)

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Figure 37. Register OCP_CH_SEL3 Format

7	6	5	4	3	2	1	0
OCP_RCVRY[1:0]		SNS_LVL[3:0]				GSP2_OCP_SEL	GSP1_OCP_SEL
R/W		R/W				R/W	R/W
OTP		OTP				OTP	OTP

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 13. Register OCP_CH_SEL3 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	OCP_RCVRY[1:0]	R/W	00	Defines the action taken when OCP alarm triggered **00 : No action taken.** 01 : LS outputs set to HiZ and FAULT mode is entered. 10 : LS outputs set HiZ and recovery on next LS_START. 11 : LS outputs set HiZ and recovery on next LS_START. If for following 3 frames OCP is detected then FAULT mode is entered.
5:2	SNS_LVL[3:0]	R/W	0000	Over-current sense level for VGH, VGL1 and VGL2 supplies **0000 : 20mA** 0001 : 40mA 0010 : 60mA 0011 : 80mA
1	GSP2_OCP_SEL	R/W	1	GSP2 channel select 0 : Over current sensing is disabled **1 : Over current sensing is active**
0	GSP1_OCP_SEL	R/W	1	GSP1 channel select 0 : Over current sensing is disabled **1 : Over current sensing is active**

7.6.1.12 Register OCP_ALARM1 (slave address: 0b100001x; register address: 0x0A; default: 0x00)

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Figure 38. Register OCP_ALARM1 Format

7	6	5	4	3	2	1	0
ALARM1[7:0]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 14. Register OCP_ALARM1 Field Descriptions

Bit	Field	Type	Reset	Description			
7:0	ALARM1[7:0]	R/W	00000000	Number of over-current events of GCK channels in a single frame triggering a OCP fault			
				00000000 : No alarm 00000001 : 1E 00000010 : 2E 00000011 : 3E 00000100 : 4E 00000101 : 5E 00000110 : 6E 00000111 : 7E 00001000 : 8E 00001001 : 9E 00001010 : 10E 00001011 : 11E 00001100 : 12E 00001101 : 13E 00001110 : 14E 00001111 : 15E 00010000 : 16E 00010001 : 17E 00010010 : 18E 00010011 : 19E 00010100 : 20E 00010101 : 21E 00010110 : 22E 00010111 : 23E 00011000 : 24E 00011001 : 25E 00011010 : 26E 00011011 : 27E 00011100 : 28E 00011101 : 29E 00011110 : 30E 00011111 : 31E 00100000 : 32E 00100001 : 33E 00100010 : 34E 00100011 : 35E 00100100 : 36E 00100101 : 37E 00100110 : 38E 00100111 : 39E 00101000 : 40E 00101001 : 41E 00101010 : 42E 00101011 : 43E 00101100 : 44E 00101101 : 45E 00101110 : 46E 00101111 : 47E 00110000 : 48E 00110001 : 49E 00110010 : 50E 00110011 : 51E 00110100 : 52E 00110101 : 53E 00110110 : 54E 00110111 : 55E 00111000 : 56E 00111001 : 57E 00111010 : 58E 00111011 : 59E 00111100 : 60E 00111101 : 61E 00111110 : 62E 00111111 : 63E	01000000 : 64E 01000001 : 65E 01000010 : 66E 01000011 : 67E 01000100 : 68E 01000101 : 69E 01000110 : 70E 01000111 : 71E 01001000 : 72E 01001001 : 73E 01001010 : 74E 01001011 : 75E 01001100 : 76E 01001101 : 77E 01001110 : 78E 01001111 : 79E 01010000 : 80E 01010001 : 81E 01010010 : 82E 01010011 : 83E 01010100 : 84E 01010101 : 85E 01010110 : 86E 01010111 : 87E 01011000 : 88E 01011001 : 89E 01011010 : 90E 01011011 : 91E 01011100 : 92E 01011101 : 93E 01011110 : 94E 01011111 : 95E 01100000 : 96E 01100001 : 97E 01100010 : 98E 01100011 : 99E 01100100 : 100E 01100101 : 101E 01100110 : 102E 01100111 : 103E 01101000 : 104E 01101001 : 105E 01101010 : 106E 01101011 : 107E 01101100 : 108E 01101101 : 109E 01101110 : 110E 01101111 : 111E 01110000 : 112E 01110001 : 113E 01110010 : 114E 01110011 : 115E 01110100 : 116E 01110101 : 117E 01110110 : 118E 01110111 : 119E 01111000 : 120E 01111001 : 121E 01111010 : 122E 01111011 : 123E 01111100 : 124E 01111101 : 125E 01111110 : 126E 01111111 : 127E	10000000 : 128E 10000001 : 129E 10000010 : 130E 10000011 : 131E 10000100 : 132E 10000101 : 133E 10000110 : 134E 10000111 : 135E 10001000 : 136E 10001001 : 137E 10001010 : 138E 10001011 : 139E 10001100 : 140E 10001101 : 141E 10001110 : 142E 10001111 : 143E 10010000 : 144E 10010001 : 145E 10010010 : 146E 10010011 : 147E 10010100 : 148E 10010101 : 149E 10010110 : 150E 10010111 : 151E 10011000 : 152E 10011001 : 153E 10011010 : 154E 10011011 : 155E 10011100 : 156E 10011101 : 157E 10011110 : 158E 10011111 : 159E 10100000 : 160E 10100001 : 161E 10100010 : 162E 10100011 : 163E 10100100 : 164E 10100101 : 165E 10100110 : 166E 10100111 : 167E 10101000 : 168E 10101001 : 169E 10101010 : 170E 10101011 : 171E 10101100 : 172E 10101101 : 173E 10101110 : 174E 10101111 : 175E 10110000 : 176E 10110001 : 177E 10110010 : 178E 10110011 : 179E 10110100 : 180E 10110101 : 181E 10110110 : 182E 10110111 : 183E 10111000 : 184E 10111001 : 185E 10111010 : 186E 10111011 : 187E 10111100 : 188E 10111101 : 189E 10111110 : 190E 10111111 : 191E	11000000 : 192E 11000001 : 193E 11000010 : 194E 11000011 : 195E 11000100 : 196E 11000101 : 197E 11000110 : 198E 11000111 : 199E 11001000 : 200E 11001001 : 201E 11001010 : 202E 11001011 : 203E 11001100 : 204E 11001101 : 205E 11001110 : 206E 11001111 : 207E 11010000 : 208E 11010001 : 209E 11010010 : 210E 11010011 : 211E 11010100 : 212E 11010101 : 213E 11010110 : 214E 11010111 : 215E 11011000 : 216E 11011001 : 217E 11011010 : 218E 11011011 : 219E 11011100 : 220E 11011101 : 221E 11011110 : 222E 11011111 : 223E 11100000 : 224E 11100001 : 225E 11100010 : 226E 11100011 : 227E 11100100 : 228E 11100101 : 229E 11100110 : 230E 11100111 : 231E 11101000 : 232E 11101001 : 233E 11101010 : 234E 11101011 : 235E 11101100 : 236E 11101101 : 237E 11101110 : 238E 11101111 : 239E 11110000 : 240E 11110001 : 241E 11110010 : 242E 11110011 : 243E 11110100 : 244E 11110101 : 245E 11110110 : 246E 11110111 : 247E 11111000 : 248E 11111001 : 249E 11111010 : 250E 11111011 : 251E 11111100 : 252E 11111101 : 253E 11111110 : 254E 11111111 : 255E

7.6.1.13 Register OCP_ALARM2 (slave address: 0b100001x; register address: 0x0B; default: 0x00)

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Figure 39. Register OCP_ALARM2 Format

7	6	5	4	3	2	1	0
NIL[3:0]				ALARM2[3:0]			
R				R/W			
--				OTP			

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 15. Register OCP_ALARM2 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	NIL[3:0]	R	0000	This bit is not implemented in hardware. During write operations data for this bit is ignored. During read operations 0 is returned.
3:0	ALARM2[3:0]	R/W	0000	GSP1-2, GCP, VSS, GGP1-2 channels : Number of over-current events in a single frame triggering a OCP fault **0000 : No Alarm** 0001 : 1 OC events 0010 : 2 OC events 0011 : 3 OC events 0100 : 4 OC events 0101 : 5 OC events 0110 : 6 OC events 0111 : 7 OC events 1000 : 8 OC events 1001 : 9 OC events 1010 : 10 OC events 1011 : 11 OC events 1100 : 12 OC events 1101 : 13 OC events 1110 : 14 OC events 1111 : 15 OC events

7.6.1.14 Register EN_DLY (slave address: 0b100001x; register address: 0x0C; default: 0x00)

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Figure 40. Register EN_DLY Format

7	6	5	4	3	2	1	0
EN_DLY[7:0]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 16. Register EN_DLY Field Descriptions

Bit	Field	Type	Reset	Description			
7:0	EN_DLY[7:0]	R/W	00000000	LS enable delay count. Level shifter outputs only toggle if LS_CNTRL pin is high and enable delay counter has expired.			
				00000000 : 0 ms	01000000 : 128 ms	10000000 : 256 ms	11000000 : 384 ms
				00000001 : 2 ms	01000001 : 130 ms	10000001 : 258 ms	11000001 : 386 ms
				00000010 : 4 ms	01000010 : 132 ms	10000010 : 260 ms	11000010 : 388 ms
				00000011 : 6 ms	01000011 : 134 ms	10000011 : 262 ms	11000011 : 390 ms
				00000100 : 8 ms	01000100 : 136 ms	10000100 : 264 ms	11000100 : 392 ms
				00000101 : 10 ms	01000101 : 138 ms	10000101 : 266 ms	11000101 : 394 ms
				00000110 : 12 ms	01000110 : 140 ms	10000110 : 268 ms	11000110 : 396 ms
				00000111 : 14 ms	01000111 : 142 ms	10000111 : 270 ms	11000111 : 398 ms
				00001000 : 16 ms	01001000 : 144 ms	10001000 : 272 ms	11001000 : 400 ms
				00001001 : 18 ms	01001001 : 146 ms	10001001 : 274 ms	11001001 : 402 ms
				00001010 : 20 ms	01001010 : 148 ms	10001010 : 276 ms	11001010 : 404 ms
				00001011 : 22 ms	01001011 : 150 ms	10001011 : 278 ms	11001011 : 406 ms
				00001100 : 24 ms	01001100 : 152 ms	10001100 : 280 ms	11001100 : 408 ms
				00001101 : 26 ms	01001101 : 154 ms	10001101 : 282 ms	11001101 : 410 ms
				00001110 : 28 ms	01001110 : 156 ms	10001110 : 284 ms	11001110 : 412 ms
				00001111 : 30 ms	01001111 : 158 ms	10001111 : 286 ms	11001111 : 414 ms
				00010000 : 32 ms	01010000 : 160 ms	10010000 : 288 ms	11010000 : 416 ms
				00010001 : 34 ms	01010001 : 162 ms	10010001 : 290 ms	11010001 : 418 ms
				00010010 : 36 ms	01010010 : 164 ms	10010010 : 292 ms	11010010 : 420 ms
				00010011 : 38 ms	01010011 : 166 ms	10010011 : 294 ms	11010011 : 422 ms
				00010100 : 40 ms	01010100 : 168 ms	10010100 : 296 ms	11010100 : 424 ms
				00010101 : 42 ms	01010101 : 170 ms	10010101 : 298 ms	11010101 : 426 ms
				00010110 : 44 ms	01010110 : 172 ms	10010110 : 300 ms	11010110 : 428 ms
				00010111 : 46 ms	01010111 : 174 ms	10010111 : 302 ms	11010111 : 430 ms
				00011000 : 48 ms	01011000 : 176 ms	10011000 : 304 ms	11011000 : 432 ms
				00011001 : 50 ms	01011001 : 178 ms	10011001 : 306 ms	11011001 : 434 ms
				00011010 : 52 ms	01011010 : 180 ms	10011010 : 308 ms	11011010 : 436 ms
				00011011 : 54 ms	01011011 : 182 ms	10011011 : 310 ms	11011011 : 438 ms
				00011100 : 56 ms	01011100 : 184 ms	10011100 : 312 ms	11011100 : 440 ms
				00011101 : 58 ms	01011101 : 186 ms	10011101 : 314 ms	11011101 : 442 ms
				00011110 : 60 ms	01011110 : 188 ms	10011110 : 316 ms	11011110 : 444 ms
				00011111 : 62 ms	01011111 : 190 ms	10011111 : 318 ms	11011111 : 446 ms
				00100000 : 64 ms	01100000 : 192 ms	10100000 : 320 ms	11100000 : 448 ms
				00100001 : 66 ms	01100001 : 194 ms	10100001 : 322 ms	11100001 : 450 ms
				00100010 : 68 ms	01100010 : 196 ms	10100010 : 324 ms	11100010 : 452 ms
				00100011 : 70 ms	01100011 : 198 ms	10100011 : 326 ms	11100011 : 454 ms
				00100100 : 72 ms	01100100 : 200 ms	10100100 : 328 ms	11100100 : 456 ms
				00100101 : 74 ms	01100101 : 202 ms	10100101 : 330 ms	11100101 : 458 ms
				00100110 : 76 ms	01100110 : 204 ms	10100110 : 332 ms	11100110 : 460 ms
				00100111 : 78 ms	01100111 : 206 ms	10100111 : 334 ms	11100111 : 462 ms
				00101000 : 80 ms	01101000 : 208 ms	10101000 : 336 ms	11101000 : 464 ms
				00101001 : 82 ms	01101001 : 210 ms	10101001 : 338 ms	11101001 : 466 ms
				00101010 : 84 ms	01101010 : 212 ms	10101010 : 340 ms	11101010 : 468 ms
				00101011 : 86 ms	01101011 : 214 ms	10101011 : 342 ms	11101011 : 470 ms
				00101100 : 88 ms	01101100 : 216 ms	10101100 : 344 ms	11101100 : 472 ms
				00101101 : 90 ms	01101101 : 218 ms	10101101 : 346 ms	11101101 : 474 ms
				00101110 : 92 ms	01101110 : 220 ms	10101110 : 348 ms	11101110 : 476 ms
				00101111 : 94 ms	01101111 : 222 ms	10101111 : 350 ms	11101111 : 478 ms
				00110000 : 96 ms	01110000 : 224 ms	10110000 : 352 ms	11110000 : 480 ms
				00110001 : 98 ms	01110001 : 226 ms	10110001 : 354 ms	11110001 : 482 ms
				00110010 : 100 ms	01110010 : 228 ms	10110010 : 356 ms	11110010 : 484 ms
				00110011 : 102 ms	01110011 : 230 ms	10110011 : 358 ms	11110011 : 486 ms
				00110100 : 104 ms	01110100 : 232 ms	10110100 : 360 ms	11110100 : 488 ms
				00110101 : 106 ms	01110101 : 234 ms	10110101 : 362 ms	11110101 : 490 ms
				00110110 : 108 ms	01110110 : 236 ms	10110110 : 364 ms	11110110 : 492 ms
				00110111 : 110 ms	01110111 : 238 ms	10110111 : 366 ms	11110111 : 494 ms
				00111000 : 112 ms	01111000 : 240 ms	10111000 : 368 ms	11111000 : 496 ms
				00111001 : 114 ms	01111001 : 242 ms	10111001 : 370 ms	11111001 : 498 ms
				00111010 : 116 ms	01111010 : 244 ms	10111010 : 372 ms	11111010 : 500 ms
				00111011 : 118 ms	01111011 : 246 ms	10111011 : 374 ms	11111011 : 502 ms
				00111100 : 120 ms	01111100 : 248 ms	10111100 : 376 ms	11111100 : 504 ms
				00111101 : 122 ms	01111101 : 250 ms	10111101 : 378 ms	11111101 : 506 ms
				00111110 : 124 ms	01111110 : 252 ms	10111110 : 380 ms	11111110 : 508 ms
				00111111 : 126 ms	01111111 : 254 ms	10111111 : 382 ms	11111111 : 510 ms

7.6.1.15 Register FWID (slave address: 0b100001x; register address: 0x0D; default: 0x00)

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Figure 41. Register FWID Format

7	6	5	4	3	2	1	0
FWID[7:0]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 17. Register FWID Field Descriptions

Bit	Field	Type	Reset	Description
7:0	FWID[7:0]	R/W	00000000	Firmware identification code

7.6.1.16 Register PNL_DCH1 (slave address: 0b100001x; register address: 0x0E; default: 0x00)

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Figure 42. Register PNL_DCH1 Format

7	6	5	4	3	2	1	0
VGH_DCH_D1	GCK78_D1	GCK56_D1	GGP_D1	VSS_D1	GCP_D1	GSP_D1	GCK14_912_D1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
OTP	OTP	OTP	OTP	OTP	OTP	OTP	OTP

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 18. Register PNL_DCH1 Field Descriptions

Bit	Field	Type	Reset	Description
7	VGH_DCH_D1	R/W	0	Enables VGH active discharge during panel discharge step 1. **0 : disabled** 1 : enabled
6	GCK78_D1	R/W	0	Defines the state of the GCK7, 8 outputs during panel discharge step 1. **0 : low** 1 : high
5	GCK56_D1	R/W	0	Defines the state of the GCK5, 6 outputs during panel discharge step 1. **0 : low** 1 : high
4	GGP_D1	R/W	0	Defines the state of the GGPx outputs during panel discharge step 1. **0 : low** 1 : high
3	VSS_D1	R/W	0	Defines the state of the VSS output during panel discharge step 1. **0 : low** 1 : high
2	GCP_D1	R/W	0	Defines the state of the GCP output during panel discharge step 1. **0 : low** 1 : high
1	GSP_D1	R/W	0	Defines the state of the GSPx outputs during panel discharge step 1. **0 : low** 1 : high
0	GCK14_912_D1	R/W	0	Defines the state of the GCK1-4 and 9-12 outputs during panel discharge step 1. **0 : low** 1 : high

7.6.1.17 Register PNL_DCH2 (slave address: 0b100001x; register address: 0x0F; default: 0x00)

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Figure 43. Register PNL_DCH2 Format

7	6	5	4	3	2	1	0
VGH_DCH_D2	GCK78_D2	GCK56_D2	GGP_D2	VSS_D2	GCP_D2	GSP_D2	GCK14_912_D2
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
OTP	OTP	OTP	OTP	OTP	OTP	OTP	OTP

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 19. Register PNL_DCH2 Field Descriptions

Bit	Field	Type	Reset	Description
7	VGH_DCH_D2	R/W	0	Enables VGH active discharge during panel discharge step 2. **0 : disabled** 1 : enabled
6	GCK78_D2	R/W	0	Defines the state of the GCK7, 8 outputs during panel discharge step 2. **0 : low** 1 : high
5	GCK56_D2	R/W	0	Defines the state of the GCK5, 6 outputs during panel discharge step 2. **0 : low** 1 : high
4	GGP_D2	R/W	0	Defines the state of the GGPx outputs during panel discharge step 2. **0 : low** 1 : high
3	VSS_D2	R/W	0	Defines the state of the VSS output during panel discharge step 2. **0 : low** 1 : high
2	GCP_D2	R/W	0	Defines the state of the GCP output during panel discharge step 2. **0 : low** 1 : high
1	GSP_D2	R/W	0	Defines the state of the GSPx outputs during panel discharge step 2. **0 : low** 1 : high
0	GCK14_912_D2	R/W	0	Defines the state of the GCKx1-4 and 9-12 outputs during panel discharge step 2. **0 : low** 1 : high

7.6.1.18 Register C1256_SEP (slave address: 0b100001x; register address: 0x10; default: 0x00)

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Figure 44. Register C1256_SEP Format

7	6	5	4	3	2	1	0
C1256_SEP[7:0]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 20. Register C1256_SEP Field Descriptions

Bit	Field	Type	Reset	Description
7:0	C1256_SEP[7:0]	R/W	00000000	C1, C2, C5, C6 separation count

7.6.1.19 Register C34_SEP (slave address: 0b100001x; register address: 0x11; default: 0x00)

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Figure 45. Register C34_SEP Format

7	6	5	4	3	2	1	0
C34_SEP[7:0]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 21. Register C34_SEP Field Descriptions

Bit	Field	Type	Reset	Description
7:0	C34_SEP[7:0]	R/W	00000000	C3, C4 separation setting.

7.6.1.20 Register D1_SEP (slave address: 0b100001x; register address: 0x12; default: 0x00)

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Figure 46. Register D1_SEP Format

7	6	5	4	3	2	1	0
D1_SEP[7:0]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 22. Register D1_SEP Field Descriptions

Bit	Field	Type	Reset	Description
7:0	D1_SEP[7:0]	R/W	00000000	D1 separation count

7.6.1.21 Register D2_SEP (slave address: 0b100001x; register address: 0x13; default: 0x00)

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Figure 47. Register D2_SEP Format

7	6	5	4	3	2	1	0
D2_SEP[7:0]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 23. Register D2_SEP Field Descriptions

Bit	Field	Type	Reset	Description
7:0	D2_SEP[7:0]	R/W	00000000	D2 separation count

7.6.1.22 Register SPARE1 (slave address: 0b100001x; register address: 0x14; default: 0x00)

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Figure 48. Register SPARE1 Format

7	6	5	4	3	2	1	0
SPARE1[7:0]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 24. Register SPARE1 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	SPARE1[7:0]	R/W	00000000	Can be used by customer to program an identification code

7.6.1.23 Register SPARE2 (slave address: 0b100001x; register address: 0x15; default: 0x00)

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Figure 49. Register SPARE2 Format

7	6	5	4	3	2	1	0
SPARE2[7:0]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 25. Register SPARE2 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	SPARE2[7:0]	R/W	00000000	Can be used by customer to program an identification code

7.6.1.24 Register MUX1 (slave address: 0b100001x; register address: 0x30; default: 0x00)

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Figure 50. Register MUX1 Format

7	6	5	4	3	2	1	0
GCK3_4_MUX	GCK1_2_MUX	GSP2_MUX[2:0]			GSP1_MUX[2:0]		
R/W	R/W	R/W			R/W		
OTP	OTP	OTP			OTP		

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 26. Register MUX1 Field Descriptions

Bit	Field	Type	Reset	Description
7	GCK3_4_MUX	R/W	0	Data source selection for GCK3 and GCK4 outputs. **0 : GCK3 data source is C2, GCK4 data source is C2A.** 1 : GCK4 data source is C2, GCK3 data source is C2A.
6	GCK1_2_MUX	R/W	0	Data source selection for GCK1 and GCK2 outputs. **0 : GCK1 data source is C1, GCK2 data source is C1A.** 1 : GCK2 data source is C1, GCK1 data source is C1A.
5:3	GSP2_MUX[2:0]	R/W	000	Data source selection for GSP2 output. **000 : GSP2 data source is D1.** 001 : GSP2 data source is D1A. 010 : GSP2 data source is D2. 011 : GSP2 data source is D2A. 100 : GSP2 data source is D3. 101 : GSP2 is low. 110 : GSP2 is high. 111 : GSP2 is high.
2:0	GSP1_MUX[2:0]	R/W	000	Data source selection for GSP1 output. **000 : GSP1 data source is D1.** 001 : GSP1 data source is D1A. 010 : GSP1 data source is D2. 011 : GSP1 data source is D2A. 100 : GSP1 data source is D3. 101 : GSP1 is low. 110 : GSP1 is high. 111 : GSP1 is high.

7.6.1.25 Register MUX2 (slave address: 0b100001x; register address: 0x31; default: 0x00)

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Figure 51. Register MUX2 Format

7	6	5	4	3	2	1	0
GCK11_12_MUX	GCK9_10_MUX	VSS_MUX[2:0]			GCP_MUX[2:0]		
R/W	R/W	R/W			R/W		
OTP	OTP	OTP			OTP		

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 27. Register MUX2 Field Descriptions

Bit	Field	Type	Reset	Description
7	GCK11_12_MUX	R/W	0	Data source selection for GCK11 and GCK12 outputs. **0 : GCK11 data source is C6, GCK12 data source is C6A.** 1 : GCK12 data source is C6, GCK11 data source is C6A.
6	GCK9_10_MUX	R/W	0	Data source selection for GCK9 and GCK10 outputs. **0 : GCK9 data source is C5, GCK10 data source is C5A.** 1 : GCK10 data source is C5, GCK9 data source is C5A.
5:3	VSS_MUX[2:0]	R/W	000	Data source selection for VSS output. **000 : VSS data source is D1.** 001 : VSS data source is D1A. 010 : VSS data source is D2. 011 : VSS data source is D2A. 100 : VSS data source is D3. 101 : VSS is low. 110 : VSS is high. 111 : VSS is high.
2:0	GCP_MUX[2:0]	R/W	000	Data source selection for GCP output. **000 : GCP data source is D1.** 001 : GCP data source is D1A. 010 : GCP data source is D2. 011 : GCP data source is D2A. 100 : GCP data source is D3. 101 : GCP is low. 110 : GCP is high. 111 : GCP is high.

7.6.1.26 Register MUX3 (slave address: 0b100001x; register address: 0x32; default: 0x00)

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Figure 52. Register MUX3 Format

7	6	5	4	3	2	1	0
NIL[1:0]		GGP2_MUX[2:0]			GGP1_MUX[2:0]		
R		R/W			R/W		
--		OTP			OTP		

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 28. Register MUX3 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	NIL[1:0]	R	00	This bit is not implemented in hardware. During write operations data for this bit is ignored. During read operations 0 is returned.
5:3	GGP2_MUX[2:0]	R/W	000	Data source selection for GGP2 output. **000 : GGP2 data source is D1.** 001 : GGP2 data source is D1A. 010 : GGP2 data source is D2. 011 : GGP2 data source is D2A. 100 : GGP2 data source is D3. 101 : GGP2 s low. 110 : GGP2 is high. 111 : GGP2 is high.
2:0	GGP1_MUX[2:0]	R/W	000	Data source selection for GGP1 output. **000 : GGP1 data source is D1.** 001 : GGP1 data source is D1A. 010 : GGP1 data source is D2. 011 : GGP1 data source is D2A. 100 : GGP1 data source is D3. 101 : GGP1 s low. 110 : GGP1 is high. 111 : GGP1 is high.

7.6.1.27 Register MUX4 (slave address: 0b100001x; register address: 0x33; default: 0x00)

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Figure 53. Register MUX4 Format

7	6	5	4	3	2	1	0
GCK8_MUX[1:0]		GCK7_MUX[1:0]		GCK6_MUX[1:0]		GCK5_MUX[1:0]	
R/W		R/W		R/W		R/W	
OTP		OTP		OTP		OTP	

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 29. Register MUX4 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	GCK8_MUX[1:0]	R/W	00	Data source selection for GCK8 output. **00 : GCK8 data source is C4.** 01 : GCK8 data source is C4A. 10 : GCK8 is low. 11 : GCK8 is high.
5:4	GCK7_MUX[1:0]	R/W	00	Data source selection for GCK7 output. **00 : GCK7 data source is C4.** 01 : GCK7 data source is C4A. 10 : GCK7 is low. 11 : GCK7 is high.
3:2	GCK6_MUX[1:0]	R/W	00	Data source selection for GCK6 output. **00 : GCK6 data source is C3.** 01 : GCK6 data source is C3A. 10 : GCK6 is low. 11 : GCK6 is high.
1:0	GCK5_MUX[1:0]	R/W	00	Data source selection for GCK5 output. **00 : GCK5 data source is C3.** 01 : GCK5 data source is C3A. 10 : GCK5 is low. 11 : GCK5 is high.

7.6.1.28 Register CHSEL1_START_ADDR (slave address: 0b100001x; register address: 0x34; default: 0x00)

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Figure 54. Register CHSEL1_START_ADDR Format

7	6	5	4	3	2	1	0
GCK8_SEL	GCK7_SEL	START_ADDR[5:0]					
R/W	R/W	R/W					
OTP	OTP	OTP					

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 30. Register CHSEL1_START_ADDR Field Descriptions

Bit	Field	Type	Reset	Description
7	GCK8_SEL	R/W	0	GCK8 channel select **0 : hold** 1 : active
6	GCK7_SEL	R/W	0	GCK7 channel select **0 : hold** 1 : active
5:0	START_ADDR[5:0]	R/W	000000	Pattern start address. Sequencer returns to this address on the rising edge of LS_START.

7.6.1.29 Register CHSEL2 (slave address: 0b100001x; register address: 0x35; default: 0x00)

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Figure 55. Register CHSEL2 Format

7	6	5	4	3	2	1	0
GCK12_SEL	GCK11_SEL	GCK10_SEL	GCK9_SEL	GCK4_SEL	GCK3_SEL	GCK2_SEL	GCK1_SEL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
OTP	OTP	OTP	OTP	OTP	OTP	OTP	OTP

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 31. Register CHSEL2 Field Descriptions

Bit	Field	Type	Reset	Description
7	GCK12_SEL	R/W	0	GCK12 channel select **0 : hold** 1 : active
6	GCK11_SEL	R/W	0	GCK11 channel select **0 : hold** 1 : active
5	GCK10_SEL	R/W	0	GCK10 channel select **0 : hold** 1 : active
4	GCK9_SEL	R/W	0	GCK9 channel select **0 : hold** 1 : active
3	GCK4_SEL	R/W	0	GCK4 channel select **0 : hold** 1 : active
2	GCK3_SEL	R/W	0	GCK3 channel select **0 : hold** 1 : active
1	GCK2_SEL	R/W	0	GCK2 channel select **0 : hold** 1 : active
0	GCK1_SEL	R/W	0	GCK1 channel select **0 : hold** 1 : active

7.6.1.30 Register CHSEL3 (slave address: 0b100001x; register address: 0x36; default: 0x00)

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Figure 56. Register CHSEL3 Format

7	6	5	4	3	2	1	0
GCK6_SEL	GCK5_SEL	GGP2_SEL	GGP1_SEL	VSS_SEL	GCP_SEL	GSP2_SEL	GSP1_SEL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
OTP	OTP	OTP	OTP	OTP	OTP	OTP	OTP

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 32. Register CHSEL3 Field Descriptions

Bit	Field	Type	Reset	Description
7	GCK6_SEL	R/W	0	GCK6 channel select **0 : hold** 1 : active
6	GCK5_SEL	R/W	0	GCK5 channel select **0 : hold** 1 : active
5	GGP2_SEL	R/W	0	GGP2 channel select **0 : hold** 1 : active
4	GGP1_SEL	R/W	0	GGP1 channel select **0 : hold** 1 : active
3	VSS_SEL	R/W	0	VSS channel select **0 : hold** 1 : active
2	GCP_SEL	R/W	0	GCP channel select **0 : hold** 1 : active
1	GSP2_SEL	R/W	0	GSP2 channel select **0 : hold** 1 : active
0	GSP1_SEL	R/W	0	GSP1 channel select **0 : hold** 1 : active

7.6.1.31 Register PRESET1 (slave address: 0b100001x; register address: 0x37; default: 0x00)

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Figure 57. Register PRESET1 Format

7	6	5	4	3	2	1	0
C6_PRESET[1:0]		C5_PRESET[1:0]		C2_PRESET[1:0]		C1_PRESET[1:0]	
R/W		R/W		R/W		R/W	
OTP		OTP		OTP		OTP	

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 33. Register PRESET1 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	C6_PRESET[1:0]	R/W	00	C6 preset for GCK11-12 **00 : LOW** 01 : HiZ 10 : charge sharing 11 : HIGH
5:4	C5_PRESET[1:0]	R/W	00	C5 preset for GCK9-10 **00 : LOW** 01 : HiZ 10 : charge sharing 11 : HIGH
3:2	C2_PRESET[1:0]	R/W	00	C2 preset for GCK3-4 **00 : LOW** 01 : HiZ 10 : charge sharing 11 : HIGH
1:0	C1_PRESET[1:0]	R/W	00	C1 preset for GCK1-2 **00 : LOW** 01 : HiZ 10 : charge sharing 11 : HIGH

7.6.1.32 Register PRESET2 (slave address: 0b100001x; register address: 0x38; default: 0x00)

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Figure 58. Register PRESET2 Format

7	6	5	4	3	2	1	0
NIL	C4_PRESET[1:0]		C3_PRESET[1:0]		D3_PRESET	D2_PRESET	D1_PRESET
R	R/W		R/W		R/W	R/W	R/W
--	OTP		OTP		OTP	OTP	OTP

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 34. Register PRESET2 Field Descriptions

Bit	Field	Type	Reset	Description
7	NIL	R	0	This bit is not implemented in hardware. During write operations data for this bit is ignored. During read operations 0 is returned.
6:5	C4_PRESET[1:0]	R/W	00	C4 preset for GCK7-8 **00 : LOW** 01 : HiZ 10 : charge sharing 11 : HIGH
4:3	C3_PRESET[1:0]	R/W	00	C3 preset for GCK5-6 **00 : LOW** 01 : HiZ 10 : charge sharing 11 : HIGH
2	D3_PRESET	R/W	0	D3 preset for GSP, GCP, VSS and GGP outputs **0 : LOW** 1 : HIGH
1	D2_PRESET	R/W	0	D2 preset for GSP, GCP, VSS and GGP outputs **0 : LOW** 1 : HIGH
0	D1_PRESET	R/W	0	D1 preset for GSP, GCP, VSS and GGP outputs **0 : LOW** 1 : HIGH

7.6.1.33 Register DATA1 (slave address: 0b100001x; register address: 0x39; default: 0x00)

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Figure 59. Register DATA1 Format

7	6	5	4	3	2	1	0
DATA1[7:0]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 35. Register DATA1 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DATA1[7:0]	R/W	00000000	8 bit data word controlled by sequencer with programmable default.

7.6.1.34 Register DATA2 (slave address: 0b100001x; register address: 0x3A; default: 0x00)

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Figure 60. Register DATA2 Format

7	6	5	4	3	2	1	0
DATA2[7:0]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 36. Register DATA2 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DATA2[7:0]	R/W	00000000	8 bit data word controlled by sequencer with programmable default.

7.6.1.35 Register DATA3 (slave address: 0b100001x; register address: 0x3B; default: 0x00)

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Figure 61. Register DATA3 Format

7	6	5	4	3	2	1	0
DATA3[7:0]							
R/W							
--							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 37. Register DATA3 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DATA3[7:0]	R/W	00000000	8 bit data word controlled by sequencer.

7.6.1.36 Register DATA4 (slave address: 0b100001x; register address: 0x3C; default: 0x00)

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Figure 62. Register DATA4 Format

7	6	5	4	3	2	1	0
DATA4[7:0]							
R/W							
--							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 38. Register DATA4 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DATA4[7:0]	R/W	00000000	8 bit data word controlled by sequencer.

7.6.1.37 Register DATA5 (slave address: 0b100001x; register address: 0x3D; default: 0x00)

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Figure 63. Register DATA5 Format

7	6	5	4	3	2	1	0
DATA5[7:0]							
R/W							
--							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 39. Register DATA5 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DATA5[7:0]	R/W	00000000	8 bit data word controlled by sequencer.

7.6.1.38 Register INSTRUCTION_0_0 (slave address: 0b100001x; register address: 0x40; default: 0x00)

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Figure 64. Register INSTRUCTION_0_0 Format

7	6	5	4	3	2	1	0
INSTRUCTION_0[23:16]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 40. Register INSTRUCTION_0_0 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_0[23:16]	R/W	00000000	

7.6.1.39 Register INSTRUCTION_0_1 (slave address: 0b100001x; register address: 0x41; default: 0x00)

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Figure 65. Register INSTRUCTION_0_1 Format

7	6	5	4	3	2	1	0
INSTRUCTION_0[15:8]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 41. Register INSTRUCTION_0_1 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_0[15:8]	R/W	00000000	

7.6.1.40 Register INSTRUCTION_0_2 (slave address: 0b100001x; register address: 0x42; default: 0x00)

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Figure 66. Register INSTRUCTION_0_2 Format

7	6	5	4	3	2	1	0
INSTRUCTION_0[7:0]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 42. Register INSTRUCTION_0_2 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_0[7:0]	R/W	00000000	

7.6.1.41 Register INSTRUCTION_1_0 (slave address: 0b100001x; register address: 0x43; default: 0x00)

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Figure 67. Register INSTRUCTION_1_0 Format

7	6	5	4	3	2	1	0
INSTRUCTION_1[23:16]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 43. Register INSTRUCTION_1_0 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_1[23:16]	R/W	00000000	

7.6.1.42 Register INSTRUCTION_1_1 (slave address: 0b100001x; register address: 0x44; default: 0x00)

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Figure 68. Register INSTRUCTION_1_1 Format

7	6	5	4	3	2	1	0
INSTRUCTION_1[15:8]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 44. Register INSTRUCTION_1_1 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_1[15:8]	R/W	00000000	

7.6.1.43 Register INSTRUCTION_1_2 (slave address: 0b100001x; register address: 0x45; default: 0x00)

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Figure 69. Register INSTRUCTION_1_2 Format

7	6	5	4	3	2	1	0
INSTRUCTION_1[7:0]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 45. Register INSTRUCTION_1_2 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_1[7:0]	R/W	00000000	

7.6.1.44 Register INSTRUCTION_2_0 (slave address: 0b100001x; register address: 0x46; default: 0x00)

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Figure 70. Register INSTRUCTION_2_0 Format

7	6	5	4	3	2	1	0
INSTRUCTION_2[23:16]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 46. Register INSTRUCTION_2_0 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_2[23:16]	R/W	00000000	

7.6.1.45 Register INSTRUCTION_2_1 (slave address: 0b100001x; register address: 0x47; default: 0x00)

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Figure 71. Register INSTRUCTION_2_1 Format

7	6	5	4	3	2	1	0
INSTRUCTION_2[15:8]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 47. Register INSTRUCTION_2_1 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_2[15:8]	R/W	00000000	

7.6.1.46 Register INSTRUCTION_2_2 (slave address: 0b100001x; register address: 0x48; default: 0x00)

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Figure 72. Register INSTRUCTION_2_2 Format

7	6	5	4	3	2	1	0
INSTRUCTION_2[7:0]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 48. Register INSTRUCTION_2_2 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_2[7:0]	R/W	00000000	

7.6.1.47 Register INSTRUCTION_3_0 (slave address: 0b100001x; register address: 0x49; default: 0x00)

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Figure 73. Register INSTRUCTION_3_0 Format

7	6	5	4	3	2	1	0
INSTRUCTION_3[23:16]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 49. Register INSTRUCTION_3_0 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_3[23:16]	R/W	00000000	

7.6.1.48 Register INSTRUCTION_3_1 (slave address: 0b100001x; register address: 0x4A; default: 0x00)

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Figure 74. Register INSTRUCTION_3_1 Format

7	6	5	4	3	2	1	0
INSTRUCTION_3[15:8]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 50. Register INSTRUCTION_3_1 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_3[15:8]	R/W	00000000	

7.6.1.49 Register INSTRUCTION_3_2 (slave address: 0b100001x; register address: 0x4B; default: 0x00)

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Figure 75. Register INSTRUCTION_3_2 Format

7	6	5	4	3	2	1	0
INSTRUCTION_3[7:0]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 51. Register INSTRUCTION_3_2 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_3[7:0]	R/W	00000000	

7.6.1.50 Register INSTRUCTION_4_0 (slave address: 0b100001x; register address: 0x4C; default: 0x00)

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Figure 76. Register INSTRUCTION_4_0 Format

7	6	5	4	3	2	1	0
INSTRUCTION_4[23:16]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 52. Register INSTRUCTION_4_0 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_4[23:16]	R/W	00000000	

7.6.1.51 Register INSTRUCTION_4_1 (slave address: 0b100001x; register address: 0x4D; default: 0x00)

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Figure 77. Register INSTRUCTION_4_1 Format

7	6	5	4	3	2	1	0
INSTRUCTION_4[15:8]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 53. Register INSTRUCTION_4_1 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_4[15:8]	R/W	00000000	

7.6.1.52 Register INSTRUCTION_4_2 (slave address: 0b100001x; register address: 0x4E; default: 0x00)

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Figure 78. Register INSTRUCTION_4_2 Format

7	6	5	4	3	2	1	0
INSTRUCTION_4[7:0]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 54. Register INSTRUCTION_4_2 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_4[7:0]	R/W	00000000	

7.6.1.53 Register INSTRUCTION_5_0 (slave address: 0b100001x; register address: 0x4F; default: 0x00)

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Figure 79. Register INSTRUCTION_5_0 Format

7	6	5	4	3	2	1	0
INSTRUCTION_5[23:16]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 55. Register INSTRUCTION_5_0 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_5[23:16]	R/W	00000000	

7.6.1.54 Register INSTRUCTION_5_1 (slave address: 0b100001x; register address: 0x50; default: 0x00)

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Figure 80. Register INSTRUCTION_5_1 Format

7	6	5	4	3	2	1	0
INSTRUCTION_5[15:8]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 56. Register INSTRUCTION_5_1 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_5[15:8]	R/W	00000000	

7.6.1.55 Register INSTRUCTION_5_2 (slave address: 0b100001x; register address: 0x51; default: 0x00)

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Figure 81. Register INSTRUCTION_5_2 Format

7	6	5	4	3	2	1	0
INSTRUCTION_5[7:0]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 57. Register INSTRUCTION_5_2 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_5[7:0]	R/W	00000000	

7.6.1.56 Register INSTRUCTION_6_0 (slave address: 0b100001x; register address: 0x52; default: 0x00)

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Figure 82. Register INSTRUCTION_6_0 Format

7	6	5	4	3	2	1	0
INSTRUCTION_6[23:16]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 58. Register INSTRUCTION_6_0 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_6[23:16]	R/W	00000000	

7.6.1.57 Register INSTRUCTION_6_1 (slave address: 0b100001x; register address: 0x53; default: 0x00)

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Figure 83. Register INSTRUCTION_6_1 Format

7	6	5	4	3	2	1	0
INSTRUCTION_6[15:8]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 59. Register INSTRUCTION_6_1 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_6[15:8]	R/W	00000000	

7.6.1.58 Register INSTRUCTION_6_2 (slave address: 0b100001x; register address: 0x54; default: 0x00)

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Figure 84. Register INSTRUCTION_6_2 Format

7	6	5	4	3	2	1	0
INSTRUCTION_6[7:0]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 60. Register INSTRUCTION_6_2 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_6[7:0]	R/W	00000000	

7.6.1.59 Register INSTRUCTION_7_0 (slave address: 0b100001x; register address: 0x55; default: 0x00)

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Figure 85. Register INSTRUCTION_7_0 Format

7	6	5	4	3	2	1	0
INSTRUCTION_7[23:16]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 61. Register INSTRUCTION_7_0 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_7[23:16]	R/W	00000000	

7.6.1.60 Register INSTRUCTION_7_1 (slave address: 0b100001x; register address: 0x56; default: 0x00)

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Figure 86. Register INSTRUCTION_7_1 Format

7	6	5	4	3	2	1	0
INSTRUCTION_7[15:8]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 62. Register INSTRUCTION_7_1 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_7[15:8]	R/W	00000000	

7.6.1.61 Register INSTRUCTION_7_2 (slave address: 0b100001x; register address: 0x57; default: 0x00)

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Figure 87. Register INSTRUCTION_7_2 Format

7	6	5	4	3	2	1	0
INSTRUCTION_7[7:0]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 63. Register INSTRUCTION_7_2 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_7[7:0]	R/W	00000000	

7.6.1.62 Register INSTRUCTION_8_0 (slave address: 0b100001x; register address: 0x58; default: 0x00)

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Figure 88. Register INSTRUCTION_8_0 Format

7	6	5	4	3	2	1	0
INSTRUCTION_8[23:16]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 64. Register INSTRUCTION_8_0 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_8[23:16]	R/W	00000000	

7.6.1.63 Register INSTRUCTION_8_1 (slave address: 0b100001x; register address: 0x59; default: 0x00)

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Figure 89. Register INSTRUCTION_8_1 Format

7	6	5	4	3	2	1	0
INSTRUCTION_8[15:8]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 65. Register INSTRUCTION_8_1 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_8[15:8]	R/W	00000000	

7.6.1.64 Register INSTRUCTION_8_2 (slave address: 0b100001x; register address: 0x5A; default: 0x00)

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Figure 90. Register INSTRUCTION_8_2 Format

7	6	5	4	3	2	1	0
INSTRUCTION_8[7:0]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 66. Register INSTRUCTION_8_2 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_8[7:0]	R/W	00000000	

7.6.1.65 Register INSTRUCTION_9_0 (slave address: 0b100001x; register address: 0x5B; default: 0x00)

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Figure 91. Register INSTRUCTION_9_0 Format

7	6	5	4	3	2	1	0
INSTRUCTION_9[23:16]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 67. Register INSTRUCTION_9_0 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_9[23:16]	R/W	00000000	

7.6.1.66 Register INSTRUCTION_9_1 (slave address: 0b100001x; register address: 0x5C; default: 0x00)

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Figure 92. Register INSTRUCTION_9_1 Format

7	6	5	4	3	2	1	0
INSTRUCTION_9[15:8]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 68. Register INSTRUCTION_9_1 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_9[15:8]	R/W	00000000	

7.6.1.67 Register INSTRUCTION_9_2 (slave address: 0b100001x; register address: 0x5D; default: 0x00)

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Figure 93. Register INSTRUCTION_9_2 Format

7	6	5	4	3	2	1	0
INSTRUCTION_9[7:0]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 69. Register INSTRUCTION_9_2 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_9[7:0]	R/W	00000000	

7.6.1.68 Register INSTRUCTION_10_0 (slave address: 0b100001x; register address: 0x5E; default: 0x00)

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Figure 94. Register INSTRUCTION_10_0 Format

7	6	5	4	3	2	1	0
INSTRUCTION_10[23:16]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 70. Register INSTRUCTION_10_0 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_10[23:16]	R/W	00000000	

7.6.1.69 Register INSTRUCTION_10_1 (slave address: 0b100001x; register address: 0x5F; default: 0x00)

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Figure 95. Register INSTRUCTION_10_1 Format

7	6	5	4	3	2	1	0
INSTRUCTION_10[15:8]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 71. Register INSTRUCTION_10_1 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_10[15:8]	R/W	00000000	

7.6.1.70 Register INSTRUCTION_10_2 (slave address: 0b100001x; register address: 0x60; default: 0x00)

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Figure 96. Register INSTRUCTION_10_2 Format

7	6	5	4	3	2	1	0
INSTRUCTION_10[7:0]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 72. Register INSTRUCTION_10_2 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_10[7:0]	R/W	00000000	

7.6.1.71 Register INSTRUCTION_11_0 (slave address: 0b100001x; register address: 0x61; default: 0x00)

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Figure 97. Register INSTRUCTION_11_0 Format

7	6	5	4	3	2	1	0
INSTRUCTION_11[23:16]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 73. Register INSTRUCTION_11_0 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_11[23:16]	R/W	00000000	

7.6.1.72 Register INSTRUCTION_11_1 (slave address: 0b100001x; register address: 0x62; default: 0x00)

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Figure 98. Register INSTRUCTION_11_1 Format

7	6	5	4	3	2	1	0
INSTRUCTION_11[15:8]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 74. Register INSTRUCTION_11_1 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_11[15:8]	R/W	00000000	

7.6.1.73 Register INSTRUCTION_11_2 (slave address: 0b100001x; register address: 0x63; default: 0x00)

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Figure 99. Register INSTRUCTION_11_2 Format

7	6	5	4	3	2	1	0
INSTRUCTION_11[7:0]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 75. Register INSTRUCTION_11_2 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_11[7:0]	R/W	00000000	

7.6.1.74 Register INSTRUCTION_12_0 (slave address: 0b100001x; register address: 0x64; default: 0x00)

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Figure 100. Register INSTRUCTION_12_0 Format

7	6	5	4	3	2	1	0
INSTRUCTION_12[23:16]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 76. Register INSTRUCTION_12_0 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_12[23:16]	R/W	00000000	

7.6.1.75 Register INSTRUCTION_12_1 (slave address: 0b100001x; register address: 0x65; default: 0x00)

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Figure 101. Register INSTRUCTION_12_1 Format

7	6	5	4	3	2	1	0
INSTRUCTION_12[15:8]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 77. Register INSTRUCTION_12_1 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_12[15:8]	R/W	00000000	

7.6.1.76 Register INSTRUCTION_12_2 (slave address: 0b100001x; register address: 0x66; default: 0x00)

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Figure 102. Register INSTRUCTION_12_2 Format

7	6	5	4	3	2	1	0
INSTRUCTION_12[7:0]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 78. Register INSTRUCTION_12_2 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_12[7:0]	R/W	00000000	

7.6.1.77 Register INSTRUCTION_13_0 (slave address: 0b100001x; register address: 0x67; default: 0x00)

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Figure 103. Register INSTRUCTION_13_0 Format

7	6	5	4	3	2	1	0
INSTRUCTION_13[23:16]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 79. Register INSTRUCTION_13_0 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_13[23:16]	R/W	00000000	

7.6.1.78 Register INSTRUCTION_13_1 (slave address: 0b100001x; register address: 0x68; default: 0x00)

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Figure 104. Register INSTRUCTION_13_1 Format

7	6	5	4	3	2	1	0
INSTRUCTION_13[15:8]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 80. Register INSTRUCTION_13_1 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_13[15:8]	R/W	00000000	

7.6.1.79 Register INSTRUCTION_13_2 (slave address: 0b100001x; register address: 0x69; default: 0x00)

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Figure 105. Register INSTRUCTION_13_2 Format

7	6	5	4	3	2	1	0
INSTRUCTION_13[7:0]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 81. Register INSTRUCTION_13_2 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_13[7:0]	R/W	00000000	

7.6.1.80 Register INSTRUCTION_14_0 (slave address: 0b100001x; register address: 0x6A; default: 0x00)

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Figure 106. Register INSTRUCTION_14_0 Format

7	6	5	4	3	2	1	0
INSTRUCTION_14[23:16]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 82. Register INSTRUCTION_14_0 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_14[23:16]	R/W	00000000	

7.6.1.81 Register INSTRUCTION_14_1 (slave address: 0b100001x; register address: 0x6B; default: 0x00)

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Figure 107. Register INSTRUCTION_14_1 Format

7	6	5	4	3	2	1	0
INSTRUCTION_14[15:8]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 83. Register INSTRUCTION_14_1 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_14[15:8]	R/W	00000000	

7.6.1.82 Register INSTRUCTION_14_2 (slave address: 0b100001x; register address: 0x6C; default: 0x00)

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Figure 108. Register INSTRUCTION_14_2 Format

7	6	5	4	3	2	1	0
INSTRUCTION_14[7:0]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 84. Register INSTRUCTION_14_2 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_14[7:0]	R/W	00000000	

7.6.1.83 Register INSTRUCTION_15_0 (slave address: 0b100001x; register address: 0x6D; default: 0x00)

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Figure 109. Register INSTRUCTION_15_0 Format

7	6	5	4	3	2	1	0
INSTRUCTION_15[23:16]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 85. Register INSTRUCTION_15_0 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_15[23:16]	R/W	00000000	

7.6.1.84 Register INSTRUCTION_15_1 (slave address: 0b100001x; register address: 0x6E; default: 0x00)

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Figure 110. Register INSTRUCTION_15_1 Format

7	6	5	4	3	2	1	0
INSTRUCTION_15[15:8]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 86. Register INSTRUCTION_15_1 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_15[15:8]	R/W	00000000	

7.6.1.85 Register INSTRUCTION_15_2 (slave address: 0b100001x; register address: 0x6F; default: 0x00)

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Figure 111. Register INSTRUCTION_15_2 Format

7	6	5	4	3	2	1	0
INSTRUCTION_15[7:0]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 87. Register INSTRUCTION_15_2 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_15[7:0]	R/W	00000000	

7.6.1.86 Register INSTRUCTION_16_0 (slave address: 0b100001x; register address: 0x70; default: 0x00)

Back to *Register Map*.

Figure 112. Register INSTRUCTION_16_0 Format

7	6	5	4	3	2	1	0
INSTRUCTION_16[23:16]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 88. Register INSTRUCTION_16_0 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_16[23:16]	R/W	00000000	

7.6.1.87 Register INSTRUCTION_16_1 (slave address: 0b100001x; register address: 0x71; default: 0x00)

Back to *Register Map*.

Figure 113. Register INSTRUCTION_16_1 Format

7	6	5	4	3	2	1	0
INSTRUCTION_16[15:8]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 89. Register INSTRUCTION_16_1 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_16[15:8]	R/W	00000000	

7.6.1.88 Register INSTRUCTION_16_2 (slave address: 0b100001x; register address: 0x72; default: 0x00)

Back to *Register Map*.

Figure 114. Register INSTRUCTION_16_2 Format

7	6	5	4	3	2	1	0
INSTRUCTION_16[7:0]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 90. Register INSTRUCTION_16_2 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_16[7:0]	R/W	00000000	

7.6.1.89 Register INSTRUCTION_17_0 (slave address: 0b100001x; register address: 0x73; default: 0x00)

Back to *Register Map*.

Figure 115. Register INSTRUCTION_17_0 Format

7	6	5	4	3	2	1	0
INSTRUCTION_17[23:16]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 91. Register INSTRUCTION_17_0 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_17[23:16]	R/W	00000000	

7.6.1.90 Register INSTRUCTION_17_1 (slave address: 0b100001x; register address: 0x74; default: 0x00)

Back to *Register Map*.

Figure 116. Register INSTRUCTION_17_1 Format

7	6	5	4	3	2	1	0
INSTRUCTION_17[15:8]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 92. Register INSTRUCTION_17_1 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_17[15:8]	R/W	00000000	

7.6.1.91 Register INSTRUCTION_17_2 (slave address: 0b100001x; register address: 0x75; default: 0x00)

Back to *Register Map*.

Figure 117. Register INSTRUCTION_17_2 Format

7	6	5	4	3	2	1	0
INSTRUCTION_17[7:0]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 93. Register INSTRUCTION_17_2 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_17[7:0]	R/W	00000000	

7.6.1.92 Register INSTRUCTION_18_0 (slave address: 0b100001x; register address: 0x76; default: 0x00)

Back to *Register Map*.

Figure 118. Register INSTRUCTION_18_0 Format

7	6	5	4	3	2	1	0
INSTRUCTION_18[23:16]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 94. Register INSTRUCTION_18_0 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_18[23:16]	R/W	00000000	

7.6.1.93 Register INSTRUCTION_18_1 (slave address: 0b100001x; register address: 0x77; default: 0x00)

Back to *Register Map*.

Figure 119. Register INSTRUCTION_18_1 Format

7	6	5	4	3	2	1	0
INSTRUCTION_18[15:8]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 95. Register INSTRUCTION_18_1 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_18[15:8]	R/W	00000000	

7.6.1.94 Register INSTRUCTION_18_2 (slave address: 0b100001x; register address: 0x78; default: 0x00)

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Figure 120. Register INSTRUCTION_18_2 Format

7	6	5	4	3	2	1	0
INSTRUCTION_18[7:0]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 96. Register INSTRUCTION_18_2 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_18[7:0]	R/W	00000000	

7.6.1.95 Register INSTRUCTION_19_0 (slave address: 0b100001x; register address: 0x79; default: 0x00)

Back to *Register Map*.

Figure 121. Register INSTRUCTION_19_0 Format

7	6	5	4	3	2	1	0
INSTRUCTION_19[23:16]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 97. Register INSTRUCTION_19_0 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_19[23:16]	R/W	00000000	

7.6.1.96 Register INSTRUCTION_19_1 (slave address: 0b100001x; register address: 0x7A; default: 0x00)

Back to *Register Map*.

Figure 122. Register INSTRUCTION_19_1 Format

7	6	5	4	3	2	1	0
INSTRUCTION_19[15:8]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 98. Register INSTRUCTION_19_1 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_19[15:8]	R/W	00000000	

7.6.1.97 Register INSTRUCTION_19_2 (slave address: 0b100001x; register address: 0x7B; default: 0x00)

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Figure 123. Register INSTRUCTION_19_2 Format

7	6	5	4	3	2	1	0
INSTRUCTION_19[7:0]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 99. Register INSTRUCTION_19_2 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_19[7:0]	R/W	00000000	

7.6.1.98 Register INSTRUCTION_20_0 (slave address: 0b100001x; register address: 0x7C; default: 0x00)

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Figure 124. Register INSTRUCTION_20_0 Format

7	6	5	4	3	2	1	0
INSTRUCTION_20[23:16]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 100. Register INSTRUCTION_20_0 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_20[23:16]	R/W	00000000	

7.6.1.99 Register INSTRUCTION_20_1 (slave address: 0b100001x; register address: 0x7D; default: 0x00)

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Figure 125. Register INSTRUCTION_20_1 Format

7	6	5	4	3	2	1	0
INSTRUCTION_20[15:8]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 101. Register INSTRUCTION_20_1 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_20[15:8]	R/W	00000000	

7.6.1.100 Register INSTRUCTION_20_2 (slave address: 0b100001x; register address: 0x7E; default: 0x00)

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Figure 126. Register INSTRUCTION_20_2 Format

7	6	5	4	3	2	1	0
INSTRUCTION_20[7:0]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 102. Register INSTRUCTION_20_2 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_20[7:0]	R/W	00000000	

7.6.1.101 Register INSTRUCTION_21_0 (slave address: 0b100001x; register address: 0x7F; default: 0x00)

Back to *Register Map*.

Figure 127. Register INSTRUCTION_21_0 Format

7	6	5	4	3	2	1	0
INSTRUCTION_21[23:16]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 103. Register INSTRUCTION_21_0 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_21[23:16]	R/W	00000000	

7.6.1.102 Register INSTRUCTION_21_1 (slave address: 0b100001x; register address: 0x80; default: 0x00)

Back to *Register Map*.

Figure 128. Register INSTRUCTION_21_1 Format

7	6	5	4	3	2	1	0
INSTRUCTION_21[15:8]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 104. Register INSTRUCTION_21_1 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_21[15:8]	R/W	00000000	

7.6.1.103 Register INSTRUCTION_21_2 (slave address: 0b100001x; register address: 0x81; default: 0x00)

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Figure 129. Register INSTRUCTION_21_2 Format

7	6	5	4	3	2	1	0
INSTRUCTION_21[7:0]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 105. Register INSTRUCTION_21_2 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_21[7:0]	R/W	00000000	

7.6.1.104 Register INSTRUCTION_22_0 (slave address: 0b100001x; register address: 0x82; default: 0x00)

Back to *Register Map*.

Figure 130. Register INSTRUCTION_22_0 Format

7	6	5	4	3	2	1	0
INSTRUCTION_22[23:16]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 106. Register INSTRUCTION_22_0 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_22[23:16]	R/W	00000000	

7.6.1.105 Register INSTRUCTION_22_1 (slave address: 0b100001x; register address: 0x83; default: 0x00)

Back to *Register Map*.

Figure 131. Register INSTRUCTION_22_1 Format

7	6	5	4	3	2	1	0
INSTRUCTION_22[15:8]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 107. Register INSTRUCTION_22_1 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_22[15:8]	R/W	00000000	

7.6.1.106 Register INSTRUCTION_22_2 (slave address: 0b100001x; register address: 0x84; default: 0x00)

Back to *Register Map*.

Figure 132. Register INSTRUCTION_22_2 Format

7	6	5	4	3	2	1	0
INSTRUCTION_22[7:0]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 108. Register INSTRUCTION_22_2 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_22[7:0]	R/W	00000000	

7.6.1.107 Register INSTRUCTION_23_0 (slave address: 0b100001x; register address: 0x85; default: 0x00)

Back to *Register Map*.

Figure 133. Register INSTRUCTION_23_0 Format

7	6	5	4	3	2	1	0
INSTRUCTION_23[23:16]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 109. Register INSTRUCTION_23_0 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_23[23:16]	R/W	00000000	

7.6.1.108 Register INSTRUCTION_23_1 (slave address: 0b100001x; register address: 0x86; default: 0x00)

Back to *Register Map*.

Figure 134. Register INSTRUCTION_23_1 Format

7	6	5	4	3	2	1	0
INSTRUCTION_23[15:8]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 110. Register INSTRUCTION_23_1 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_23[15:8]	R/W	00000000	

7.6.1.109 Register INSTRUCTION_23_2 (slave address: 0b100001x; register address: 0x87; default: 0x00)

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Figure 135. Register INSTRUCTION_23_2 Format

7	6	5	4	3	2	1	0
INSTRUCTION_23[7:0]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 111. Register INSTRUCTION_23_2 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_23[7:0]	R/W	00000000	

7.6.1.110 Register INSTRUCTION_24_0 (slave address: 0b100001x; register address: 0x88; default: 0x00)

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Figure 136. Register INSTRUCTION_24_0 Format

7	6	5	4	3	2	1	0
INSTRUCTION_24[23:16]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 112. Register INSTRUCTION_24_0 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_24[23:16]	R/W	00000000	

7.6.1.111 Register INSTRUCTION_24_1 (slave address: 0b100001x; register address: 0x89; default: 0x00)

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Figure 137. Register INSTRUCTION_24_1 Format

7	6	5	4	3	2	1	0
INSTRUCTION_24[15:8]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 113. Register INSTRUCTION_24_1 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_24[15:8]	R/W	00000000	

7.6.1.112 Register INSTRUCTION_24_2 (slave address: 0b100001x; register address: 0x8A; default: 0x00)

Back to *Register Map*.

Figure 138. Register INSTRUCTION_24_2 Format

7	6	5	4	3	2	1	0
INSTRUCTION_24[7:0]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 114. Register INSTRUCTION_24_2 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_24[7:0]	R/W	00000000	

7.6.1.113 Register INSTRUCTION_25_0 (slave address: 0b100001x; register address: 0x8B; default: 0x00)

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Figure 139. Register INSTRUCTION_25_0 Format

7	6	5	4	3	2	1	0
INSTRUCTION_25[23:16]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 115. Register INSTRUCTION_25_0 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_25[23:16]	R/W	00000000	

7.6.1.114 Register INSTRUCTION_25_1 (slave address: 0b100001x; register address: 0x8C; default: 0x00)

Back to *Register Map*.

Figure 140. Register INSTRUCTION_25_1 Format

7	6	5	4	3	2	1	0
INSTRUCTION_25[15:8]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 116. Register INSTRUCTION_25_1 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_25[15:8]	R/W	00000000	

7.6.1.115 Register INSTRUCTION_25_2 (slave address: 0b100001x; register address: 0x8D; default: 0x00)

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Figure 141. Register INSTRUCTION_25_2 Format

7	6	5	4	3	2	1	0
INSTRUCTION_25[7:0]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 117. Register INSTRUCTION_25_2 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_25[7:0]	R/W	00000000	

7.6.1.116 Register INSTRUCTION_26_0 (slave address: 0b100001x; register address: 0x8E; default: 0x00)

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Figure 142. Register INSTRUCTION_26_0 Format

7	6	5	4	3	2	1	0
INSTRUCTION_26[23:16]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 118. Register INSTRUCTION_26_0 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_26[23:16]	R/W	00000000	

7.6.1.117 Register INSTRUCTION_26_1 (slave address: 0b100001x; register address: 0x8F; default: 0x00)

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Figure 143. Register INSTRUCTION_26_1 Format

7	6	5	4	3	2	1	0
INSTRUCTION_26[15:8]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 119. Register INSTRUCTION_26_1 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_26[15:8]	R/W	00000000	

7.6.1.118 Register INSTRUCTION_26_2 (slave address: 0b100001x; register address: 0x90; default: 0x00)

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Figure 144. Register INSTRUCTION_26_2 Format

7	6	5	4	3	2	1	0
INSTRUCTION_26[7:0]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 120. Register INSTRUCTION_26_2 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_26[7:0]	R/W	00000000	

7.6.1.119 Register INSTRUCTION_27_0 (slave address: 0b100001x; register address: 0x91; default: 0x00)

Back to *Register Map*.

Figure 145. Register INSTRUCTION_27_0 Format

7	6	5	4	3	2	1	0
INSTRUCTION_27[23:16]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 121. Register INSTRUCTION_27_0 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_27[23:16]	R/W	00000000	

7.6.1.120 Register INSTRUCTION_27_1 (slave address: 0b100001x; register address: 0x92; default: 0x00)

Back to *Register Map*.

Figure 146. Register INSTRUCTION_27_1 Format

7	6	5	4	3	2	1	0
INSTRUCTION_27[15:8]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 122. Register INSTRUCTION_27_1 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_27[15:8]	R/W	00000000	

7.6.1.121 Register INSTRUCTION_27_2 (slave address: 0b100001x; register address: 0x93; default: 0x00)

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Figure 147. Register INSTRUCTION_27_2 Format

7	6	5	4	3	2	1	0
INSTRUCTION_27[7:0]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 123. Register INSTRUCTION_27_2 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_27[7:0]	R/W	00000000	

7.6.1.122 Register INSTRUCTION_28_0 (slave address: 0b100001x; register address: 0x94; default: 0x00)

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Figure 148. Register INSTRUCTION_28_0 Format

7	6	5	4	3	2	1	0
INSTRUCTION_28[23:16]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 124. Register INSTRUCTION_28_0 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_28[23:16]	R/W	00000000	

7.6.1.123 Register INSTRUCTION_28_1 (slave address: 0b100001x; register address: 0x95; default: 0x00)

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Figure 149. Register INSTRUCTION_28_1 Format

7	6	5	4	3	2	1	0
INSTRUCTION_28[15:8]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 125. Register INSTRUCTION_28_1 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_28[15:8]	R/W	00000000	

7.6.1.124 Register INSTRUCTION_28_2 (slave address: 0b100001x; register address: 0x96; default: 0x00)

Back to *Register Map*.

Figure 150. Register INSTRUCTION_28_2 Format

7	6	5	4	3	2	1	0
INSTRUCTION_28[7:0]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 126. Register INSTRUCTION_28_2 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_28[7:0]	R/W	00000000	

7.6.1.125 Register INSTRUCTION_29_0 (slave address: 0b100001x; register address: 0x97; default: 0x00)

Back to *Register Map*.

Figure 151. Register INSTRUCTION_29_0 Format

7	6	5	4	3	2	1	0
INSTRUCTION_29[23:16]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 127. Register INSTRUCTION_29_0 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_29[23:16]	R/W	00000000	

7.6.1.126 Register INSTRUCTION_29_1 (slave address: 0b100001x; register address: 0x98; default: 0x00)

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Figure 152. Register INSTRUCTION_29_1 Format

7	6	5	4	3	2	1	0
INSTRUCTION_29[15:8]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 128. Register INSTRUCTION_29_1 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_29[15:8]	R/W	00000000	

7.6.1.127 Register INSTRUCTION_29_2 (slave address: 0b100001x; register address: 0x99; default: 0x00)

Back to *Register Map*.

Figure 153. Register INSTRUCTION_29_2 Format

7	6	5	4	3	2	1	0
INSTRUCTION_29[7:0]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 129. Register INSTRUCTION_29_2 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_29[7:0]	R/W	00000000	

7.6.1.128 Register INSTRUCTION_30_0 (slave address: 0b100001x; register address: 0x9A; default: 0x00)

Back to *Register Map*.

Figure 154. Register INSTRUCTION_30_0 Format

7	6	5	4	3	2	1	0
INSTRUCTION_30[23:16]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 130. Register INSTRUCTION_30_0 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_30[23:16]	R/W	00000000	

7.6.1.129 Register INSTRUCTION_30_1 (slave address: 0b100001x; register address: 0x9B; default: 0x00)

Back to *Register Map*.

Figure 155. Register INSTRUCTION_30_1 Format

7	6	5	4	3	2	1	0
INSTRUCTION_30[15:8]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 131. Register INSTRUCTION_30_1 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_30[15:8]	R/W	00000000	

7.6.1.130 Register INSTRUCTION_30_2 (slave address: 0b100001x; register address: 0x9C; default: 0x00)

Back to *Register Map*.

Figure 156. Register INSTRUCTION_30_2 Format

7	6	5	4	3	2	1	0
INSTRUCTION_30[7:0]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 132. Register INSTRUCTION_30_2 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_30[7:0]	R/W	00000000	

7.6.1.131 Register INSTRUCTION_31_0 (slave address: 0b100001x; register address: 0x9D; default: 0x00)

Back to *Register Map*.

Figure 157. Register INSTRUCTION_31_0 Format

7	6	5	4	3	2	1	0
INSTRUCTION_31[23:16]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 133. Register INSTRUCTION_31_0 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_31[23:16]	R/W	00000000	

7.6.1.132 Register INSTRUCTION_31_1 (slave address: 0b100001x; register address: 0x9E; default: 0x00)

Back to *Register Map*.

Figure 158. Register INSTRUCTION_31_1 Format

7	6	5	4	3	2	1	0
INSTRUCTION_31[15:8]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 134. Register INSTRUCTION_31_1 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_31[15:8]	R/W	00000000	

7.6.1.133 Register INSTRUCTION_31_2 (slave address: 0b100001x; register address: 0x9F; default: 0x00)

Back to *Register Map*.

Figure 159. Register INSTRUCTION_31_2 Format

7	6	5	4	3	2	1	0
INSTRUCTION_31[7:0]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 135. Register INSTRUCTION_31_2 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_31[7:0]	R/W	00000000	

7.6.1.134 Register INSTRUCTION_32_0 (slave address: 0b100001x; register address: 0xA0; default: 0x00)

Back to *Register Map*.

Figure 160. Register INSTRUCTION_32_0 Format

7	6	5	4	3	2	1	0
INSTRUCTION_32[23:16]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 136. Register INSTRUCTION_32_0 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_32[23:16]	R/W	00000000	

7.6.1.135 Register INSTRUCTION_32_1 (slave address: 0b100001x; register address: 0xA1; default: 0x00)

Back to *Register Map*.

Figure 161. Register INSTRUCTION_32_1 Format

7	6	5	4	3	2	1	0
INSTRUCTION_32[15:8]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 137. Register INSTRUCTION_32_1 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_32[15:8]	R/W	00000000	

7.6.1.136 Register INSTRUCTION_32_2 (slave address: 0b100001x; register address: 0xA2; default: 0x00)

Back to *Register Map*.

Figure 162. Register INSTRUCTION_32_2 Format

7	6	5	4	3	2	1	0
INSTRUCTION_32[7:0]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 138. Register INSTRUCTION_32_2 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_32[7:0]	R/W	00000000	

7.6.1.137 Register INSTRUCTION_33_0 (slave address: 0b100001x; register address: 0xA3; default: 0x00)

Back to *Register Map*.

Figure 163. Register INSTRUCTION_33_0 Format

7	6	5	4	3	2	1	0
INSTRUCTION_33[23:16]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 139. Register INSTRUCTION_33_0 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_33[23:16]	R/W	00000000	

7.6.1.138 Register INSTRUCTION_33_1 (slave address: 0b100001x; register address: 0xA4; default: 0x00)

Back to *Register Map*.

Figure 164. Register INSTRUCTION_33_1 Format

7	6	5	4	3	2	1	0
INSTRUCTION_33[15:8]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 140. Register INSTRUCTION_33_1 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_33[15:8]	R/W	00000000	

7.6.1.139 Register INSTRUCTION_33_2 (slave address: 0b100001x; register address: 0xA5; default: 0x00)

Back to *Register Map*.

Figure 165. Register INSTRUCTION_33_2 Format

7	6	5	4	3	2	1	0
INSTRUCTION_33[7:0]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 141. Register INSTRUCTION_33_2 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_33[7:0]	R/W	00000000	

7.6.1.140 Register INSTRUCTION_34_0 (slave address: 0b100001x; register address: 0xA6; default: 0x00)

Back to *Register Map*.

Figure 166. Register INSTRUCTION_34_0 Format

7	6	5	4	3	2	1	0
INSTRUCTION_34[23:16]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 142. Register INSTRUCTION_34_0 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_34[23:16]	R/W	00000000	

7.6.1.141 Register INSTRUCTION_34_1 (slave address: 0b100001x; register address: 0xA7; default: 0x00)

Back to *Register Map*.

Figure 167. Register INSTRUCTION_34_1 Format

7	6	5	4	3	2	1	0
INSTRUCTION_34[15:8]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 143. Register INSTRUCTION_34_1 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_34[15:8]	R/W	00000000	

7.6.1.142 Register INSTRUCTION_34_2 (slave address: 0b100001x; register address: 0xA8; default: 0x00)

Back to *Register Map*.

Figure 168. Register INSTRUCTION_34_2 Format

7	6	5	4	3	2	1	0
INSTRUCTION_34[7:0]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 144. Register INSTRUCTION_34_2 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_34[7:0]	R/W	00000000	

7.6.1.143 Register INSTRUCTION_35_0 (slave address: 0b100001x; register address: 0xA9; default: 0x00)

Back to *Register Map*.

Figure 169. Register INSTRUCTION_35_0 Format

7	6	5	4	3	2	1	0
INSTRUCTION_35[23:16]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 145. Register INSTRUCTION_35_0 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_35[23:16]	R/W	00000000	

7.6.1.144 Register INSTRUCTION_35_1 (slave address: 0b100001x; register address: 0xAA; default: 0x00)

Back to *Register Map*.

Figure 170. Register INSTRUCTION_35_1 Format

7	6	5	4	3	2	1	0
INSTRUCTION_35[15:8]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 146. Register INSTRUCTION_35_1 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_35[15:8]	R/W	00000000	

7.6.1.145 Register INSTRUCTION_35_2 (slave address: 0b100001x; register address: 0xAB; default: 0x00)

Back to *Register Map*.

Figure 171. Register INSTRUCTION_35_2 Format

7	6	5	4	3	2	1	0
INSTRUCTION_35[7:0]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 147. Register INSTRUCTION_35_2 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_35[7:0]	R/W	00000000	

7.6.1.146 Register INSTRUCTION_36_0 (slave address: 0b100001x; register address: 0xAC; default: 0x00)

Back to *Register Map*.

Figure 172. Register INSTRUCTION_36_0 Format

7	6	5	4	3	2	1	0
INSTRUCTION_36[23:16]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 148. Register INSTRUCTION_36_0 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_36[23:16]	R/W	00000000	

7.6.1.147 Register INSTRUCTION_36_1 (slave address: 0b100001x; register address: 0xAD; default: 0x00)

Back to *Register Map*.

Figure 173. Register INSTRUCTION_36_1 Format

7	6	5	4	3	2	1	0
INSTRUCTION_36[15:8]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 149. Register INSTRUCTION_36_1 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_36[15:8]	R/W	00000000	

7.6.1.148 Register INSTRUCTION_36_2 (slave address: 0b100001x; register address: 0xAE; default: 0x00)

Back to *Register Map*.

Figure 174. Register INSTRUCTION_36_2 Format

7	6	5	4	3	2	1	0
INSTRUCTION_36[7:0]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 150. Register INSTRUCTION_36_2 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_36[7:0]	R/W	00000000	

7.6.1.149 Register INSTRUCTION_37_0 (slave address: 0b100001x; register address: 0xAF; default: 0x00)

Back to *Register Map*.

Figure 175. Register INSTRUCTION_37_0 Format

7	6	5	4	3	2	1	0
INSTRUCTION_37[23:16]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 151. Register INSTRUCTION_37_0 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_37[23:16]	R/W	00000000	

7.6.1.150 Register INSTRUCTION_37_1 (slave address: 0b100001x; register address: 0xB0; default: 0x00)

Back to *Register Map*.

Figure 176. Register INSTRUCTION_37_1 Format

7	6	5	4	3	2	1	0
INSTRUCTION_37[15:8]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 152. Register INSTRUCTION_37_1 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_37[15:8]	R/W	00000000	

7.6.1.151 Register INSTRUCTION_37_2 (slave address: 0b100001x; register address: 0xB1; default: 0x00)

Back to *Register Map*.

Figure 177. Register INSTRUCTION_37_2 Format

7	6	5	4	3	2	1	0
INSTRUCTION_37[7:0]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 153. Register INSTRUCTION_37_2 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_37[7:0]	R/W	00000000	

7.6.1.152 Register INSTRUCTION_38_0 (slave address: 0b100001x; register address: 0xB2; default: 0x00)

Back to *Register Map*.

Figure 178. Register INSTRUCTION_38_0 Format

7	6	5	4	3	2	1	0
INSTRUCTION_38[23:16]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 154. Register INSTRUCTION_38_0 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_38[23:16]	R/W	00000000	

7.6.1.153 Register INSTRUCTION_38_1 (slave address: 0b100001x; register address: 0xB3; default: 0x00)

Back to *Register Map*.

Figure 179. Register INSTRUCTION_38_1 Format

7	6	5	4	3	2	1	0
INSTRUCTION_38[15:8]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 155. Register INSTRUCTION_38_1 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_38[15:8]	R/W	00000000	

7.6.1.154 Register INSTRUCTION_38_2 (slave address: 0b100001x; register address: 0xB4; default: 0x00)

Back to *Register Map*.

Figure 180. Register INSTRUCTION_38_2 Format

7	6	5	4	3	2	1	0
INSTRUCTION_38[7:0]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 156. Register INSTRUCTION_38_2 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_38[7:0]	R/W	00000000	

7.6.1.155 Register INSTRUCTION_39_0 (slave address: 0b100001x; register address: 0xB5; default: 0x00)

Back to *Register Map*.

Figure 181. Register INSTRUCTION_39_0 Format

7	6	5	4	3	2	1	0
INSTRUCTION_39[23:16]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 157. Register INSTRUCTION_39_0 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_39[23:16]	R/W	00000000	

7.6.1.156 Register INSTRUCTION_39_1 (slave address: 0b100001x; register address: 0xB6; default: 0x00)

Back to *Register Map*.

Figure 182. Register INSTRUCTION_39_1 Format

7	6	5	4	3	2	1	0
INSTRUCTION_39[15:8]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 158. Register INSTRUCTION_39_1 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_39[15:8]	R/W	00000000	

7.6.1.157 Register INSTRUCTION_39_2 (slave address: 0b100001x; register address: 0xB7; default: 0x00)

Back to *Register Map*.

Figure 183. Register INSTRUCTION_39_2 Format

7	6	5	4	3	2	1	0
INSTRUCTION_39[7:0]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 159. Register INSTRUCTION_39_2 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_39[7:0]	R/W	00000000	

7.6.1.158 Register INSTRUCTION_40_0 (slave address: 0b100001x; register address: 0xB8; default: 0x00)

Back to *Register Map*.

Figure 184. Register INSTRUCTION_40_0 Format

7	6	5	4	3	2	1	0
INSTRUCTION_40[23:16]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 160. Register INSTRUCTION_40_0 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_40[23:16]	R/W	00000000	

7.6.1.159 Register INSTRUCTION_40_1 (slave address: 0b100001x; register address: 0xB9; default: 0x00)

Back to *Register Map*.

Figure 185. Register INSTRUCTION_40_1 Format

7	6	5	4	3	2	1	0
INSTRUCTION_40[15:8]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 161. Register INSTRUCTION_40_1 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_40[15:8]	R/W	00000000	

7.6.1.160 Register INSTRUCTION_40_2 (slave address: 0b100001x; register address: 0xBA; default: 0x00)

Back to *Register Map*.

Figure 186. Register INSTRUCTION_40_2 Format

7	6	5	4	3	2	1	0
INSTRUCTION_40[7:0]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 162. Register INSTRUCTION_40_2 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_40[7:0]	R/W	00000000	

7.6.1.161 Register INSTRUCTION_41_0 (slave address: 0b100001x; register address: 0xBB; default: 0x00)

Back to *Register Map*.

Figure 187. Register INSTRUCTION_41_0 Format

7	6	5	4	3	2	1	0
INSTRUCTION_41[23:16]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 163. Register INSTRUCTION_41_0 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_41[23:16]	R/W	00000000	

7.6.1.162 Register INSTRUCTION_41_1 (slave address: 0b100001x; register address: 0xBC; default: 0x00)

Back to *Register Map*.

Figure 188. Register INSTRUCTION_41_1 Format

7	6	5	4	3	2	1	0
INSTRUCTION_41[15:8]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 164. Register INSTRUCTION_41_1 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_41[15:8]	R/W	00000000	

7.6.1.163 Register INSTRUCTION_41_2 (slave address: 0b100001x; register address: 0xBD; default: 0x00)

Back to *Register Map*.

Figure 189. Register INSTRUCTION_41_2 Format

7	6	5	4	3	2	1	0
INSTRUCTION_41[7:0]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 165. Register INSTRUCTION_41_2 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_41[7:0]	R/W	00000000	

7.6.1.164 Register INSTRUCTION_42_0 (slave address: 0b100001x; register address: 0xBE; default: 0x00)

Back to *Register Map*.

Figure 190. Register INSTRUCTION_42_0 Format

7	6	5	4	3	2	1	0
INSTRUCTION_42[23:16]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 166. Register INSTRUCTION_42_0 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_42[23:16]	R/W	00000000	

7.6.1.165 Register INSTRUCTION_42_1 (slave address: 0b100001x; register address: 0xBF; default: 0x00)

Back to *Register Map*.

Figure 191. Register INSTRUCTION_42_1 Format

7	6	5	4	3	2	1	0
INSTRUCTION_42[15:8]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 167. Register INSTRUCTION_42_1 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_42[15:8]	R/W	00000000	

7.6.1.166 Register INSTRUCTION_42_2 (slave address: 0b100001x; register address: 0xC0; default: 0x00)

Back to *Register Map*.

Figure 192. Register INSTRUCTION_42_2 Format

7	6	5	4	3	2	1	0
INSTRUCTION_42[7:0]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 168. Register INSTRUCTION_42_2 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_42[7:0]	R/W	00000000	

7.6.1.167 Register INSTRUCTION_43_0 (slave address: 0b100001x; register address: 0xC1; default: 0x00)

Back to *Register Map*.

Figure 193. Register INSTRUCTION_43_0 Format

7	6	5	4	3	2	1	0
INSTRUCTION_43[23:16]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 169. Register INSTRUCTION_43_0 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_43[23:16]	R/W	00000000	

7.6.1.168 Register INSTRUCTION_43_1 (slave address: 0b100001x; register address: 0xC2; default: 0x00)

Back to *Register Map*.

Figure 194. Register INSTRUCTION_43_1 Format

7	6	5	4	3	2	1	0
INSTRUCTION_43[15:8]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 170. Register INSTRUCTION_43_1 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_43[15:8]	R/W	00000000	

7.6.1.169 Register INSTRUCTION_43_2 (slave address: 0b100001x; register address: 0xC3; default: 0x00)

Back to *Register Map*.

Figure 195. Register INSTRUCTION_43_2 Format

7	6	5	4	3	2	1	0
INSTRUCTION_43[7:0]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 171. Register INSTRUCTION_43_2 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_43[7:0]	R/W	00000000	

7.6.1.170 Register INSTRUCTION_44_0 (slave address: 0b100001x; register address: 0xC4; default: 0x00)

Back to *Register Map*.

Figure 196. Register INSTRUCTION_44_0 Format

7	6	5	4	3	2	1	0
INSTRUCTION_44[23:16]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 172. Register INSTRUCTION_44_0 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_44[23:16]	R/W	00000000	

7.6.1.171 Register INSTRUCTION_44_1 (slave address: 0b100001x; register address: 0xC5; default: 0x00)

Back to *Register Map*.

Figure 197. Register INSTRUCTION_44_1 Format

7	6	5	4	3	2	1	0
INSTRUCTION_44[15:8]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 173. Register INSTRUCTION_44_1 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_44[15:8]	R/W	00000000	

7.6.1.172 Register INSTRUCTION_44_2 (slave address: 0b100001x; register address: 0xC6; default: 0x00)

Back to *Register Map*.

Figure 198. Register INSTRUCTION_44_2 Format

7	6	5	4	3	2	1	0
INSTRUCTION_44[7:0]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 174. Register INSTRUCTION_44_2 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_44[7:0]	R/W	00000000	

7.6.1.173 Register INSTRUCTION_45_0 (slave address: 0b100001x; register address: 0xC7; default: 0x00)

Back to *Register Map*.

Figure 199. Register INSTRUCTION_45_0 Format

7	6	5	4	3	2	1	0
INSTRUCTION_45[23:16]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 175. Register INSTRUCTION_45_0 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_45[23:16]	R/W	00000000	

7.6.1.174 Register INSTRUCTION_45_1 (slave address: 0b100001x; register address: 0xC8; default: 0x00)

Back to *Register Map*.

Figure 200. Register INSTRUCTION_45_1 Format

7	6	5	4	3	2	1	0
INSTRUCTION_45[15:8]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 176. Register INSTRUCTION_45_1 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_45[15:8]	R/W	00000000	

7.6.1.175 Register INSTRUCTION_45_2 (slave address: 0b100001x; register address: 0xC9; default: 0x00)

Back to *Register Map*.

Figure 201. Register INSTRUCTION_45_2 Format

7	6	5	4	3	2	1	0
INSTRUCTION_45[7:0]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 177. Register INSTRUCTION_45_2 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_45[7:0]	R/W	00000000	

7.6.1.176 Register INSTRUCTION_46_0 (slave address: 0b100001x; register address: 0xCA; default: 0x00)

Back to *Register Map*.

Figure 202. Register INSTRUCTION_46_0 Format

7	6	5	4	3	2	1	0
INSTRUCTION_46[23:16]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 178. Register INSTRUCTION_46_0 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_46[23:16]	R/W	00000000	

7.6.1.177 Register INSTRUCTION_46_1 (slave address: 0b100001x; register address: 0xCB; default: 0x00)

Back to *Register Map*.

Figure 203. Register INSTRUCTION_46_1 Format

7	6	5	4	3	2	1	0
INSTRUCTION_46[15:8]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 179. Register INSTRUCTION_46_1 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_46[15:8]	R/W	00000000	

7.6.1.178 Register INSTRUCTION_46_2 (slave address: 0b100001x; register address: 0xCC; default: 0x00)

Back to *Register Map*.

Figure 204. Register INSTRUCTION_46_2 Format

7	6	5	4	3	2	1	0
INSTRUCTION_46[7:0]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 180. Register INSTRUCTION_46_2 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_46[7:0]	R/W	00000000	

7.6.1.179 Register INSTRUCTION_47_0 (slave address: 0b100001x; register address: 0xCD; default: 0x00)

Back to *Register Map*.

Figure 205. Register INSTRUCTION_47_0 Format

7	6	5	4	3	2	1	0
INSTRUCTION_47[23:16]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 181. Register INSTRUCTION_47_0 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_47[23:16]	R/W	00000000	

7.6.1.180 Register INSTRUCTION_47_1 (slave address: 0b100001x; register address: 0xCE; default: 0x00)

Back to *Register Map*.

Figure 206. Register INSTRUCTION_47_1 Format

7	6	5	4	3	2	1	0
INSTRUCTION_47[15:8]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 182. Register INSTRUCTION_47_1 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_47[15:8]	R/W	00000000	

7.6.1.181 Register INSTRUCTION_47_2 (slave address: 0b100001x; register address: 0xCF; default: 0x00)

Back to *Register Map*.

Figure 207. Register INSTRUCTION_47_2 Format

7	6	5	4	3	2	1	0
INSTRUCTION_47[7:0]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 183. Register INSTRUCTION_47_2 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_47[7:0]	R/W	00000000	

7.6.1.182 Register INSTRUCTION_48_0 (slave address: 0b100001x; register address: 0xD0; default: 0x00)

Back to *Register Map*.

Figure 208. Register INSTRUCTION_48_0 Format

7	6	5	4	3	2	1	0
INSTRUCTION_48[23:16]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 184. Register INSTRUCTION_48_0 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_48[23:16]	R/W	00000000	

7.6.1.183 Register INSTRUCTION_48_1 (slave address: 0b100001x; register address: 0xD1; default: 0x00)

Back to *Register Map*.

Figure 209. Register INSTRUCTION_48_1 Format

7	6	5	4	3	2	1	0
INSTRUCTION_48[15:8]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 185. Register INSTRUCTION_48_1 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_48[15:8]	R/W	00000000	

7.6.1.184 Register INSTRUCTION_48_2 (slave address: 0b100001x; register address: 0xD2; default: 0x00)

Back to *Register Map*.

Figure 210. Register INSTRUCTION_48_2 Format

7	6	5	4	3	2	1	0
INSTRUCTION_48[7:0]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 186. Register INSTRUCTION_48_2 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_48[7:0]	R/W	00000000	

7.6.1.185 Register INSTRUCTION_49_0 (slave address: 0b100001x; register address: 0xD3; default: 0x00)

Back to *Register Map*.

Figure 211. Register INSTRUCTION_49_0 Format

7	6	5	4	3	2	1	0
INSTRUCTION_49[23:16]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 187. Register INSTRUCTION_49_0 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_49[23:16]	R/W	00000000	

7.6.1.186 Register INSTRUCTION_49_1 (slave address: 0b100001x; register address: 0xD4; default: 0x00)

Back to *Register Map*.

Figure 212. Register INSTRUCTION_49_1 Format

7	6	5	4	3	2	1	0
INSTRUCTION_49[15:8]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 188. Register INSTRUCTION_49_1 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_49[15:8]	R/W	00000000	

7.6.1.187 Register INSTRUCTION_49_2 (slave address: 0b100001x; register address: 0xD5; default: 0x00)

Back to *Register Map*.

Figure 213. Register INSTRUCTION_49_2 Format

7	6	5	4	3	2	1	0
INSTRUCTION_49[7:0]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 189. Register INSTRUCTION_49_2 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_49[7:0]	R/W	00000000	

7.6.1.188 Register INSTRUCTION_50_0 (slave address: 0b100001x; register address: 0xD6; default: 0x00)

Back to *Register Map*.

Figure 214. Register INSTRUCTION_50_0 Format

7	6	5	4	3	2	1	0
INSTRUCTION_50[23:16]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 190. Register INSTRUCTION_50_0 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_50[23:16]	R/W	00000000	

7.6.1.189 Register INSTRUCTION_50_1 (slave address: 0b100001x; register address: 0xD7; default: 0x00)

Back to *Register Map*.

Figure 215. Register INSTRUCTION_50_1 Format

7	6	5	4	3	2	1	0
INSTRUCTION_50[15:8]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 191. Register INSTRUCTION_50_1 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_50[15:8]	R/W	00000000	

7.6.1.190 Register INSTRUCTION_50_2 (slave address: 0b100001x; register address: 0xD8; default: 0x00)

Back to *Register Map*.

Figure 216. Register INSTRUCTION_50_2 Format

7	6	5	4	3	2	1	0
INSTRUCTION_50[7:0]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 192. Register INSTRUCTION_50_2 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_50[7:0]	R/W	00000000	

7.6.1.191 Register INSTRUCTION_51_0 (slave address: 0b100001x; register address: 0xD9; default: 0x00)

Back to *Register Map*.

Figure 217. Register INSTRUCTION_51_0 Format

7	6	5	4	3	2	1	0
INSTRUCTION_51[23:16]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 193. Register INSTRUCTION_51_0 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_51[23:16]	R/W	00000000	

7.6.1.192 Register INSTRUCTION_51_1 (slave address: 0b100001x; register address: 0xDA; default: 0x00)

Back to *Register Map*.

Figure 218. Register INSTRUCTION_51_1 Format

7	6	5	4	3	2	1	0
INSTRUCTION_51[15:8]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 194. Register INSTRUCTION_51_1 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_51[15:8]	R/W	00000000	

7.6.1.193 Register INSTRUCTION_51_2 (slave address: 0b100001x; register address: 0xDB; default: 0x00)

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Figure 219. Register INSTRUCTION_51_2 Format

7	6	5	4	3	2	1	0
INSTRUCTION_51[7:0]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 195. Register INSTRUCTION_51_2 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_51[7:0]	R/W	00000000	

7.6.1.194 Register INSTRUCTION_52_0 (slave address: 0b100001x; register address: 0xDC; default: 0x00)

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Figure 220. Register INSTRUCTION_52_0 Format

7	6	5	4	3	2	1	0
INSTRUCTION_52[23:16]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 196. Register INSTRUCTION_52_0 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_52[23:16]	R/W	00000000	

7.6.1.195 Register INSTRUCTION_52_1 (slave address: 0b100001x; register address: 0xDD; default: 0x00)

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Figure 221. Register INSTRUCTION_52_1 Format

7	6	5	4	3	2	1	0
INSTRUCTION_52[15:8]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 197. Register INSTRUCTION_52_1 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_52[15:8]	R/W	00000000	

7.6.1.196 Register INSTRUCTION_52_2 (slave address: 0b100001x; register address: 0xDE; default: 0x00)

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Figure 222. Register INSTRUCTION_52_2 Format

7	6	5	4	3	2	1	0
INSTRUCTION_52[7:0]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 198. Register INSTRUCTION_52_2 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_52[7:0]	R/W	00000000	

7.6.1.197 Register INSTRUCTION_53_0 (slave address: 0b100001x; register address: 0xDF; default: 0x00)

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Figure 223. Register INSTRUCTION_53_0 Format

7	6	5	4	3	2	1	0
INSTRUCTION_53[23:16]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 199. Register INSTRUCTION_53_0 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_53[23:16]	R/W	00000000	

7.6.1.198 Register INSTRUCTION_53_1 (slave address: 0b100001x; register address: 0xE0; default: 0x00)

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Figure 224. Register INSTRUCTION_53_1 Format

7	6	5	4	3	2	1	0
INSTRUCTION_53[15:8]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 200. Register INSTRUCTION_53_1 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_53[15:8]	R/W	00000000	

7.6.1.199 Register INSTRUCTION_53_2 (slave address: 0b100001x; register address: 0xE1; default: 0x00)

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Figure 225. Register INSTRUCTION_53_2 Format

7	6	5	4	3	2	1	0
INSTRUCTION_53[7:0]							
R/W							
OTP							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 201. Register INSTRUCTION_53_2 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	INSTRUCTION_53[7:0]	R/W	00000000	

7.6.1.200 Register PMICID (slave address: 0b100001x; register address: 0xF0; default: 0x65)

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Figure 226. Register PMICID Format

7	6	5	4	3	2	1	0
PMICID[7:0]							
R							
--							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 202. Register PMICID Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PMICID[7:0]	R	01100101	PMIC identification code

7.6.1.201 Register REVID (slave address: 0b100001x; register address: 0xF1; default: 0x01)

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Figure 227. Register REVID Format

7	6	5	4	3	2	1	0
MAJOR[3:0]				MINOR[3:0]			
R				R			
ROM				ROM			

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 203. Register REVID Field Descriptions

Bit	Field	Type	Reset	Description
7:4	MAJOR[3:0]	R	0000	Major die revision. **0000 : revision A, 0001 : revision B**
3:0	MINOR[3:0]	R	0001	Minor die revision. **0000 : revision 0, 0001 : revision 1, 0010 : revision 2**

7.6.1.202 Register NVM_COUNT1 (slave address: 0b100001x; register address: 0xF2; default: 0x00)

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Figure 228. Register NVM_COUNT1 Format

7	6	5	4	3	2	1	0
NVM_POINTER[7:0]							
R							
--							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 204. Register NVM_COUNT1 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	NVM_POINTER[7:0]	R	00000000	Number of bytes written to OTP memory during programming cycle 1.

7.6.1.203 Register NVM_COUNT2 (slave address: 0b100001x; register address: 0xF3; default: 0x00)

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Figure 229. Register NVM_COUNT2 Format

7	6	5	4	3	2	1	0
NVM_POINTER[7:0]							
R							
--							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 205. Register NVM_COUNT2 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	NVM_POINTER[7:0]	R	00000000	Number of bytes written to OTP memory during programming cycle 2.

7.6.1.204 Register NVM_COUNT3 (slave address: 0b100001x; register address: 0xF4; default: 0x00)

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Figure 230. Register NVM_COUNT3 Format

7	6	5	4	3	2	1	0
NVM_POINTER[7:0]							
R							
--							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 206. Register NVM_COUNT3 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	NVM_POINTER[7:0]	R	00000000	Number of bytes written to OTP memory during programming cycle 3.

7.6.1.205 Register NVM_COUNT4 (slave address: 0b100001x; register address: 0xF5; default: 0x00)

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Figure 231. Register NVM_COUNT4 Format

7	6	5	4	3	2	1	0
NVM_POINTER[7:0]							
R							
--							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 207. Register NVM_COUNT4 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	NVM_POINTER[7:0]	R	00000000	Number of bytes written to OTP memory during programming cycle 4.

7.6.1.206 Register NVM_COUNT5 (slave address: 0b100001x; register address: 0xF6; default: 0x00)

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Figure 232. Register NVM_COUNT5 Format

7	6	5	4	3	2	1	0
NVM_POINTER[7:0]							
R							
--							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 208. Register NVM_COUNT5 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	NVM_POINTER[7:0]	R	00000000	Number of bytes written to OTP memory during programming cycle 5.

7.6.1.207 Register NVM_COUNT6 (slave address: 0b100001x; register address: 0xF7; default: 0x00)

Back to *Register Map*.

Figure 233. Register NVM_COUNT6 Format

7	6	5	4	3	2	1	0
NVM_POINTER[7:0]							
R							
--							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 209. Register NVM_COUNT6 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	NVM_POINTER[7:0]	R	00000000	Number of bytes written to OTP memory during programming cycle 6.

7.6.1.208 Register NVM_COUNT7 (slave address: 0b100001x; register address: 0xF8; default: 0x00)

Back to *Register Map*.

Figure 234. Register NVM_COUNT7 Format

7	6	5	4	3	2	1	0
NVM_POINTER[7:0]							
R							
--							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 210. Register NVM_COUNT7 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	NVM_POINTER[7:0]	R	00000000	Number of bytes written to OTP memory during programming cycle 7.

7.6.1.209 Register NVM_COUNT8 (slave address: 0b100001x; register address: 0xF9; default: 0x00)

Back to *Register Map*.

Figure 235. Register NVM_COUNT8 Format

7	6	5	4	3	2	1	0
NVM_POINTER[7:0]							
R							
--							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 211. Register NVM_COUNT8 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	NVM_POINTER[7:0]	R	00000000	Number of bytes written to OTP memory during programming cycle 8.

7.6.1.210 Register NVM_COUNT9 (slave address: 0b100001x; register address: 0xFA; default: 0x00)

Back to *Register Map*.

Figure 236. Register NVM_COUNT9 Format

7	6	5	4	3	2	1	0
NVM_POINTER[7:0]							
R							
--							

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 212. Register NVM_COUNT9 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	NVM_POINTER[7:0]	R	00000000	Number of bytes written to OTP memory during programming cycle 9.

7.6.1.211 Register NVM_CONTROL (slave address: 0b100001x; register address: 0xFF; default: 0x00)

Back to *Register Map*.

Figure 237. Register NVM_CONTROL Format

7	6	5	4	3	2	1	0
NIL[5:0]						RELOAD	WRITE
R						R/W	R/W
--						--	--

LEGEND: R/W = Read/Write; R = Read only ; -- = No NVM option; ROM = Read Only Memory; OTP = One Time Programmable; EEPROM = EEPROM

Table 213. Register NVM_CONTROL Field Descriptions

Bit	Field	Type	Reset	Description
7:2	NIL[5:0]	R	000000	This bit is not implemented in hardware. During write operations data for this bit is ignored. During read operations 0 is returned.
1	RELOAD	R/W	0	Reload only USER settings
0	WRITE	R/W	0	Setting this bit copies the content of all user registers into NVM, thereby making them the default values at power-up.

8 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

Figure 238 shows a typical application circuit suitable for driving a GOA/GIP LCD panel. The circuit is designed to operate from a single-cell Li-ion battery or a regulated 3.3 V supply and requires V_{GH} and V_{GL1}/V_{GL2} from an external source. Table 214 shows the stuffing options for R060, R061 and R062.

Capacitor C1 is only needed if the OTP of the TPS65680 device is programmed in the application circuit. If the device is programmed before being soldered to the PCB, you do not need this capacitor.

8.2 Typical Application

Table 214. Stuffing Options for Different LCD Technologies

LCD technology	R060	R061	R062
Gate-Voltage Shaping	Depopulated	Populated	Populated
Charge Sharing	Populated	Depopulated	Depopulated

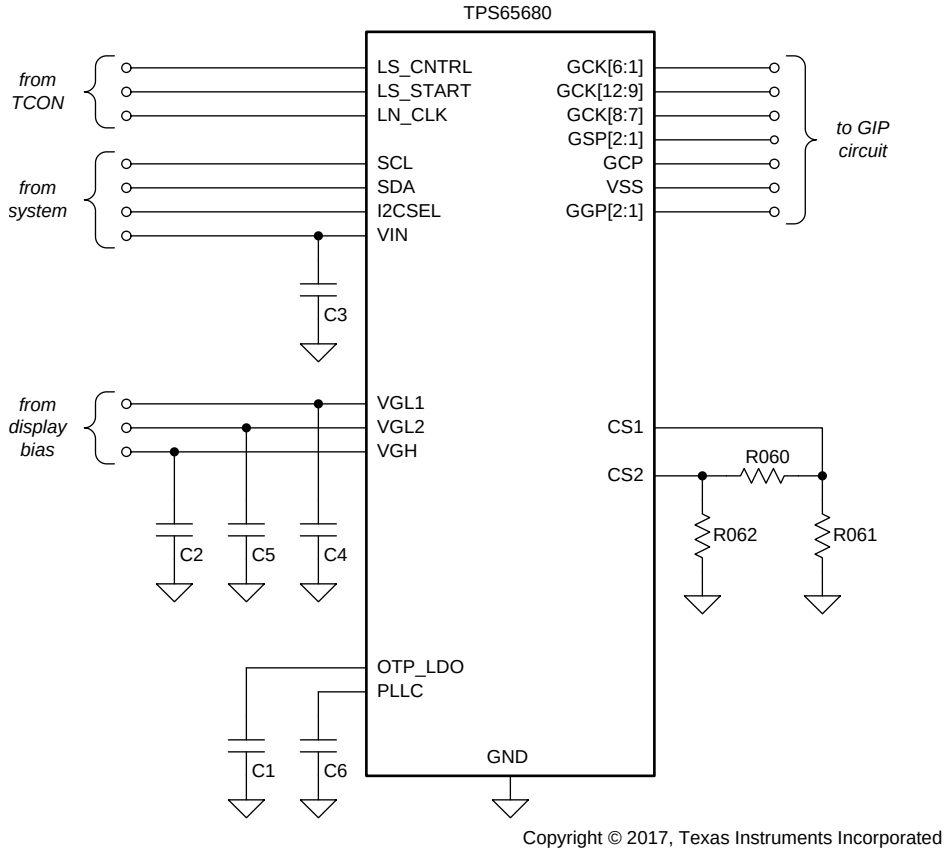


Figure 238. Application Schematic.

8.2.1 Design Requirements

The following parameters were used for the application schematic shown in Figure 238.

Table 215. Design Parameters

DESIGN PARAMETER	EXAMPLE
Input voltages	V_{IN} = 3.3 V
	V_{GH} = 14 V
	V_{GL1} = –15 V
	V_{GL2} = –15 V
Output loads	$C_{L, GCLKx}$ = 1 nF
	$C_{L, GSPx}$ = 470 pF
	$C_{L, GCPx}$ = 470 pF
	$C_{L, GGPx}$ = 470 pF
Charge sharing / gate voltage resistors	R060 = 1 kΩ

8.2.2 Detailed Design Procedure

To maximize performance, the TPS65680 device has been optimized for a relatively narrow range of component values, and customers are strongly recommended to use the application circuit shown in with the components listed in Table 216. If other components are used, customers are recommended to characterize performance fully to ensure proper operation.

Care should be applied to the choice of external components since they greatly affect overall performance. The TPS65680 was developed with the twin goals of high performance and small/low-profile solution size. Since these two goals are often in direct opposition to one another (e.g. larger capacitors tend to achieve higher effective capacitance values), some trade-off is always necessary.

Capacitors must provide adequate *effective* capacitance under the applicable dc bias conditions they experience in the application. MLCC capacitors typically exhibit only a fraction of their nominal capacitance under real-world conditions, and this must be taken into consideration when selecting them. This problem is especially acute in low profile capacitors, in which the dielectric field strength is higher than in taller components. In general, the capacitance values shown in circuit diagrams in this data sheet refer to the effective capacitance after dc bias effects have been taken into account. Reputable capacitor manufacturers provide capacitance versus dc bias curves that greatly simplify component selection.

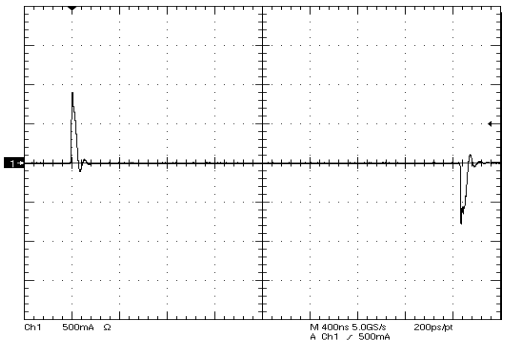
The following tables list some components suitable for use with the TPS65680. The list is not exhaustive – other components may exist that are equally suitable (or better), however, these components have been proven to work well and were used extensively during the development of the TPS65680.

Table 216. Recommended External Components

DESCRIPTION		PART NUMBER	MANUFACTURER(1)	SIZE (LxWxH)
VIN				
C3	(1×) 10 µF ±20% X5R, 10 V, 0402(2)	GRM155R61A106ME21	Murata	1.0 mm × 0.5 mm × 0.5 mm
VGH, VGL1, VGL2				
C2, C4, C5	(2×) 2.2 µF ±20% X5R, 35 V, 0402(2)	GRM155R6YA225ME11	Murata	1.0 mm × 0.5 mm × 0.5 mm
PLLC (optional)				
C6	(1×) 10 nF ±20% X5R, 10 V, 0402(2)	GCM155R71E103KA37D	Murata	1.0 mm × 0.5 mm × 0.5 mm
OTP_LDO (optional)				
C1	(1×) 2.2 µF ±20% X5R, 35 V, 0402(2)	GRM155R6YA225ME11	Murata	1.0 mm × 0.5 mm × 0.5 mm

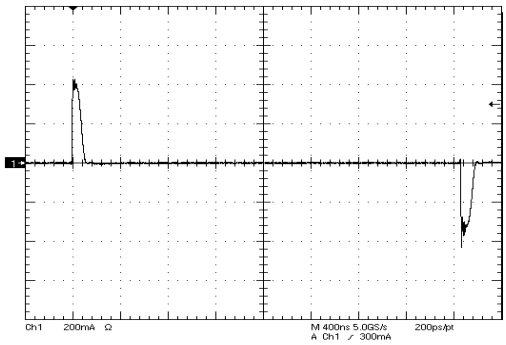
(1) See Third-party Products disclaimer.
(2) Component used for characterization.

8.2.3 Application Curves



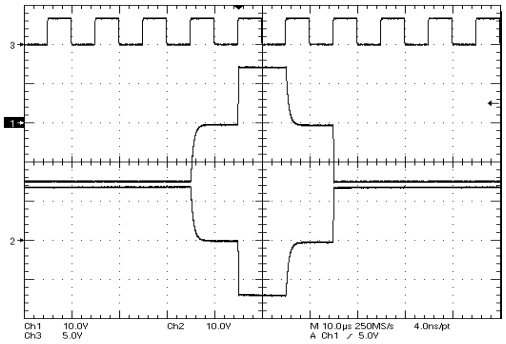
C_L = 1 nF V_{GH} = 14 V
V_{GL1} = –15 V
V_{GL2} = –15 V

Figure 239. Peak Output Current (GCKx)



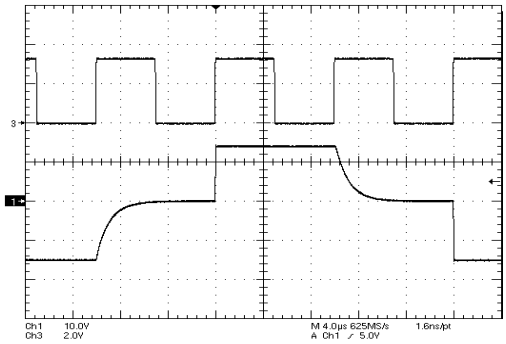
C_L = 1 nF V_{GH} = 14 V
V_{GL1} = –15 V
V_{GL2} = –15 V

Figure 240. Peak Output Current (GSPx,GGPx,GCP)



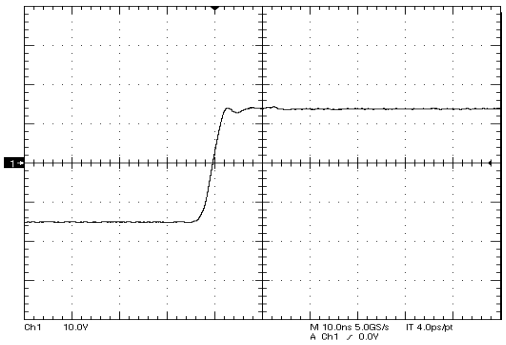
C_L = 1 nF V_{GH} = 14 V CH1 = GCK1
R_{CS} = 1 kΩ V_{GL1} = –15 V CH2 = GCK11
V_{GL2} = –15 V CH3 = LN_CLK

Figure 241. Charge-Sharing



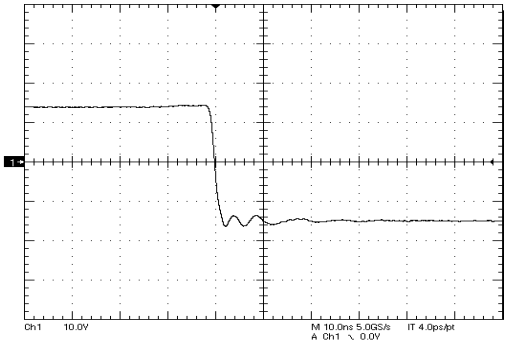
C_L = 1 nF V_{GH} = 14 V CH1 = GCK1
R_{GVS} = 1 kΩ V_{GL1} = –15 V CH3 = LN_CLK
V_{GL2} = –15 V

Figure 242. Gate-Voltage Shaping



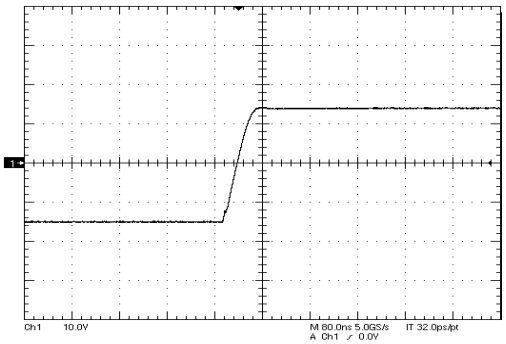
C_L = 8 pF V_{GH} = 14 V
V_{GL1} = –15 V
V_{GL2} = –15 V

Figure 243. Rise Time (GCKx)



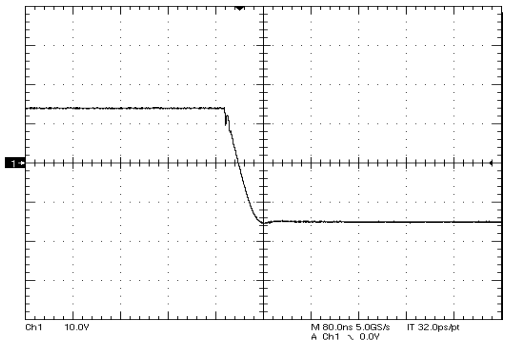
C_L = 8 pF V_{GH} = 14 V
V_{GL1} = –15 V
V_{GL2} = –15 V

Figure 244. Fall Time (GCKx)



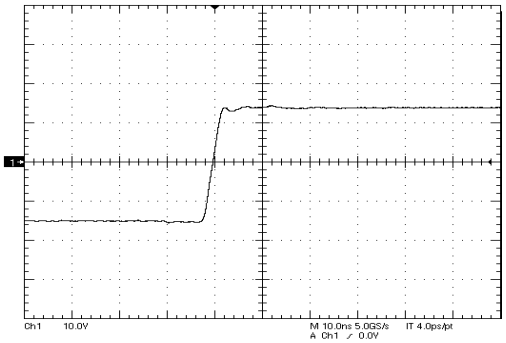
C_L = 1 nF
V_{GH} = 14 V
V_{GL1} = –15 V
V_{GL2} = –15 V

Figure 245. Rise Time (GCKx)



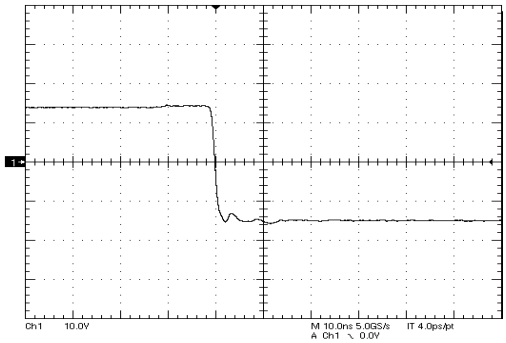
C_L = 1 nF
90% and 10%
V_{GH} = 14 V
V_{GL1} = –15 V
V_{GL2} = –15 V

Figure 246. Fall Time (GCKx)



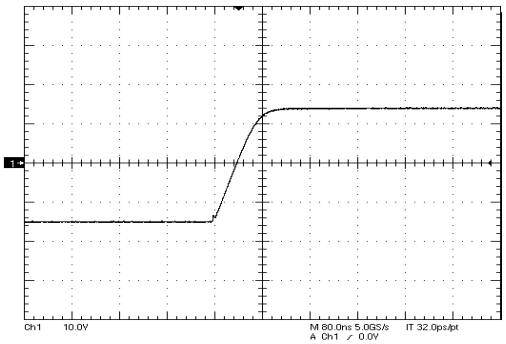
C_L = 8 pF
V_{GH} = 14 V
V_{GL1} = –15 V
V_{GL2} = –15 V

Figure 247. Rise Time (GSPx,GGPx,GCP)



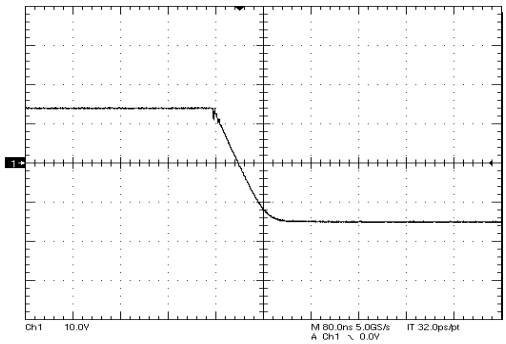
C_L = 8 pF
V_{GH} = 14 V
V_{GL1} = –15 V
V_{GL2} = –15 V

Figure 248. Fall Time (GSPx,GGPx,GCP)



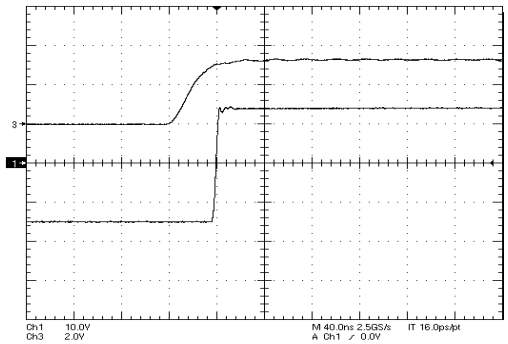
C_L = 1 nF
V_{GH} = 14 V
V_{GL1} = –15 V
V_{GL2} = –15 V

Figure 249. Rise Time (GSPx,GGPx,GCP)



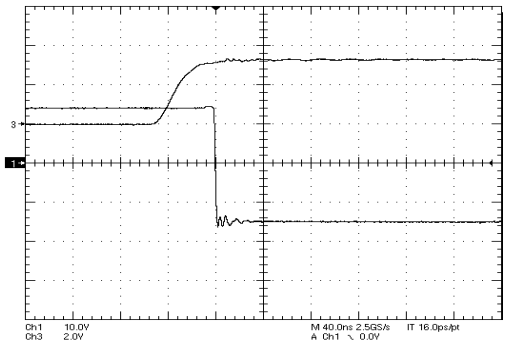
C_L = 1 nF
V_{GH} = 14 V
V_{GL1} = –15 V
V_{GL2} = –15 V

Figure 250. Fall Time (GSPx,GGPx,GCP)



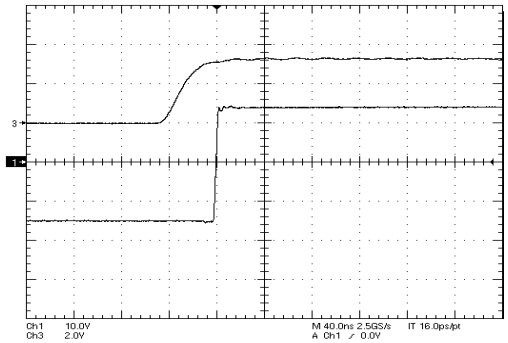
PLL bypassed
C_L = 8 pF
V_{GH} = 14 V
V_{GL1} = –15 V
V_{GL2} = –15 V
CH1 = GCK1
CH3 = LN_CLK

Figure 251. Propagation Delay t_{PLH} (GCKx)



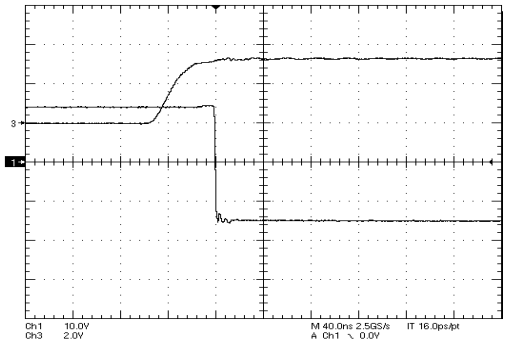
PLL bypassed
C_L = 8 pF
V_{GH} = 14 V
V_{GL1} = –15 V
V_{GL2} = –15 V
CH1 = GCK1
CH3 = LN_CLK

Figure 252. Propagation Delay t_{PHL} (GCKx)



PLL bypassed
C_L = 8 pF
V_{GH} = 14 V
V_{GL1} = –15 V
V_{GL2} = –15 V
CH1 = GGP2
CH3 = LN_CLK

Figure 253. Propagation Delay t_{PLH} (GSPx,GGPx,GCP)



PLL bypassed
C_L = 8 pF
V_{GH} = 14 V
V_{GL1} = –15 V
V_{GL2} = –15 V
CH1 = GGP2
CH3 = LN_CLK

Figure 254. Propagation Delay t_{PHL} (GSPx,GGPx,GCP)

9 Power Supply Recommendations

The device is designed to operate from an input supply (VIN) voltage ranging from 2.8 V to 5.5 V. This input supply may be the regulated output of another voltage regulator or the unregulated voltage of a Li-Ion battery. The AVDDP, AVDDN, VGH, VGL1, and VGL2 supplies are typically provided from another PMIC in the system such as the TPS65157 and the allowed input voltage ranges are shown in the *Recommended Operating Conditions* section. The input capacitance shown in the application schematic is suffcient for typical applications. If the input supply is located more than a few centimeters away from the device, additional bulk capacitance may be required in addition to the ceramic bypass capacitors.

10 Layout

10.1 Layout Guidelines

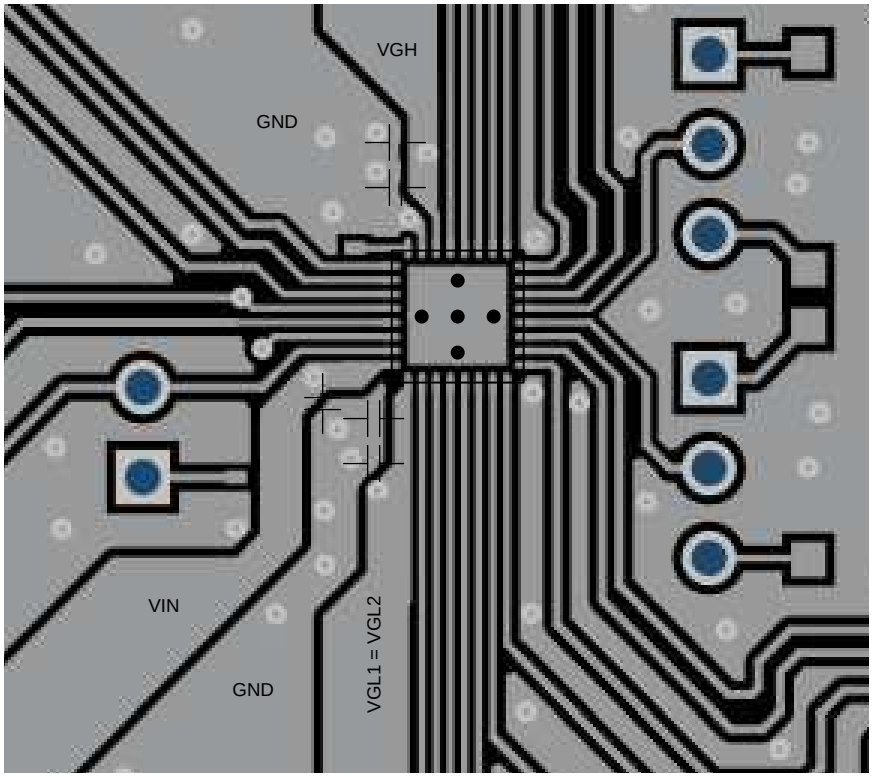
A good PCB layout is necessary for the TPS65680 device to achieve its specified performance.

The main PCB layout recommendations for the TPS65680 device are:

- Connect one or more decoupling capacitors between each power supply pin and ground. The power supply pins are VIN, VGH, VGL1 and VGL2 (VGH and VGL1 are the most important). Because VGL1 and VGL2 use the same supply voltage, these pins can share the same decoupling capacitors.
- We recommend an effective capacitance of at least 1 µF for each decoupling capacitor. Make sure you consider the DC bias effect – when a DC voltage is applied to a ceramic capacitor it has much less capacitance than its nominal value. Good capacitor manufacturers provide graphs showing the effective capacitance at different DC bias voltages.
- Connect the decoupling capacitors to the pins of the TPS65680 device with short, wide tracks on the top layer. Because vias have parasitic resistance and inductance, try not to use them to connect to the decoupling capacitors (this is not always possible, so just do your best).
- Include a ground plane on layer 2 beneath the TPS65680 device, its external components and output signals. This ground plane reduces the parasitic inductance of the PCB tracks on layer 1.
- Include a large copper plane on one of the internal layers and connect it to VGL2 with thermal vias. The package information at the end of this data sheet tells you the number and the size of the thermal vias we recommend. This copper plane is the primary path to conduct heat away from the TPS65680 device. If the area of this copper plane is too small, or if the number and size of the thermal vias is wrong, the TPS65680 device can get hot.

No PCB layout is perfect, and some trade-offs are usually required. Use the above list as a guideline and follow as many of the recommendations as you can. shows an extract from the PCB layout of the TPS65680 Evaluation Module. It illustrates how the above recommendations can be used (as far as possible) in a practical PCB design.

10.2 Layout Example



- Thermal via to copper pour on bottom or internal layer

Figure 255. Recommended PCB Layout.

11 Device and Documentation Support

11.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.2 Trademarks

All trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

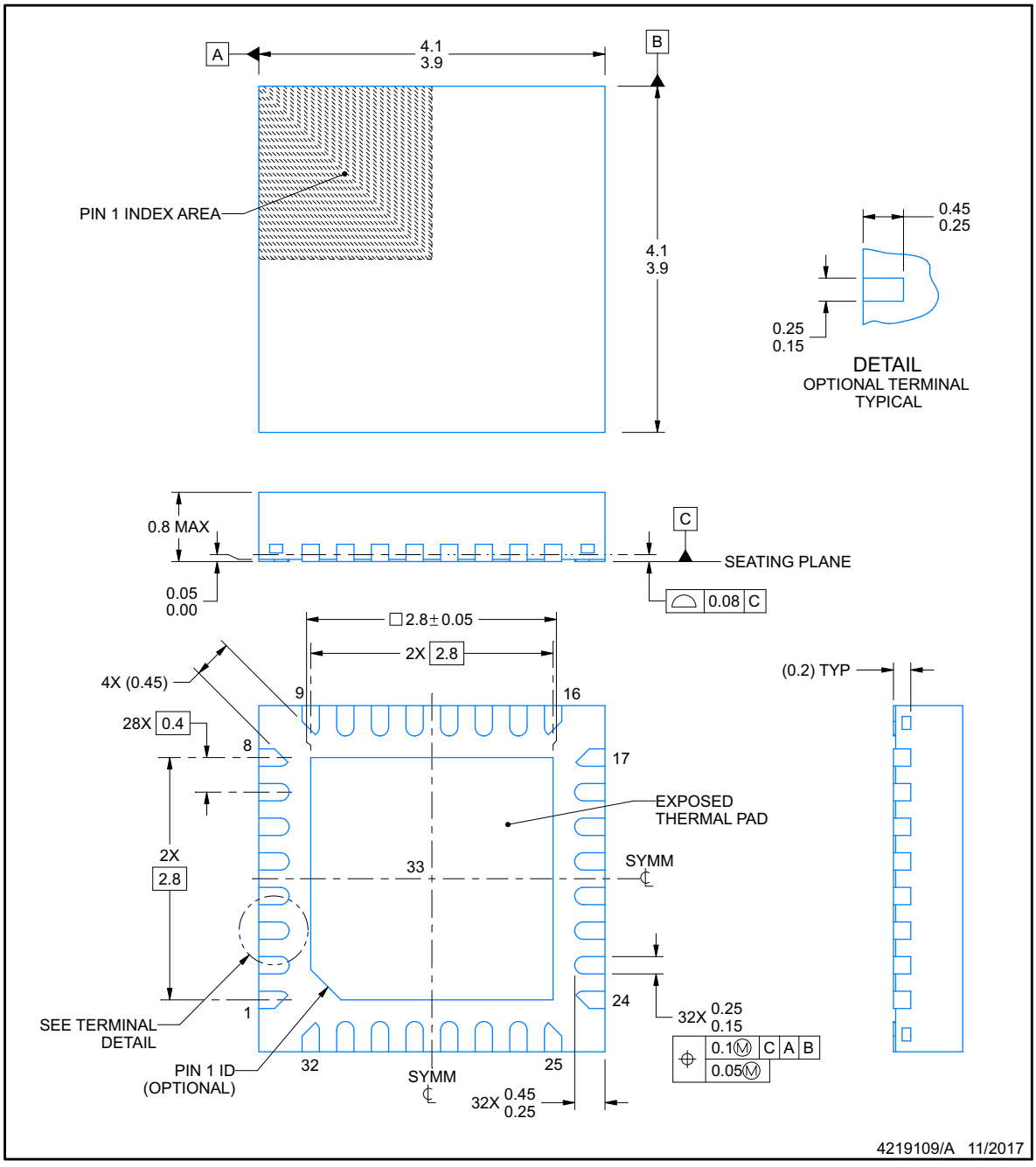
The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

RSN0032B

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

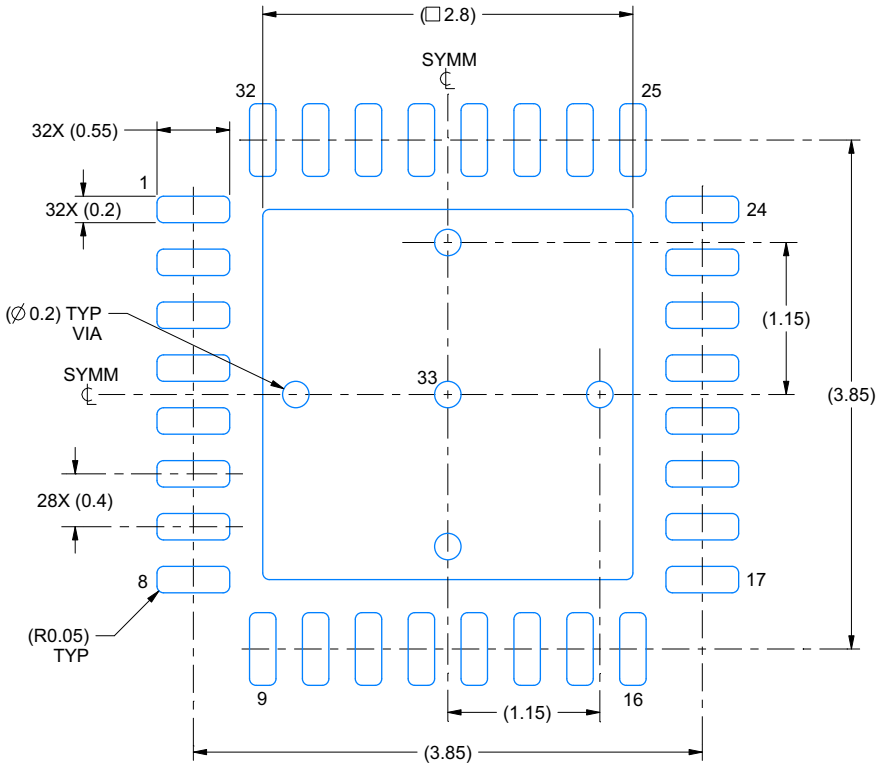
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

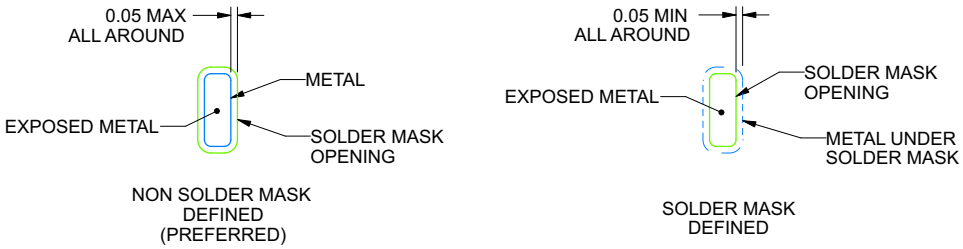
RSN0032B

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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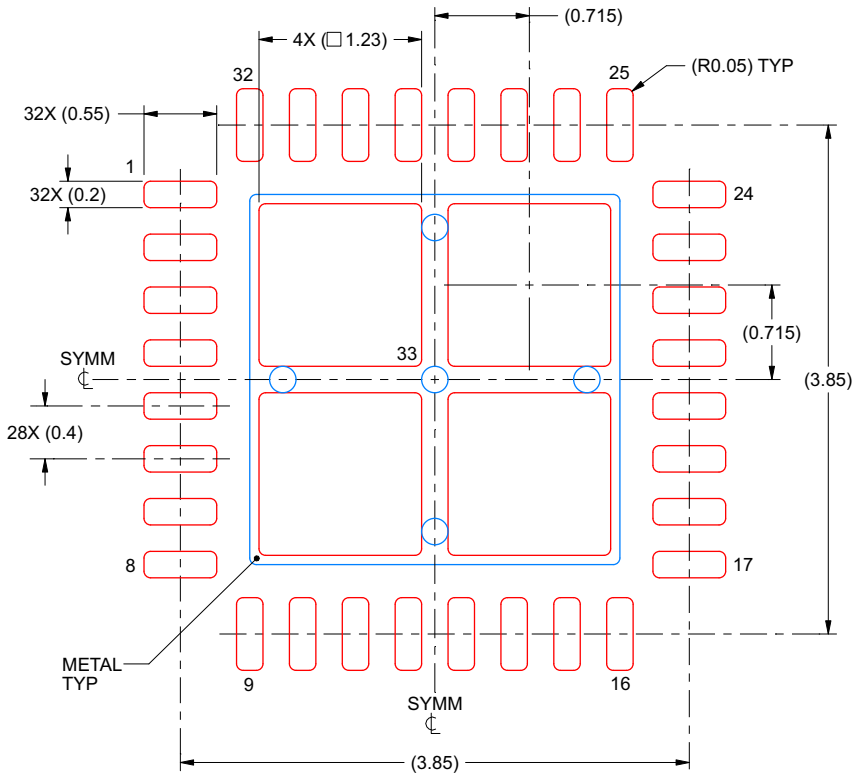
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RSN0032B — **WQFN - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 33:
77% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65680RSNR	ACTIVE	QFN	RSN	32	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS 65680	Samples
TPS65680RSNT	ACTIVE	QFN	RSN	32	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS 65680	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

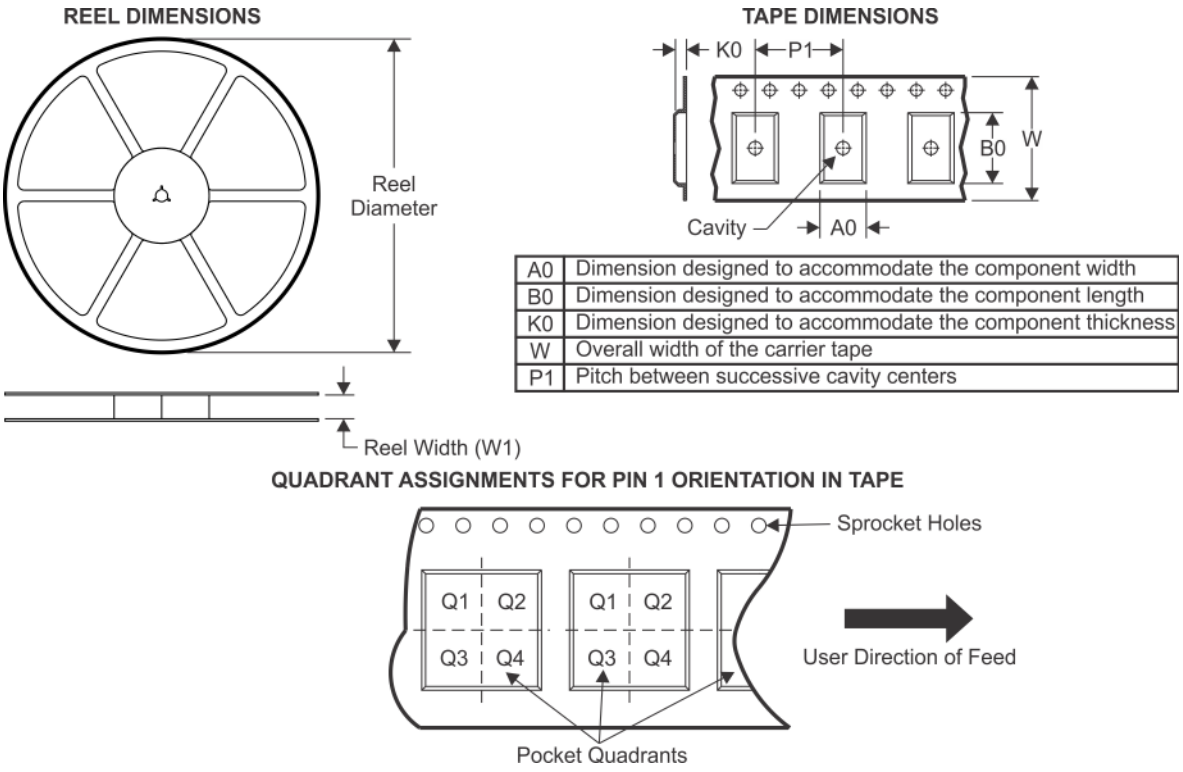
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

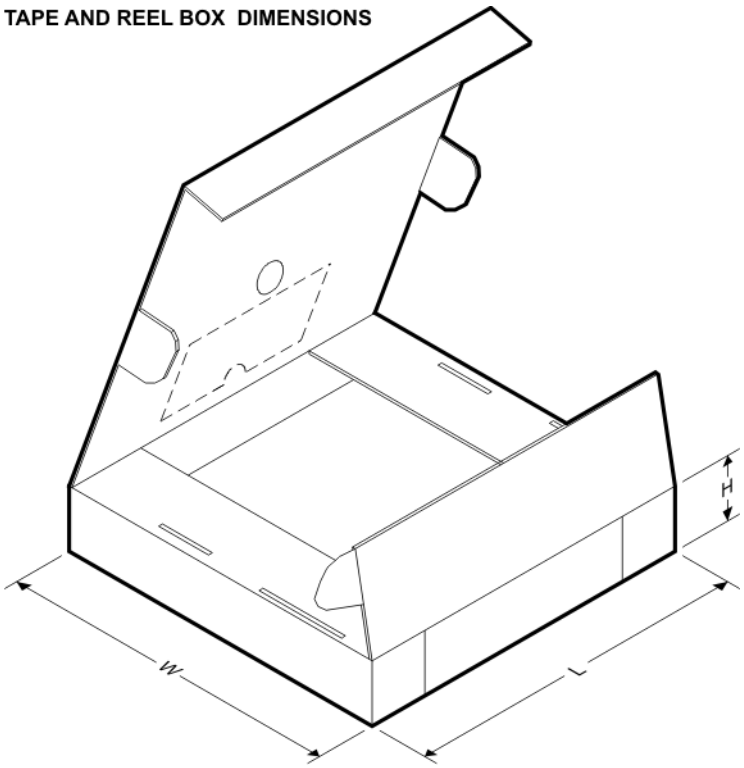


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65680RSNR	QFN	RSN	32	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS65680RSNT	QFN	RSN	32	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65680RSNR	QFN	RSN	32	3000	367.0	367.0	35.0
TPS65680RSNT	QFN	RSN	32	250	210.0	185.0	35.0

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