



# AirPrime HL7802

## Product Technical Specification



**SIERRA**  
WIRELESS®

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| 1.0     | October 03, 2019 | Creation                                         |
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# 1. Introduction

This document is the Product Technical Specification for the AirPrime HL7802 Embedded Module designed for M2M and Internet of Things (IoT) markets. It defines the high-level product features and illustrates the interfaces for these features. This document is intended to cover the hardware aspects of the product, including electrical and mechanical.

The AirPrime HL7802 module belongs to the AirPrime HL Series from Essential Connectivity Module family. These are industrial grade Embedded Wireless Modules that provides data connectivity on LTE and 2G (as listed in Table 1 Supported Bands/Connectivity).

The AirPrime HL7802 supports a large variety of interfaces such as USB FS, UART, ADC, GPIOs, and it also supports the new ultra-low power consumption hibernation modes to provide customers with the highest level of flexibility in implementing high-end solutions.

Table 1. Supported Bands/Connectivity

| RF Band   | Transmit Band (Tx) |            | Receive Band (Rx) |            | Cat-M1 | Cat-NB1 | 2G |
|-----------|--------------------|------------|-------------------|------------|--------|---------|----|
|           | Minimum            | Maximum    | Minimum           | Maximum    |        |         |    |
| LTE B1    | 1920 MHz           | 1980 MHz   | 2110 MHz          | 2170 MHz   | ✓      | ✓       |    |
| LTE B2    | 1850 MHz           | 1910 MHz   | 1930 MHz          | 1990 MHz   | ✓      | ✓       |    |
| LTE B3    | 1710 MHz           | 1785 MHz   | 1805 MHz          | 1880 MHz   | ✓      | ✓       |    |
| LTE B4    | 1710 MHz           | 1755 MHz   | 2110 MHz          | 2155 MHz   | ✓      | ✓       |    |
| LTE B5    | 824 MHz            | 849 MHz    | 869 MHz           | 894 MHz    | ✓      | ✓       |    |
| LTE B8    | 880 MHz            | 915 MHz    | 925 MHz           | 960 MHz    | ✓      | ✓       |    |
| LTE B9    | 1749.9 MHz         | 1784.9 MHz | 1844.9 MHz        | 1879.9 MHz | *      | *       |    |
| LTE B10   | 1710 MHz           | 1770 MHz   | 2110 MHz          | 2170 MHz   | *      | *       |    |
| LTE B12   | 699 MHz            | 716 MHz    | 729 MHz           | 746 MHz    | ✓      | ✓       |    |
| LTE B13   | 777 MHz            | 787 MHz    | 746 MHz           | 756 MHz    | ✓      | ✓       |    |
| LTE B14   | 788 MHz            | 798 MHz    | 758 MHz           | 768 MHz    | ✓      | ✓       |    |
| LTE B17   | 704 MHz            | 716 MHz    | 734 MHz           | 746 MHz    | *      | ✓       |    |
| LTE B18   | 815 MHz            | 830 MHz    | 860 MHz           | 875 MHz    | ✓      | ✓       |    |
| LTE B19   | 830 MHz            | 845 MHz    | 875 MHz           | 890 MHz    | ✓      | ✓       |    |
| LTE B20   | 832 MHz            | 862 MHz    | 791 MHz           | 821 MHz    | ✓      | ✓       |    |
| LTE B25   | 1850 MHz           | 1915 MHz   | 1930 MHz          | 1995 MHz   | ✓      | ✓       |    |
| LTE B26   | 814 MHz            | 849 MHz    | 859 MHz           | 894 MHz    | ✓      | ✓       |    |
| LTE B27   | 807 MHz            | 824 MHz    | 852 MHz           | 869 MHz    | ✓      | *       |    |
| LTE B28   | 703 MHz            | 748 MHz    | 758 MHz           | 803 MHz    | ✓      | ✓       |    |
| LTE B66   | 1710 MHz           | 1780 MHz   | 2110 MHz          | 2200 MHz   | ✓      | ✓       |    |
| GSM 850   | 824 MHz            | 849 MHz    | 869 MHz           | 894 MHz    |        |         | ✓  |
| E-GSM 900 | 880 MHz            | 915 MHz    | 925 MHz           | 960 MHz    |        |         | ✓  |
| DCS 1800  | 1710 MHz           | 1785 MHz   | 1805 MHz          | 1880 MHz   |        |         | ✓  |
| PCS 1900  | 1850 MHz           | 1910 MHz   | 1930 MHz          | 1990 MHz   |        |         | ✓  |

\* Will be supported in a future release.

*Note: RF bands supported are configurable through AT command. The software-based radio allows for the ability to support extra bands for worldwide connectivity.*

## 1.1. Common Flexible Form Factor (CF<sup>3</sup>)

The AirPrime HL7802 belongs to the Common Flexible Form Factor (CF<sup>3</sup>) family of modules. This family consists of a series of WWAN modules that share the same mechanical dimensions (same width and length with varying thicknesses) and footprint. The CF<sup>3</sup> form factor provides a unique solution to a series of problems faced commonly in the WWAN module space as it:

- Accommodates multiple radio technologies (LTE advanced) and band groupings.
- Supports bit-pipe (Essential Module Series) and value add (Smart Module Series) solutions.
- Offers electrical and functional compatibility.
- Provides Direct Mount as well as Socket-ability depending on customer needs.

## 1.2. Physical Dimensions

AirPrime HL7802 modules are compact, robust, fully shielded modules with the following dimensions:

- Length: 18.0 mm
- Width: 15.0 mm
- Thickness: 2.4 mm
- Weight: 1.17 g

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*Note: Dimensions specified above are typical values.*

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## 1.3. General Features

The table below summarizes the AirPrime HL7802's features.

Table 2. General Features

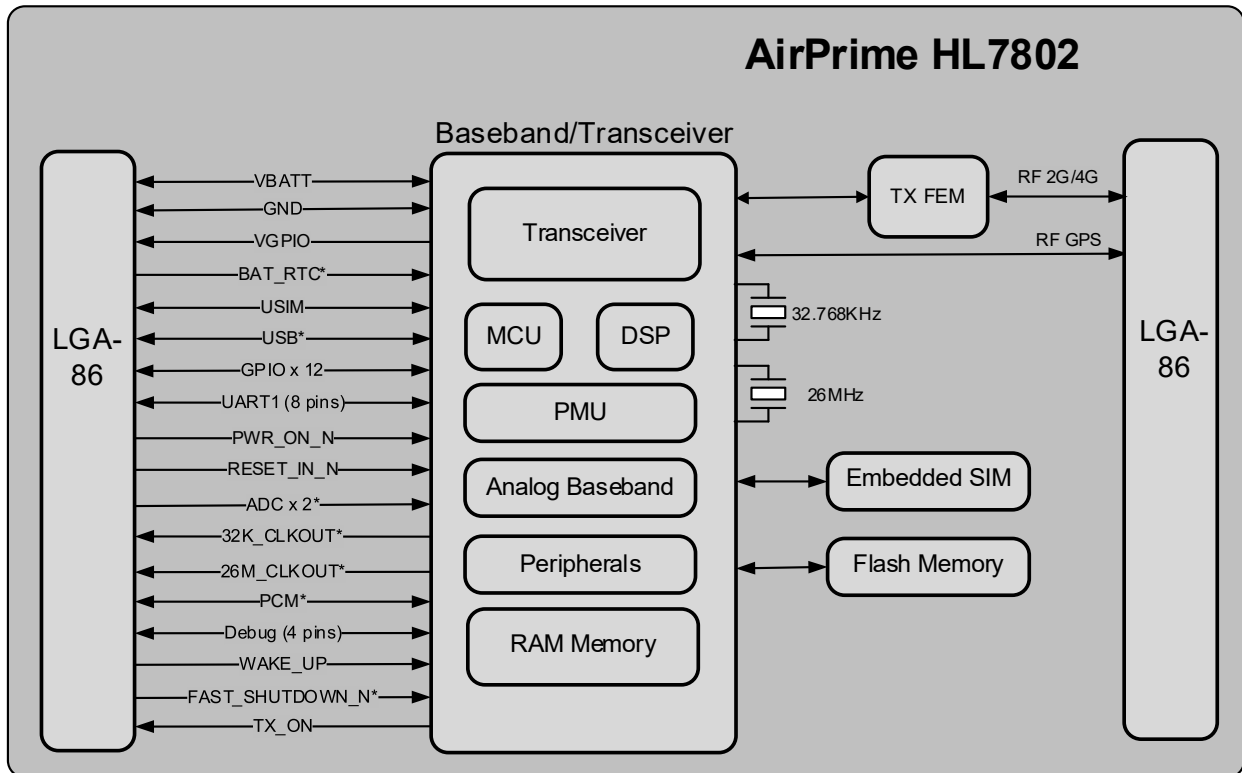
| Feature      | Description                                                                                                                                                                                                                                                 |
|--------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Physical     | <ul style="list-style-type: none"> <li>• Small form factor (86-pad solderable LGA pad) – 15.0mm x 18.0mm x 2.4mm (nominal)</li> <li>• Metal shield can</li> <li>• RF connection pads (RF main and RF GPS)</li> <li>• Baseband signals connection</li> </ul> |
| Power supply | Single or double supply voltage (VBATT and VBATT_PA) – 3.2V – 4.35V                                                                                                                                                                                         |

| Feature               | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|-----------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| RF                    | <ul style="list-style-type: none"> <li>• 2G <ul style="list-style-type: none"> <li>▪ 850/900 Power Class 4 (33 dBm), GPRS</li> <li>▪ 1800/1900 Power Class 1 (30 dBm), GPRS</li> </ul> </li> <li>• Cat-M1 <ul style="list-style-type: none"> <li>▪ Power Class 3 (23dBm)</li> <li>▪ Software based radio allowing support of extra bands for worldwide operation (will be supported in a future release)</li> </ul> </li> <li>• Cat-NB1 <ul style="list-style-type: none"> <li>▪ Power Class 3 (23dBm)</li> <li>▪ Software based radio allowing support of extra bands for worldwide operation (will be supported in a future release)</li> </ul> </li> <li>• GPS <ul style="list-style-type: none"> <li>▪ 1575.42 MHz</li> </ul> </li> </ul> <hr/> <p><i>Note: The GPS receiver shares the same RF resources as the 4G receiver. The end-device target should allow GPS positioning for asset management applications where infrequent and no real-time position updates are required.</i></p> <hr/> |
| SIM interface         | <ul style="list-style-type: none"> <li>• 1.8V only support (legacy 3V SIM is not supported; this should not have any impact on design)</li> <li>• SIM extraction / hot plug detection</li> <li>• SIM/USIM support</li> <li>• Conforms with ETSI UICC Specifications.</li> <li>• Supports SIM application tool kit with proactive SIM commands</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| Application interface | <ul style="list-style-type: none"> <li>• AT command interface – 3GPP 27.007 standard, plus proprietary extended AT commands</li> <li>• CMUX multiplexing over UART</li> <li>• USB Full Speed</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |

| Feature        | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Protocol stack | <ul style="list-style-type: none"> <li>• 2G <ul style="list-style-type: none"> <li>▪ GPRS Class 10</li> </ul> </li> <li>• Cat-M1 <ul style="list-style-type: none"> <li>▪ 3GPP Rel. 13</li> <li>▪ Half-duplex</li> <li>▪ Channel bandwidth 1.4MHz</li> <li>▪ LTE carrier bandwidth 1.4 / 3 / 5 / 10 / 15 / 20 MHz</li> <li>▪ Up to 375kbit/s uplink, 300 kbit/s downlink</li> <li>▪ Extended Coverage Mode A</li> <li>▪ PSM (Power Save Mode)</li> <li>▪ I-DRX (Idle Mode Discontinuous Reception)</li> <li>▪ C-DRX (Connected Mode Discontinuous Reception)</li> <li>▪ Idle mode mobility</li> <li>▪ Connected mode mobility</li> <li>▪ eDRX (Extended Discontinuous Reception)</li> <li>▪ CiOT optimizations (U-Plane, C-Plan)</li> </ul> </li> <li>• Cat-NB1 <ul style="list-style-type: none"> <li>▪ 3GPP Rel. 13</li> <li>▪ Half-duplex</li> <li>▪ Channel bandwidth 180KHz</li> <li>▪ LTE carrier bandwidth 1.4 / 3 / 5 / 10 / 15 / 20 MHz</li> <li>▪ Up to 100 kbit/s in downlink</li> <li>▪ Operational mode – Inband, Guard band, Standalone</li> <li>▪ CiOT EPS optimizations (Data over NAS)</li> <li>▪ NIDD over SGI tunneling</li> <li>▪ NIDD over SCEF</li> <li>▪ Extended coverage</li> </ul> </li> </ul> |
| Protocol stack | <ul style="list-style-type: none"> <li>• Flexible selection <ul style="list-style-type: none"> <li>▪ Manual system selection across RATs</li> <li>▪ Dynamic system selection across RATs (preferred RAT)</li> </ul> </li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| SMS            | <ul style="list-style-type: none"> <li>• SMS over SG</li> <li>• MO/MT</li> <li>• SMS storage to SIM card or ME storage</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| Connectivity   | <ul style="list-style-type: none"> <li>• Multiple cellular packet data profiles</li> <li>• Sleep mode for minimum idle power draw</li> <li>• Mobile-originated PDP context activation / deactivation</li> <li>• Static and Dynamic IP address. The network may assign a fixed IP address or dynamically assign one using DHCP (Dynamic Host Configuration Protocol).</li> <li>• PDP context type (IPv4, IPv6, IPv4v6). IP Packet Data Protocol context</li> <li>• RFC1144 TCP/IP header compression</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| Environmental  | <p>Operating temperature ranges (industrial grade):</p> <ul style="list-style-type: none"> <li>• Class A: -30°C to +70°C</li> <li>• Class B: -40°C to +85°C</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| RTC            | Real Time Clock (RTC)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |

## 1.4. Architecture

The figure below presents an overview of the AirPrime HL7802's internal architecture and external interfaces.



\* Will be available in a future release

Figure 1. Architecture Overview

## 1.5. Interfaces

The AirPrime HL7802 provides the following interfaces and peripheral connectivity:

- 1x – VGPIO (1.8V)
- 1x – BAT\_RTC backup battery interface (will be available in a future firmware release)
- 1x – 1.8V USIM
- 1x – USB FS (will be available in a future firmware release)
- 12x – GPIOs
- 1x – 8-wire UART
- 1x – Active Low POWER ON (will be available in a future firmware release)
- 1x – Active Low RESET
- 2x – ADC (will be available in a future firmware release)
- 2x – System clock out (32.768 KHz and 26 MHz) (will be available in a future release)
- 1x – PCM (will be available in a future firmware release)
- 1x – 4-wire UART for debug interface only
- 1x – Wake up signal

- 1x – Fast shutdown signal (will be available in a future firmware release)
- 1x – Main RF Antenna
- 1x – TX indicator
- 1x – GPS Antenna

## 1.6. Connection Interface

AirPrime HL7802 modules are LGA form factor devices. All electrical and mechanical connections are made through the 86 Land Grid Array (LGA) pads on the bottom side of the PCB.

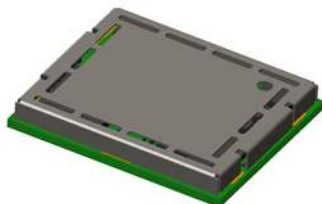


Figure 2. Mechanical Overview (Top View)

The 86 pads have the following distribution:

- 66 inner signal pads, 1x0.5mm, pitch 0.8mm
- 16 inner ground pads, 1.0x1.0mm, pitch 1.825mm/1.475mm
- 4 outer corner ground pads, 0.85x0.97mm

## 1.7. ESD Specifications

- IEC-61000-4-2 (test carried out on test vehicle including ESD protection)
  - Contact Voltage:  $\pm 2\text{kV}$ ,  $\pm 4\text{kV}$ ,  $\pm 6\text{kV}$
  - GPS pad C38:  $\pm 500\text{V}$
  - Air Voltage:  $\pm 2\text{kV}$ ,  $\pm 4\text{kV}$ ,  $\pm 8\text{kV}$
- JESD22-A114  $\pm 250\text{V}$  Human Body Model
- JESD22-C101C  $\pm 250\text{V}$  Charged Device Model

## 1.8. Environmental and Certifications

### 1.8.1. Environmental Specifications

The environmental specification for both operating and storage conditions are defined in the table below.

Table 3. Environmental Specifications

| Conditions        | Range                                          |
|-------------------|------------------------------------------------|
| Operating Class A | $-30^{\circ}\text{C}$ to $+70^{\circ}\text{C}$ |

| Conditions        | Range          |
|-------------------|----------------|
| Operating Class B | -40°C to +85°C |
| Storage           | -40°C to +85°C |

Class A is defined as the operating temperature ranges that the device:

- Shall exhibit normal function during and after environmental exposure.
- Shall meet the minimum requirements of 3GPP or appropriate wireless standards.

Class B is defined as the operating temperature ranges that the device:

- Shall remain fully functional during and after environmental exposure
- Shall exhibit the ability to establish an SMS or DATA call (emergency call) at all times even when one or more environmental constraint exceeds the specified tolerance.
- Unless otherwise stated, full performance should return to normal after the excessive constraint(s) have been removed.

## 1.8.2. Frequency Drift Correction

The HL7802 are environment-sensitive like any electronic device, but able to correct temperature and aging effects automatically. Parameters to be considered when addressing the environmental effect on the HL7802 are as follows:

- Maximum deviation correction: 20 ppm
- Environmental Temperature effect: 0.5 ppm
- Factory reflow effect: 1 ppm + 1 ppm / reflow
- Aging effect: 1 ppm / year of use

For example, if an HL7802 module is mounted on a single side (1 reflow) customer PCB and used for 10 years between -40 and +85°C, the frequency drift will be up to  $0.5 + (1 + 1) + (1 * 10) = 12.5$  ppm, which is in the limits of the 20 ppm maximum correction.

## 1.8.3. ATEX Compliance

The following table lists the inductor and capacitor values to be considered for ATEX certification of the system hosting the HL7802 modules. All supplies in the modules are linear LDO except for one 1.3V DC/DC step-down.

Table 4. Values for ATEX Compliance

| Parameter         | Value        | Tolerance |
|-------------------|--------------|-----------|
| Total Inductance  | 2.21 $\mu$ H | 30%       |
| Total Capacitance | 58 $\mu$ F   | 20%       |



## 1.8.4. Regulatory

The AirPrime HL7802 will be compliant with the following regulations:

- RED
- FCC
- IC
- RCM

## 1.8.5. RoHS Directive Compliance

AirPrime HL7802 modules are compliant with RoHS Directive 2011/65/EU, including directive 2015/863 amending annex II, which sets limits for the use of certain restricted hazardous substances. This directive states that electrical and electronic equipment put on the market does not contain lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB), polybrominated diphenyl ethers (PBDE), Bis (2-ethylhexyl) phthalate (DEHP), Butyl benzyl phthalate (BBP), Dibutyl phthalate (DBP) or Di-isobutyl phthalate (DIBP) above threshold limits.

## 1.8.6. Disposing of the Product

This electronic product is subject to the EU Directive 2012/19/EU for Waste Electrical and Electronic Equipment (WEEE). As such, this product must not be disposed of at a municipal waste collection point. Please refer to local regulations for directions on how to dispose of this product in an environmentally friendly manner.



## 1.9. References

- [1] AirPrime HL78xx Customer Process Guidelines  
Reference Number: 41112095
- [2] AirPrime HL78xx AT Commands Interface Guide  
Reference Number: 41111821
- [3] AirPrime HL Series Development Kit User Guide  
Reference Number: 4114877
- [4] AirPrime HL7800 Low Power Modes Application Note  
Reference Number: 2174229
- [5] AirPrime HL7800-M MNO and RF Band Customization at Customer Production Site  
Application Note  
Reference Number: 2174213

## 2. Pad Definition

AirPrime HL7802 pins are divided into 2 functional categories.

- **Core functions and associated pins** cover all the mandatory features for M2M connectivity and will be available by default across all CF<sup>3</sup> family of modules. These Core functions are always available and always at the same physical pad locations. A customer platform using only these functions and associated pads are guaranteed to be forward and/or backward compatible with the next generation of CF<sup>3</sup> modules.
- **Extension functions and associated pins** bring additional capabilities to the customer. Whenever an Extension function is available on a module, it is always at the same pad location.

Other pins marked as “not connected” or “reserved” should not be used.

Table 5. Pin Definition

| Pad # | Signal Name | Function                       | I/O | Pre and Post Reset State* | Power Supply Domain | Recommendation for Unused Pads | Type      |
|-------|-------------|--------------------------------|-----|---------------------------|---------------------|--------------------------------|-----------|
| C1    | GPIO1       | General purpose input/output   | I/O | PU                        | 1.8V (VGPIO)        | Left open                      | Extension |
| C2    | UART1_RI    | UART1 Ring indicator           | O   | PU**                      | 1.8V (VGPIO)        | Connect to test point          | Core      |
| C3    | UART1_RTS   | UART1 Request to send          | I   | PU                        | 1.8V (VGPIO)        | Connect to test point          | Core      |
| C4    | UART1_CTS   | UART1 Clear to send            | O   | PU                        | 1.8V (VGPIO)        | Connect to test point          | Core      |
| C5    | UART1_TX    | UART1 Transmit data            | I   | PU                        | 1.8V (VGPIO)        | Connect to test point          | Core      |
| C6    | UART1_RX    | UART1 Receive data             | O   | PU                        | 1.8V (VGPIO)        | Connect to test point          | Core      |
| C7    | UART1_DTR   | UART1 Data terminal ready      | I   | PU                        | 1.8V (VGPIO)        | Connect to test point          | Core      |
| C8    | UART1_DCD   | UART1 Data carrier detect      | O   | PU                        | 1.8V (VGPIO)        | Connect to test point          | Core      |
| C9    | UART1_DSR   | UART1 Data set ready           | O   | PU                        | 1.8V (VGPIO)        | Connect to test point          | Core      |
| C10   | GPIO2       | General purpose input/output   | I/O | PD**                      | 1.8V (VGPIO)        | Connect to test point          | Core      |
| C11   | RESET_IN_N  | Input reset signal             | I   |                           | 1.8V                | Left open                      | Core      |
| C12   | USB_D-      | USB Data Negative (Full Speed) | I/O |                           | 3.3V                | Connect to test point          | Extension |
| C13   | USB_D+      | USB Data Positive (Full Speed) | I/O |                           | 3.3V                | Connect to test point          | Extension |

| Pad # | Signal Name | Function                      | I/O | Pre and Post Reset State* | Power Supply Domain | Recommendation for Unused Pads              | Type          |
|-------|-------------|-------------------------------|-----|---------------------------|---------------------|---------------------------------------------|---------------|
| C14   | NC          | Not Connected                 |     |                           |                     | Left open                                   | Not connected |
| C15   | NC          | Not Connected                 |     |                           |                     | Left open                                   | Not connected |
| C16   | USB_VBUS    | USB VBUS                      | I   |                           | 5V                  | Mandatory connection if USB is used         | Extension     |
| C17   | NC          | Not Connected                 |     |                           |                     | Left open                                   | Not connected |
| C18   | NC          | Not Connected                 |     |                           |                     | Left open                                   | Not connected |
| C19   | NC          | Not Connected                 |     |                           |                     | Left open                                   | Not Connected |
| C20   | NC          | Not Connected                 |     |                           |                     | Left open                                   | Not Connected |
| C21   | BAT_RTC     | Power supply for RTC backup   | I   |                           |                     | Left open                                   | Extension     |
| C22   | 26M_CLKOUT  | 26M System Clock Output       | O   | PD                        | 1.8V (VGPIO)        | Left open                                   | Extension     |
| C23   | 32K_CLKOUT  | 32.768kHz System Clock Output | O   | PU                        | 1.8V (VGPIO)        | Left open                                   | Extension     |
| C24   | ADC1        | Analog to digital converter   | I   |                           | 1.8V                | Left open                                   | Extension     |
| C25   | ADC0        | Analog to digital converter   | I   |                           | 1.8V                | Left open                                   | Extension     |
| C26   | UIM1_VCC    | 1.8V USIM1 Power supply       | O   |                           | 1.8V (VGPIO)        | Mandatory connection                        | Core          |
| C27   | UIM1_CLK    | 1.8V USIM1 Clock              | O   |                           | 1.8V (VGPIO)        | Mandatory connection                        | Core          |
| C28   | UIM1_DATA   | 1.8V USIM1 Data               | I/O |                           | 1.8V (VGPIO)        | Mandatory connection                        | Core          |
| C29   | UIM1_RESET  | 1.8V USIM1 Reset              | O   |                           | 1.8V (VGPIO)        | Mandatory connection                        | Core          |
| C30   | GND         | Ground                        | 0V  |                           | 0V                  | Recommended connection but can be left open | Extension     |
| C31   | NC          | Not Connected                 |     |                           |                     |                                             | Not connected |
| C32   | GND         | Ground                        | 0V  |                           | 0V                  | Recommended connection but can be left open | Extension     |
| C33   | PCM_OUT     | PCM data out                  | O   | PU                        | 1.8V (VGPIO)        | Left open                                   | Extension     |
| C34   | PCM_IN      | PCM data in                   | I   | PU                        | 1.8V (VGPIO)        | Left open                                   | Extension     |
| C35   | PCM_SYNC    | PCM sync out                  | I/O | PU                        | 1.8V (VGPIO)        | Left open                                   | Extension     |
| C36   | PCM_CLK     | PCM clock                     | I/O | PD                        | 1.8V (VGPIO)        | Left open                                   | Extension     |

| Pad # | Signal Name         | Function                                                   | I/O | Pre and Post Reset State* | Power Supply Domain | Recommendation for Unused Pads | Type          |
|-------|---------------------|------------------------------------------------------------|-----|---------------------------|---------------------|--------------------------------|---------------|
| C37   | GND                 | Ground                                                     | 0V  |                           | 0V                  | Mandatory connection           | Core          |
| C38   | RF_GPS              | RF_GPS                                                     |     |                           |                     | Left open                      | Core          |
| C39   | GND                 | Ground                                                     | 0V  |                           | 0V                  | Mandatory connection           | Core          |
| C40   | GPIO7               | General purpose input/output                               | I/O | PU                        | 1.8V (VGPIO)        | Left open                      | Core          |
| C41   | GPIO8 / VBATT_PA_EN | General purpose input/output / External RF voltage control | I/O | PD                        | 1.8V (VGPIO)        | Left open                      | Core          |
| C42   | NC                  | Not Connected                                              |     |                           |                     |                                | Not connected |
| C43   | EXT_LNA_GPS_EN      | External GPS LNA enable                                    |     | PU                        |                     | Left open                      | Extension     |
| C44   | WAKE_UP             | Wake up signal                                             | I   | PD                        | 1.8V                | Mandatory connection           | Extension     |
| C45   | VGPIO               | GPIO voltage output                                        | O   |                           | 1.8V (VGPIO)        | Left open                      | Core          |
| C46   | GPIO6               | General purpose input/output                               | I/O | PD                        | 1.8V (VGPIO)        | Left open                      | Core          |
| C47   | NC                  | Not Connected                                              |     |                           |                     | Left open                      | Not connected |
| C48   | GND                 | Ground                                                     | 0V  |                           | 0V                  | Mandatory connection           | Core          |
| C49   | RF_MAIN             | RF Input/output                                            |     |                           |                     | Mandatory connection           | Core          |
| C50   | GND                 | Ground                                                     | 0V  |                           | 0V                  | Mandatory connection           | Core          |
| C51   | GPIO14              | General purpose input/output                               | I/O | PU                        | 1.8V (VGPIO)        | Connect to test point          | Extension     |
| C52   | GPIO10              | General purpose input/output                               | I/O | PU                        | 1.8V (VGPIO)        | Connect to test point          | Extension     |
| C53   | GPIO11              | General purpose input/output                               | I/O | PU                        | 1.8V (VGPIO)        | Connect to test point          | Extension     |
| C54   | GPIO15              | General purpose input/output                               | I/O | PU                        | 1.8V (VGPIO)        | Connect to test point          | Extension     |
| C55   | UART0_RX            | Debug Receive data                                         | O   | PU                        | 1.8V (VGPIO)        | Mandatory connection           | Extension     |
| C56   | UART0_TX            | Debug Transmit data                                        | I   | PU                        | 1.8V (VGPIO)        | Mandatory connection           | Extension     |
| C57   | UART0_CTS           | Debug Clear to Send                                        | O   | PU                        | 1.8V (VGPIO)        | Mandatory connection           | Extension     |
| C58   | UART0_RTS           | Debug Request to Send                                      | I   | PD                        | 1.8V (VGPIO)        | Mandatory connection           | Extension     |
| C59   | PWR_ON_N            | Active Low Power On control signal                         | I   |                           | 1.8V                | Mandatory connection           | Core          |
| C60   | TX_ON               | TX transmission indication                                 | O   | PU                        | 1.8V (VGPIO)        | Left open                      | Extension     |

| Pad #                  | Signal Name             | Function                                                              | I/O | Pre and Post Reset State* | Power Supply Domain                     | Recommendation for Unused Pads | Type      |
|------------------------|-------------------------|-----------------------------------------------------------------------|-----|---------------------------|-----------------------------------------|--------------------------------|-----------|
| C61                    | VBATT_PA                | Power supply (refer to section 3.1 Power Supply for more information) | I   |                           | 3.2V (min)<br>3.7V (typ)<br>4.35V (max) | Mandatory connection           | Core      |
| C62                    | VBATT_PA                | Power supply (refer to section 3.1 Power Supply for more information) | I   |                           | 3.2V (min)<br>3.7V (typ)<br>4.35V (max) | Mandatory connection           | Core      |
| C63                    | VBATT                   | Power supply (refer to section 3.1 Power Supply for more information) | I   |                           | 3.2V (min)<br>3.7V (typ)<br>4.35V (max) | Mandatory connection           | Core      |
| C64                    | UIM1_DET / GPIO3        | USIM1 Detection / General purpose input/output                        | I/O | PD                        | 1.8V (VGPIO)                            | Left open                      | Core      |
| C65                    | FAST_SHUTDOWN_N / GPIO4 | Fast Shutdown signal / General purpose input/output                   | I/O | PU                        | 1.8V (VGPIO)                            | Left open                      | Extension |
| C66                    | GPIO5                   | General purpose input/output                                          | I/O | PU                        | 1.8V (VGPIO)                            | Left open                      | Extension |
| CG1 – CG4,<br>G1 – G16 | GND                     | Ground                                                                | GND |                           | 0V                                      |                                | Core      |

\* This refers to the state before and after RESET\_IN\_N; state is Undefined during Reset, Hibernate or OFF modes. Refer to section 3.12 Reset Signal (RESET\_IN\_N) for more details.

\*\* During hibernation (not applicable to Lite Hibernate mode), all the pulled up (PU) signals will toggle at the rate of wake events. Therefore, if the RI signal is to be used in a system to warn the main MCU of an incoming network event (like SMS or DATA), this RI signal cannot be used as it will toggle at the rate of the eDRX or PSM recurrent wakes. It is therefore recommended to use GPIO2 with a built-in pull down (PD) instead of RI. This will allow the module to trigger the GPIO instead of the RI safely, without unwanted toggles.

## 2.1. Pin Types

Table 6. Pin Type Codes

| Type | Definition                      |
|------|---------------------------------|
| I    | Digital Input                   |
| O    | Digital Output                  |
| I/O  | Digital Input / Output          |
| L    | Active High                     |
| H    | Active Low                      |
| T    | Tristate                        |
| T/PU | Tristate with pull-up enabled   |
| T/PD | Tristate with pull-down enabled |
| PU   | Pull-up enabled                 |
| PD   | Pull-down enabled               |
| N/A  | Not Applicable                  |

## 2.2. Pad Configuration (Top View, Through Module)

Note: The following diagram shows the pad configuration from DV2 onwards.

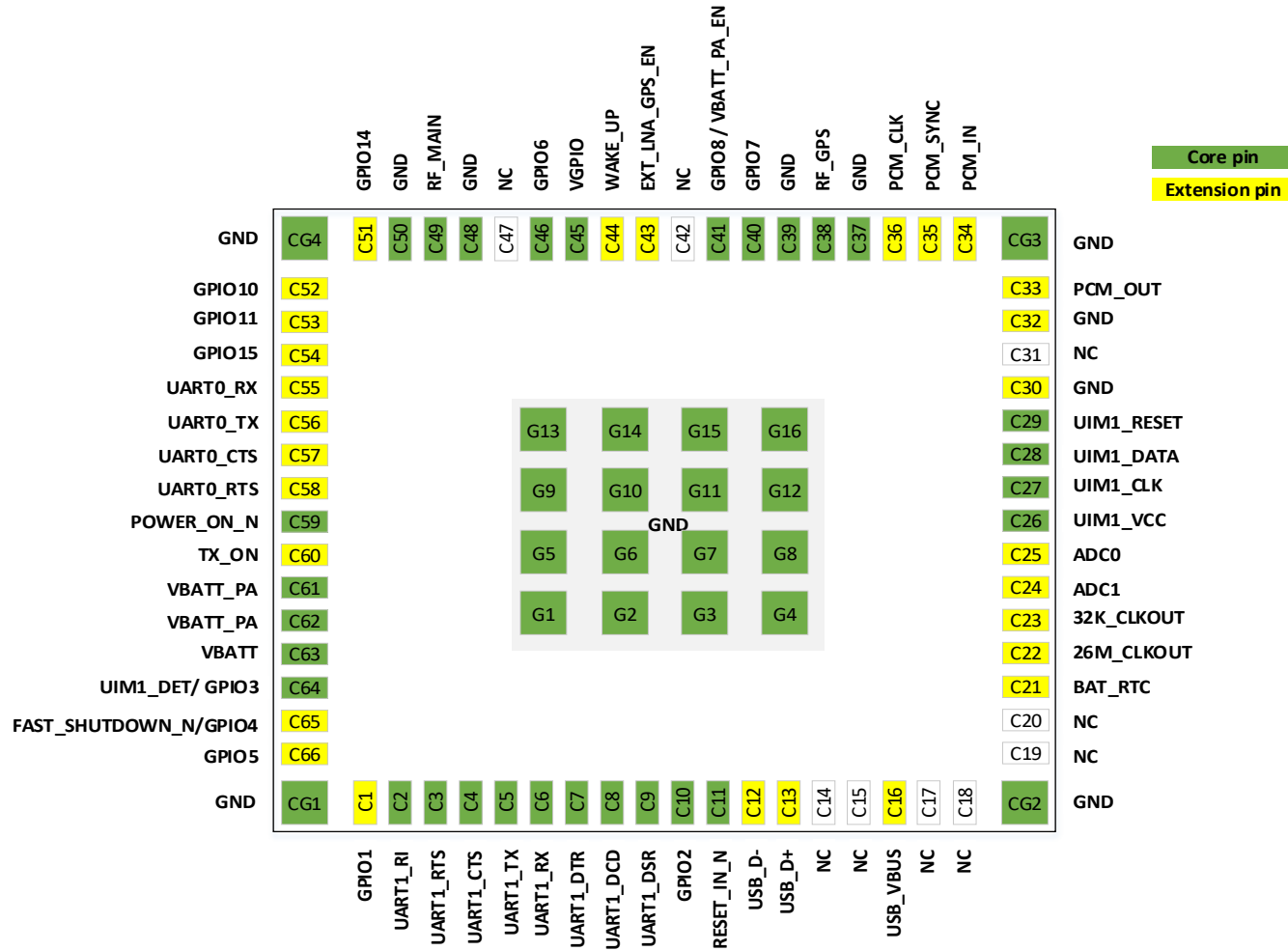


Figure 3. Pad Configuration (Top View through Module)



# 3. Detailed Interface Specifications

**Note:** If not specified, all electrical values are given for VBATT=3.7V and an operating temperature of 25°C.

For standard applications, VBATT and VBATT\_PA must be tied externally to the same power supply. For some specific applications, the module supports separate VBATT and VBATT\_PA connection if the requirements below are fulfilled.

## 3.1. Power Supply

The module is supplied through the VBATT and VBATT\_PA signals.

The rise of the VBATT power signal initiates the power on sequence of the HL7802 modules. Refer to sections 3.11 Power On Signal (PWR\_ON\_N) and 0 \* Any external capacitor or resistor added on the customer application will change these values.

**Note:** Reset Signal (RESET\_IN\_N) for additional information.

Refer to the following table for the pin description of the Power Supply interface.

**Table 7. Power Supply Pin Description**

| Pad Number          | Signal Name | I/O | Description                    |
|---------------------|-------------|-----|--------------------------------|
| C63                 | VBATT       | I   | Power supply (base band)       |
| C61, C62            | VBATT_PA    | I   | Power supply (radio frequency) |
| CG1 – CG4, G1 – G16 | GND         |     | Ground                         |

Refer to the following table for the electrical characteristics of the Power Supply interface.

**Table 8. Power Supply Electrical Characteristics**

| Supply                                  | Minimum | Typical | Maximum |
|-----------------------------------------|---------|---------|---------|
| VBATT voltage (V)                       | 3.2     | 3.7     | 4.35    |
| VBATT_PA voltage (V) Full Specification | 3.2     | 3.7     | 4.35    |
| VBATT_PA voltage (V) Extended Range     | 2.8*    | 3.7     | 4.35    |

\* No guarantee of 3GPP performances for VBATT\_PA from 2.8 to 3.2V.

**Table 9. Maximum Current Consumption (TBC)**

| Supply                   | Typical | Maximum |
|--------------------------|---------|---------|
| VBATT                    |         | 300mA   |
| VBATT_PA LTE             |         | 500mA   |
| VBATT_PA 2G Peak Current | 2A      | 3A      |

**Note:** If a single PSU is used, the recommended power supply capability is 3A.

Maximum values are provided for VSWR 2.5:1 with worst conditions among supported ranges of voltages and temperature (including GPS consumption).



## 3.2. Current Consumption

The following tables list the current consumption of the module at different conditions.

*Note:* Typical values are defined for VBATT/VBATT\_PA at 3.7V and 25°C, for 50Ω impedance at all RF ports. USIM current consumption is not included.

Table 10. Low Current Consumption Mode Cat-M1 (TBC)

| Modem Radio State                 | Lowest Power Mode                            | Configuration                                                | Typical Average Value                 | Unit |
|-----------------------------------|----------------------------------------------|--------------------------------------------------------------|---------------------------------------|------|
| OFF                               | OFF                                          | Module is switched off by AT command and VBATs are connected | 1.8                                   | μA   |
| PSM                               | Hibernate                                    | Floor during PSM dormant                                     | 1.8                                   | μA   |
|                                   | Lite Hibernate                               |                                                              | 30                                    | μA   |
|                                   | Hibernate                                    | 1h cycle and T3324 = 20s                                     | 175 <sup>a</sup>                      | μA   |
|                                   | Lite Hibernate                               |                                                              | 185 <sup>a</sup>                      | μA   |
|                                   | Hibernate                                    | 24h cycle and T3324 = 20s                                    | 9 <sup>a</sup>                        | μA   |
|                                   | Lite Hibernate                               |                                                              | 35 <sup>a</sup>                       | μA   |
| eDRX <sup>e</sup>                 | TAU                                          | Occurrence is network dependent                              | 82                                    | μAh  |
|                                   | Calibration                                  | Applies to eDRX 81.92s and more                              | 12                                    | μAh  |
|                                   | Hibernate                                    | Floor during eDRX                                            | 26                                    | μA   |
|                                   | Lite Hibernate <sup>b</sup>                  |                                                              | 28                                    | μA   |
|                                   | Hibernate Cycle                              | eDRX cycle (TI-eDRX) = 20.48s and PTW and DRX = 1.28s        | 135 <sup>c</sup>                      | μA   |
|                                   | Lite Hibernate Cycle <sup>b</sup>            | Refer to section 3.3.1.2 Extended DRX (eDRX)                 | 135 <sup>c</sup>                      | μA   |
|                                   | Hibernate Cycle                              | eDRX cycle (TI-eDRX) = 81.92s and PTW and DRX = 1.28s        | 50 <sup>c</sup>                       | μA   |
| Lite Hibernate Cycle <sup>b</sup> | Refer to section 3.3.1.2 Extended DRX (eDRX) | 55 <sup>c</sup>                                              | μA                                    |      |
| DRX                               | SMS Reception                                | 50 characters received                                       | 120                                   | μAh  |
|                                   | Sleep                                        | 1.28s                                                        | 2.4<br>(Target: 450 μA <sup>d</sup> ) | mA   |
|                                   |                                              | 2.56s                                                        | 1.9<br>(Target: 300 μA <sup>d</sup> ) | mA   |
|                                   | Running                                      | DRX independent, +KSLEEP=2 or Wake active                    | 35                                    | mA   |

a Values are T3324 dependent.

b Recommended mode.

c Values are PTW and DRX dependent.

d Enhancement will be available in a future firmware version.

e Values are with 250kB of retention memory.

Refer to section 3.3.2 Power Modes for details regarding different low power modes.

The values above assume the following conditions:

- Cat-M1
- Good channel conditions (SINR > 5dB)
- Static scenario
- Cycle includes boot, cell acquisition, network attachment, wait for timer expiry and back to sleep

Table 11. Low Current Consumption Mode Cat-NB1<sup>e</sup>

| Modem Radio State | Lowest Power Mode                 | Configuration                                                | Typical Average Value                 | Unit |
|-------------------|-----------------------------------|--------------------------------------------------------------|---------------------------------------|------|
| OFF               | OFF                               | Module is switched off by AT command and VBATs are connected | 1.8                                   | μA   |
| PSM               | Hibernate                         | Floor during PSM dormant                                     | 1.8                                   | μA   |
|                   | Lite Hibernate                    |                                                              | 30                                    | μA   |
|                   | Hibernate                         | 1h cycle and T3324 = 20s                                     | 235 <sup>a</sup>                      | μA   |
|                   | Lite Hibernate                    |                                                              | 265 <sup>a</sup>                      | μA   |
|                   | Hibernate                         | 24h cycle and T3324 = 20s                                    | 10 <sup>a</sup>                       | μA   |
|                   | Lite Hibernate                    |                                                              | 40 <sup>a</sup>                       | μA   |
| eDRX              | TAU                               | Occurrence is network dependent                              | 100                                   | μAh  |
|                   | Calibration                       | Applies to eDRX 81.92s and more                              | 21                                    | μAh  |
|                   | Hibernate                         | Floor during eDRX                                            | 22                                    | μA   |
|                   | Lite Hibernate <sup>b</sup>       |                                                              | 27                                    | μA   |
|                   | Hibernate Cycle                   | eDRX cycle (TI-eDRX) = 20.48s and PTW and DRX = 1.28s        | 550 <sup>c</sup>                      | μA   |
|                   | Lite Hibernate Cycle <sup>b</sup> | Refer to section 3.3.1.2 Extended DRX (eDRX)                 | 560 <sup>c</sup>                      | μA   |
|                   | Hibernate Cycle                   | eDRX cycle (TI-eDRX) = 81.92s and PTW and DRX = 1.28s        | 145 <sup>c</sup>                      | μA   |
|                   | Lite Hibernate Cycle <sup>b</sup> | Refer to section 3.3.1.2 Extended DRX (eDRX)                 | 150 <sup>c</sup>                      | μA   |
| DRX               | Sleep                             | 1.28s                                                        | 10<br>(Target: 1.3 mA <sup>d</sup> )  | mA   |
|                   |                                   | 2.56s                                                        | 4.2<br>(Target: 700 μA <sup>d</sup> ) | mA   |
|                   |                                   | 10.24s                                                       | 2.5<br>(Target: 200 μA <sup>d</sup> ) | mA   |
|                   | Running                           | DRX independent, <b>+KSLEEP=2</b> or Wake active             | 38                                    | mA   |

a Values are T3324 dependent.

b Recommended mode.

c Values are PTW and DRX dependent.

d Enhancement will be available in a future firmware version.

e All values are preliminary and subject to change.

Refer to section 3.3.2 Power Modes for details regarding different low power modes.

The values above assume the following conditions:

- Cat-NB1
- Good channel conditions (SINR > 5dB) (TBC)
- Static scenario
- Cycle includes boot, cell acquisition, network attachment, wait for timer expiry and back to sleep

Hibernate mode assumes the following conditions:

- I/Os are not held (I/O state is undefined; VGPIO is off)
- Customer application is not allowed to drive the module's I/Os to level > 0.2V
- UICC / USIM is off (ensure using a power saving compliant USIM/UICC)
- The module only wakes up by a high level on the WAKE\_UP pin

Refer to document [4] AirPrime HL7800 Low Power Modes Application Note for additional information.

**Table 12. Typical Current Consumption for LTE Cat-M1 in Connected Mode for All Bands (TBC)**

| Parameter                                                                                                                                                           | Band                                     | Output Power | Average Current (Typical Values) |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------|--------------|----------------------------------|
| LTE Cat-M1 <ul style="list-style-type: none"> <li>• Modem State: Connected (Connection is established)</li> <li>• 4RB_DL and 1RB_UL on 3UL/DL sub frames</li> </ul> | 1, 2, 3, 4, 25, 66                       | 23 dBm       | 205 mA                           |
|                                                                                                                                                                     |                                          | 0 dBm        | 115 mA                           |
|                                                                                                                                                                     | 5, 8, 12, 13, 14, 18, 19, 20, 26, 27, 28 | 23 dBm       | 210 mA                           |
|                                                                                                                                                                     |                                          | 0 dBm        | 120 mA                           |

**Table 13. Expected Typical Current Consumption for NB -1 in Connected Mode for All Bands (TBC)**

| Parameter                                                                                     | Band                                                         | Output Power | Average Current (Typical Values) |
|-----------------------------------------------------------------------------------------------|--------------------------------------------------------------|--------------|----------------------------------|
| NB1 DL peak throughput (27.2kbps)<br>1 NPDCCH, 4 Guard, 3 NPDSCH, 12 Guard, 2 NPUSCH, 3 Guard | 1, 2, 3, 4, 5, 8, 12, 13, 14, 17, 18, 19, 20, 25, 26, 28, 66 | 23 dBm       | 105 mA                           |
|                                                                                               |                                                              | 0 dBm        | 100 mA                           |
| NB1 UL peak throughput (62.5kbps)<br>1 NPDCCH, 8 Guard, 4 NPUSCH, 3 Guard                     |                                                              | 23 dBm       | 165 mA                           |
|                                                                                               |                                                              | 0 dBm        | 130 mA                           |

**Table 14. Expected Typical Current Consumption for 2G Connected Mode for all Bands**

| Parameter | Band          | Output Power | Average Current (Typical Values) <sup>a,b</sup> |
|-----------|---------------|--------------|-------------------------------------------------|
| PCL5      | 850/900 MHz   | 33 dBm       | 310 mA                                          |
| PCL19     | 850/900 MHz   | 5 dBm        | 160 mA                                          |
| PCL0      | 1800/1900 MHz | 30 dBm       | 260 mA                                          |
| PCL15     | 1800/1900 MHz | 0 dBm        | 160 mA                                          |

a Typical average current values for 1 time slot.

b Measured at 3.7V.

## 3.3. Power Consumption States

### 3.3.1. 3GPP Power Saving Features

This section describes power saving features that are specified by 3GPP and that are supported by the module. As per 3GPP specification, these features include power states and behaviors that pertain only to the cellular communication part of the module and do not consider memory states, I/O states, etc., of the module overall.

#### 3.3.1.1. Power Saving Mode (PSM)

Power Saving Mode (PSM) is a 3GPP feature that allows the HL7802 to minimize power consumption by registering on a PSM-supporting LTE network and entering PSM state (a very low power 'dormant' state). For the LTE network to know that the module is still present while it is in PSM state, the network will require the module to periodically send a TAU (Tracking Area Update). If the module sends any data or does any other type of network transmission, the periodic TAU timer would be restarted. The periodic TAU periodicity is negotiated with the LTE network (i.e. the module will request the desired duration and the network will reply with the value to be used).

During the PSM state, the module is unreachable by the network until it wakes up to perform the periodic TAU or the module is woken up by the WAKE\_UP pin. The host processor can wake the module up using WAKE\_UP and send data to the network at any time during the PSM state. It is not necessary to synchronize the application data transmission periodicity with that of the periodic TAU.

While the module is in PSM:

- Power consumption is significantly reduced with longer dormant periods
- Networking layer signaling overhead is reduced
- Radio resource signaling is reduced

Typical candidates for PSM are systems (such as monitors and sensors) that:

- Require long battery life (low power consumption).
- Infrequently send mobile originated data (every few hours, days, weeks, etc.), with optional reply data from the network.
- Tolerate modules being inaccessible for long periods of time.
- Do not use mobile-terminated voice/data/SMS. Some networks may not allow mobile terminated data during PSM but using eDRX is a better option for applications than need mobile terminated (network originated) data.

PSM can be activated by the user either before or after the module attaches to the network. If PSM is activated before the attach, the module will request PSM during the attach. If PSM is activated after the attach, the module will immediately request PSM from the network with a TAU message. The user may also modify the requested PSM parameters; afterwards, the module will update the network using a TAU. The following example describes how the module uses PSM by requesting PSM after the attach (as shown in Figure 4 PSM Example (Simplified)):

1. Module attaches on an LTE network.
2. User enables PSM via `+CPSMS`, specifying the desired periodic TAU timer and Active timer periods.
3. The PSM request including the settings (as specified in `AT+CPSMS`) are sent to the network by the module within a TAU message .

4. Network response indicates if the UE may use PSM and the PSM parameters that should be used. The network may adjust the PSM parameters from those requested by the UE .
5. If the network supports PSM:
  - a. Module enters idle mode (waiting for Rx from network).
  - b. When module has remained idle for the Active timer period, module powers off (except for maintaining timer and interrupts) and enters PSM.
  - c. Module remains in PSM for the specified TAU timer period or until the WAKE\_UP pin wakes it.
    - i. If the module does not send any data or does not access the network before the TAU timer period expires, then the module sends a TAU to the network.
    - ii. If the module sends data to the network before the TAU timer period expires, the TAU timer is restarted. The module can be woken with WAKE\_UP in order to send data at any time. The network application server may send data back to the module before the PSM active timer expires. If the module sends data to the network more often than the periodic TAU timer period, the UE would not need to send a TAU.
  - d. Module enters idle mode and cycle repeats.

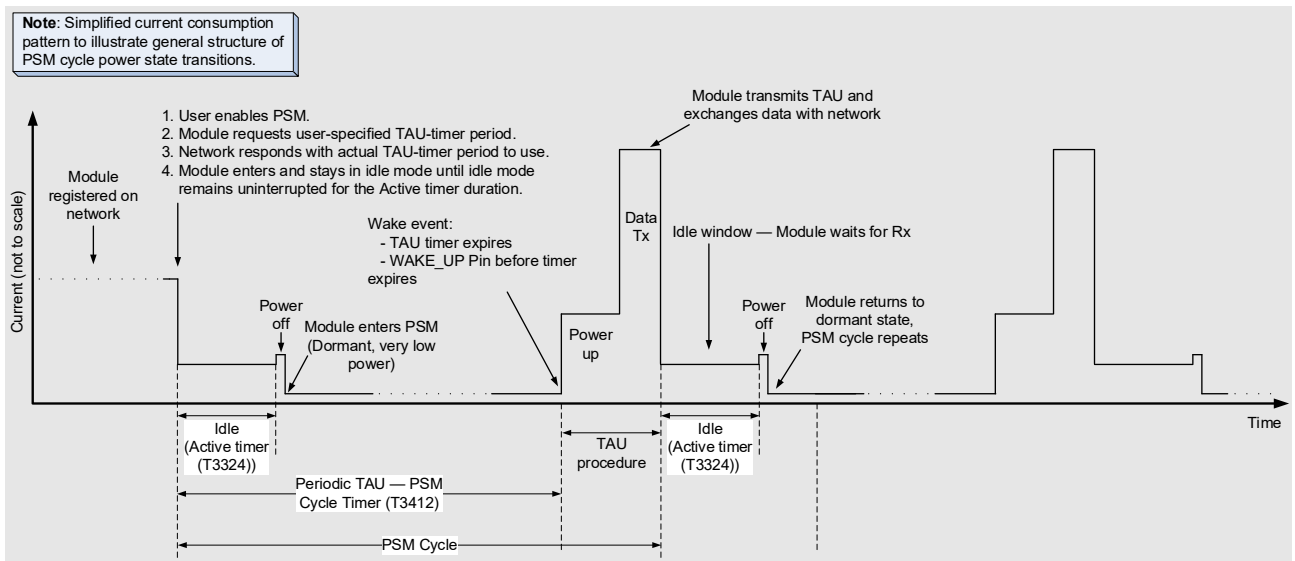


Figure 4. PSM Example (Simplified)

Note that:

- The PSM Periodic-TAU timer and Active Time values must be carefully selected to match the intended use case(s) for the module:
  - Periodic TAU PSM Cycle timer (T3412) – This is the maximum time the module can be away from the network (i.e. without a transmission). The module will automatically send a periodic TAU message to the network when this timer expires. If the module accesses the network (for example for mobile originated data) this timer would restart, and the module does not need to access the network for another T3412 duration. Typically, PSM should be used for applications that originate data from the module so the requested T3412 should be much longer than the expected period of the data originating from the module. Reducing the number of TAU will help reduce current consumption. Note that if the module were to fail to access the network within this time, the module would need to reattach to the network. While the module is in PSM, the network will not attempt to access the module.

- Active Time (T3324) – This is the duration of time that the module and the network are to be idle (without sending/receiving any data) to trigger the module to enter PSM state. This timer starts when the module enters idle state and will restart when there are any data transfers (to/from the module). If the module/network do not send any data for T3324 period, the module will enter PSM state. The intent of this timer is to allow for a period of time for the module and the network server to communicate. The value of this timer should be selected to match the expected module to/from network server packet delays (using shorter durations would save more current).
- While it may be possible to set a large Active Time (T3324) such that mobile terminated access after a TAU is possible, it may be difficult to reliably send data to the UE as the exact time of the TAU may vary. Instead, the module application should periodically poll the network server if the module is to be accessible. With this approach a shorter Active Time (T3324) can be used and a longer periodic TAU time (T3412) – the timing of when the module is accessible is also more accurate. The polling packet sent by the module would use a similar amount of current as a TAU. It is recommended to use eDRX (as described in the next section) instead of PSM if the module needs to be truly accessible.
- When using multiple devices, consider scheduling the modules to wake at different times so that the network does not get flooded by all modules waking and transmitting simultaneously.

### 3.3.1.2. Extended DRX (eDRX)

The Extended Idle DRX (I-eDRX) is a 3GPP specified feature that reduces the number of Paging Occasions (PO) that the module needs to monitor. Many data module applications are tolerant to delays in downlink data packets so extending the paging cycle would allow for current consumption savings for these applications. The HL7802 supports eDRX and can take advantage of the feature by entering a low power state between the eDRX cycles. The periodicity of the eDRX cycles ( $T_{I-eDRX}$ ) and the duration of the Paging Transmission Window (PTW) are shown in the diagram below. The module application can negotiate specific eDRX parameter values with the network.

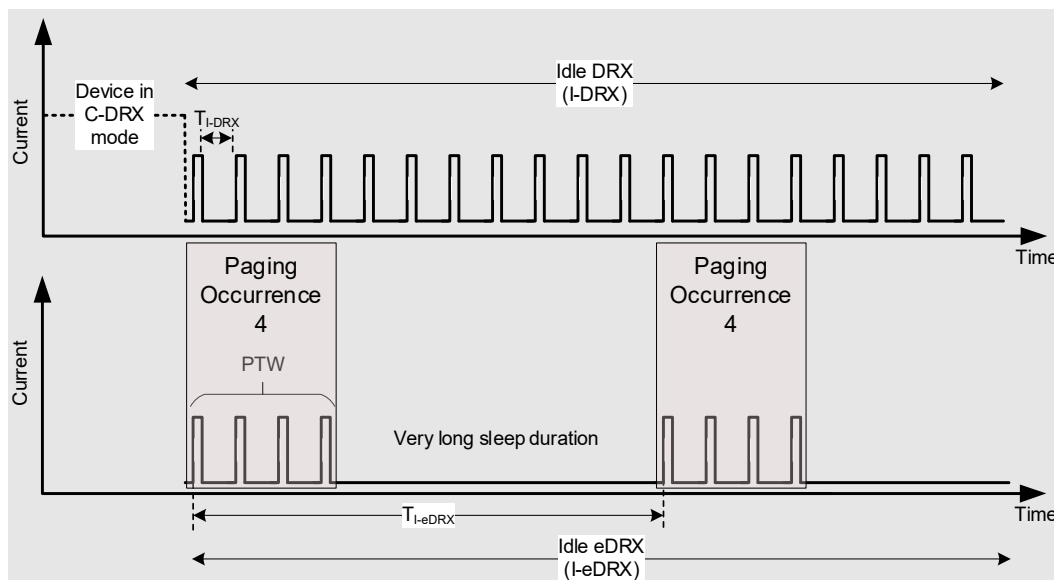


Figure 5. eDRX Example (PTW: 4 Paging Occurrences)

The HL7802 enters a very low current consumption state between eDRX cycles. However, for a short period of time right after the module enters idle state, the module will have a few extra short wake ups for clock calibration (shorter than an eDRX monitor). The following figure shows an eDRX power consumption profile with a periodic TAU event. Notice that after the TAU, the eDRX 81.92s cycle is restored slowly by several iterations from 10s to 20s then to 40s before reaching the 81.92s wake. This behavior is mandatory by design and cannot be avoided.

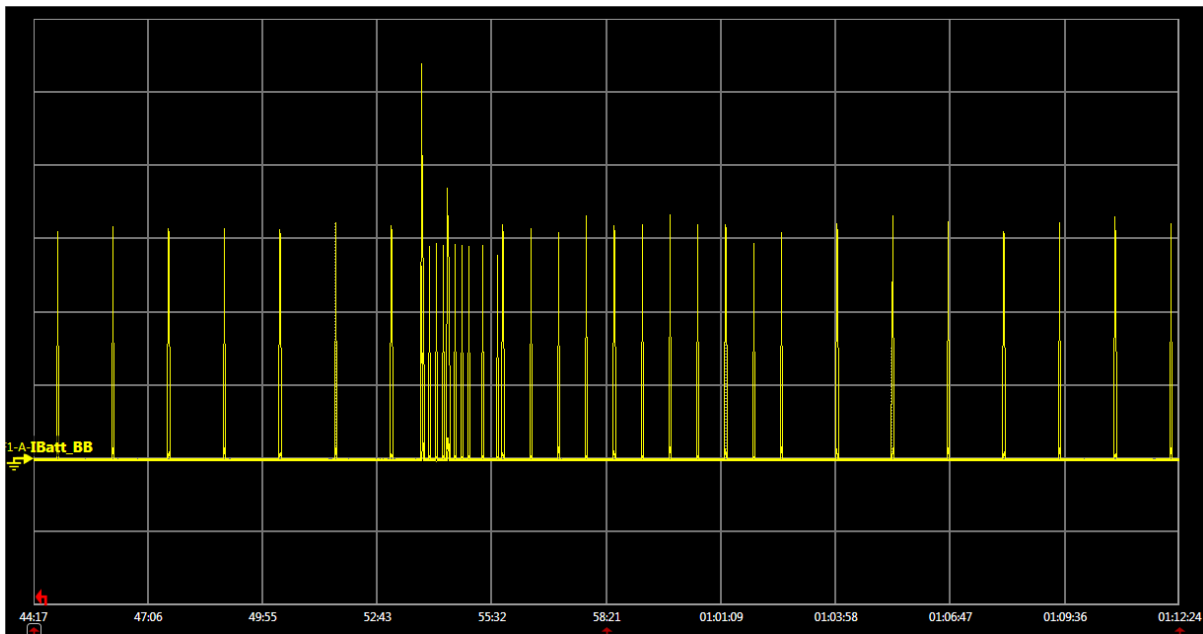


Figure 6. eDRX Power Consumption Profile Interruption

The following table describes available methods for configuring eDRX.

Table 15. eDRX-Related Commands

| AT Command  | Description                                        |
|-------------|----------------------------------------------------|
| AT+CEDRXS   | Enable/disable eDRX and configure related settings |
| AT+CEDRXRDP | Display current eDRX settings                      |

For example:

- Use the **AT+CEDRXS** command to configure the desired  $T_{I-eDRX}$  value.
- During the network attach or TAU process:
  - eDRX request with the settings (as specified in **AT+CEDRXS**) are sent to the network.
  - Network response indicates if the UE may use eDRX and the eDRX parameters that should be used. The network may adjust the eDRX parameters from those requested by the UE.
- If eDRX is accepted by the network, the UE will only need to monitor during the eDRX paging occurrences. The UE may enter low power mode state between the eDRX paging occurrences (depending on the UE configuration).

Note that:

- The eDRX parameters must be carefully selected to match the intended use case(s) for the module. The module can only be paged at an eDRX paging occasion, hence, longer eDRX cycles will delay mobile terminated data reception. Selecting shorter eDRX cycles will reduce the latency but if the eDRX cycles are too short then there will be lower power savings. The duration of the eDRX cycle should be appropriately selected for the specific use case.
- Network-side store and forward is supported – Packets will be stored until the module’s next eDRX paging occurrence.

### 3.3.1.3. Possible Concurrent Modes

These two modes may run concurrently in a future firmware release; that is, eDRX may be performed during the active window of PSM.

For example, for a PSM of one day (T3412 of 86400s) with an active window (T3324) of 5 minutes (300s), the module may be in an eDRX power saving mode of 82s for 3 cycles then sleep for 23h55 until the next TAU during the 5-minute active window.

### 3.3.2. Power Modes

In addition to the 3GPP power saving features, several low power modes are defined for the AirPrime HL7802. There are three power modes defined, as follows:

- Sleep mode: 26Mhz system clock is OFF, all memories and I/O states are retained. The module can wake-up via the WAKE\_UP signal or UART1\_DTR.
- Lite Hibernate mode: RTC, I/O states and a part of the RAM are ON (RAM is only used for 4G protocol state and data). The module can wake-up via the WAKE\_UP signal or UART1\_DTR.
- Hibernate mode: RTC and optionally part of the RAM (depending on the 4G modem state) are ON. The module can only wake-up only via the WAKE\_UP signal. (All I/Os are in undefined state.)

These modes can be configured using the **+KSLEEP** AT command.

Note that:

- When the module exits from Lite Hibernate or Hibernate mode, the host processor will act as after a module reset (all non-persistent configurations are lost).
- Sleep mode is recommended for regular DRX mode.
- Hibernate mode is recommended when the module is configured in PSM or eDRX mode.

The table below summarizes these low power modes.

Table 16. Low Power Modes

| Power Mode     | Possible Modem State                  | I/O State    | Hardware Wake-Up Signal Source |
|----------------|---------------------------------------|--------------|--------------------------------|
| Sleep          | Stack OFF, DRX, eDRX, PSM, No service | Retained     | UART1_DTR<br>WAKE_UP           |
| Lite Hibernate | Stack OFF, eDRX, PSM, No service      | Retained     | UART1_DTR<br>WAKE_UP           |
| Hibernate      | Stack OFF, eDRX, PSM                  | Not retained | WAKE_UP                        |

**Warning:** *If USB\_VBUS is connected, it will not be possible to enter Lite Hibernate or Hibernate mode.*

Refer to document [4] AirPrime HL7800 Low Power Modes Application Note for additional details, especially on the relationship between 3GPP power saving features and the HL7802 power modes. Additionally, refer to document [5] AirPrime HL7800-M MNO and RF Band Customization at Customer Production Site Application Note for band selection details since it impacts power consumption.



### 3.3.3. Digital I/O during Hibernate Power Mode

The following behavior are only applicable to digital I/Os in Hibernate mode in eDRX and PSM; it is not applicable when in Lite Hibernate or Sleep mode.

- VGPI0 is OFF.
- No I/O should be biased as no internal source exists. The maximum allowed voltage is  $\pm 0.2V$  at any I/O.
- All I/Os referenced to VGPI0 are undefined.
- All I/Os referenced to VGPI0 are restored to their state at every wake; that also includes their reset state as described in Table 5 Pin Definition.

For example, if an I/O has a low state before entering Hibernate mode but has a PU state during reset, the I/O state will be undefined during Hibernate mode and then will be high due to the PU during the few hundred ms reset mode and then restored at its low level; this happens at every wake cycle of hibernate mode.

The behavior described above generates a toggling of various I/Os like the UART lines and the GPIOs during the Hibernate mode and can result in unwanted I/O activity from the host processor's point of view.

Every line referenced to VGPI0 as described in section 2 Pad Definition is affected by this behavior.

#### 3.3.3.1. In PSM Mode

VGPI0 and I/O (with Pull Up by default) are both high for 34.9 s corresponding to the TAU procedure + 30s of activity window, time duration while the module can be reach from the network (T3324).

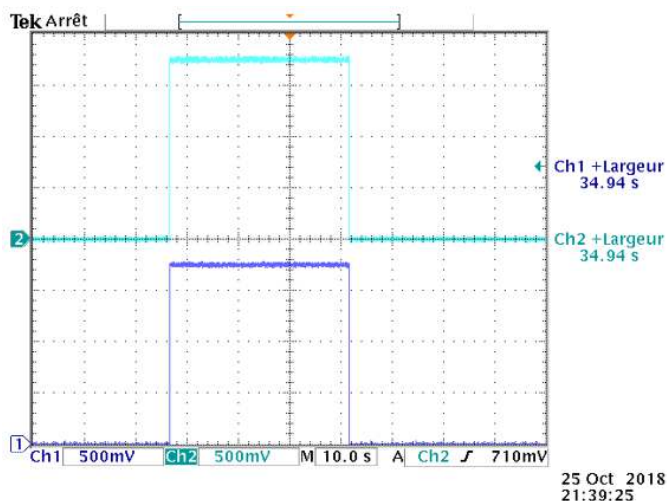


Figure 7. PSM I/O Toggling during TAU and the Active Window (T3324)

### 3.3.3.2. In eDRX Mode

At every eDRX paging wake, the VGPIO is present and so is any GPIO (with Pull Up by default). In the figure below, the eDRX cycle is 20s of sleep and 1.024s of activity.

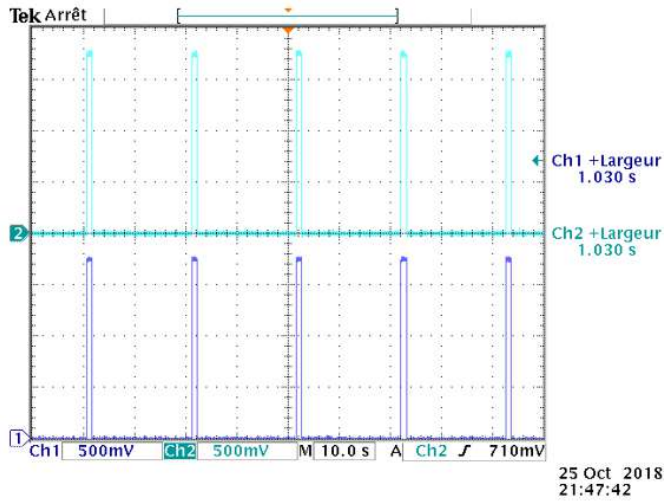


Figure 8. eDRX Cycle of 20s Sleep and 1.024s of Activity

For eDRX cycles of 81.92 s or longer, that is a 10-minute internal calibration period that repeats at every TAU cycle. In this case, the eDRX wakes are added to the internal calibration wakes and results in thin extra wakes of VGPIO that results in I/O toggling. This may influence the application processor or customers' interface. Also, these thin internal calibration wakes (that lasts for 10 minutes) repeat every 10 seconds, then every 20 s, then every 40 s before reaching the final 80 seconds wake.

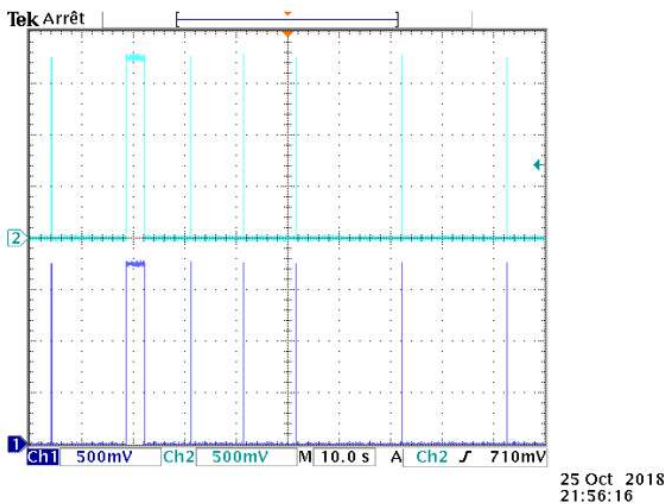


Figure 9. eDRX with Extra Calibration Wakes

Eventually, a stable eDRX wake repeats every cycle without extra wakes. In the following figure, a PTW of 1.02 is used with a cycle of 81.92s.

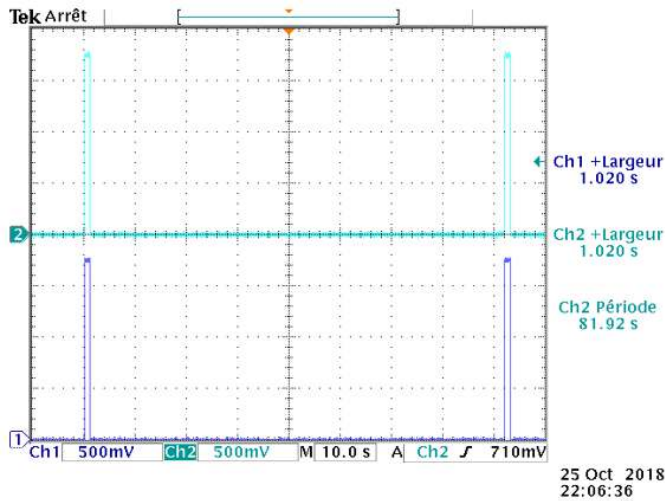


Figure 10. Stable eDRX Cycle of 81.92s after Calibration

### 3.4. VGPIO

The VGPIO output can be used to:

- Pull-up signals such as I/Os.
- Supply the digital transistors driving LEDs.

The VGPIO output is available when the module is switched ON. (This output is not available in low power mode.) Note that VGPIO is OFF during Hibernate mode.

Refer to the following table for the pin description of the VGPIO interface.

Table 17. VGPIO Pin Description

| Pad Number | Signal Name | I/O | Description         |
|------------|-------------|-----|---------------------|
| C45        | VGPIO       | O   | GPIO voltage output |

Refer to the following table for the electrical characteristics of the VGPIO interface.

Table 18. VGPIO Electrical Characteristics

| Parameter                           | Minimum | Typical | Maximum | Remarks                                                                                   |
|-------------------------------------|---------|---------|---------|-------------------------------------------------------------------------------------------|
| Voltage level (V)                   | 1.7     | 1.8     | 1.9     | Both active mode and sleep mode                                                           |
| Current capability Active Mode (mA) | -       | -       | 50      | The total current from all I/Os combined, and supplied by VGPIO, should not exceed 50 mA. |
| Current capability Sleep Mode (mA)  |         |         | 1       |                                                                                           |
| Rise Time (ms)                      | -       | -       | 0.5     | Start-Up time from 0V                                                                     |

## 3.5. Real Time Clock (BAT\_RTC)

*Note: This interface will be available in a future firmware release.*

The AirPrime HL7802 provides an input to connect a Real Time Clock power supply.

This pin is used as a back-up power supply for the internal Real Time Clock. The RTC is supported when VBATT is available but a back-up power supply is needed to save date and hour when VBATT is switched off.

This pin is input only and is not capable of charging a backup capacitor.

Table 19. BAT\_RTC Electrical Characteristics

| Parameter                 | Minimum | Typical | Maximum | Unit |
|---------------------------|---------|---------|---------|------|
| Input voltage             | 2.2     | -       | 4.35    | V    |
| Input current consumption | -       |         | 10      | μA   |

## 3.6. USIM Interface

The AirPrime HL7802 has one physical USIM interface, USIM1, and an optional internal USIM or eUICC.

The USIM1 interface allows control of an only 1.8V USIM and is fully compliant with GSM 11.11 recommendations concerning USIM functions.

The five signals used by this interface UIM1 are as follows:

- UIM1\_VCC: Power supply
- UIM1\_CLK: Clock
- UIM1\_DATA: I/O port
- UIM1\_RESET: Reset
- UIM1\_DET/GPIO3: Hardware SIM detection

Refer to the following table for the pad description of the USIM1 interface.

Table 20. USIM1 Pin Description

| Pad Number | Signal Name | Description             | Multiplex |
|------------|-------------|-------------------------|-----------|
| C26        | UIM1_VCC    | 1.8V USIM1 Power supply |           |
| C27        | UIM1_CLK    | 1.8V USIM1 Clock        |           |
| C28        | UIM1_DATA   | 1.8V USIM1 Data         |           |
| C29        | UIM1_RESET  | 1.8V USIM1 Reset        |           |
| C64        | UIM1_DET    | 1.8V USIM1 Detection    | GPIO3     |

Refer to the following table for the electrical characteristics of the USIM1 interface.

**Table 21. USIM1 Electrical Characteristics**

| Parameter                                                 | Minimum | Typical | Maximum | Remarks                                                                   |
|-----------------------------------------------------------|---------|---------|---------|---------------------------------------------------------------------------|
| UIM1 Interface Voltage (V)<br>(VCC, CLK, I/O, RESET)      | -       | 1.80    | -       | The appropriate output voltage is auto detected and selected by software. |
| UIM1 Detect                                               | -       | 1.80    | -       | High active                                                               |
| UIM1_VCC Current (mA)                                     | -       | -       | 50      | Max output current in sleep mode = 3 mA                                   |
| UIM1_VCC Power-up Setting Time ( $\mu$ s) from power down | -       | 10      | -       |                                                                           |

### 3.6.1. UIM1\_DET

*Note: This interface will be available in a future release.*

UIM1\_DET is used to detect and notify the application about the insertion and removal of a USIM device in the USIM socket connected to the main USIM interface (UIM1). When a USIM is inserted, the state of UIM1\_DET transitions from logic 0 to logic 1. Inversely, when a USIM is removed, the state of UIM1\_DET transitions from logic 1 to logic 0.

Enabling or disabling this USIM detect feature can be done using the **AT+KSIMDET** command. For more information about this command, refer to document [2] AirPrime HL78xx AT Commands Interface Guide. (Note that this command is not yet available.)

## 3.7. USB Interface

*Note: This interface will be available in a future firmware release.*

The AirPrime HL7802 has one Universal Serial Bus Interface Full Speed.

Refer to the following table for the pad description of the USB interface.

**Table 22. USB Pin Description**

| Pad Number | Signal Name | I/O | Function          |
|------------|-------------|-----|-------------------|
| C12        | USB_D-      | I/O | USB Data Negative |
| C13        | USB_D+      | I/O | USB Data Positive |
| C16        | USB_VBUS    | I   | USB VBUS          |

Refer to the following table for the electrical characteristics of the USB interface.

**Table 23. USB Electrical Characteristics**

| Parameter                             | Minimum | Typical | Maximum | Unit |
|---------------------------------------|---------|---------|---------|------|
| Input voltage at pins USB_D+ / USB_D- | 3.15    | 3.3     | 3.45    | V    |
| USB_VBUS                              | 4.75    | 5.0     | 5.25    | V    |

*Note:* `USB_VBUS` is a mandatory connection to supply the USB interface.

When USB is used, the lowest power mode supported is Sleep mode.

`USB_VBUS` must not be connected if Hibernate or Lite Hibernate mode is used.

## 3.8. Electrical Information for Digital I/O

The table below enumerates the electrical characteristics of the following digital interfaces.

- UART
- PCM
- GPIOs
- FAST\_SHUTDOWN\_N
- EXT\_LNA\_GPS\_EN

**Table 24. Digital I/O Electrical Characteristics**

| Parameter        | Description                 | Minimum      | Typical | Maximum      | Unit |
|------------------|-----------------------------|--------------|---------|--------------|------|
| V <sub>IH</sub>  | Logic High Input Voltage    | 0, 7 x VGPIO |         | **           | V    |
| V <sub>IL</sub>  | Logic Low Input Voltage     | **           |         | 0, 3 x VGPIO | V    |
| V <sub>OH</sub>  | Logic High Output Voltage   | 0, 8 x VGPIO |         |              | V    |
| V <sub>OL</sub>  | Logic Low Output Voltage    |              |         | 0, 2 x VGPIO | V    |
| I <sub>o</sub> * | I/O Drive Strength          | 2            |         | 4            | mA   |
| I <sub>IH</sub>  | Input current in Pull Down  | +10          | +35     | +45          | μA   |
| I <sub>IL</sub>  | Input Current in Pull up    | -10          | -35     | -45          | μA   |
| R <sub>PU</sub>  | Internal Pull-Down Resistor | 13           | 50      | 65           | KΩ   |
| R <sub>PD</sub>  | Internal Pull-Up Resistor   | 13           | 50      | 65           | KΩ   |

\* The total current from all I/Os combined, and supplied by VGPIO, should not exceed 50mA.

\*\* The maximum voltage allowed on digital I/O is ±0.2V during Hibernate mode.

## 3.9. General Purpose Input/Output (GPIO)

The AirPrime HL7802 provides 12 GPIOs, 3 of which are multiplexed.

The following table describes the pin description of the GPIO interface.

**Table 25. GPIO Pin Description**

| Pad Number | Signal Name | Multiplex   | I/O | Power Supply Domain |
|------------|-------------|-------------|-----|---------------------|
| C1         | GPIO1       |             | I/O | 1.8V                |
| C10        | GPIO2       |             | I/O | 1.8V                |
| C40        | GPIO7       |             | I/O | 1.8V                |
| C41        | GPIO8       | VBATT_PA_EN | I/O | 1.8V                |
| C46        | GPIO6       |             | I/O | 1.8V                |

| Pad Number | Signal Name | Multiplex       | I/O | Power Supply Domain |
|------------|-------------|-----------------|-----|---------------------|
| C51        | GPIO14      |                 | I/O | 1.8V                |
| C52        | GPIO10      |                 | I/O | 1.8V                |
| C53        | GPIO11      |                 | I/O | 1.8V                |
| C54        | GPIO15      |                 | I/O | 1.8V                |
| C64        | GPIO3       | UIM1_DET        | I/O | 1.8V                |
| C65        | GPIO4*      | FAST_SHUTDOWN_N | I/O | 1.8V                |
| C66        | GPIO5       |                 | I/O | 1.8V                |

\* GPIO4 will be available in a future release.

### 3.10. Main Serial Link (UART1)

The main serial link (UART1 up to 921.6Kbps) is used for communication between the module and a PC or host processor. It consists of a flexible 8-wire serial interface that complies with RS-232 interface. The main serial link (UART1) is an asynchronous serial interface; and is also used to upgrade the firmware locally.

If possible, it is highly recommended to add 0Ω on every line to help the debug process. This will force the UART signal layout to the top PCB layer and allow access to the signal on the resistors.

The signals used by UART1 are as follows:

- TX data (UART1\_TX)
- RX data (UART1\_RX)
- Request To Send (UART1\_RTS)
- Clear To Send (UART1\_CTS)
- Data Terminal Ready (UART1\_DTR)
- Data Set Ready (UART1\_DSR)
- Data Carrier Detect (UART1\_DCD)
- Ring Indicator (UART1\_RI)

---

*Note:* Signal names are according to PC view.

---

Refer to the following table for the pin description of the main serial link (UART1) interface.

Table 26. UART1 Pin Description

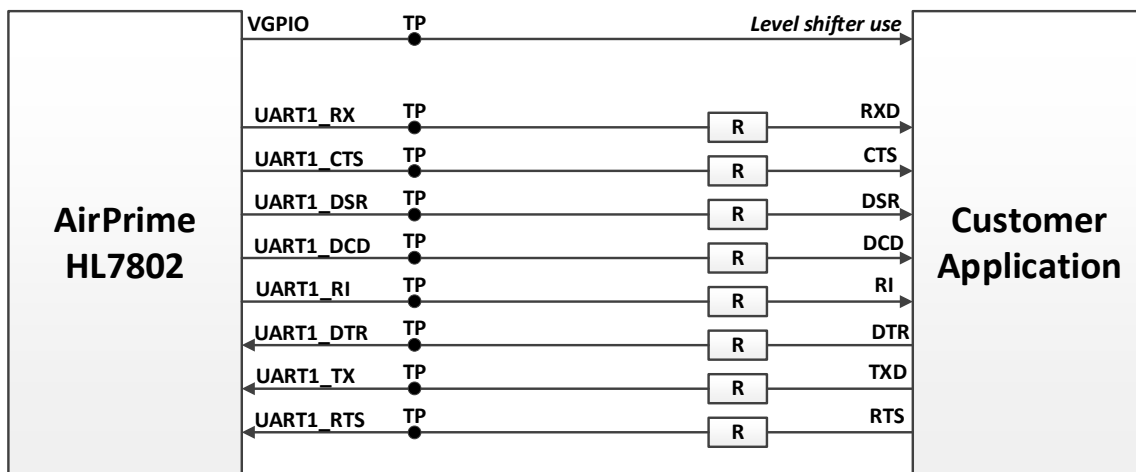
| Pad Number | Signal Name* | I/O*           | Description                                                                                                         |
|------------|--------------|----------------|---------------------------------------------------------------------------------------------------------------------|
| C2         | UART1_RI     | O (active low) | Signal incoming calls (data only), SMS, etc.                                                                        |
| C3         | UART1_RTS    | I (active low) | Request to send                                                                                                     |
| C4         | UART1_CTS    | O (active low) | The module is ready to receive AT commands                                                                          |
| C5         | UART1_TX     | I              | Transmit data                                                                                                       |
| C6         | UART1_RX     | O              | Receive data                                                                                                        |
| C7         | UART1_DTR    | I (active low) | Prevents the module from entering sleep mode, switches between data mode and command mode, and wakes the module up. |
| C8         | UART1_DCD    | O (active low) | Signal data connection in progress                                                                                  |

| Pad Number | Signal Name* | I/O*           | Description                 |
|------------|--------------|----------------|-----------------------------|
| C9         | UART1_DSR    | O (active low) | Signal UART interface is ON |

\* DTE (Data Terminal Equipment) convention, i.e. according to PC view.

Some customer applications require to wake-up its host processor with the RI signal after SMS or IP reception. When using eDRX mode in combination with Hibernate low power mode, this use case cannot be handled through the standard UART1\_RI signal because it is active low and cannot remain high in Hibernate mode. In order to overcome this system issue, several GPIOs can be configured as an inverted RI signal (RI\_inverse\_gpio; refer to **AT+KRIC** in documents [2] AirPrime HL78xx AT Commands Interface Guide and [4] AirPrime HL7800 Low Power Modes Application Note for details.) GPIO2 is used by default for this function; however, all GPIOs with an internal Pull Down (see Table 5) can also be used with **AT+KRIC** (it is recommended to add an external 470kΩ PD to keep the I/O in a defined state during Hibernate mode).

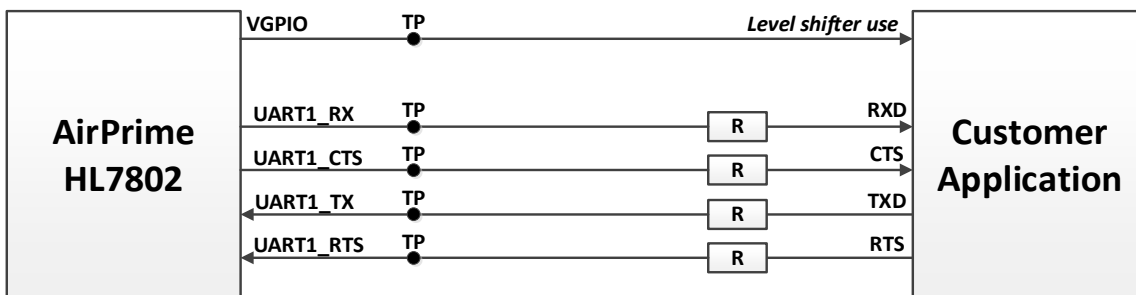
### 3.10.1. 8-wire Application



Note: R is a 0Ω resistor (default value)

Figure 11. 8-wire UART Application Example

### 3.10.2. 4-wire Application

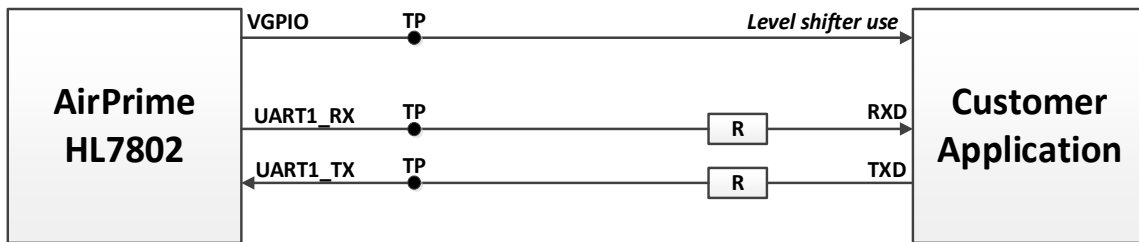


Note: R is a 0Ω resistor (default value)

Figure 12. 4-wire UART Application Example



### 3.10.3. 2-wire Application



Note: R is a 0Ω resistor (default value)

Figure 13. 2-wire UART Application Example

## 3.11. Power On Signal (PWR\_ON\_N)

The PWR\_ON\_N signal is internally pulled-up. Once VBATT is supplied to the module, the internal supply regulator is enabled and so the PWR\_ON\_N signal is by default at high level.

In case the PWR\_ON\_N pin is not configured as managed by host (default configuration), the module starts regardless of the PWR\_ON\_N state. In case the RESET\_IN\_N signal is maintained low, the module will not start until RESET\_IN\_N is released.

In case the PWR\_ON\_N pin is configured as managed by host, a low-level signal must be provided to switch the module ON.

Table 27. PWR\_ON\_N Pin Description

| Pad Number | Signal Name | I/O | Description          |
|------------|-------------|-----|----------------------|
| C59        | PWR_ON_N    | I   | Powers the module ON |

Table 28. PWR\_ON\_N Electrical Characteristics

| Parameter             | Minimum | Typical | Maximum |
|-----------------------|---------|---------|---------|
| Input Voltage-Low (V) |         |         | 0.3     |

Note: As PWR\_ON\_N is internally pulled up, an open collector or open drain transistor must be used for ignition.

VGPIO is an output from the module that can be used to check if the module is active.

- When VGPIO = 0V, the module is OFF (or in low power mode)
- When VGPIO = 1.8V, the module is ON (it can be in idle, communication or sleep mode)

Note: PWR\_ON\_N cannot be used to power the module off. To power the module off, use AT command **AT+CPOF** or the RESET\_IN\_N pin. Also, don't put the PWR\_ON\_N at low level or the WAKE\_UP pin at high level during the power off sequence. The module may be damaged if these conditions are not met.

### 3.11.1. PWR\_ON\_N Not Managed (Default)

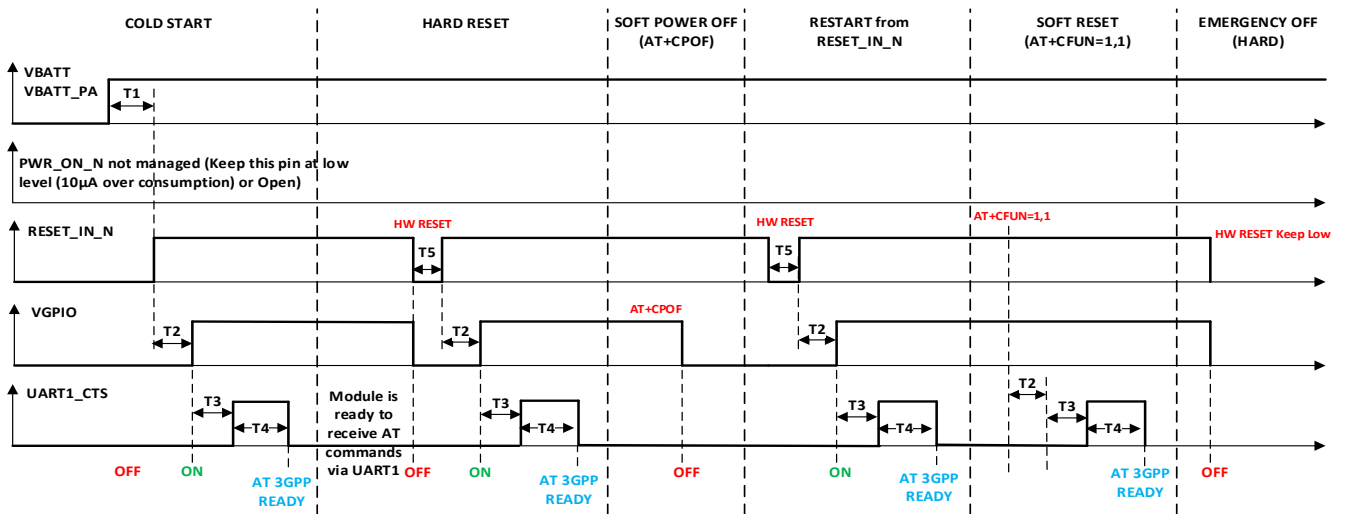


Figure 14. Power Up and Power Down Sequence without PWR\_ON\_N

Table 29. PWR\_ON\_N Not Managed Timing

| Parameter                              | Minimum | Typical | Maximum* | Unit |
|----------------------------------------|---------|---------|----------|------|
| T1: delay between VBATT and RESET_IN_N |         |         | 1        | ms   |
| T2: delay between RESET_IN_N and VGPIO |         |         | 5        | ms   |
| T3: delay between VGPIO and UART1_CTS  |         |         | 100      | µs   |
| T4: delay                              |         | 2 (TBC) | 7        | s    |
| T5: HW RESET delay                     | 1       |         |          | ms   |

\* Any external capacitor or resistor added on the customer application will change these values.

### 3.11.2. PWR\_ON\_N Managed

*Note: This interface will be available in a future firmware release. All figures and timings are still TBC.*

#### 3.11.2.1. First Power On

On the first battery connection, the first power on sequence (cold start) will appear one time after PWR\_ON\_N configuration via AT command. Refer to section 3.11.2.2 Power Up and Power Down after the First Cold Start for details.

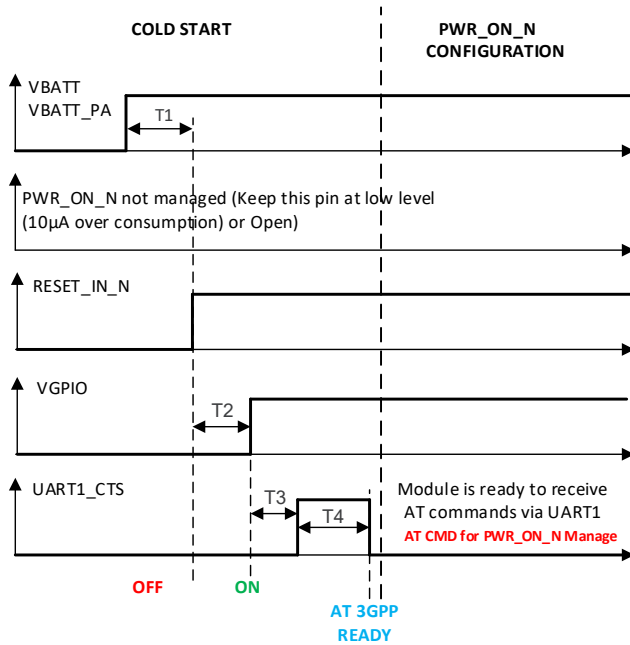
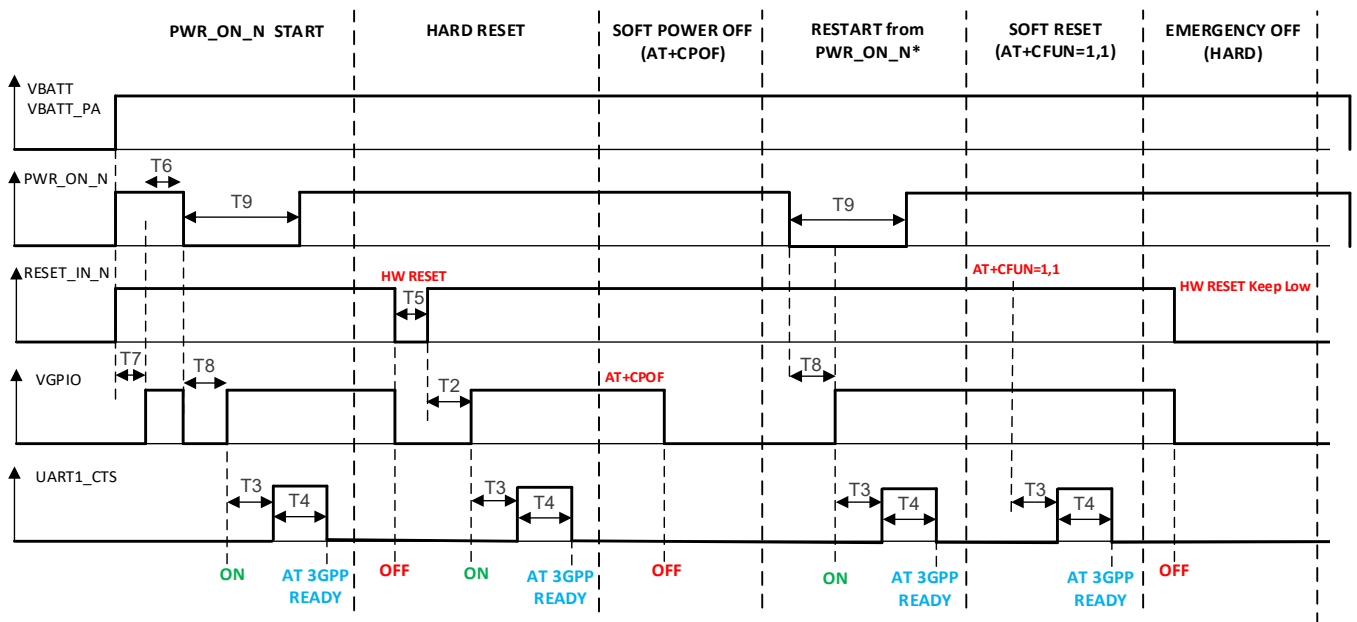


Figure 15. Power Up Sequence with PWR\_ON\_N Cold Start

### 3.11.2.2. Power Up and Power Down after the First Cold Start



\* After AT+CPOF, the module can be woken up by either the PWR\_ON\_N or WAKE\_UP pin

Figure 16. Power On Sequence with PWR\_ON\_N

### 3.11.2.3. Timing

Table 30. PWR\_ON\_N Managed Timing

| Parameter                              | Minimum | Typical | Maximum* | Unit |
|----------------------------------------|---------|---------|----------|------|
| T1: delay between VBATT and RESET_IN_N | 0       |         |          | ms   |

| Parameter                              | Minimum | Typical | Maximum* | Unit |
|----------------------------------------|---------|---------|----------|------|
| T2: delay between RESET_IN_N and VGPIO |         | 5       |          | ms   |
| T3: delay between VGPIO and UART1_CTS  |         |         | 100      | ms   |
| T4: delay                              |         | 2 (TBC) | 7        | s    |
| T5: HW RESET delay                     | 1       |         |          | ms   |
| T6: delay between VBATT and PWR_ON_N   |         | 100     |          | ms   |
| T7: delay between VBATT and VGPIO      |         | 5       |          | ms   |
| T8: delay between PWR_ON_N and VGPIO   |         | 5       |          | ms   |
| T9: PWR_ON_N assertion time            | 25      |         | 1500     | ms   |

\* Any external capacitor or resistor added on the customer application will change these values.

## 3.12. Reset Signal (RESET\_IN\_N)

To reset the module, a low-level pulse must be sent on the RESET\_IN\_N pad for at least 1 ms. This action will immediately restart the module. During reset, all I/Os will be undefined if no external signal is driven high (if the host processor drives some I/O high, a voltage leakage will appear on VGPIO and on all GPIOs with a pull-up).

**Warning:** *It is forbidden to drive any I/Os during reset or Hibernate mode to high electrical level over 0.2V.*

*It is also forbidden to set RESET\_IN\_N low during a power recycle. VBATT must always be  $\geq 3.2V$  when reset is at low level.*

As RESET\_IN\_N is internally pulled up, an open collector or open drain transistor should be used to control this signal.

Refer to the following table for the pad description of the RESET\_IN\_N interface.

Table 31. RESET\_IN\_N Pin Description

| Pad Number | Signal Name | I/O | Description  |
|------------|-------------|-----|--------------|
| C11        | RESET_IN_N  | I   | Reset signal |

Refer to the following table for the electrical characteristics of the RESET\_IN\_N interface.

Table 32. RESET\_IN\_N Electrical Characteristics

| Parameter                 | Minimum | Typical | Maximum |
|---------------------------|---------|---------|---------|
| Input Voltage-Low (V)     |         |         | 0.3V    |
| Input Voltage-High (V)    | 1.3V    |         |         |
| Reset assertion time (ms) | 1 ms    |         |         |

**Note:** *As RESET\_IN\_N is internally pulled up, an open collector or open drain transistor must be used for ignition.*

### 3.13. Analog to Digital Converter (ADC)

*Note: This interface will be available in a future release.*

Two Analog to Digital Converter inputs, ADC0 and ADC1, are provided by AirPrime HL7802. These converters are 12-bit resolution ADCs ranging from 0 to 1.8V.

Typical ADC use is for monitoring external voltage, wherein an application is used to safely power OFF an external supply in case of overvoltage.

Refer to the following table for the pad description of the ADC interface.

Table 33. ADC Pin Description

| Pad Number | Signal Name | I/O | Description                 |
|------------|-------------|-----|-----------------------------|
| C24        | ADC1        | I   | Analog to digital converter |
| C25        | ADC0        | I   | Analog to digital converter |

Refer to the following table for the electrical characteristics of the ADC interface.

Table 34. ADC Electrical Characteristics

| Parameter                               | Minimum | Typical                  | Maximum     | Unit | Remarks                      |
|-----------------------------------------|---------|--------------------------|-------------|------|------------------------------|
| ADCx Resolution                         | 6       |                          | 12          | bits |                              |
| F <sub>CLK</sub>                        | 4       | 40                       | 52          | MHz  |                              |
| F <sub>s</sub>                          |         | F <sub>CLK</sub> / (N+3) |             | MSPS | Conversion rate per channel* |
| Input Voltage Range                     |         | 1.8                      |             | V    | General purpose input        |
| Integral Nonlinearity                   |         | ± 1.0 (TBC)              | ± 2.0 (TBC) | LSB  |                              |
| Differential Nonlinearity               | -0.9    |                          | 0.9         | LSB  |                              |
| Offset Error                            |         | ±1 (TBC)                 | ±2 (TBC)    | LSB  | % FS                         |
| Gain Error                              |         | ±1 (TBC)                 | ±2 (TBC)    | LSB  | % FS                         |
| Input Resistance                        |         | TBD                      | 0.5         | kΩ   |                              |
| Input Capacitance during sampling phase |         | 2.6                      |             | pF   |                              |

\* The general formula for this conversion rate is  $F_s = F_{CLK} / (N+3) / \text{number of sources}$ .

### 3.14. Clock Interface

*Note: This interface will be available in a future firmware release.*

The AirPrime HL7802 supports two digital clock interfaces.

Enabling or disabling the clock out feature can be done using AT commands. For more information about AT commands; refer to document [2] AirPrime HL78xx AT Commands Interface Guide.

Refer to the following table for the pad description of the clock out interfaces.

Table 35. Clock Interface Pin Description

| Pad Number | Signal Name | I/O | I/O Type | Description                    |
|------------|-------------|-----|----------|--------------------------------|
| C22        | 26M_CLKOUT  | O   | 1.8V     | 26MHz Digital Clock output     |
| C23        | 32K_CLKOUT  | O   | 1.8V     | 32.768kHz Digital Clock output |

## 3.15. PCM

*Note:* This interface will be available in a future release.

## 3.16. Debug Interfaces

The AirPrime HL7802 provides two 4-wire debug port interfaces. The CLI interface and the Modem Logs interface can be used with the AT interface for full debug capability.

### 3.16.1. Command Line Interface (CLI)

Table 36. CLI Interface Pin Description

| Pad Number | Signal Name* | I/O* | I/O Type | Description           |
|------------|--------------|------|----------|-----------------------|
| C55        | UART0_RX     | O    | 1.8V     | Debug Receive Data    |
| C56        | UART0_TX     | I    | 1.8V     | Debug Transmit Data   |
| C57        | UART0_CTS    | O    | 1.8V     | Debug Clear to Send   |
| C58        | UART0_RTS    | I    | 1.8V     | Debug Request to Send |

\* According to PC/host view.

*Note:* It is highly recommended to provide access through Test Points to this UART0 interface (required to enter in recovery mode; for example, for Flash dump).

### 3.16.2. Modem Logs interface

Table 37. Modem Logs Interface Pin Description

| Pad Number | Signal Name* | I/O* | I/O Type | Description |
|------------|--------------|------|----------|-------------|
| C51        | GPIO14       | O    | 1.8V     | UART3_CTS   |
| C52        | GPIO10       | I    | 1.8V     | UART3_TX    |
| C53        | GPIO11       | I    | 1.8V     | UART3_RTS   |
| C54        | GPIO15       | O    | 1.8V     | UART3_RX    |

\* According to PC/host view.

*Note:* If there are no constraints on GPIO use, it is highly recommended to provide access through Test Points to these 4 GPIOs to access to the UART3 interface (required to debug modem logs).

## 3.17. Wake Up Signal (WAKE\_UP)

The AirPrime HL7802 provides one WAKE\_UP signal.

The WAKE\_UP pin is used to wake up the system from low power modes (from OFF, Sleep modes, FAST\_SHUTDOWN, or after a software power off). This signal should be set to high level (external 1.8V) until the system is active to wake the module up from these modes.

The system will not be allowed to go into low power or off mode for as long as this signal is kept high.

By default, the software waits for a high state to wake up (100KΩ internal pull-down).

Refer to the following table for the pad description of the WAKE\_UP signal.

Table 38. WAKE\_UP Pin Description

| Pad Number | Signal Name | I/O | I/O Type | Description                             |
|------------|-------------|-----|----------|-----------------------------------------|
| C44        | WAKE_UP     | I   | 1.8V     | Wakes the module up from low power mode |

Refer to the following table for the electrical characteristics of the WAKE\_UP signal.

Table 39. WAKE\_UP Electrical Characteristics

| I/O Type | Parameter       | Minimum | Typical | Maximum | Unit |
|----------|-----------------|---------|---------|---------|------|
| Digital  | V <sub>IL</sub> |         |         | 0.3     | V    |
|          | V <sub>IH</sub> | 1.2     |         |         | V    |

## 3.18. Fast Shutdown Signal (FAST\_SHUTDOWN\_N)

*Note: This signal will be available in a future firmware release.*

The AirPrime HL7802 provides one Fast Shutdown signal, FAST\_SHUTDOWN\_N.

Refer to the following table for the pad description.

Table 40. FAST\_SHUTDOWN\_N Pin Description

| Pad Number | Signal Name     | I/O | I/O Type | Description                                                   |
|------------|-----------------|-----|----------|---------------------------------------------------------------|
| C65        | FAST_SHUTDOWN_N | I   | 1.8V     | Shuts the module down without deregistration from the network |

Refer to the following table for the electrical characteristics of the FAST\_SHUTDOWN\_N signal.

Table 41. FAST\_SHUTDOWN\_N Electrical Characteristics

| I/O Type | Parameter       | Minimum     | Typical | Maximum   | Unit |
|----------|-----------------|-------------|---------|-----------|------|
| Digital  | V <sub>IL</sub> |             |         | 0.3xVGPIO | V    |
|          | V <sub>IH</sub> | 0.7 x VGPIO |         |           | V    |

\* VGPIO typical = 1.8 V.

## 3.19. RF Interface

The RF interface of the AirPrime HL7802 allows the transmission of RF signals.

Contact Sierra Wireless technical support for assistance in integrating the AirPrime HL7802 on applications with embedded antennas.

### 3.19.1. RF Connection

A 50Ω (with maximum VSWR 1.1:1, and 0.5dB loss) RF track is recommended to be connected to standard RF connectors such as SMA, UFL, etc. for antenna connection.

Refer to the following table for the pad description of the RF interface.

Table 42. RF Main Pin Description

| Pad Number | RF Signal | Impedance | VSWR Rx (max) | VSWR Tx (max) |
|------------|-----------|-----------|---------------|---------------|
| C48        | GND       |           |               |               |
| C49        | RF_MAIN   | 50Ω       | 2.5:1         | 2.5:1         |
| C50        | GND       |           |               |               |

### 3.19.2. LTE RF Interface

#### 3.19.2.1. Maximum Output Power

The maximum transmitter output power of the AirPrime HL7802 for all bands in normal operation conditions (25°C) is specified in the following table.

Table 43. Maximum Output Power

| Minimum | Typical | Maximum | Units | Notes         |
|---------|---------|---------|-------|---------------|
| 21.5    | 23      | 24.5    | dBm   | Power class 3 |

#### 3.19.2.2. Rx Sensitivity

The module's receiver sensitivity is specified in the following table. The test condition used for the following values are those defined in 3GPP TS36.521v13, as follows:

- Cat-M1: BW of 5 MHz, on Reference Measurement Channel
- NB1: on DL Reference Measurement Channel defined

Table 44. Typical Conducted Cat-M1 RX Sensitivity (TBC)

| LTE Band | Typical Reference Sensitivity Level @ 95% of the Maximum Throughput |                |                  |
|----------|---------------------------------------------------------------------|----------------|------------------|
|          | @+25°C (dBm)                                                        | @Class A (dBm) | 3GPP Limit (dBm) |
| B1       | -104                                                                | -102.5         | -102.3           |



| LTE Band | Typical Reference Sensitivity Level @ 95% of the Maximum Throughput |                |                  |
|----------|---------------------------------------------------------------------|----------------|------------------|
|          | @+25°C (dBm)                                                        | @Class A (dBm) | 3GPP Limit (dBm) |
| B2       | -104                                                                | -103           | -100.3           |
| B3       | -105                                                                | -103.5         | -99.3            |
| B4       | -104                                                                | -102.5         | -102.3           |
| B5       | -105                                                                | -104           | -100.8           |
| B8       | -105                                                                | -103           | -99.8            |
| B9       | -105                                                                | -103.5         |                  |
| B10      | -104                                                                | -102.5         |                  |
| B12      | -105                                                                | -103.5         | -99.3            |
| B13      | -105                                                                | -104           | -99.3            |
| B14      | -105                                                                | -104           |                  |
| B17      | -105                                                                | -103.5         |                  |
| B18      | -105                                                                | -104           | -100.3           |
| B19      | -105                                                                | -104           | -102.3           |
| B20      | -105                                                                | -104           | -99.8            |
| B25      | -105                                                                | -103           |                  |
| B26      | -105                                                                | -104.5         | -100.3           |
| B27      | -105                                                                | -104.5         | -100.8           |
| B28      | -105                                                                | -104           | -100.8           |
| B66      | -104                                                                | -102.5         |                  |

Table 45. Typical Conducted NB1 RX Sensitivity (TBC)

| LTE Band | Typical Reference Sensitivity Level @ 95% of the Maximum Throughput |                |                  |
|----------|---------------------------------------------------------------------|----------------|------------------|
|          | @+25°C (dBm)                                                        | @Class A (dBm) | 3GPP Limit (dBm) |
| B1       | -113                                                                | -111.5         | -107.5           |
| B2       | -113.5                                                              | -112.1         | -107.5           |
| B3       | -114                                                                | -112.5         | -107.5           |
| B4       | -113                                                                | -111.6         | -107.5           |
| B5       | -113.5                                                              | -112.3         | -107.5           |
| B8       | -113                                                                | -111.8         | -107.5           |
| B9       | NA                                                                  | NA             | NA               |
| B10      | NA                                                                  | NA             | NA               |
| B12      | -112.5                                                              | -111.2         | -107.5           |
| B13      | -113                                                                | -111.8         | -107.5           |
| B14      | -112.5                                                              | -111.3         | -107.5           |
| B17      | -113                                                                | -111.7         | -107.5           |
| B18      | -113.5                                                              | -112.2         | -107.5           |
| B19      | -113.5                                                              | -112.2         | -107.5           |
| B20      | -113                                                                | -111.7         | -107.5           |
| B25      | -113                                                                | -111.7         | -107.5           |
| B26      | -113.8                                                              | -112.5         | -107.5           |

| LTE Band | Typical Reference Sensitivity Level @ 95% of the Maximum Throughput |                |                  |
|----------|---------------------------------------------------------------------|----------------|------------------|
|          | @+25°C (dBm)                                                        | @Class A (dBm) | 3GPP Limit (dBm) |
| B27      | NA                                                                  | NA             | NA               |
| B28      | -113                                                                | -111.7         | -107.5           |
| B66      | -113                                                                | -111.5         | -107.5           |

### 3.19.3. 2G RF Interface

The HL7802 module is a GPRS only device (no EGPRS support) supporting GSM multislot class 10 (4 DL/2UL max (5 slots)).

#### 3.19.3.1. Tx Output Power

The module's 2G maximum transmitter output power is specified in the following table.

Table 46. Conducted Tx Max Output Power Tolerances – 2G<sup>a,b</sup>

| RF Band   | Minimum | Typical | Maximum | Units | Notes                            |
|-----------|---------|---------|---------|-------|----------------------------------|
| GSM 850   | 31.5    | 32.5    | 33.5    | dBm   | GMSK mode (Class 4; 2 W, 33 dBm) |
| E-GSM 900 | 31.5    | 32.5    | 33.5    | dBm   | GMSK mode (Class 4; 2 W, 33 dBm) |
| DCS 1800  | 28.5    | 29.5    | 30.5    | dBm   | GMSK mode (Class 1; 1 W, 30 dBm) |
| PCS 1900  | 28.5    | 29.5    | 30.5    | dBm   | GMSK mode (Class 1; 1 W, 30 dBm) |

a Stated power tolerances satisfy 3GPP TS 51.010-1 requirements for normal (25°C) and Class A (extreme) conditions.

b Stated power tolerances for input voltage of 3.7V.

#### 3.19.3.2. Rx Sensitivity

The module's GPRS receiver sensitivity is specified in the following table.

Table 47. Conducted Rx Sensitivity – GPRS Bands<sup>a</sup>

| Bands    | Parameters |          | Sensitivity @ +25°C (dBm) <sup>b</sup> | Sensitivity @ Class A (dBm) <sup>c</sup> | Standard Limit (dBm) |
|----------|------------|----------|----------------------------------------|------------------------------------------|----------------------|
| GSM 850  | 10% BLER   | GMSK CS1 | -110                                   | -108                                     | -102                 |
| EGSM 900 | 10% BLER   | GMSK CS1 | -111                                   | -108                                     | -102                 |
| DCS 1800 | 10% BLER   | GMSK CS1 | -112                                   | -108                                     | -102                 |
| PCS 1900 | 10% BLER   | GMSK CS1 | -112                                   | -108                                     | -102                 |

a Stated sensitivity values satisfy 3GPP TS 51.010-1 requirements for normal (25°C) and Class A (extreme) conditions.

b Typical value.

c Typical value, tested at Class A extreme conditions.

### 3.20. TX Burst Indicator (TX\_ON)

*Note: This signal will be available in a future firmware release.*

The AirPrime HL7802 provides a signal, TX\_ON, for TX emission indication.

Table 48. TX\_ON Pin Description

| Pad Number | Signal Name | I/O | I/O Type | Description                                      |
|------------|-------------|-----|----------|--------------------------------------------------|
| C60        | TX_ON       | O   | 1.8V     | High during TX emission, low when there is no TX |

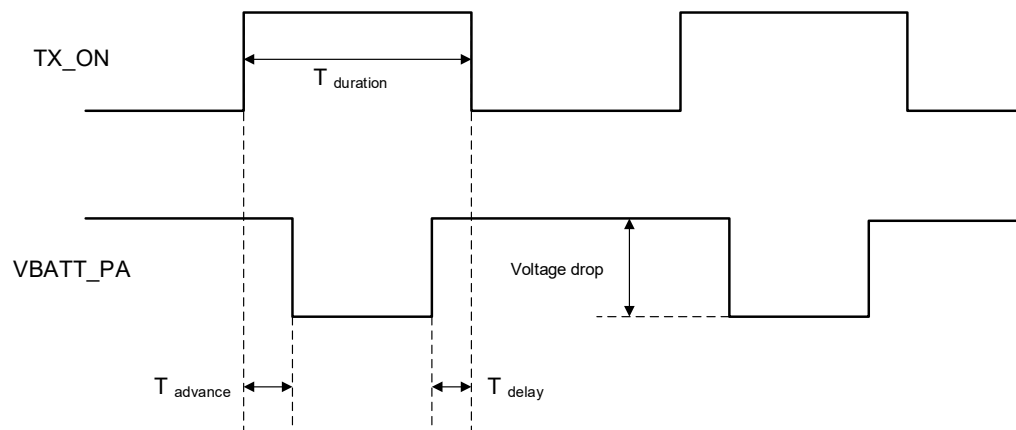


Figure 17. TX\_ON State during TX Burst

During TX burst, there is a higher current drain from the VBATT\_PA power supply which causes a voltage drop. This voltage drop from VBATT\_PA is a good indication of a high current drain situation during TX burst.

The blinking frequency is about 217Hz.

The output logic high duration, T<sub>duration</sub>, depends on the number of TX slots and is computed as follows:

$$T_{duration} = T_{advance} + (0.577ms \times \text{number of TX slots}) + T_{delay}$$

Table 49. TX\_ON Characteristics

| Parameter            | Typical     |
|----------------------|-------------|
| T <sub>advance</sub> | 30 μs (TBC) |
| T <sub>delay</sub>   | 10 μs (TBC) |

### 3.21. External RF Voltage Control Indicator

*Note: This signal will be available in a future firmware release.*

The AirPrime HL7802 provides a signal, VBATT\_PA\_EN, for RF activity indication. VBATT\_PA\_EN is used to drive an external LDO or DCDC that provides VBATT\_PA power supply. It is recommended to add an external 470kΩ PD to keep the I/O in a defined state during Hibernate mode.

Table 50. VBATT\_PA\_EN Pin Description

| Pad Number | Signal Name         | I/O | I/O Type | Description                                                        |
|------------|---------------------|-----|----------|--------------------------------------------------------------------|
| C41        | GPIO8 / VBATT_PA_EN | O   | 1.8V     | High when VBATT_PA is supplied, low if no power supply is required |

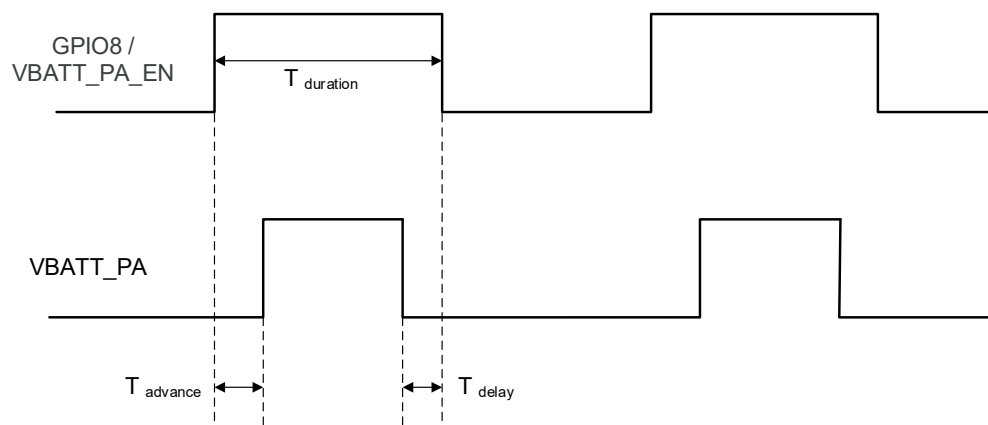


Figure 18. VBATT\_PA\_EN State during RX/TX Windows

Table 51. VBATT\_PA\_EN Characteristics

| Parameter            | Typical      |
|----------------------|--------------|
| T <sub>advance</sub> | 400 μs (TBC) |
| T <sub>delay</sub>   | 400 μs (TBC) |

## 3.22. GNSS Interface

The AirPrime HL7802's GPS supports GPS L1 signal ( $1575.42 \pm 20$  MHz) and GLONASS L1 FDMA signals (1597.5 – 1605.8 MHz), with 50 $\Omega$  connection on the RF\_GPS pad.

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*Note:* The GPS receiver shares the same RF resources as the 4G receiver. The end-device target should allow GPS positioning for asset management applications where infrequent and no real-time position updates are required.

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GPS antenna interface specifications are defined in the table below. Note that the HL7802 does not support an active GPS/GNSS antenna.

Table 52. GPS Antenna Specifications

| Characteristics           |        | Value            |
|---------------------------|--------|------------------|
| Frequency (MHz)           | GPS L1 | $1575.42 \pm 20$ |
| RF Impedance ( $\Omega$ ) |        | 50               |
| VSWR max                  |        | 2:1              |

### 3.22.1. GPS Performance

Refer to the following table for GPS performance details.

Table 53. GPS Performance

| Parameters        | Conditions                      | Typical Value |
|-------------------|---------------------------------|---------------|
| Sensitivity       | Cold Start                      | -146dBm (TBC) |
|                   | Hot Start                       | -152dBm (TBC) |
|                   | Tracking                        | -161dBm (TBC) |
| TTFF              | Cold start, Input power -130dBm | 35s (TBC)     |
|                   | Hot start, Input power -130dBm  | 2s (TBC)      |
| 2D Position Error | Input power -130dBm             | 2.5m (TBC)    |

### 3.22.2. GPS Antenna Indicator (EXT\_LNA\_GPS\_EN)

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*Note:* This signal will be available in a future firmware release.

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# 4. Mechanical Drawings

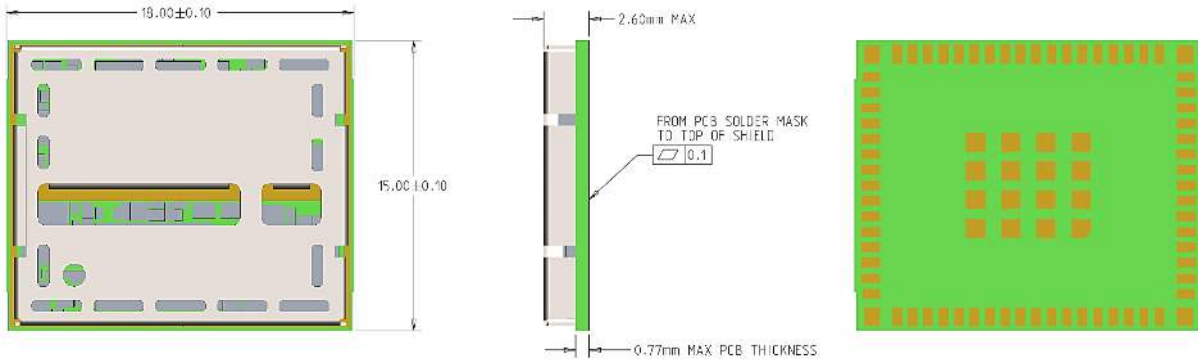


Figure 19. Mechanical Drawing

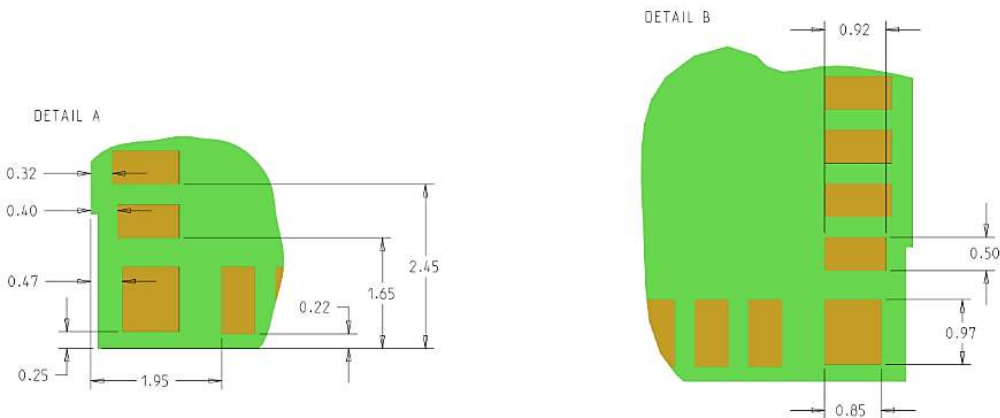
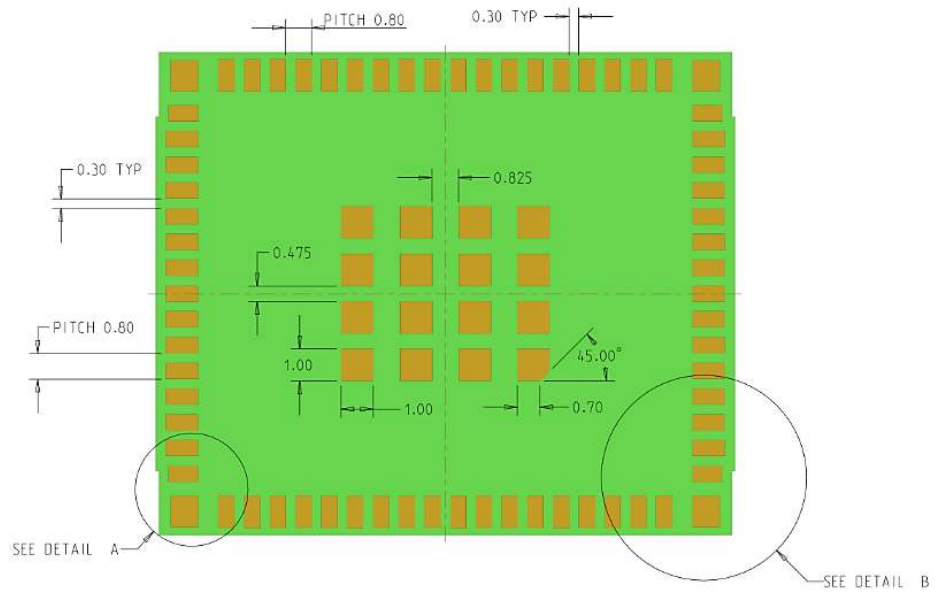


Figure 20. Dimensions Drawing

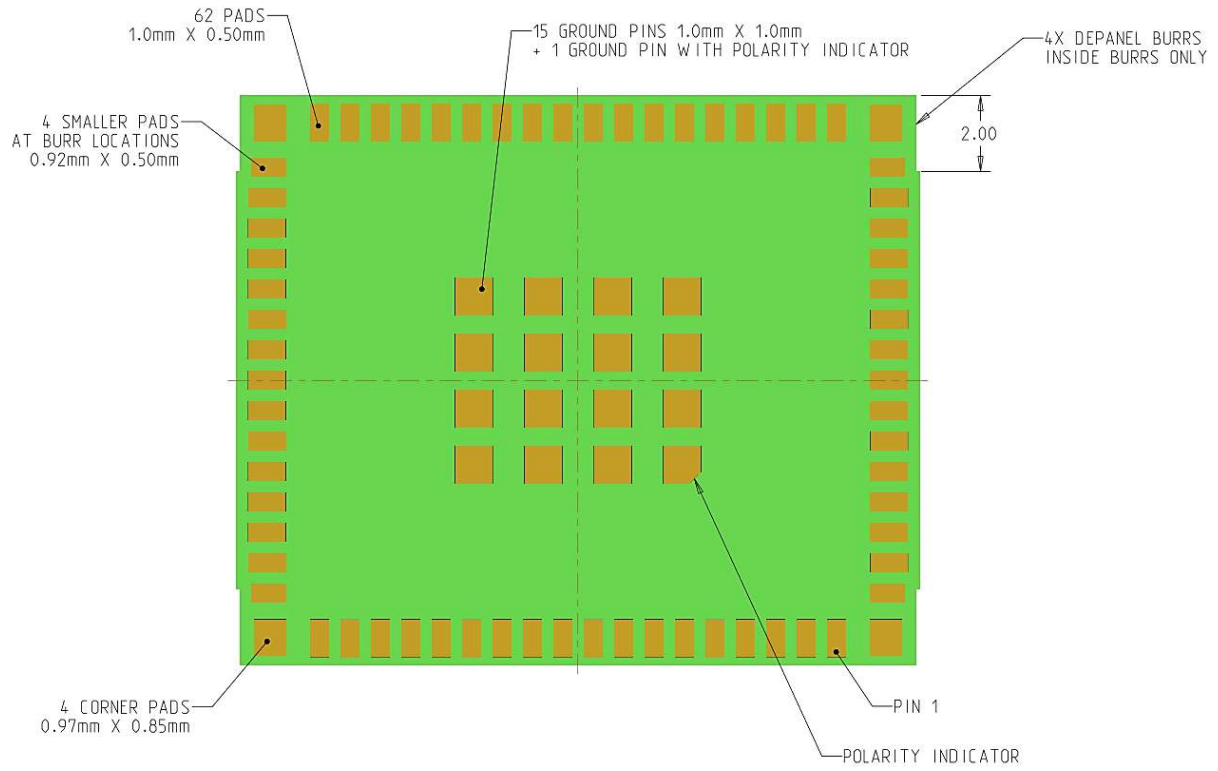


Figure 21. Footprint Drawing

## 5. Design Guidelines

### 5.1. Power Supply Design

The AirPrime HL7802 should not be supplied with voltage over 4.35V, even temporarily or however briefly.

If the system's main board power supply unit is unstable or supplied with voltage over 4.35V, even in the case of transient voltage presence on the circuit, the module's power amplifier may be severely damaged.

To avoid such issues, add a voltage limiter to the module's power supply lines so that VBATT and VBATT\_PA signal pads will never receive a voltage surge over 4.35V. The voltage limiter can be as simple as a Zener diode.

### 5.2. Power Cycle

In addition to Sierra Wireless' reliable recovery mechanisms, it is highly recommended that the ability for a power cycle to reboot the module be included in the design in case the module becomes blocked and stops responding to reset commands.

### 5.3. ESD Guidelines for USIM

Decoupling capacitors must be added according to the drawings below as close as possible to the USIM connectors on UIM1\_CLK, UIM1\_RST, UIM1\_VCC, UIM1\_DATA and UIM1\_DET signals to avoid EMC issues and to comply with the requirements of ETSI and 3GPP standards covering the USIM electrical interface.

A typical schematic including USIM detection is provided below.



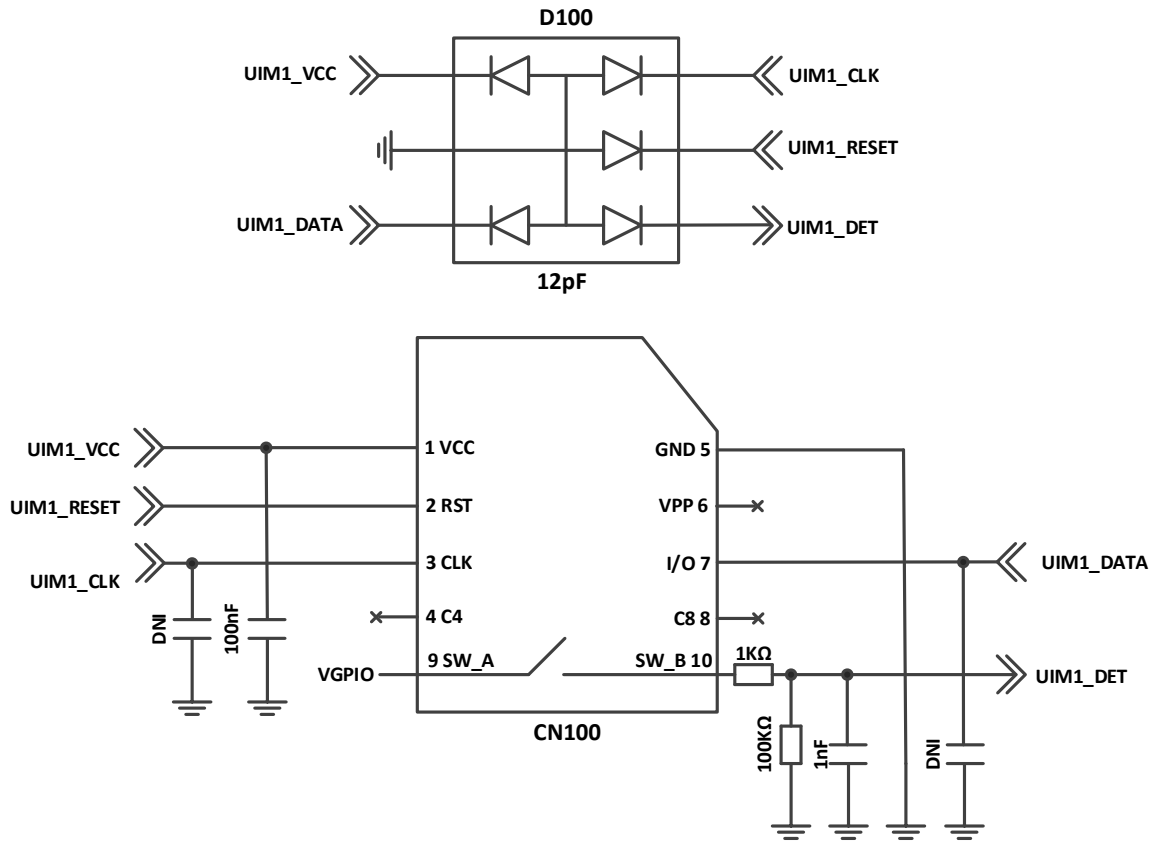


Figure 22. EMC and ESD Components Close to the USIM

Sierra Wireless recommends using diode ESDALC6V1-5P6 ESD for D100.

## 5.4. ESD Guidelines for USB (TBC)

When the USB interface is externally accessible, it is required to have ESD protection on the USB\_VBUS, USB\_D+ and USB\_D- signals.

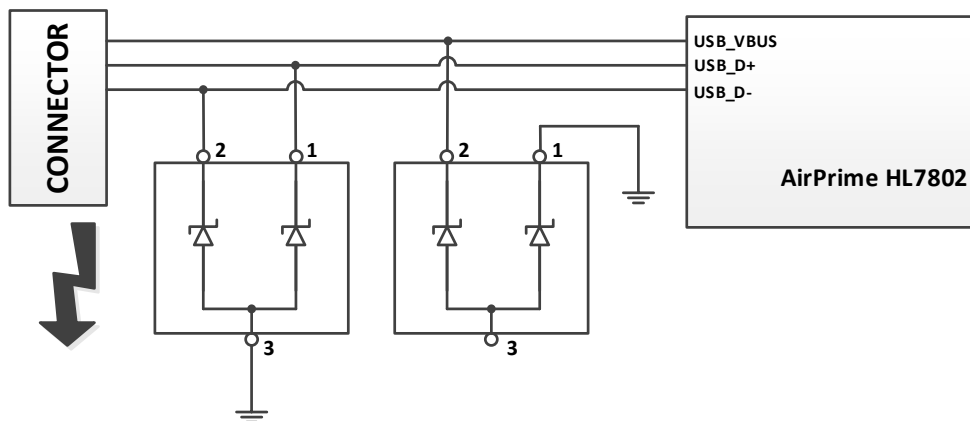


Figure 23. ESD Protection for USB

Note: It is not recommended to have an ESD diode with feedback path from USB\_VBUS to either USB\_D+ or USB\_D-.

Sierra Wireless recommends using ESD diode RCLAMP0503N or ESD5V3U2U-03LRH.

## 5.5. Radio Frequency Integration

The AirPrime HL7802 is equipped with an external antenna. A 50Ω line matching circuit between the module, the customer’s board and the RF antenna is required as shown in the example below.

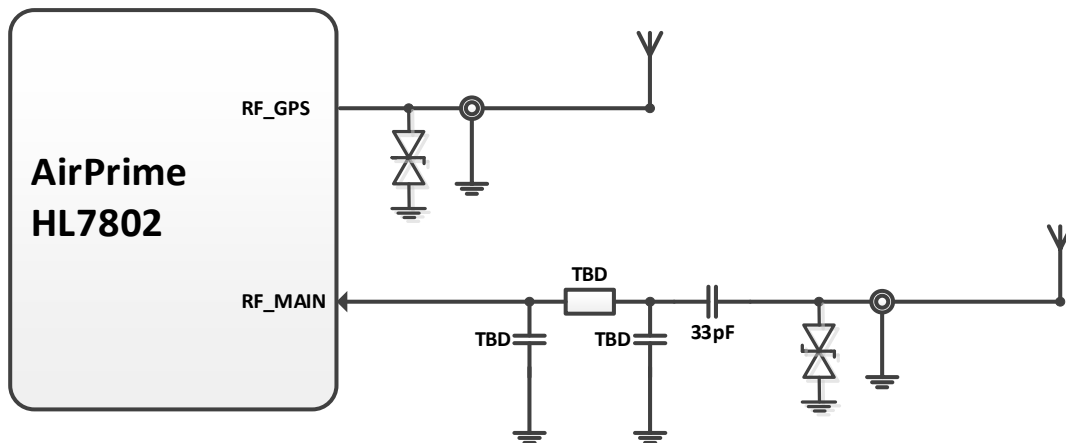


Figure 24. Antenna Connection

Sierra Wireless recommends using ESD diode ESD103-B1-02EL E6327 for RF\_MAIN and ESD8011MUT5G for RF\_GPS.

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**Note:** The (optional) antenna detection circuit will be available in a future release.

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## 6. Reliability Specification (TBC)

The AirPrime HL7802 will be tested against the Sierra Wireless Industrial Reliability Specification defined below.

### 6.1. Preconditioning Test


Per JESD22A113, this test the preconditioning of non-hermetic surface mount devices prior to reliability testing.

Table 54. Preconditioning Test

| Designation                  | Condition                           |
|------------------------------|-------------------------------------|
| Preconditioning Test<br>PCRM | 2 reflow cycles with Tmax 245-250°C |



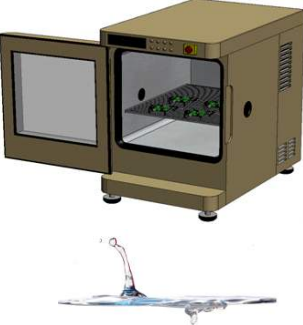
### 6.2. Performance Test

Table 55. Performance Test

| Designation                                                                                                            | Condition                                                                                                                                                                                                                                                                                             |
|------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Performance Test<br>PT3T & PTRT<br> | Standard: N/A                                                                                                                                                                                                                                                                                         |
|                                                                                                                        | Special conditions: <ul style="list-style-type: none"> <li>• Temperature:               <ul style="list-style-type: none"> <li>▪ Class A: -30°C to +70°C</li> <li>▪ Class B: -40°C to +85°C</li> <li>▪ Rate of temperature change: ± 3°C/min</li> </ul> </li> <li>• Recovery time: 3 hours</li> </ul> |
|                                                                                                                        | Operating conditions: Powered                                                                                                                                                                                                                                                                         |
|                                                                                                                        | Duration: 14 days                                                                                                                                                                                                                                                                                     |



### 6.3. Aging Tests

Table 56. Aging Tests

| Designation                                                                                                                                   | Condition                                                                                                                                                                                                                                                                                                                              |
|-----------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <p><b>High Temperature Operating Life test</b><br/>HTOL</p>  | <p>Standard: IEC 680068-2-2, Test Bb</p> <p>Special conditions:</p> <ul style="list-style-type: none"> <li>• Temperature: +85°C</li> <li>• Temperature variation: 1°C/min</li> </ul> <p>Operating conditions: Powered ON with a power cycle of 45 minutes ON and 15 minutes Idle</p> <p>Duration: 20 days</p>                          |
| <p><b>Thermal Shock Test</b><br/>TSKT</p>                   | <p>Standard: IEC 60068-2-14, Test Na</p> <p>Special conditions:</p> <ul style="list-style-type: none"> <li>• Temperature: -40°C to +85°C</li> <li>• Temperature Variation: less than 30s</li> <li>• Number of cycles: 300</li> <li>• Dwell Time: 10 minutes</li> </ul> <p>Operating conditions: Un-powered</p> <p>Duration: 7 days</p> |
| <p><b>Humidity Test</b><br/>HUT</p>                        | <p>Standard: IEC 60068-2-3, Test Ca</p> <p>Special conditions:</p> <ul style="list-style-type: none"> <li>• Temperature: +85°C</li> <li>• RH: 85%</li> </ul> <p>Operating conditions: Powered on, DUT is powered up for 15 minutes and OFF for 15 minutes</p> <p>Duration: 10 days</p>                                                 |

## 6.4. Characterization Tests

Table 57. Characterization Tests

| Designation                                                                                                                             | Condition                                                                                                                                                              |
|-----------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Low Temperature and Cold Start Cycles</b><br><b>LTCS</b>                                                                             | Special conditions: <ul style="list-style-type: none"> <li>• Temperature: -40°C</li> <li>• AT commands read or write memory</li> </ul>                                 |
|                                                                                                                                         | Operating conditions: 5 mins powered ON, 30 mins powered OFF (1 power cycle)                                                                                           |
|                                                                                                                                         | Duration: 5 days                                                                                                                                                       |
| <b>Component Solder Wettability</b><br><b>CSW</b><br>  | Standard: JESD22 – B102, Method 1/Condition C, Solderability Test Method                                                                                               |
|                                                                                                                                         | Special conditions: <ul style="list-style-type: none"> <li>• Test method: Surface mount process simulation test (preconditioning 16 h ±30 minutes dry bake)</li> </ul> |
|                                                                                                                                         | Operating conditions: Un-powered                                                                                                                                       |
|                                                                                                                                         | Duration: 1 day                                                                                                                                                        |
| <b>Unprotected Free Fall Test</b><br><b>FFT 1</b><br> | Standard: IEC 60068-2-32, Test Ed                                                                                                                                      |
|                                                                                                                                         | Special conditions: <ul style="list-style-type: none"> <li>• Number of drops: 6 drops per unit (1 drop per direction: ±X, ±Y, ±Z)</li> <li>• Height: 1m</li> </ul>     |
|                                                                                                                                         | Operating conditions: Un-powered                                                                                                                                       |
|                                                                                                                                         | Duration: 1 day                                                                                                                                                        |

## 7. Ordering Information

Table 58. Ordering Information

| Model Name | Description            | Part Number                                |
|------------|------------------------|--------------------------------------------|
| HL7802     | HL7802 embedded module | Contact Sierra Wireless for the latest SKU |
| DEV-KIT    | HL780x Development Kit | 6001210                                    |



## 8. Terms and Abbreviations

| Abbreviation | Definition                                      |
|--------------|-------------------------------------------------|
| ADC          | Analog to Digital Converter                     |
| AGC          | Automatic Gain Control                          |
| AT           | Attention (prefix for modem commands)           |
| CDMA         | Code Division Multiple Access                   |
| CF3          | Common Flexible Form Factor                     |
| CLK          | Clock                                           |
| CODEC        | Coder Decoder                                   |
| CPU          | Central Processing Unit                         |
| DAC          | Digital to Analog Converter                     |
| DTR          | Data Terminal Ready                             |
| DRX          | Discontinuous Reception                         |
| eDRX         | Extended DRX                                    |
| EMC          | Electro-Magnetic Compatibility                  |
| EMI          | Electro-Magnetic Interference                   |
| EN           | Enable                                          |
| ESD          | Electro-Static Discharges                       |
| ETSI         | European Telecommunications Standards Institute |
| FDMA         | Frequency-division multiple access              |
| GLONASS      | Global Navigation Satellite System              |
| GND          | Ground                                          |
| GNSS         | Global Navigation Satellite System              |
| GPIO         | General Purpose Input Output                    |
| GPRS         | General Packet Radio Service                    |
| GPS          | Global Positioning System                       |
| GSM          | Global System for Mobile communications         |
| Hi Z         | High impedance (Z)                              |
| IC           | Integrated Circuit                              |
| IMEI         | International Mobile Equipment Identification   |
| I/O          | Input / Output                                  |
| LED          | Light Emitting Diode                            |
| LNA          | Low Noise Amplifier                             |
| MAX          | Maximum                                         |
| MIN          | Minimum                                         |
| N/A          | Not Applicable                                  |
| PA           | Power Amplifier                                 |
| PC           | Personal Computer                               |
| PCB          | Printed Circuit Board                           |
| PCL          | Power Control Level                             |
| PLL          | Phase Lock Loop                                 |
| PSM          | Power Save Mode                                 |
| PSRAM        | Pseudo Static RAM                               |

| <b>Abbreviation</b> | <b>Definition</b>                              |
|---------------------|------------------------------------------------|
| PSU                 | Power Supply Unit                              |
| PTW                 | Paging Transmission Window                     |
| PWM                 | Pulse Width Modulation                         |
| RF                  | Radio Frequency                                |
| RFI                 | Radio Frequency Interference                   |
| RMS                 | Root Mean Square                               |
| RST                 | Reset                                          |
| RTC                 | Real Time Clock                                |
| RX                  | Receive                                        |
| SCL                 | Serial Clock                                   |
| SDA                 | Serial Data                                    |
| SIM                 | Subscriber Identification Module               |
| SMD                 | Surface Mounted Device/Design                  |
| SPI                 | Serial Peripheral Interface                    |
| SW                  | Software                                       |
| TAU                 | Tracking Area Update                           |
| TBC                 | To Be Confirmed                                |
| TBD                 | To Be Defined                                  |
| TP                  | Test Point                                     |
| TX                  | Transmit                                       |
| TYP                 | Typical                                        |
| UART                | Universal Asynchronous Receiver-Transmitter    |
| UICC                | Universal Integrated Circuit Card              |
| USB                 | Universal Serial Bus                           |
| UIM                 | User Identity Module                           |
| VBATT               | Main Supply Voltage from Battery or DC adapter |
| VSWR                | Voltage Standing Wave Ratio                    |