X9119

1024 Tap, Low Power, 2-Wire Interface, Digitally Controlled (XDCP™) Potentiometer

FN8162
Rev 5.00
July 5, 2016

The X9119 integrates a single digitally controlled potentiometer (XDCP™) on a monolithic CMOS integrated circuit.

The digital controlled potentiometer is implemented using 1023 resistive elements in a series array. Between each element are tap points connected to the wiper terminal through switches. The position of the wiper on the array is controlled by the user through the 2-wire bus interface. The potentiometer has associated with it a volatile Wiper Counter Register (WCR) and four nonvolatile data registers that can be directly written to and read by the user. The contents of the WCR controls the position of the wiper on the resistor array through the switches. Power-up recalls the contents of the default data register (DR0) to the WCR.

The XDCP™ can be used as a 3-terminal potentiometer or as a 2-terminal variable resistor in a wide variety of applications including control, parameter adjustments and signal processing.

Features

- 1024 resistor taps – 10-bit resolution
- 2-Wire serial interface for write, read, and transfer operations of the potentiometer
- Wiper resistance, 40Ω typical at V_{CC} = 5V
- Four nonvolatile data registers
- Nonvolatile storage of multiple wiper positions
- Power-on recall, loads saved wiper position on power-up.
- Standby current <3µA maximum
- V_{CC}: 2.7V to 5.5V operation
- 100kΩ end-to-end resistance
- 100 yr. data retention
- Endurance: 100,000 data changes per bit per register
- 14 Ld TSSOP
- Low power CMOS
- Single supply version of the X9118
- Pb-free available (RoHS compliant)

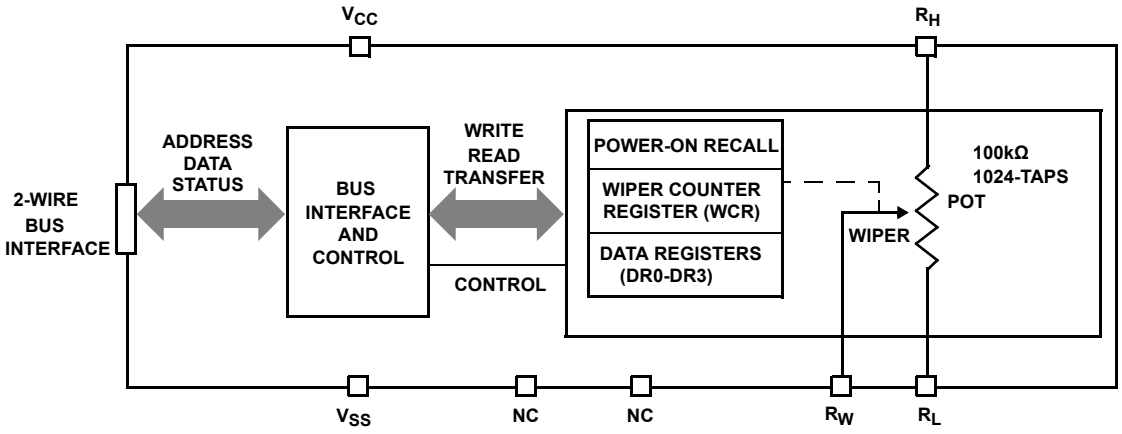


FIGURE 1. FUNCTIONAL DIAGRAM

Applications

Circuit Level

- Vary the gain of a voltage amplifier
- Provide programmable DC reference voltages for comparators and detectors
- Control the volume in audio circuits
- Trim out the offset voltage error in a voltage amplifier circuit
- Set the output voltage of a voltage regulator
- Trim the resistance in Wheatstone bridge circuits
- Control the gain, characteristic frequency and Q-factor in filter circuits
- Set the scale factor and zero point in sensor signal conditioning circuits
- Vary the frequency and duty cycle of timer ICs
- Vary the DC biasing of a pin diode attenuator in RF circuits
- Provide a control variable (I, V, or R) in feedback circuits

System Level

- Adjust the contrast in LCD displays
- Control the power level of LED transmitters in communication systems
- Set and regulate the DC biasing point in an RF power amplifier in wireless systems
- Control the gain in audio and home entertainment systems
- Provide the variable DC bias for tuners in RF wireless systems
- Set the operating points in temperature control systems
- Control the operating point for sensors in industrial systems
- Trim offset and gain errors in artificial intelligent systems

Ordering Information

PART NUMBER (Notes 2, 3)	PART MARKING	V_{CC} LIMITS (V)	POTENTIOMETER ORGANIZATION (kΩ)	TEMP RANGE (°C)	PACKAGE RoHS COMPLIANT	PKG. DWG.#
X9119TV14IZ	X9119 TVZI	5 ±10%	100	-40 to +85	14 Ld TSSOP (4.4mm)	M14.173
X9119TV14Z	X9119 TVZ			0 to +70	14 Ld TSSOP (4.4mm)	M14.173
X9119TV14Z-2.7	X9119 TVZF	2.7 to 5.5		0 to +70	14 Ld TSSOP (4.4mm)	M14.173
X9119TV14IZ-2.7 (Note 1)	X9119 TVZG			-40 to +85	14 Ld TSSOP (4.4mm)	M14.173

NOTES:

1. Add “T1” suffix for 2.5k unit tape and reel option.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see product information page for X9119. For more information on MSL, please see tech brief TB363.

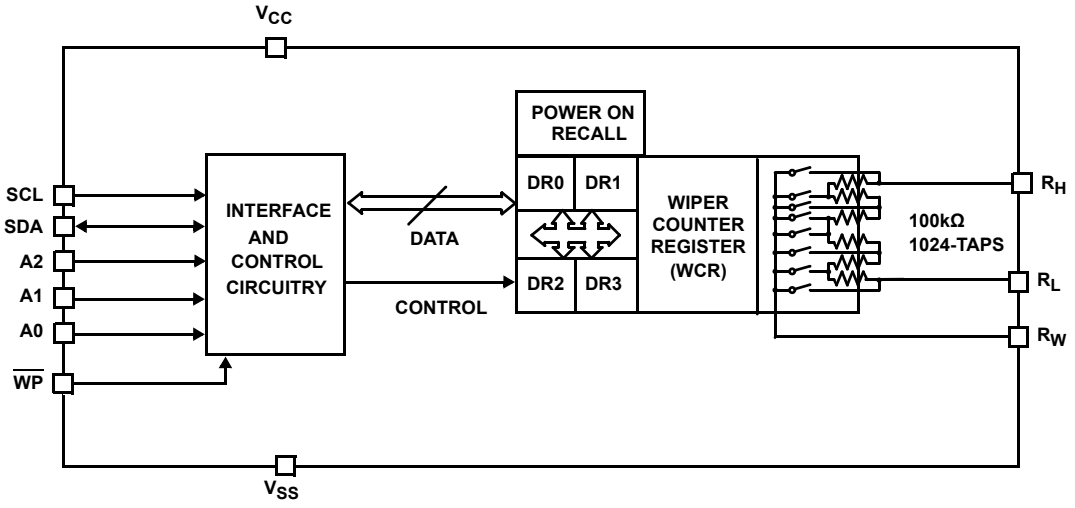
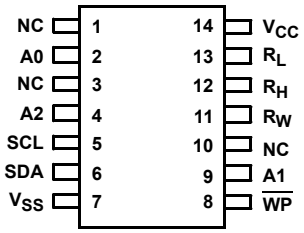


FIGURE 2. DETAILED FUNCTIONAL DIAGRAM

Pin Configuration

X9119
(14 LD TSSOP)
TOP VIEW



Pin Assignments

PIN NUMBER	PIN NAME	FUNCTION
1, 3, 10	NC	No connect
2	A0	Device address for 2-wire bus
4	A2	Device address for 2-wire bus
5	SCL	Serial clock for 2-wire bus
6	SDA	Serial data input/output for 2-wire bus
7	V_{SS}	System ground
8	$\overline{WP}$	Hardware write protect
9	A1	Device address for 2-wire bus
11	R_W	Wiper terminal of the potentiometer
12	R_H	High terminal of the potentiometer
13	R_L	Low terminal of the potentiometer
14	V_{CC}	System supply voltage

Bus Interface Pins

SERIAL DATA INPUT/OUTPUT (SDA)

The SDA is a bidirectional serial data input/output pin for a 2-wire slave device and is used to transfer data into and out of the device. It receives device address, opcode, wiper register address and data sent from a 2-wire master at the rising edge of the serial clock SCL, and it shifts out data after each falling edge of the serial clock SCL.

It is an open-drain output and may be wire-ORed with any number of open-drain or open collector outputs. An open-drain output requires the use of a pull-up resistor. For selecting typical values, refer to the guidelines for calculating typical values on the bus pull-up resistors graph.

SERIAL CLOCK (SCL)

This input is used by a 2-wire master to supply a 2-wire serial clock to the X9119.

DEVICE ADDRESS (A_2–A_0)

The Address inputs are used to set the least significant 3 bits of the 8-bit slave address. A match in the slave address serial data stream must be made with the Address input in order to initiate communication with the X9119. A maximum of 8 devices may occupy the 2-wire serial bus.

HARDWARE WRITE PROTECT INPUT ($\overline{WP}$)

The $\overline{WP}$ pin when LOW, prevents nonvolatile writes to the Data Registers.

Potentiometer Pins

R_H, R_L

The R_H and R_L pins are equivalent to the terminal connections on a mechanical potentiometer.

R_W

The wiper pin are equivalent to the wiper terminal of a mechanical potentiometer.

Bias Supply Pins

SYSTEM SUPPLY VOLTAGE (V_{CC}) AND SUPPLY GROUND (V_{SS})

The V_{CC} pin is the system supply voltage. The V_{SS} pin is the system ground.

Other Pins

NO CONNECT

No connect pins should be left open. These pins are used for Intersil manufacturing and testing purposes.

Principals of Operation

The X9119 is an integrated microcircuit incorporating a resistor array and its associated registers and counters and the serial interface logic providing direct communication between the host and the digitally controlled potentiometer. This section provides detail description of the following:

- Resistor Array Description
- Serial Interface Description
- Instruction and Register Description

Resistor Array Description

The X9119 is comprised of a resistor array. The array contains, in effect, 1023 discrete resistive segments that are connected in series (Figure 3 on page 4). The physical ends of each array are equivalent to the fixed terminals of a mechanical potentiometer (R_H and R_L inputs).

At both ends of each array and between each resistor segment is a CMOS switch connected to the wiper (R_W) output. Within each individual array only one switch may be turned on at a time. These switches are controlled by the Wiper Counter Register (WCR). The 10-bits of the WCR (WCR[9:0]) are decoded to select, and enable, one of 1024 switches.

The WCR may be written directly. The data registers and the WCR can be read and written by the host system.

Serial Interface Description

SERIAL INTERFACE

The X9119 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the X9119 will be considered a slave device in all applications.

CLOCK AND DATA CONVENTIONS

Data states on the SDA line can change only during SCL LOW periods. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions (Figure 6 on page 8).

START CONDITION

All commands to the X9119 are preceded by the start condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The X9119 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition is met (Figure 6).

STOP CONDITION

All communications must be terminated by a stop condition, which is a LOW to HIGH transition of SDA while SCL is HIGH (see Figure 6).

ACKNOWLEDGE

Acknowledge is a software convention used to provide a positive handshake between the master and slave devices on the bus to indicate the successful receipt of data. The transmitting device, either the master or the slave, will release the SDA bus after transmitting eight bits. The master generates a ninth clock cycle and during this period the receiver pulls the SDA line LOW to acknowledge that it successfully received the eight bits of data.

The X9119 will respond with an acknowledge after recognition of a start condition and its slave address and once again after successful receipt of the command byte. If the command is followed by a data byte the X9119 will respond with a final acknowledge (see Figure 4).

ACKNOWLEDGE POLLING

The disabling of the inputs, during the internal nonvolatile write operation, can be used to take advantage of the typical 5ms EEPROM write cycle time. Once the stop condition is issued to indicate the end of the nonvolatile write command the X9119 initiates the internal write cycle. ACK polling, Flow 1 (see Figure 5 on page 5), can be initiated immediately. This involves issuing the start condition followed by the device slave address. If the X9119 is still busy with the write operation, no ACK will be returned. If the X9119 has completed the write operation, an ACK will be returned and the master can then proceed with the next operation.

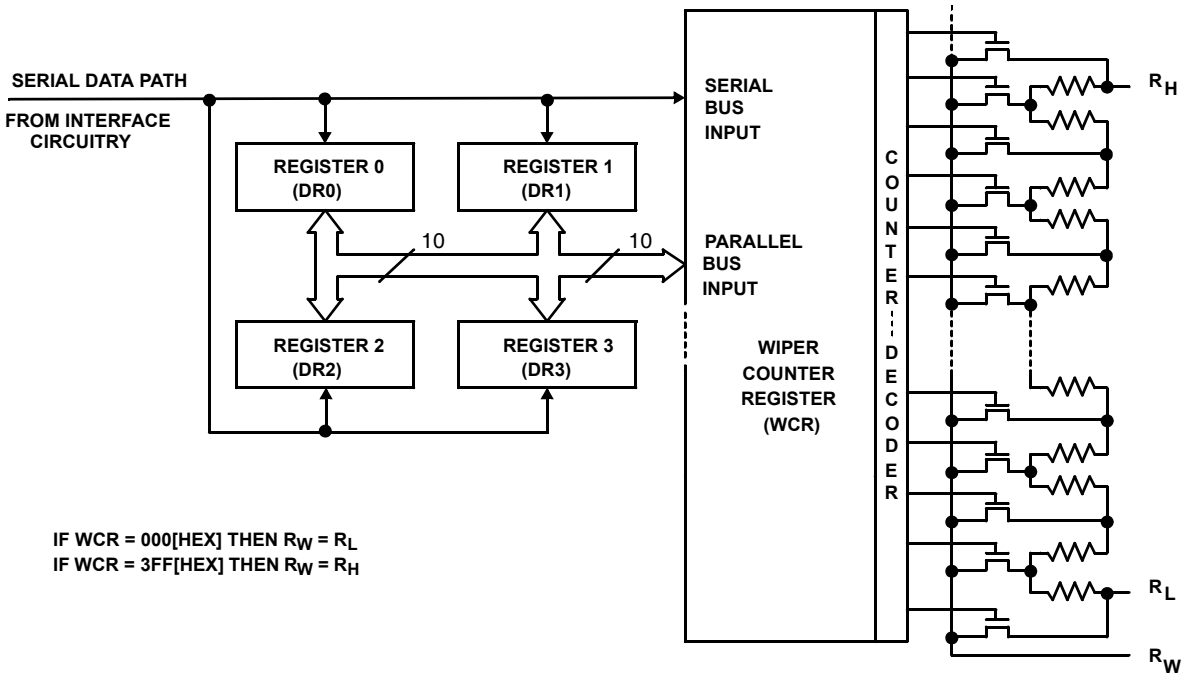


FIGURE 3. DETAILED POTENTIOMETER BLOCK DIAGRAM SERIAL INTERFACE DESCRIPTION

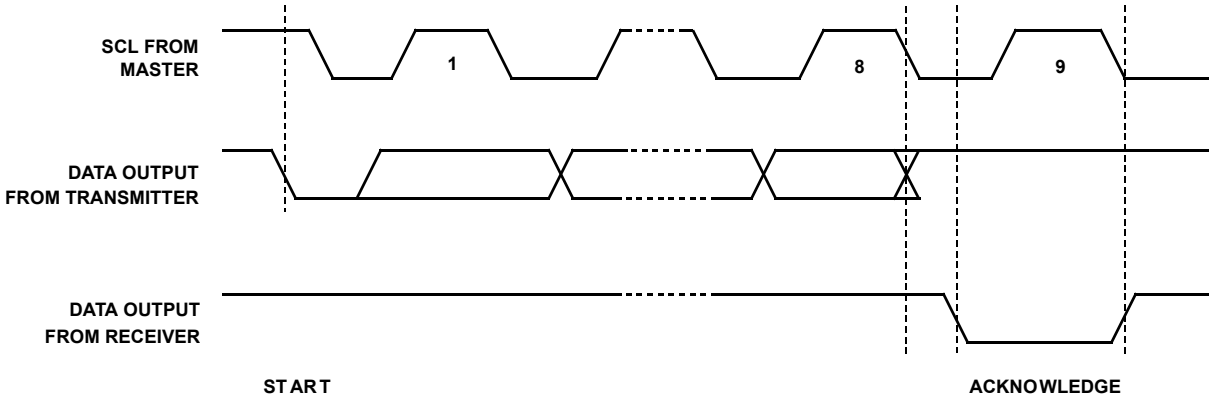


FIGURE 4. ACKNOWLEDGE RESPONSE FROM RECEIVER

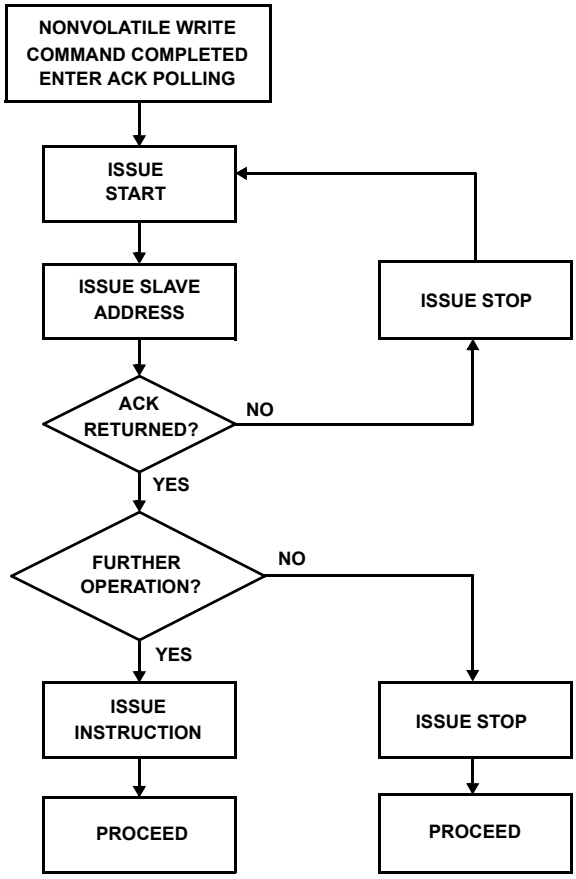


FIGURE 5. FLOW 1. ACK POLLING SEQUENCE

Instruction and Register Description

Device Addressing: Identification Byte (ID and A)

Following a start condition, the master must output the address of the slave it is accessing. The most significant four bits of the slave address are the device type identifier. The ID[3:0] bits is the device ID for the X9119; this is fixed as 0101[B] (refer to Table 1).

The A2–A0 bits in the ID byte is the internal slave address. The physical device address is defined by the state of the A2–A0 input pins. The slave address is externally specified by the user. The X9119 compares the serial data stream with the address input state; a successful compare of both address bits is required for the X9119 to successfully continue the command sequence.

Only the device which slave address matches the incoming device address sent by the master executes the instruction. The A2–A0 inputs can be actively driven by CMOS input signals or tied to V_{CC} or V_{SS}. The R/$\overline{W}$ bit is the LSB and is be used to program the device for read or write operations.

INSTRUCTION BYTE AND REGISTER SELECTION

The next byte sent to the X9119 contains the instruction and register pointer information. The three most significant bits are used provide the instruction opcode (IOP[2:0]). The RB and RA bits point to one of the four registers. The format is shown in Table 2.

Table 3 provides a complete summary of the instruction set opcodes.

TABLE 1. IDENTIFICATION BYTE FORMAT

	DEVICE TYPE IDENTIFIES				INTERNAL SLAVE ADDRESS			READ OR WRITE BIT
	ID3	ID2	ID1	ID0	A2	A1	A0	R/$\overline{W}$
	0	1	0	1				
	(MSB)							(LSB)

TABLE 2. INSTRUCTION BYTE FORMAT

	INSTRUCTION OPCODE				REGISTER SELECTION			
	I2	I1	I0	0	RB	RA	0	0
	(MSB)							(LSB)

REGISTER SELECTED	RB	RA
DR0	0	0
DR1	0	1
DR2	1	0
DR3	1	1

TABLE 3. INSTRUCTION SET

INSTRUCTION	INSTRUCTION SET									OPERATION
	R/$\overline{W}$	I_2	I_1	I_0	0	RB	RA	0	0	
Read Wiper Counter Register	1	1	0	0	0	0	0	0	0	Read the contents of the wiper counter register.
Write Wiper Counter Register	0	1	0	1	0	0	0	0	0	Write new value to the wiper counter register.
Read Data Register	1	1	0	1	0	1/0	1/0	0	0	Read the contents of the data register pointed to RB-RA.
Write Data Register	0	1	1	0	0	1/0	1/0	0	0	Write new value to the data register pointed to RB-RA.
XFR Data Register to Wiper Counter Register	1	1	1	0	0	1/0	1/0	0	0	Transfer the contents of the data register pointed to by RB-RA to the wiper counter register.
XFR Wiper Counter Register to Data Register	0	1	1	1	0	1/0	1/0	0	0	Transfer the contents of the wiper counter register to the data register pointed to by RB-RA.

NOTE: 1/0 = data is one or zero.

Instruction and Register Description

Device Addressing

WIPER COUNTER REGISTER (WCR)

The X9119 contains a wiper counter register (refer to Table 4) for the XDCP potentiometer. The WCR is equivalent to a serial-in, parallel-out register/counter with its outputs decoded to select one of 1024 switches along its resistor array. The contents of the WCR can be altered in one of three ways:

1. It may be written directly by the host via the write wiper counter register instruction (serial load).
2. It may be written indirectly by transferring the contents of one of four associated data registers via the XFR data register.
3. It is loaded with the contents of its data register zero (R0) upon power-up.

The wiper counter register is a volatile register; that is, its contents are lost when the X9119 is powered-down. Although the register is automatically loaded with the value in DR0 upon power-up, this may be different from the value present at power-down. Power-up guidelines are recommended to ensure proper loadings of the DR0 value into the WCR.

DATA REGISTERS (DR0 TO DR3)

The potentiometer has four 10-bit nonvolatile data registers. These can be read or written directly by the host. Data can also be transferred between any of the four data registers and the wiper counter register. All operations changing data in one of the data registers is a nonvolatile operation and will take a maximum of 10ms.

If the application does not require storage of multiple settings for the potentiometer, the Data Registers can be used as regular memory locations for system parameters or user preference data.

Bit 9 to Bit 0 are used to store one of the 1024 wiper position (0 ~1023).

Four of the six instructions are four bytes in length. These instructions are:

- **Read Wiper Counter Register** – Reads the current wiper position of the selected potentiometer.
- **Write Wiper Counter Register** – Changes current wiper position of the selected potentiometer.
- **Read Data Register** – Reads the contents of the selected Data Register.
- **Write Data Register** – Writes a new value to the selected Data Register.

The basic sequence of the four byte instructions is illustrated in Figure 6 on page 8. These 4-byte instructions exchange data between the WCR and one of the data registers. A transfer from a data register to a WCR is essentially a write to a static RAM, with the static RAM controlling the wiper position. The response of the wiper to this action will be delayed by t_{WRL}. A transfer from the WCR (current wiper position), to a data register is a write-to-nonvolatile memory and takes a minimum of t_{WR} to complete. The transfer can occur between one of the four potentiometers and one of its associated registers.

Two instructions (Figure 7 on page 8) require a 2-byte sequence to complete. These instructions transfer data between the host and the X9119; either between the host and one of the data registers or directly between the host and the wiper counter register. These instructions are:

- **XFR Data Register to Wiper Counter Register** – This transfers the contents of one specified data register to the wiper counter register.
- **XFR Wiper Counter Register to Data Register** – This transfers the contents of the wiper counter register to the specified data register.

See "Instruction Format" on page 8 for more details.

POWER-UP AND POWER-DOWN REQUIREMENTS

There are no restrictions on the power-up condition of V_{CC} and the voltages applied to the potentiometer pins provided that the V_{CC} is always more positive than or equal to the voltages at R_H, R_L, and R_W, i.e., $V_{CC} \geq R_H, R_L, R_W$. There are no restrictions on the power-down condition. However, the datasheet parameters for the DCP do not apply until 1ms after V_{CC} reaches its final value.

TABLE 4. WIPER CONTROL REGISTER, WCR (10-BIT), WCR9–WCR0: USED TO STORE THE CURRENT WIPER POSITION (VOLATILE, V)

WCR9	WCR8	WCR7	WCR6	WCR5	WCR4	WCR3	WCR2	WCR1	WCR0
V	V	V	V	V	V	V	V	V	V
(MSB)									(LSB)

TABLE 5. DATA REGISTER, DR (10-BIT), BIT 9–BIT 0: USED TO STORE WIPER POSITIONS OR DATA (NONVOLATILE, NV)

BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NV	NV	NV	NV	NV	NV	NV	NV	NV	NV
MSB									LSB

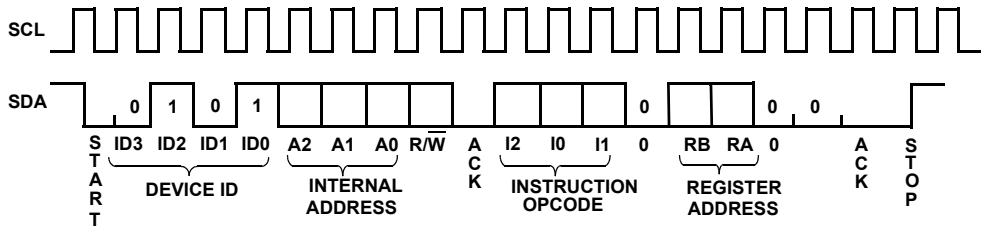


FIGURE 6. TWO-BYTE INSTRUCTION SEQUENCE

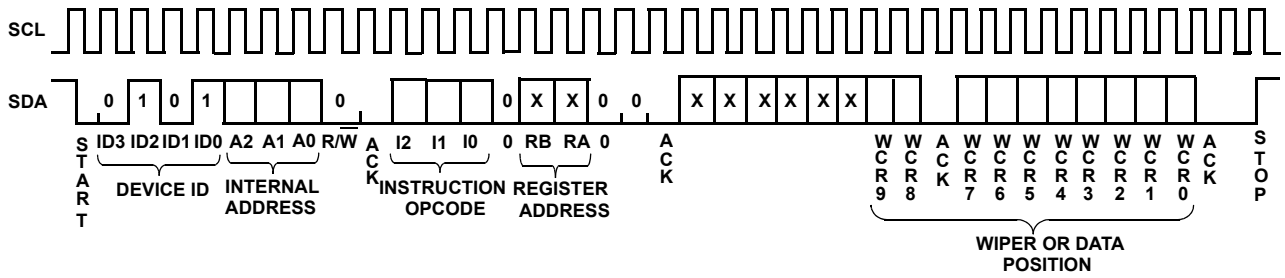


FIGURE 7. FOUR-BYTE INSTRUCTION SEQUENCE (WRITE OR READ FOR WCR OR DATA REGISTERS)

Instruction Format

READ WIPER COUNTER REGISTER (WCR)

START	DEVICE TYPE IDENTIFIER				DEVICE ADDRESSES				SACK	INSTRUCTION OPCODE				REGISTER ADDRESSES				SACK	WIPER POSITION (SENT BY SLAVE ON SDA)								MACK	WIPER POSITION (SENT BY SLAVE ON SDA)								MACK	STOP
	0	1	0	1	A2	A1	A0	R/$\overline{W}$ = 1		1	0	0	0	0	0	0	0		X	X	X	X	X	X	WCR9	WCR8		WCR7	WCR6	WCR5	WCR4	WCR3	WCR2	WCR1	WCR0		

WRITE WIPER COUNTER REGISTER (WCR)

START	DEVICE TYPE IDENTIFIER				DEVICE ADDRESSES				SACK	INSTRUCTION OPCODE				REGISTER ADDRESSES				SACK	WIPER POSITION (SENT BY MASTER ON SDA)								SACK	WIPER POSITION (SENT BY MASTER ON SDA)								SACK	STOP
	0	1	0	1	A2	A1	A0	R/$\overline{W}$ = 0		1	0	1	0	0	0	0	0		X	X	X	X	X	X	WCR9	WCR8		WCR7	WCR6	WCR5	WCR4	WCR3	WCR2	WCR1	WCR0		

READ DATA REGISTER (DR)

START	DEVICE TYPE IDENTIFIER				DEVICE ADDRESSES				SACK	INSTRUCTION OPCODE				REGISTER ADDRESSES				SACK	WIPER POSITION (SENT BY SLAVE ON SDA)								MACK	WIPER POSITION OR DATA (SENT BY SLAVE ON SDA)								MACK	STOP
	0	1	0	1	A2	A1	A0	R/$\overline{W}$ = 1		1	0	1	0	RB	RA	0	0		X	X	X	X	X	X	WCR9	WCR8		WCR7	WCR6	WCR5	WCR4	WCR3	WCR2	WCR1	WCR0		

WRITE DATA REGISTER (DR)

START	DEVICE TYPE IDENTIFIER				DEVICE ADDRESSES				SACK	INSTRUCTION OPCODE				REGISTER ADDRESSES				SACK	WIPER POSITION OR DATA (SENT BY MASTER ON SDA)								SACK	WIPER POSITION OR DATA (SENT BY MASTER ON SDA)								SACK	STOP	HIGH-VOLTAGE WRITE CYCLE
	0	1	0	1	A2	A1	A0	R/$\overline{W}$ = 0		1	1	0	0	RB	RA	0	0		X	X	X	X	X	X	WCR9	WCR8		WCR7	WCR6	WCR5	WCR4	WCR3	WCR2	WCR1	WCR0			

TRANSFER WIPER COUNTER REGISTER (WCR) TO DATA REGISTER (DR)

START	DEVICE TYPE IDENTIFIER				DEVICE ADDRESSES				SACK	INSTRUCTION OPCODE				REGISTER ADDRESSES				SACK	STOP	
	0	1	0	1	A2	1	A0	R / $\overline{W}$ = 0		1	1	1	0	RB	RA	0	0			HIGH-VOLTAGE WRITE CYCLE

TRANSFER DATA REGISTER (DR) TO WIPER COUNTER REGISTER (WCR)

START	DEVICE TYPE IDENTIFIER				DEVICE ADDRESSES				SACK	INSTRUCTION OPCODE				REGISTER ADDRESSES				SACK	STOP
	0	1	0	1	A2	A1	A0	R / $\overline{W}$ = 1		1	1	0	0	RB	RA	0	0		

NOTES:

4. A2 ~ A0": stand for the device addresses sent by the master.
5. WCRx refers to wiper position data in the wiper counter register.

Absolute Maximum Ratings

Voltage on SCL, SDA, or any address input
with respect to V_{SS} . . . . . -1V to +7V
$\Delta V = | (VH-VL) |$ 5V
I_W (10s) . . . . . ±6mA

Thermal Information

Temperature under bias . . . . . -65°C to +135°C
Storage temperature . . . . . -65°C to +150°C
Lead temperature (soldering, 10s) . . . . . 300°C
Pb-Free Reflow Profile . . . . . see TB493

Operating Conditions

Commercial . . . . . 0°C to +70°C
Industrial . . . . . -40° to +85°C
Supply Voltage (V_{CC}) Limits (Note 9)
X9119 . . . . . 5V ±10%
X9119-2.7 . . . . . 2.7V to 5.5V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

Analog Specifications (Over recommended operation conditions unless otherwise stated.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 13)	TYP	MAX (Note 13)	UNIT
End-to-End Resistance	R_{TOTAL}			100		kΩ
End-to-End Resistance Tolerance					±20	%
Power Rating		+25°C, each pot			50	mW
Wiper Current	I_W				±3	mA
Wiper Resistance	R_W	Wiper Current = ± 50µA, V_{CC} = 5V		40	110	Ω
		Wiper Current = ± 50µA, V_{CC} = 3V		150	300	Ω
Voltage on any R_H or R_L Pin	V_{TERM}	V_{SS} = 0V	V_{SS}		5	V
Noise		Ref: 1V		-120		dBV
Resolution				0.1		%
Absolute Linearity (Note 6)		$R_{w(n)(actual)} - R_{w(n)(expected)}$, where n = 8 to 1006			±1.5	MI (Note 8)
		$R_{w(n)(actual)} - R_{w(n)(expected)}$ (Note 9)		±1.5	±2.0	MI (Note 8)
Relative Linearity (Note 7)		$R_{w(m+1)} - [R_{w(m)} + MI]$, where m = 8 to 1006			±0.5	MI (Note 8)
		$R_{w(m+1)} - [R_{w(m)} + MI]$ (Note 9)		±0.5	±1.0	MI (Note 8)
Temperature Coefficient of R_{TOTAL}				±300		ppm/°C
Ratiometric Temperature Coefficient				20		ppm/°C
Potentiometer Capacitances	$C_H/C_L/C_W$	See Macro model		10/10/25		pF

NOTES:

6. Absolute linearity is utilized to determine actual wiper voltage vs expected voltage as determined by wiper position when used as a potentiometer.
7. Relative linearity is utilized to determine the actual change in voltage between two successive tap positions when used as a potentiometer. It is a measure of the error in step size.
8. MI = $R_{TOT}/1023$ or $(R_H - R_L)/1023$, single potentiometer
9. n = 0, 1, 2, ...,1023; m = 0, 1, 2, ..., 1022.
10. ESD Rating on R_H, R_L, R_W pins is 1.5kV (HBM, 1.0µA leakage maximum), ESD rating on all other pins is 2.0kV.

Operating Specifications (Over the recommended operating conditions unless otherwise specified.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC} Supply Current (Active)	I_{CC1}	f_{SCL} = 400kHz; V_{CC} = +5.5V; SDA = Open; (for 2-wire, active, read and volatile write states only)			3	mA
V_{CC} Supply Current (Nonvolatile Write)	I_{CC2}	f_{SCL} = 400kHz; V_{CC} = +5.5V; SDA = Open; (for 2-wire, active, non-volatile write state only)			5	mA
V_{CC} Current (Standby)	I_{SB}	V_{CC} = +5.5V; V_{IN} = V_{SS} or V_{CC}; SDA = V_{CC}; (for 2-wire, standby state only)			3	µA
Input Leakage Current	I_{LI}	V_{IN} = V_{SS} to V_{CC}			10	µA
Output Leakage Current	I_{LO}	V_{OUT} = V_{SS} to V_{CC}			10	µA
Input HIGH Voltage	V_{IH}		V_{CC} x 0.7		V_{CC} + 1	V
Input LOW Voltage	V_{IL}		-1		V_{CC} x 0.3	V
Output LOW Voltage	V_{OL}	I_{OL} = 3mA			0.4	V
Output HIGH Voltage	V_{OH}					

Endurance and Data Retention

PARAMETER	MIN	UNITS
Minimum Endurance	100,000	Data changes per bit per register
Data Retention	100	years

Capacitance

TEST	SYMBOL	TEST CONDITIONS	MAX	UNIT
Input/Output Capacitance (SI)	$C_{IN/OUT}$ (Note 11)	V_{OUT} = 0V	8	pF
Input Capacitance (SCL, $\overline{WP}$, A1 and A0)	C_{IN} (Note 11)	V_{IN} = 0V	6	pF

Power-Up Timing

PARAMETER	SYMBOL	MIN	MAX	UNIT
V_{CC} Power-Up Rate	t_r V_{CC} (Note 11)	0.2	50	V/ms
Power-Up to Initiation Of Read Operation	t_{PUR} (Note 12)		1	ms
Power-Up to Initiation Of Write Operation	t_{PUW} (Note 12)		50	ms

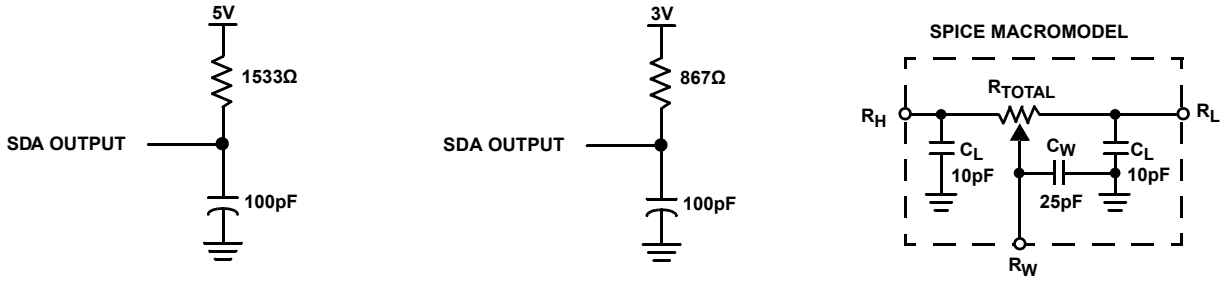
NOTES:

11. Limits should be considered typical and are not production tested.
12. t_{PUR} and t_{PUW} are the delays required from the time the (last) power supply (Vcc-) is stable until the specific instruction can be issued. These parameters are not 100% tested.
13. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

AC Test Conditions

Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10ns
Input and Output Timing Level	V_{CC} x 0.5

Equivalent A.C. Load Circuit



AC Timing High-Voltage Write Cycle Timing

PARAMETER	SYMBOL	MIN	MAX	UNIT
Clock Frequency	f_{SCL}		400	kHz
Clock Cycle Time	t_{CYC}	2500		ns
Clock High Time	t_{HIGH}	600		ns
Clock Low Time	t_{LOW}	1300		ns
Start Set-Up Time	$t_{SU:STA}$	600		ns
Start Hold Time	$t_{HD:STA}$	600		ns
Stop Set-Up Time	$t_{SU:STO}$	600		ns
SDA Data Input Set-Up Time	$t_{SU:DAT}$	100		ns
SDA Data Input Hold Time	$t_{HD:DAT}$	0		ns
SCL and SDA Rise Time	t_R		300	ns
SCL and SDA Fall Time	t_F		300	ns
SCL Low to SDA Data Output Valid Time	t_{AA}	250		ns
SDA Data Output Hold Time	t_{DH}	0		ns
Noise Suppression Time Constant at SCL and SDA Inputs	T_I	50		ns
Bus Free Time (Prior to Any Transmission)	t_{BUF}	1300		ns
A0, A1, A2 Set-Up Time	$t_{SU:WPA}$	0		ns
A0, A1, A2 Hold Time	$t_{HD:WPA}$	0		ns

High-Voltage Write Cycle Timing

PARAMETER	SYMBOL	TYP	MAX	UNIT
High-Voltage Write Cycle Time (Store Instructions)	t_{WR}	5	10	ms

XDCP Timing

PARAMETER	SYMBOL	MIN	MAX	UNIT
Wiper Response Time After the Third (Last) Power Supply is Stable	t_{WRPO}	5	10	µs
Wiper Response Time After Instruction Issued (All Load Instructions)	t_{WRL}	5	10	µs

Symbol Table

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is HIGH Impedance

Timing Diagrams

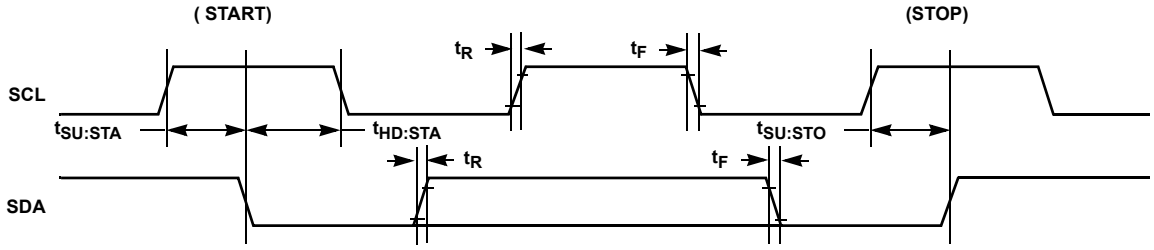


FIGURE 8. START AND STOP TIMING

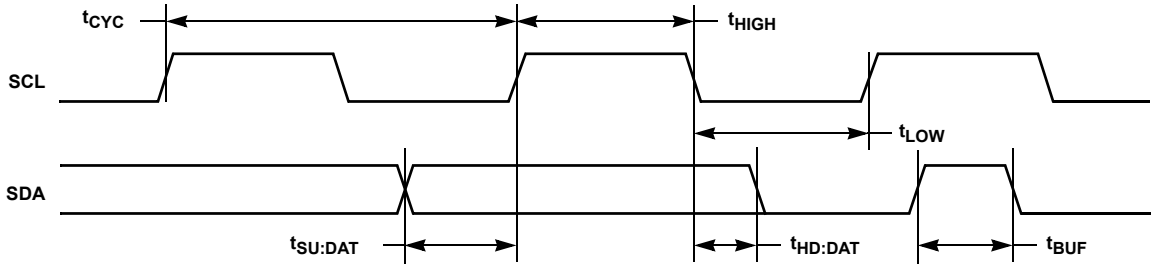


FIGURE 9. INPUT TIMING

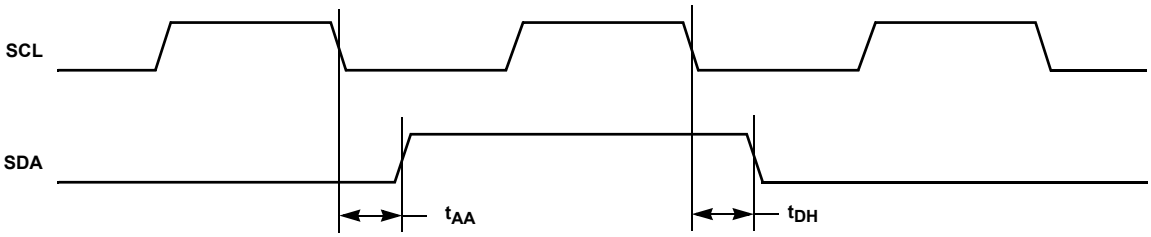


FIGURE 10. OUTPUT TIMING

Timing Diagrams

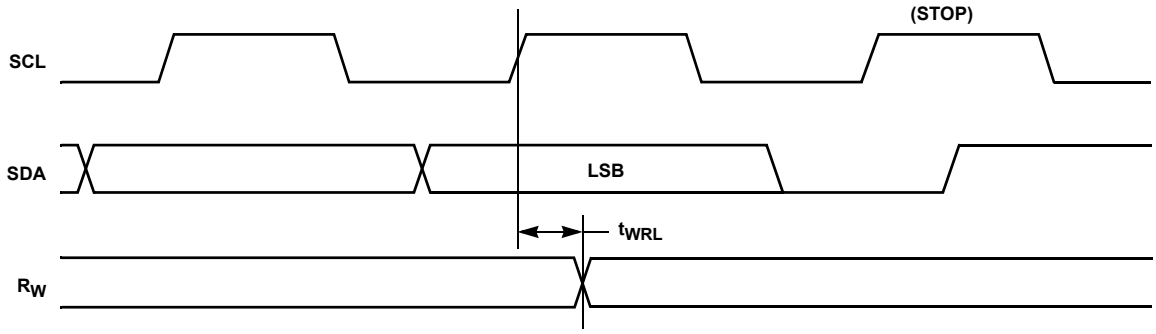


FIGURE 11. XDCP TIMING (FOR ALL LOAD INSTRUCTIONS)

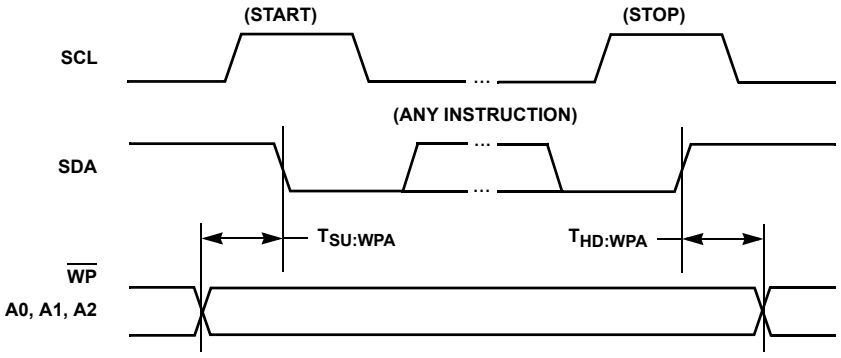


FIGURE 12. WRITE PROTECT AND DEVICE ADDRESS PINS TIMING

Applications information

Basic Configurations of Electronic Potentiometers

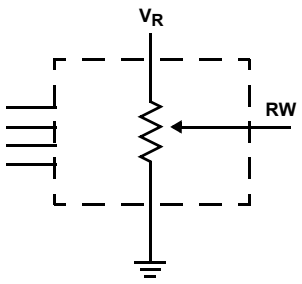


FIGURE 13. THREE-TERMINAL POTENTIOMETER; VARIABLE VOLTAGE DIVIDER

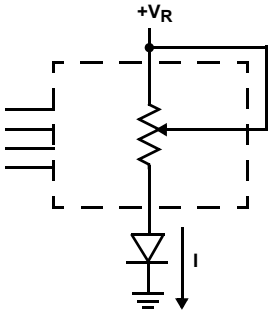


FIGURE 14. TWO-TERMINAL VARIABLE RESISTOR; VARIABLE CURRENT

Application Circuits

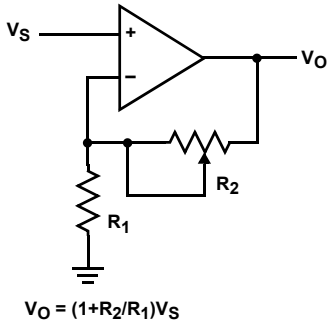


FIGURE 15. NONINVERTING AMPLIFIER

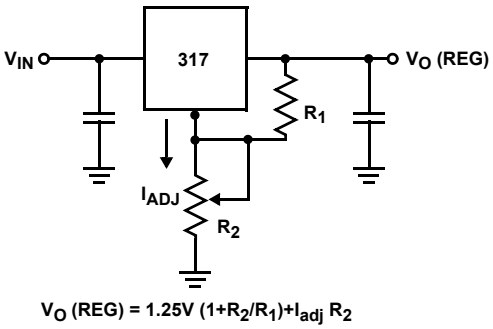


FIGURE 16. VOLTAGE REGULATOR

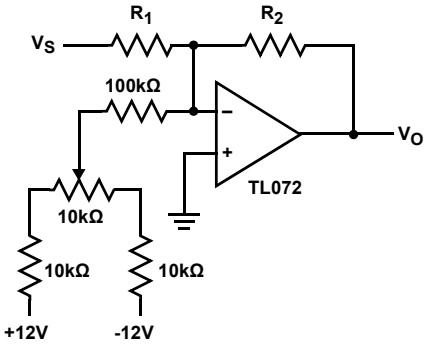


FIGURE 17. OFFSET VOLTAGE ADJUSTMENT

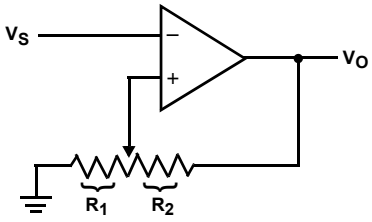
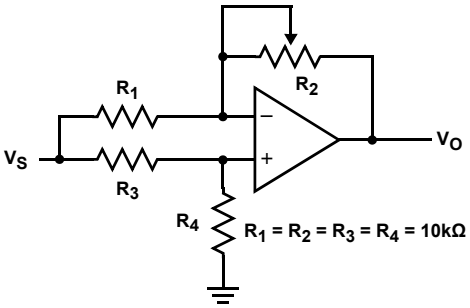


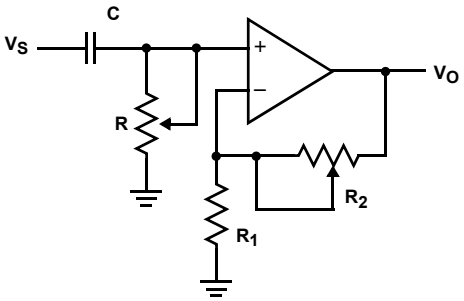
FIGURE 18. COMPARATOR WITH HYSTERESIS

Application Circuits (Continued)



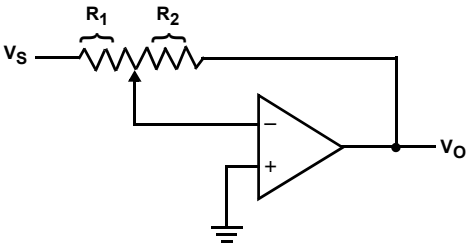
$V_O = G V_S$
$-1/2 \leq G \leq +1/2$

FIGURE 19. ATTENUATOR



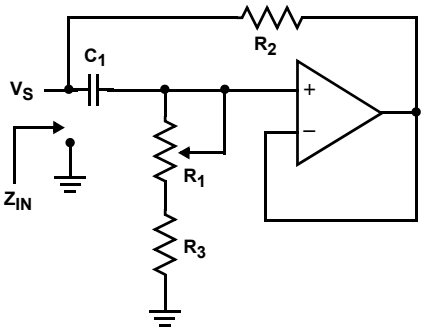
$G_O = 1 + R_2/R_1$
$fc = 1/(2pRC)$

FIGURE 20. FILTER



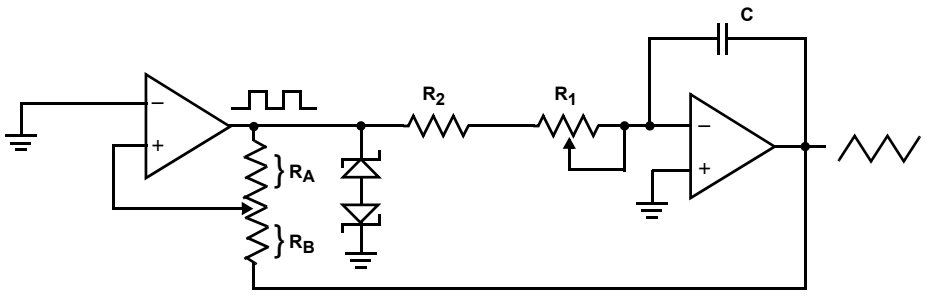
$V_O = G V_S$
$G = - R_2/R_1$

FIGURE 21. INVERTING AMPLIFIER



$Z_{IN} = R_2 + s R_2 (R_1 + R_3) C_1 = R_2 + s Leq$
$(R_1 + R_3) >> R_2$

FIGURE 22. EQUIVALENT L-R CIRCUIT



FREQUENCY µ R_1, R_2, C
AMPLITUDE µ R_A, R_B

FIGURE 23. FUNCTION GENERATOR

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
July 5, 2016	FN8162.5	Updated entire datasheet applying Intersil's new standards. Updated title. Updated Ordering Information table by removing obsolete parts, updating Note 1 and adding Note 3. Removed Lead temperature (soldering, 10s) from the Thermal Information section on page 10. Updated Absolute Linearity maximum specification from "±1" to "±1.5". Added Revision History and About Intersil sections. Updated POD to the latest revision changes are as follows: Updated drawing to remove table and added land pattern.

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

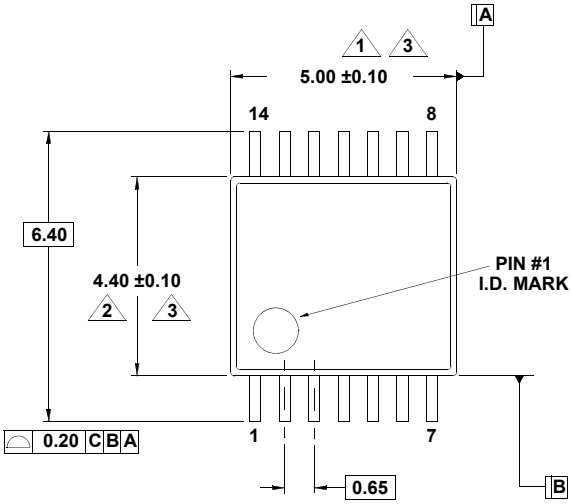
Reliability reports are also available from our website at www.intersil.com/support.

Package Outline Drawing

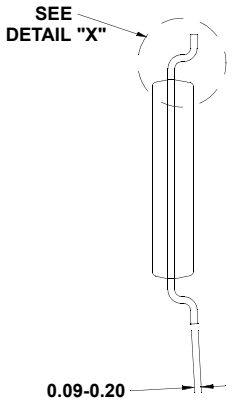
M14.173

14 LEAD THIN SHRINK SMALL OUTLINE PACKAGE (TSSOP)

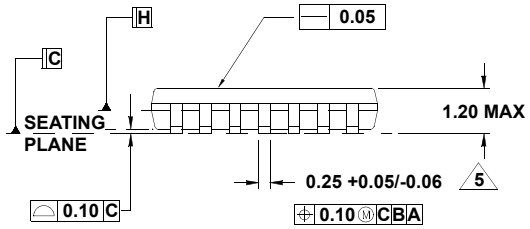
Rev 3, 10/09



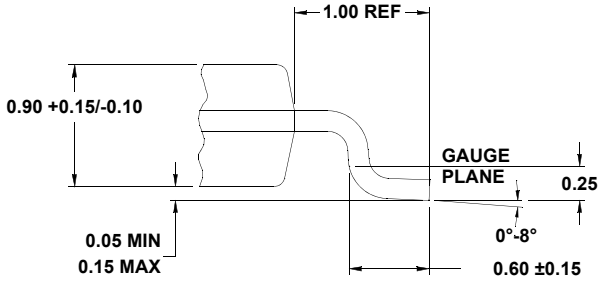
TOP VIEW



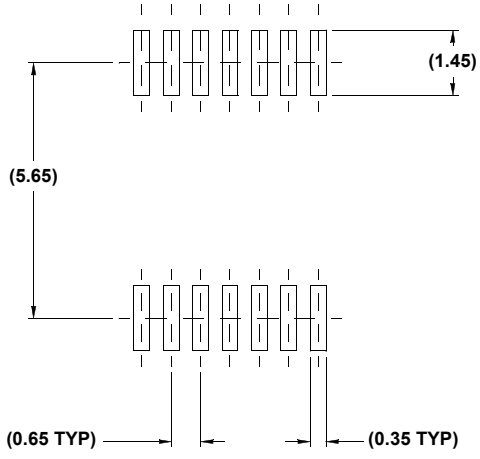
END VIEW



SIDE VIEW



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.
2. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
3. Dimensions are measured at datum plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Dimension does not include dambar protrusion. Allowable protrusion shall be 0.80mm total in excess of dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm.
6. Dimension in ( ) are for reference only.
7. Conforms to JEDEC MO-153, variation AB-1.