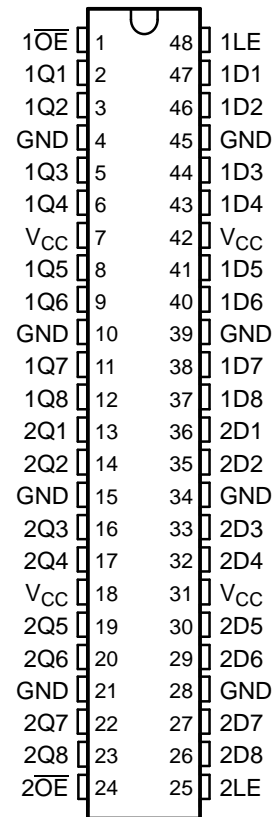


## FEATURES

- **Controlled Baseline**
  - One Assembly/Test Site, One Fabrication Site
- **Extended Temperature Performance of –55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product Change Notification**
- **Qualification Pedigree <sup>(1)</sup>**
- **Member of the Texas Instruments Widebus™ Family**
- **State-of-the-Art EPIC-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical  $V_{OLP}$  (Output Ground Bounce) <0.8 V at  $V_{CC} = 5 V$ ,  $T_A = 25^\circ C$**
- **High-Impedance State During Power Up and Power Down**
- **Distributed  $V_{CC}$  and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **High-Drive Outputs (–24-mA  $I_{OH}$ , 48-mA  $I_{OL}$ )**
- **Plastic 300-mil Shrink Small-Outline (DL) Package**

- (1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold-compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

**DL PACKAGE  
(TOP VIEW)**



## DESCRIPTION/ORDERING INFORMATION

The SN74ABT16373A-EP is a 16-bit transparent D-type latch with 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. The SN74ABT16373A-EP is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

### ORDERING INFORMATION

$T_A$	PACKAGE <sup>(1)</sup>	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	SSOP – DL Tape and reel	CABT16373AMDREP	ABT16373AMEP

- (1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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# SN74ABT16373A-EP

## 16-BIT TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

SCBS810–MARCH 2006

### DESCRIPTION/ORDERING INFORMATION (CONTINUED)

The SN74ABT16373A-EP can be used as two 8-bit latches or one 16-bit latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

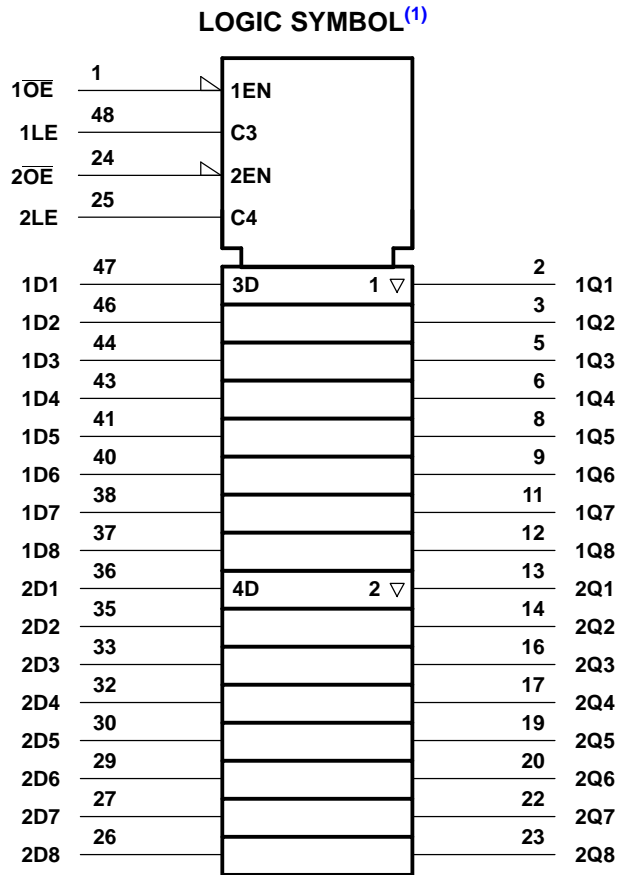
$\overline{OE}$  does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

When  $V_{CC}$  is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT16373A-EP is characterized for operation from  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .

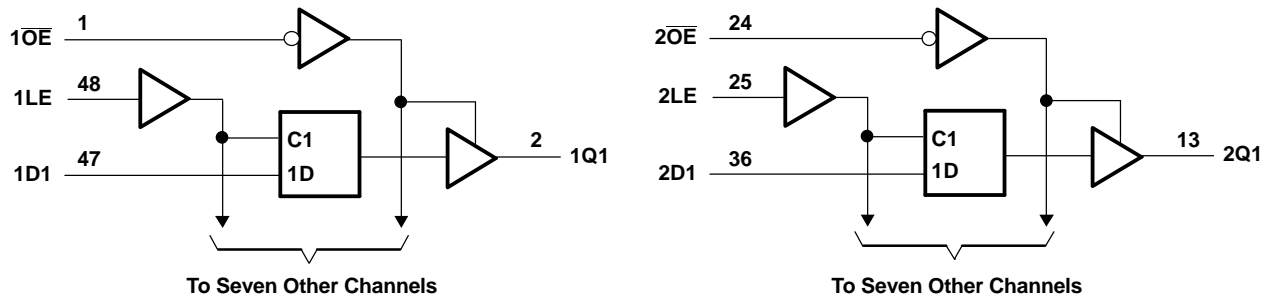
**FUNCTION TABLE**  
(each 8-bit section)

INPUTS			OUTPUT Q
$\overline{OE}$	LE	D	
L	H	H	H
L	H	L	L
L	L	X	$Q_0$
H	X	X	Z



(1) This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

**LOGIC DIAGRAM (POSITIVE LOGIC)**



# SN74ABT16373A-EP

## 16-BIT TRANSPARENT D-TYPE LATCH

### WITH 3-STATE OUTPUTS

SCBS810–MARCH 2006

### Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage range	-0.5	7	V
$V_I$	Input voltage range <sup>(2)</sup>	-0.5	7	V
$V_O$	Voltage range applied to any output in the high or power-off state	-0.5	5.5	V
$I_O$	Current into any output in the low state		96	mA
$I_{IK}$	Input clamp current	$V_I < 0$	-18	mA
$I_{OK}$	Output clamp current	$V_O < 0$	-50	mA
$\theta_{JA}$	Package thermal impedance <sup>(3)</sup>		94	°C/W
$T_{stg}$	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD 51.

### Recommended Operating Conditions<sup>(1)</sup>

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	4.5	5.5	V
$V_{IH}$	High-level input voltage	2		V
$V_{IL}$	Low-level input voltage		0.8	V
$V_I$	Input voltage	0	$V_{CC}$	V
$I_{OH}$	High-level output current		-24	mA
$I_{OL}$	Low-level output current		48	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		10	ns/V
				Outputs enabled
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		$\mu$ s/V
$T_A$	Operating free-air temperature	-55	125	°C

- (1) Unused inputs must be held high or low to prevent them from floating.

## Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
		MIN	TYP <sup>(1)</sup>	MAX			
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA				-1.2	V	
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -3 mA	2.5			2.5	V	
	V <sub>CC</sub> = 5 V, I <sub>OH</sub> = -3 mA	3			3		
	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -24 mA	2			2		
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 48 mA				0.55	V	
V <sub>hys</sub>		100				mV	
I <sub>I</sub>	V <sub>CC</sub> = 0 to 5.5 V, V <sub>I</sub> = V <sub>CC</sub> or GND				±1	μA	
I <sub>OZPU</sub> <sup>(2)</sup>	V <sub>CC</sub> = 0 to 2.1 V, V <sub>O</sub> = 0.5 V to 2.7 V, $\overline{OE} = X$				±50	μA	
I <sub>OZPD</sub> <sup>(2)</sup>	V <sub>CC</sub> = 2.1 V to 0, V <sub>O</sub> = 0.5 V to 2.7 V, $\overline{OE} = X$				±50	μA	
I <sub>OZH</sub>	V <sub>CC</sub> = 2.1 V to 5.5 V, V <sub>O</sub> = 2.7 V, $\overline{OE} \geq 2 V$				10	μA	
I <sub>OZL</sub>	V <sub>CC</sub> = 2.1 V to 5.5 V, V <sub>O</sub> = 0.5 V, $\overline{OE} \geq 2 V$				-10	μA	
I <sub>off</sub>	V <sub>CC</sub> = 0, V <sub>I</sub> or V <sub>O</sub> ≤ 4.5 V				±100	μA	
I <sub>CEX</sub>	Outputs high V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 5.5 V				50	μA	
I <sub>O</sub> <sup>(3)</sup>	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.5 V	-50	-100	-180	-50 -180	mA	
I <sub>CC</sub>	Outputs high				2	mA	
	Outputs low	V <sub>CC</sub> = 5.5 V, I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND			85		
	Outputs disabled				2		
ΔI <sub>CC</sub> <sup>(4)</sup>	V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND				1.5	mA	
C <sub>i</sub>	V <sub>I</sub> = 2.5 V or 0.5 V		3.5			pF	
C <sub>o</sub>	V <sub>O</sub> = 2.5 V or 0.5 V		9.5			pF	

 (1) All typical values are at V<sub>CC</sub> = 5 V.

(2) This parameter is characterized, but not production tested.

(3) Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

 (4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V<sub>CC</sub> or GND.

## Timing Requirements

 over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 1](#))

		V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		MIN	MAX	UNIT
		MIN	MAX			
t <sub>w</sub>	Pulse duration, LE high	3.3		3.3		ns
t <sub>su</sub>	Setup time, data before LE↓	1.5		2.4		ns
t <sub>h</sub>	Hold time, data after LE↓	1		2.2		ns

# SN74ABT16373A-EP

## 16-BIT TRANSPARENT D-TYPE LATCH

### WITH 3-STATE OUTPUTS

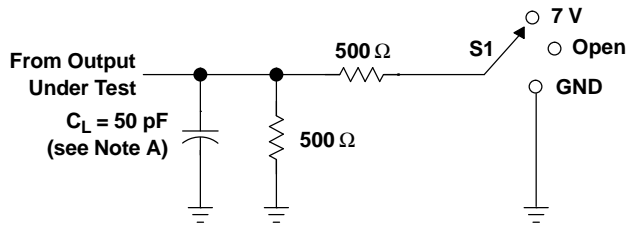
SCBS810–MARCH 2006

#### Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50$  pF (unless otherwise noted)  
(see [Figure 1](#))

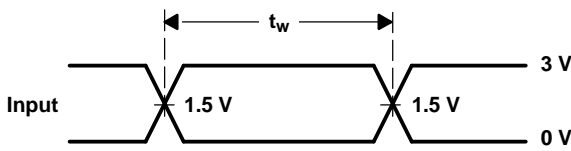
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5$ V, $T_A = 25^\circ$ C			MIN	MAX	UNIT
			MIN	TYP	MAX			
$t_{PLH}$	D	Q	1.4	3.7	5.3	1.4	6.5	ns
$t_{PHL}$			2	4	5.4	2	6.5	
$t_{PLH}$	LE	Q	1.7	4.1	5.7	1.7	7	ns
$t_{PHL}$			2.3	4.3	5.6	2.3	6.3	
$t_{PZH}$	$\overline{OE}$	Q	1.1	3.4	5	1.1	6.4	ns
$t_{PZL}$			1.5	3.5	4.9	1.5	5.8	
$t_{PHZ}$	$\overline{OE}$	Q	2.4	5.1	7.1	2.4	8.3	ns
$t_{PLZ}$			1.6	4.4	6.3	1.6	8	

PARAMETER MEASUREMENT INFORMATION

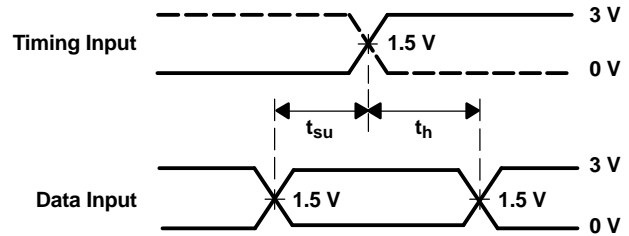


LOAD CIRCUIT

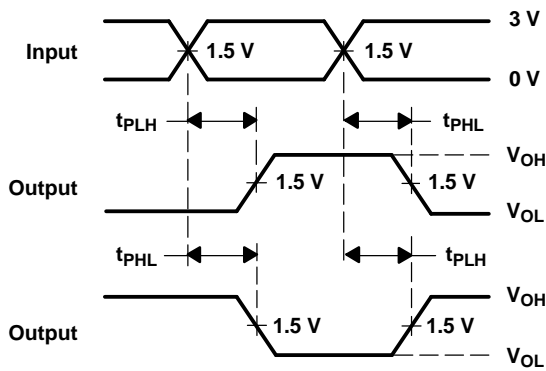
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PZH}$	Open



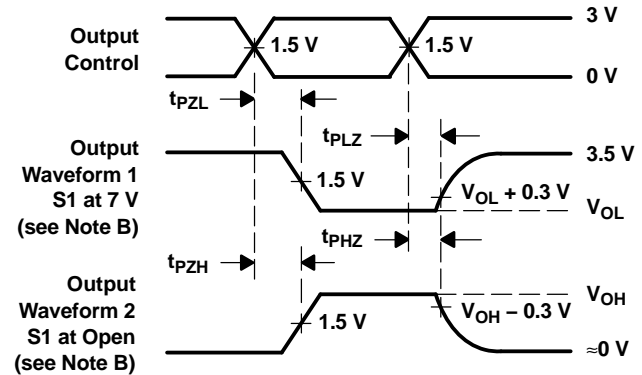
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .  
D. The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

APPLICATION INFORMATION

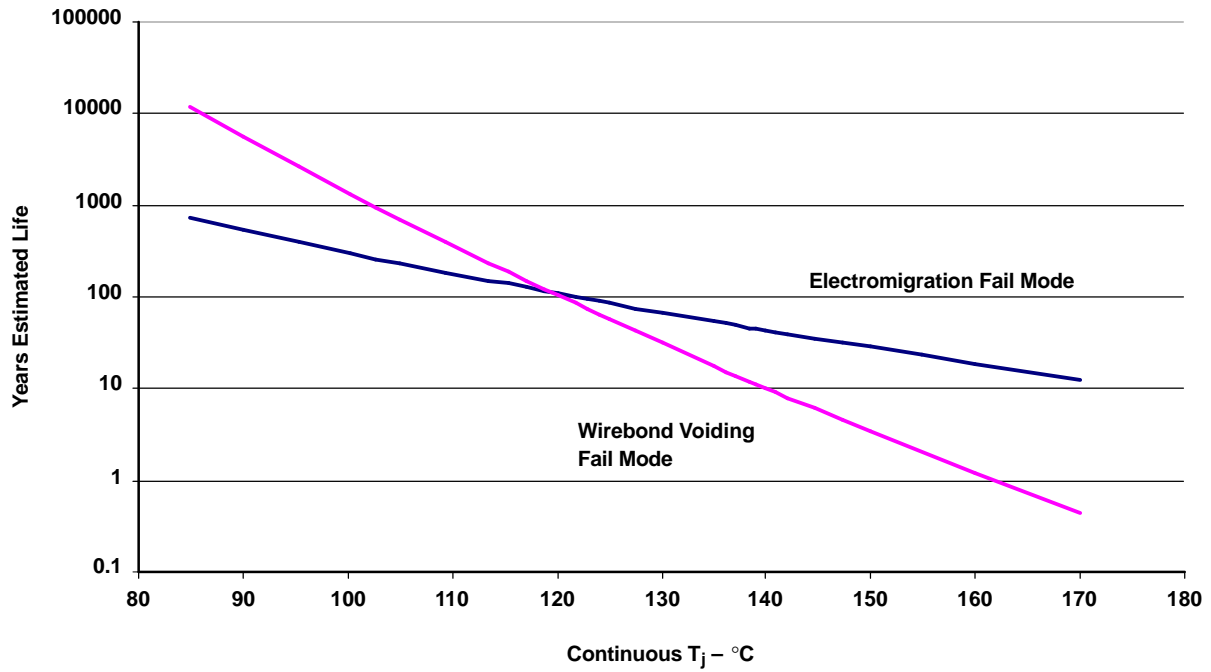


Figure 2. CABT16373AMDLREP Operating Life Derating Chart



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CABT16373AMDREP	ACTIVE	SSOP	DL	48	1000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	ABT16373AMEP	<a href="#">Samples</a>
V62/06628-01XE	ACTIVE	SSOP	DL	48	1000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	ABT16373AMEP	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN74ABT16373A-EP :**

- Catalog: [SN74ABT16373A](#)
- Military: [SN54ABT16373A](#)

## NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CABT16373AMDREP	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS



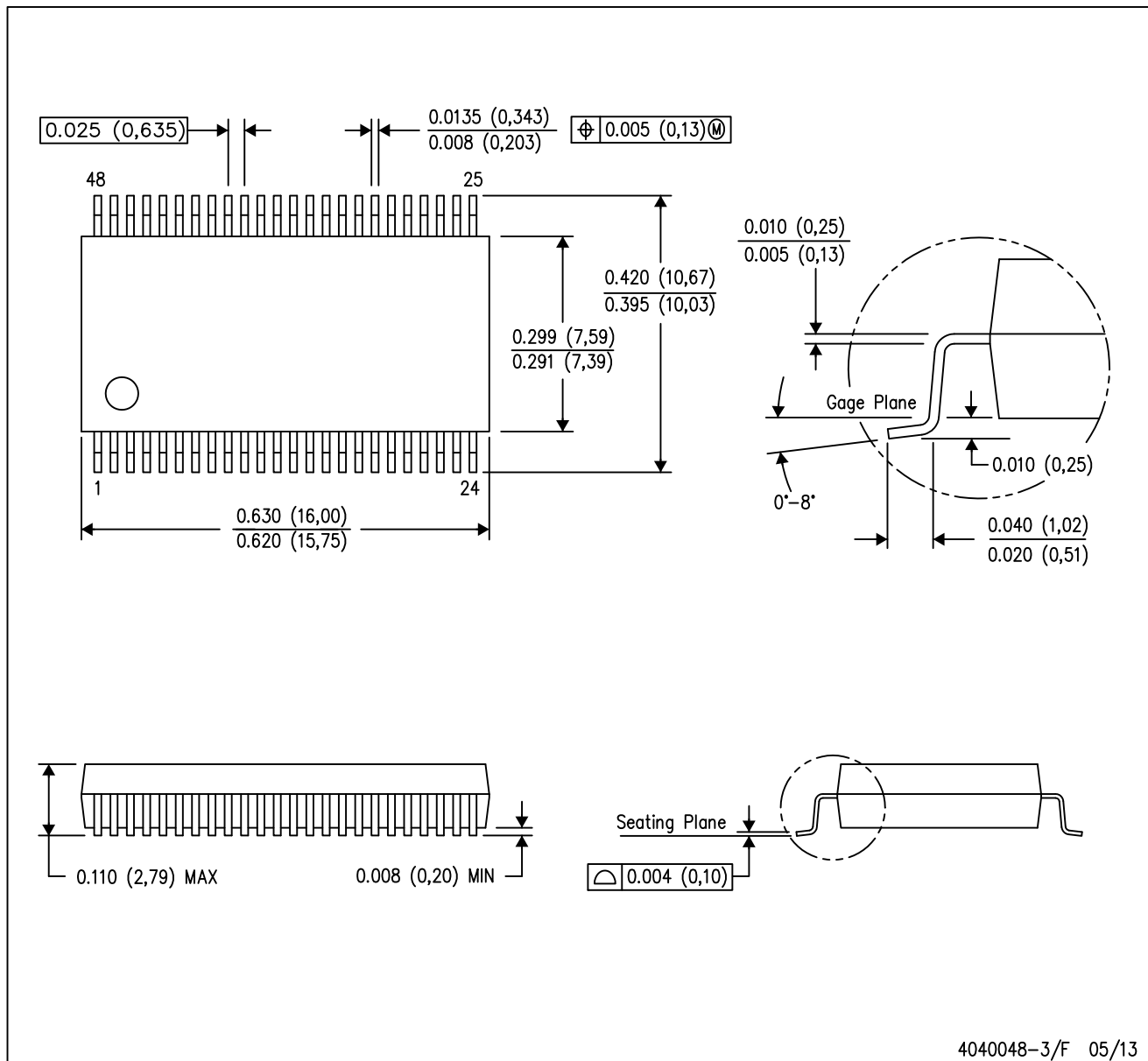
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CABT16373AMDREP	SSOP	DL	48	1000	367.0	367.0	55.0

# MECHANICAL DATA

DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MO-118

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