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FDMT1D3N08B

N-Channel Dual Cool™ 88 PowerTrench® MOSFET

80 V, 164 A, 1.35 mΩ

Features

- Max $r_{DS(on)}$ = 1.35 mΩ at $V_{GS} = 10$ V, $I_D = 36$ A
- Max $r_{DS(on)}$ = 1.8 mΩ at $V_{GS} = 8$ V, $I_D = 31$ A
- Advanced Package and Silicon Combination for Low $r_{DS(on)}$ and High Efficiency
- Next Generation Enhanced Body Diode Technology, Engineered for Soft Recovery
- Low Profile 8x8 mm MLP Package
- MSL1 Robust Package Design
- 100% UIL Tested
- RoHS Compliant

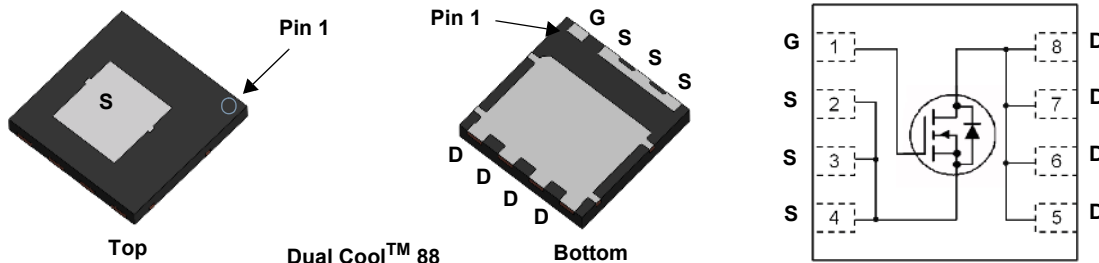


General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process. Advancements in both silicon and Dual Cool™ package technologies have been combined to offer the lowest $r_{DS(on)}$ while maintaining excellent switching performance by extremely low Junction-to-Ambient thermal resistance.

Applications

- OringFET / Load Switching
- Synchronous Rectification
- DC-DC Conversion



MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Rated	Units
V_{DS}	Drain to Source Voltage	80	V
V_{GS}	Gate to Source Voltage	± 20	V
I_D	Drain Current -Continuous	$T_C = 25^\circ\text{C}$ (Note 5)	164
	-Continuous	$T_C = 100^\circ\text{C}$ (Note 5)	103
	-Continuous	$T_A = 25^\circ\text{C}$ (Note 1a)	36
	-Pulsed	(Note 4)	864
E_{AS}	Single Pulse Avalanche Energy	(Note 3)	1734
P_D	Power Dissipation	$T_C = 25^\circ\text{C}$	178
	Power Dissipation	$T_A = 25^\circ\text{C}$ (Note 1a)	3.3
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Top Source)	1.9	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Bottom Drain)	0.7	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	38	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1b)	81	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1i)	15	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1j)	21	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1k)	9	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
1D3N08B	FDMT1D3N08B	Dual Cool™ 88	13"	13.3 mm	3000 units

Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\ \mu\text{A}, V_{GS} = 0\ \text{V}$	80			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$		50		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 64\ \text{V}, V_{GS} = 0\ \text{V}$			1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\ \text{V}, V_{DS} = 0\ \text{V}$			100	nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	2.0	3.2	4.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$		-11		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\ \text{V}, I_D = 36\ \text{A}$		1.1	1.35	m Ω
		$V_{GS} = 8\ \text{V}, I_D = 31\ \text{A}$		1.3	1.8	
		$V_{GS} = 10\ \text{V}, I_D = 36\ \text{A}, T_J = 125\text{ }^\circ\text{C}$		1.8	2.2	
g_{FS}	Forward Transconductance	$V_{DS} = 5\ \text{V}, I_D = 36\ \text{A}$		116		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 40\ \text{V}, V_{GS} = 0\ \text{V},$ $f = 1\ \text{MHz}$		14000	19600	pF
C_{oss}	Output Capacitance			2050	2870	pF
C_{rss}	Reverse Transfer Capacitance			50	150	pF
R_g	Gate Resistance		0.1	1.4	2.1	Ω

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 40\ \text{V}, I_D = 36\ \text{A},$ $V_{GS} = 10\ \text{V}, R_{GEN} = 6\ \Omega$		63	101	ns	
t_r	Rise Time			56	90	ns	
$t_{d(off)}$	Turn-Off Delay Time			68	109	ns	
t_f	Fall Time			20	32	ns	
$Q_{g(TOT)}$	Total Gate Charge		$V_{GS} = 0\ \text{V to } 10\ \text{V}$		186	260	nC
$Q_{g(TOT)}$	Total Gate Charge		$V_{GS} = 0\ \text{V to } 8\ \text{V}$	$V_{DD} = 40\ \text{V},$ $I_D = 36\ \text{A}$	152	213	nC
Q_{gs}	Gate to Source Charge			67		nC	
Q_{gd}	Gate to Drain "Miller" Charge			37		nC	
Q_{oss}	Output Charge	$V_{DD} = 40\ \text{V}, V_{GS} = 0\ \text{V}$		185		nC	

Drain-Source Diode Characteristics

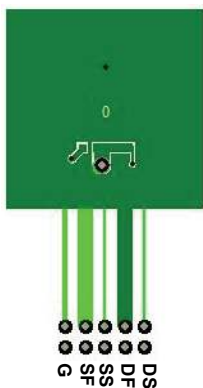
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\ \text{V}, I_S = 2.6\ \text{A}$ (Note 2)		0.7	1.1	V
		$V_{GS} = 0\ \text{V}, I_S = 36\ \text{A}$ (Note 2)		0.8	1.2	
t_{rr}	Reverse Recovery Time	$I_F = 36\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}$		83	132	ns
Q_{rr}	Reverse Recovery Charge			90	143	nC

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Top Source)	1.9	$^{\circ}\text{C}/\text{W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Bottom Drain)	0.7	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	38	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1b)	81	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1c)	26	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1d)	34	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1e)	14	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1f)	16	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1g)	26	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1h)	60	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1i)	15	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1j)	21	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1k)	9	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1l)	11	

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a FR-4 board using a specified pad of 2 oz copper as shown below. $R_{\theta CA}$ is determined by the user's board design.



a. 38 $^{\circ}\text{C}/\text{W}$ when mounted on a 1 in² pad of 2 oz copper



b. 81 $^{\circ}\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper

- c. Still air, 20.9x10.4x12.7mm Aluminum Heat Sink, 1 in² pad of 2 oz copper
- d. Still air, 20.9x10.4x12.7mm Aluminum Heat Sink, minimum pad of 2 oz copper
- e. Still air, 45.2x41.4x11.7mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, 1 in² pad of 2 oz copper
- f. Still air, 45.2x41.4x11.7mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, minimum pad of 2 oz copper
- g. 200FPM Airflow, No Heat Sink, 1 in² pad of 2 oz copper
- h. 200FPM Airflow, No Heat Sink, minimum pad of 2 oz copper
- i. 200FPM Airflow, 20.9x10.4x12.7mm Aluminum Heat Sink, 1 in² pad of 2 oz copper
- j. 200FPM Airflow, 20.9x10.4x12.7mm Aluminum Heat Sink, minimum pad of 2 oz copper
- k. 200FPM Airflow, 45.2x41.4x11.7mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, 1 in² pad of 2 oz copper
- l. 200FPM Airflow, 45.2x41.4x11.7mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0%.

3. E_{AS} of 1734 mJ is based on starting $T_J = 25^{\circ}\text{C}$; N-ch: $L = 3\text{ mH}$, $I_{AS} = 34\text{ A}$, $V_{DD} = 80\text{ V}$, $V_{GS} = 10\text{ V}$. 100% test at $L = 0.3\text{ mH}$, $I_{AS} = 77\text{ A}$.

4. Pulsed Id please refer to Fig 11 SOA graph for more details.

5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted.

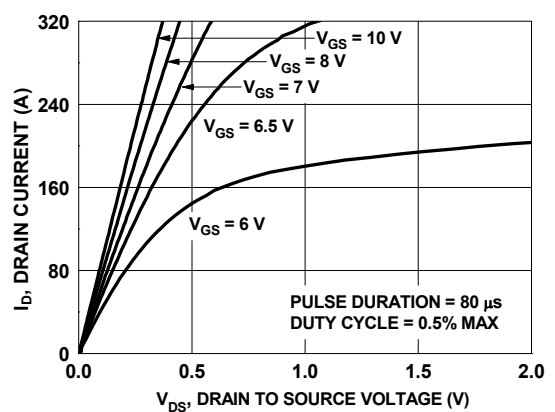


Figure 1. On Region Characteristics

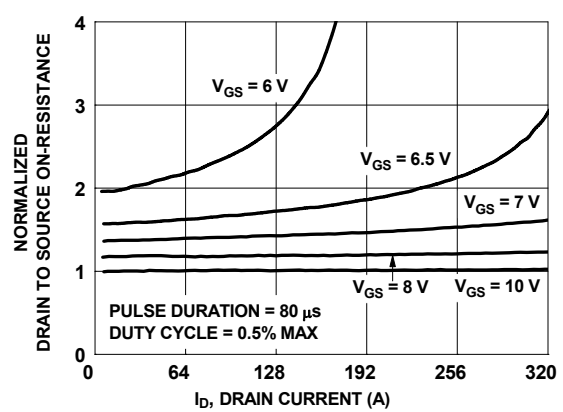


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

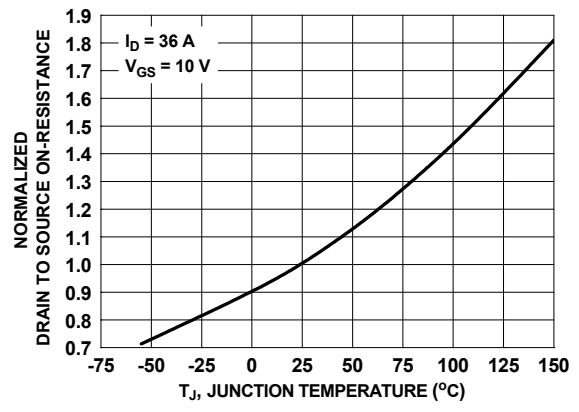


Figure 3. Normalized On Resistance vs. Junction Temperature

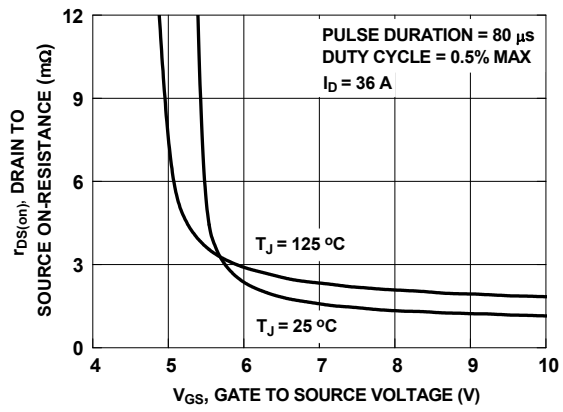


Figure 4. On-Resistance vs. Gate to Source Voltage

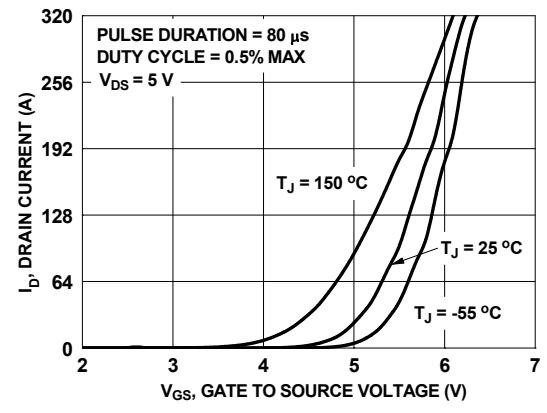


Figure 5. Transfer Characteristics

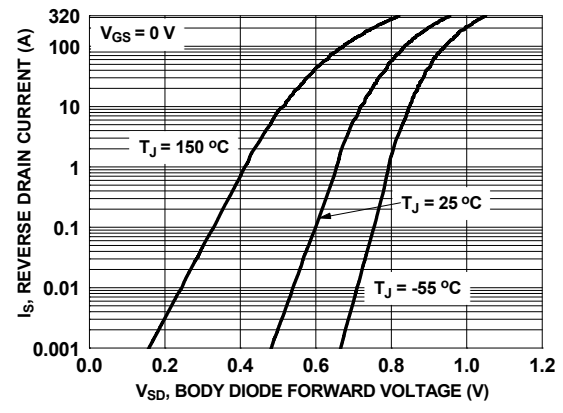


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted.

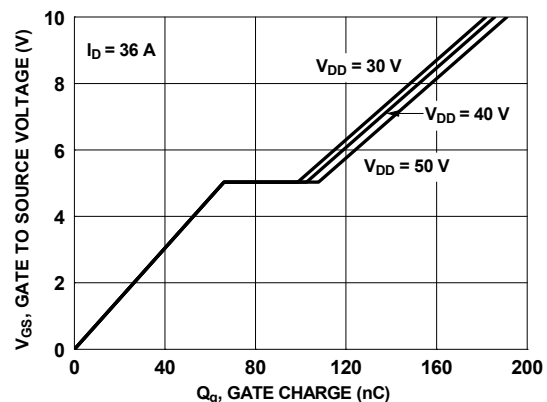


Figure 7. Gate Charge Characteristics

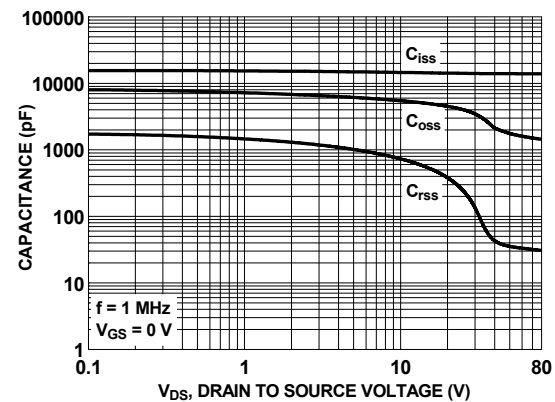


Figure 8. Capacitance vs. Drain to Source Voltage

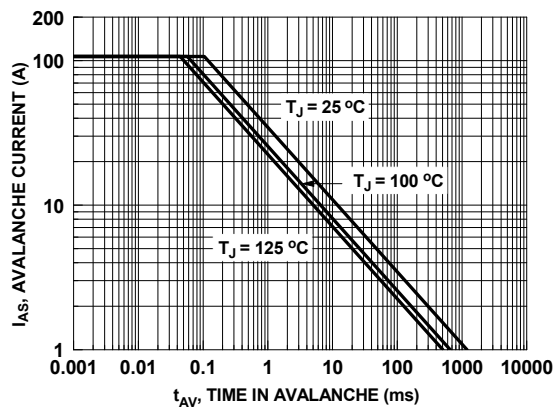


Figure 9. Unclamped Inductive Switching Capability

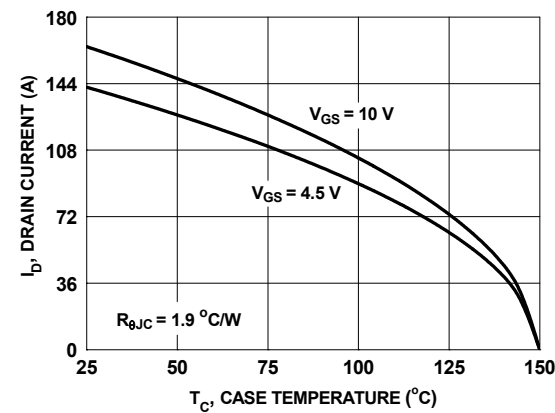


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

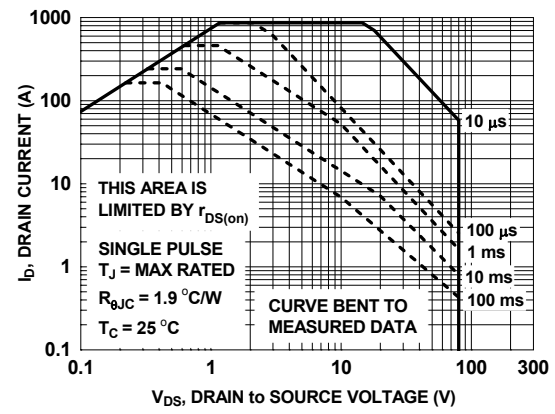


Figure 11. Forward Bias Safe Operating Area

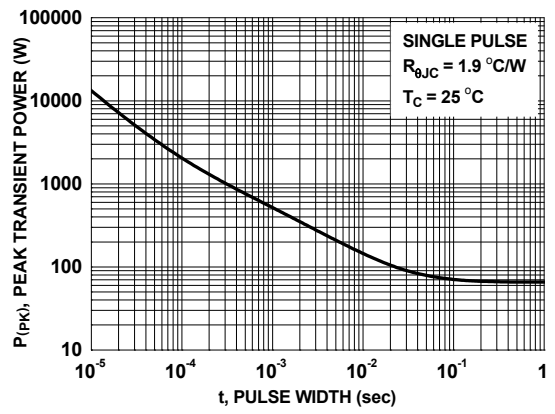


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted.

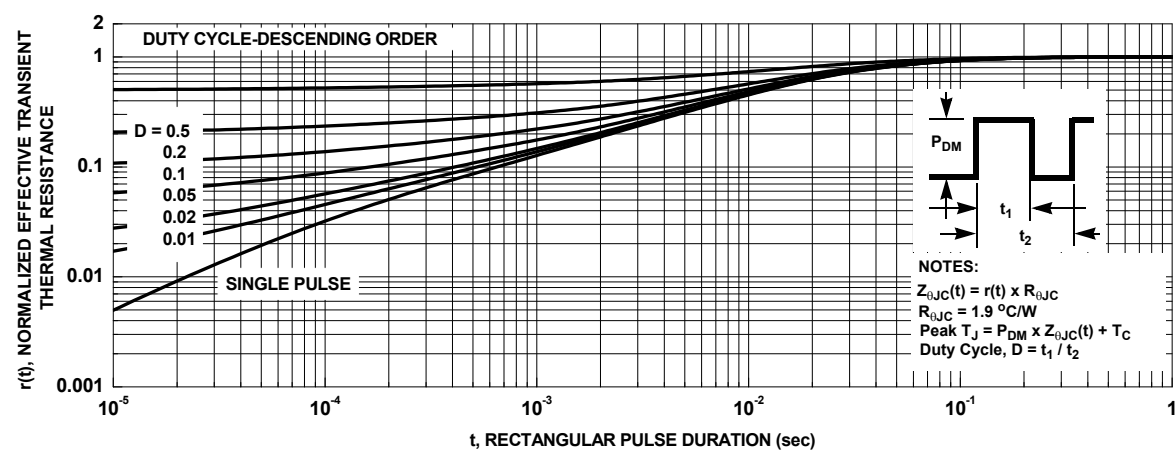
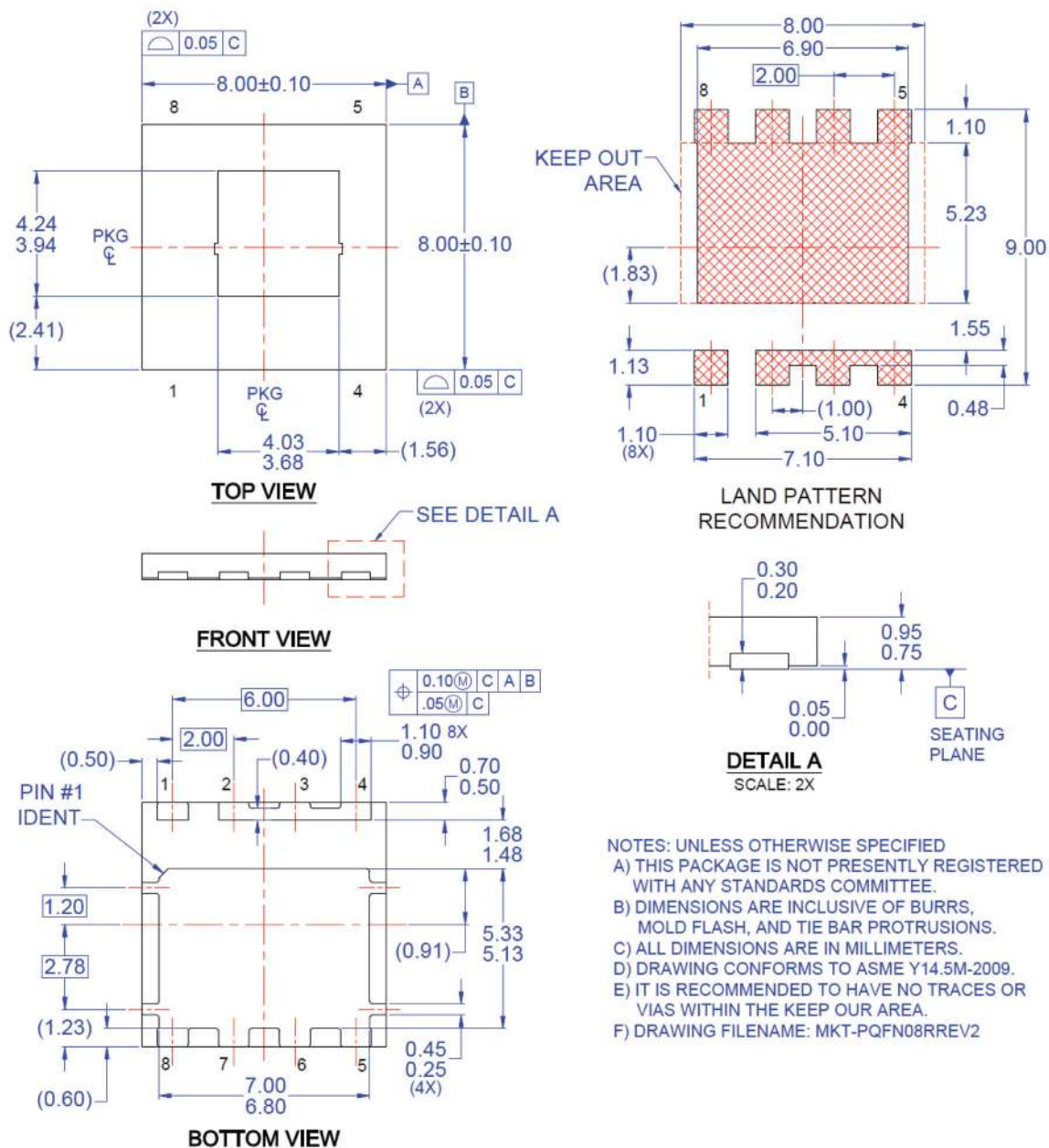


Figure 13. Junction-to-Case Transient Thermal Response Curve

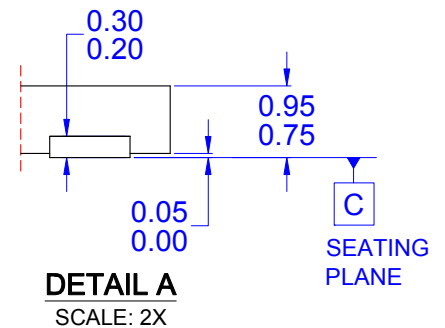
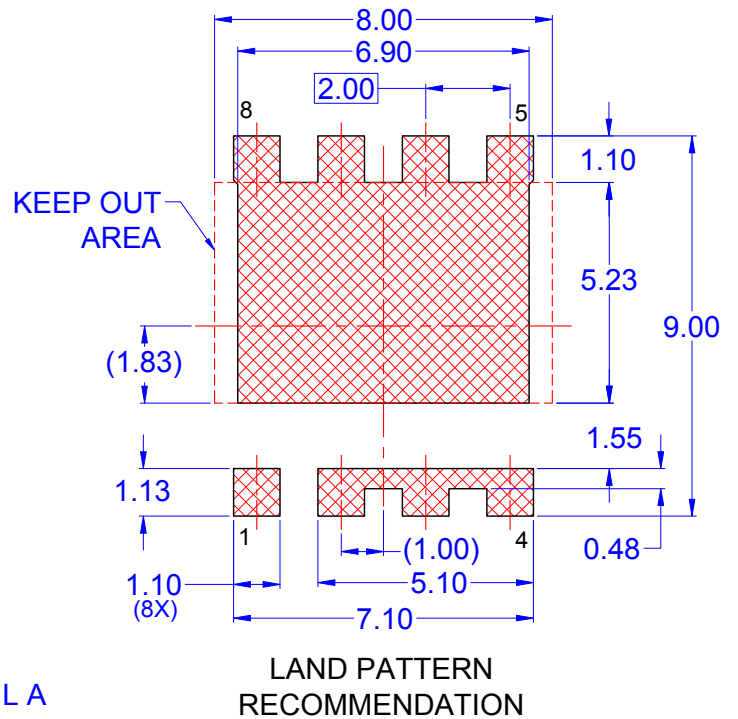
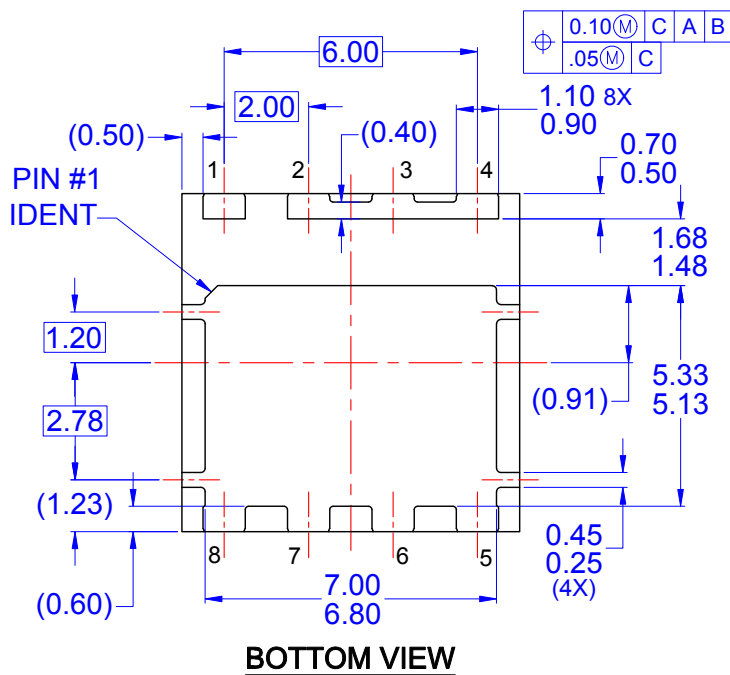
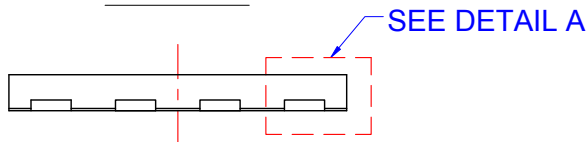
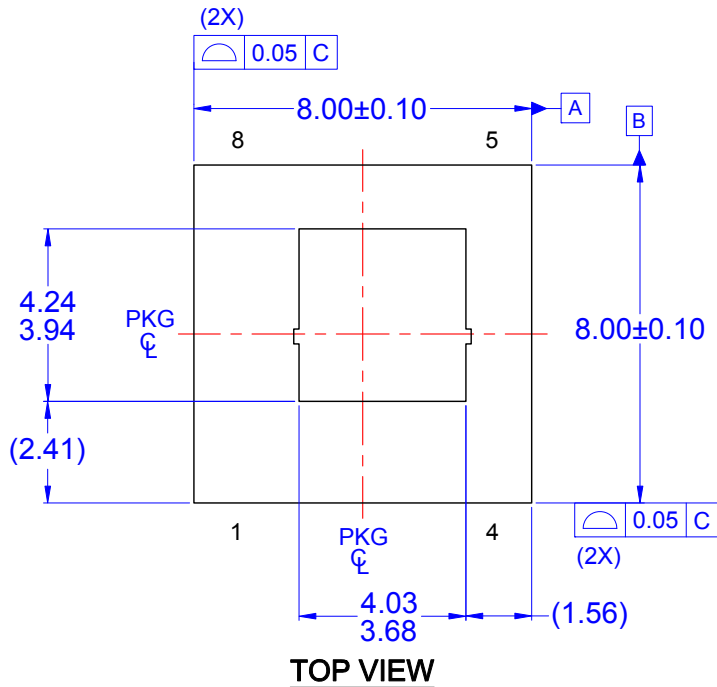
Dimensional Outline and Pad Layout



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