NAU83P20
20W Stereo Class-D Audio Amplifier

GENERAL DESCRIPTION

The NAU83P20 is single supply, 20W, high efficiency, Class-D audio power stage for driving Stereo bridge-tied speakers. Operating from a single VDD 4.5V-24V supply, the design includes under-voltage, over-current and over-temperature detection.

NAU83P20 is available in the QFN 48 package.

FEATURES

- Class D power 2x20W into 8Ohms (10% THD)
- Typical power efficiency of 90%
- 105dB SNR
- Supports multiple output configurations:
  - 2-CH Bridged outputs (20Wx2)
  - 4-CH single ended outputs (10Wx4)
  - 2-CH single ended + 1-CH bridged (10Wx2 + 20Wx1)
- Fault Detection:
  - Over-Temperature
  - Under-Voltage
  - Over-Current

Applications

- LCD TV's
- TV sound bars
- Car Audio
- Portable Media "Boom Boxes"
- Home entertainment systems

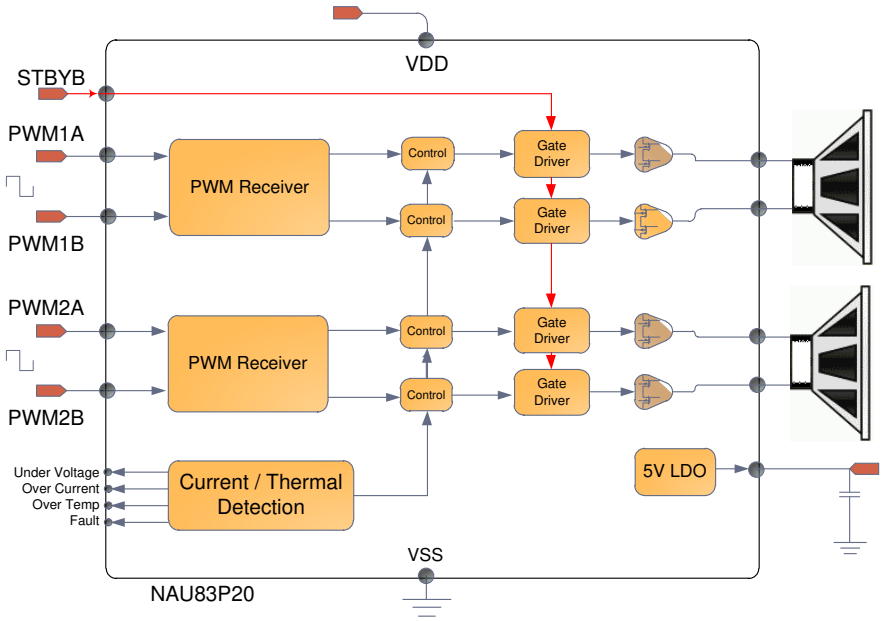
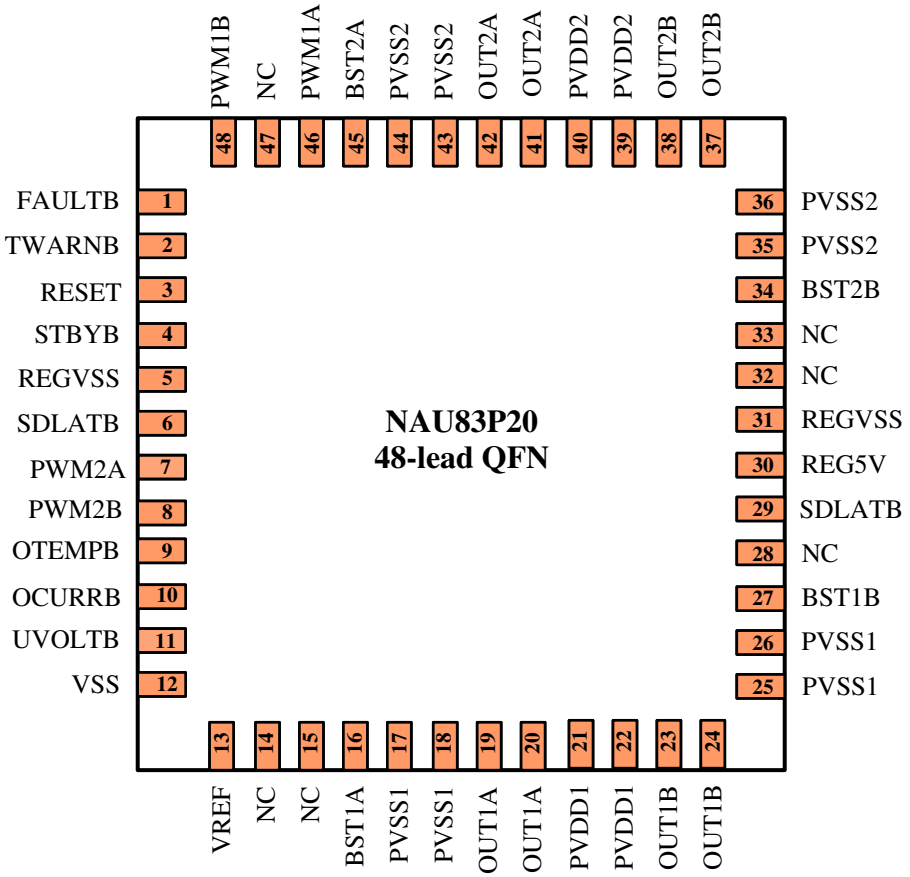


Figure 1: NAU83P20 Block Diagram

1 Pinout



Part Number	Dimension	Package	Package Material
NAU83P20YGB	7 x 7 mm	48-QFN	Green

2 Pin Descriptions

Pin #	Name	Type	Functionality
1	FAULTB	Digital Output	Device Error Signal. Active Low if Over current, Under Voltage or Over temperature faults occur. Open Drain Output w/ 100KOhm Pull Up
2	TWARNB	Digital Output	Over Temperature Warning Signal. Active Low if device internal temperature is 110°C. Open Drain Output
3	RESET	Digital Input	Resets SDLATB.
4	STBYB	Digital Input	Standby Bar, Disables all 4 PWM Outputs. 100KOhm Pull Down
5	REGVSS	Supply	5V Regulator Ground
6	SDLATB	Digital Output	Device Shutdown Latch Signal, This signal will latch low, if the Over current fault occurs. This flag is cleared by RESET. Open Drain Output
7	PWM2A	PWM Input	Channel 2A Pulse Width Modulation Signal Input. 150kΩ PullDown
8	PWM2B	PWM Input	Channel 2B Pulse Width Modulation Signal Input. 150kΩ PullDown
9	OTEMPB	Digital Output	Over Temperature Fault Signal. Active Low if device internal temperature is 140°C. Open Drain Output
10	OCURRB	Digital Output	Over Current Fault Signal. Active Low if current drawn from any of the output drivers is > 5A. Open Drain Output
11	UVOLTB	Digital Output	Under Voltage Fault Signal. Active Low if the supply voltage is under 3.5V. Open Drain Output
12	VSS	Supply	Ground
13	VREF	Output	Internal Reference Voltage
14	N/C	-	No Connect
15	N/C	-	No Connect
16	BST1A	Supply	Channel 1A High Side Bootstrap Supply
17	PVSS1	Supply	Channel 1 Power Ground
18	PVSS1	Supply	Channel 1 Power Ground
19	OUT1A	PWM Output	Channel 1A Pulse Width Modulation Signal Output
20	OUT1A	PWM Output	Channel 1A Pulse Width Modulation Signal Output
21	PVDD1	Supply	Channel 1 Power Supply
22	PVDD1	Supply	Channel 1 Power Supply
23	OUT1B	PWM Output	Channel 1B Pulse Width Modulation Signal Output
24	OUT1B	PWM Output	Channel 1B Pulse Width Modulation Signal Output
25	PVSS1	Supply	Channel 1 Power Ground
26	PVSS1	Supply	Channel 1 Power Ground
27	BST1B	Supply	Channel 1B High Side Bootstrap Supply
28	N/C	-	No Connect

29	N/C	-	No Connect
30	REG5V	Supply Output	5V Regulator Supply Output
31	REGVSS	Supply	5V Regulator Ground
32	N/C	-	No Connect
33	N/C	-	No Connect
34	BST2B	Supply	Channel 2B High Side Bootstrap Supply
35	PVSS2	Supply	Channel 2 Power Ground
36	PVSS2	Supply	Channel 2 Power Ground
37	OUT2B	PWM Output	Channel 2B Pulse Width Modulation Signal Output
38	OUT2B	PWM Output	Channel 2B Pulse Width Modulation Signal Output
39	PVDD2	Supply	Channel 2 Power Supply
40	PVDD2	Supply	Channel 2 Power Supply
41	OUT2A	PWM Output	Channel 2A Pulse Width Modulation Signal Output
42	OUT2A	PWM Output	Channel 2A Pulse Width Modulation Signal Output
43	PVSS2	Supply	Channel 2 Power Ground
44	PVSS2	Supply	Channel 2 Power Ground
45	BST2A	Supply	Channel 2A High Side Bootstrap Supply
46	PWM1A	PWM Input	Channel 1A Pulse Width Modulation Signal Input. 150kΩ PullDown
47	N/C	-	No Connect
48	PWM1B	PWM Input	Channel 1B Pulse Width Modulation Signal Input. 150kΩ PullDown

Table 1: NAU83P20 Pin description

Table of Contents

3 Electrical Characteristics

3.1 AC Characteristics (Bridge Tied Load)

Conditions: PVDDx = 18V, R_{load} = 8 Ohms, Audio Frequency = 1KHz, AES17 filter, F_PWM = 300KHz, Ambient temp = 25C. NAU82011 are used as input device unless otherwise stated

Parameter	Symbol	Comments/Conditions		Min	Typ	Max	Units
Power Delivered							
Power Output per Channel	P_o	Z_L = 8Ω + 68μH THD + N = 10%	PVDDx = 18V		20		W
			PVDDx = 12V		9		
		Z_L = 8Ω + 68μH THD + N = 1%	PVDDx = 18V		17		
			PVDDx = 12V		7		
Total Harmonic Distortion + Noise	THD+ N	Po=10W (Half Power)	PVDDx = 18V		0.4		%
		Po=4.5W(Half Power)	PVDDx = 12V		0.3		
Output Integrated Noise*	V_n	A-Weighted			50		uVrms
Signal to Noise Ratio*	SNR	A-Weighted			105		dB
Dynamic Range*	DNR	A-Weighted Input=-60dbFS			85		dB
Power Dissipation Due to Idle Losses	P_D	P_o=0W, 4 channels switching			0.8		W

* Using a signal generator with the same input applied to all channels

3.2 AC Characteristics (Single Ended)

Conditions: PVDDx = 18V, R_{load} = 8 Ohms, Audio Frequency = 1KHz, AES17 filter, F_PWM = 300KHz, Ambient temp = 25C NAU82011 are used as input device unless otherwise stated.

Parameter	Symbol	Comments/Conditions		Min	Typ	Max	Units
Power Delivered							
Power Output per Channel	P_o	Z_L = 8Ω + 68μH THD + N = 10%	PVDDx = 18V		10		W
			PVDDx = 12V		4.5		
		Z_L = 8Ω + 68μH THD + N = 1%	PVDDx = 18V		8.5		
			PVDDx = 12V		3.5		
Total Harmonic Distortion + Noise	THD+ N	Po=10W (Half Power)	PVDDx = 18V		0.4		%
		Po=4.5W(Half Power)	PVDDx = 12V		0.3		
Output Integrated Noise	V_n	A-Weighted			50		uVrms
Signal to Noise Ratio*	SNR	A-Weighted			105		dB
Dynamic Range*	DNR	A-Weighted Input=-60dbFS			85		dB
Power Dissipation Due to Idle Losses	P_D	P_o=0W, 4 channels switching			0.8		W

*Using a signal generator with the same input applied to all channels

3.3 DC Characteristics

Conditions: PVDDx = 18V R_{load} = 8Ohms, F_PWM = 300KHz

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
Half-bridge supply	PVDDX		4.5	18	24	V
Quiescent Current Consumption	I_{QUI}	STBYB= 1 Input at 50% duty cycle with output filter		60		mA
		STBYB= 0 Input at 50% duty cycle with output filter		13		mA
I/O Detection						
Under voltage detection limit, falling	V_{uvp}			3.5		V
Under voltage detection limit, rising	V_{uvp}			4.2		V
Over temperature warning	OTW			110		ºC
Over temperature Error	OTE			140		ºC
Over temperature Hysteresis	OTW_{HYST}			30		ºC
Overcurrent Limit detection	I_{OC}			5		A
Overcurrent Response Time	I_{OCT}	22uH O/P Inductor		15		us
High-level input voltage	V_{IH}	PWM1A/1B/2A/2B, STBY	2.0		5.0	V
Low-level input voltage	V_{IL}				0.8	V
Input leakage Current, High	I_{lkg}	PWM1A/1B/2A/2B, STBY			100	uA
Input leakage Current, Low			-10		10	

3.4 Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply	-0.50	25	V
Industrial operating temperature	-40	+85	°C
Storage temperature range	-65	+150	°C
Junction temperature range	-40	+150	°C

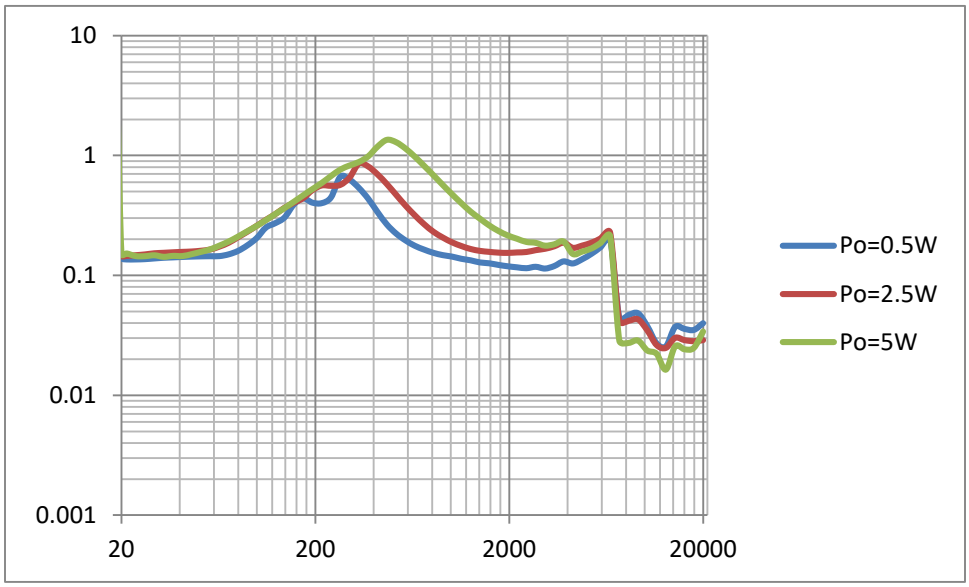
CAUTION: Do not operate at or near the maximum ratings listed for extended periods. Exposure to such conditions may adversely influence product reliability and result in failures not covered by warranty.

3.5 Recommended Operating Conditions

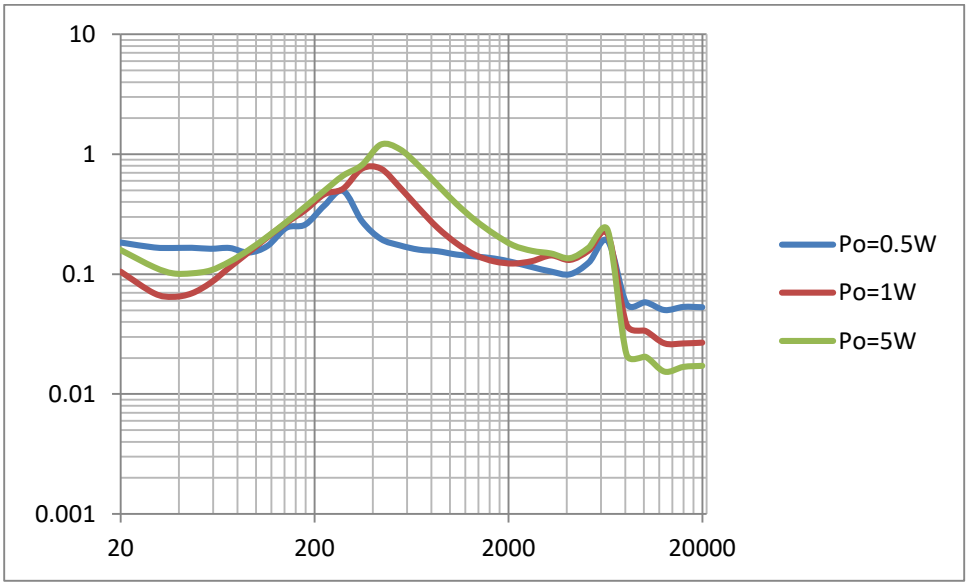
Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Supply range	PVDD1,2	DC supply voltage	4.5	18	24	V
Ground	VSS	DC Ground		0		V
PWM frame rate	F_{pwm}		192	384	432	Khz
Corresponding min pulse width of PWMIN			139	156	313	ns
Junction Temperature	Tj		0		125	ºC
Load Impedance	RL(BTL)	Output filter: L =10µH, C= 470nF Output AD modulation switching frequency >350Khz		6-8		Ω
	RL(SE)			3-4		Ω
	RL(PBTL)			3-4		Ω
Output Filter inductance	Lo(BTL)	Minimum output inductance under short circuit condition		200		nH
	Lo(SE)			200		nH
	Lo(PBTL)			200		nH

4 Typical Operating Characteristics

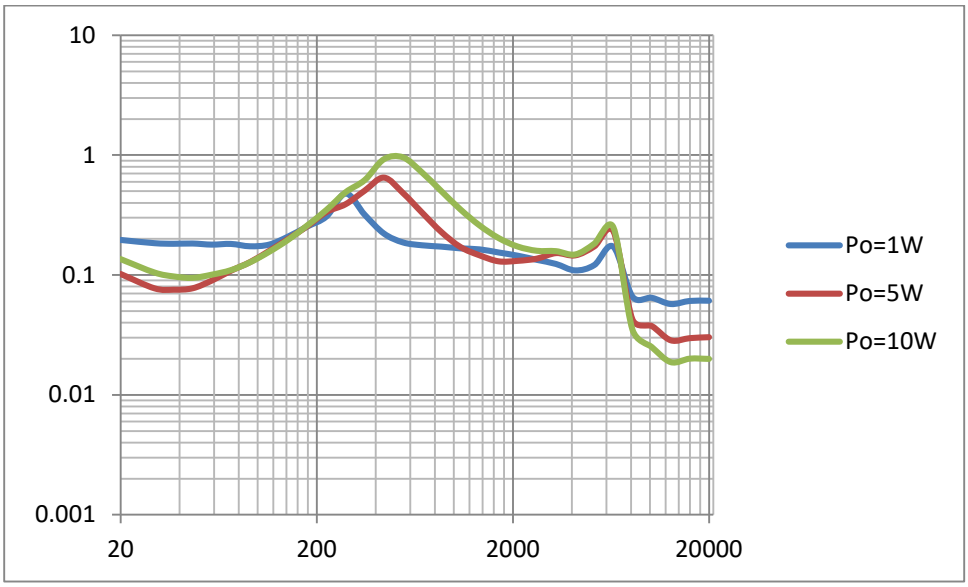
4.1 BTL



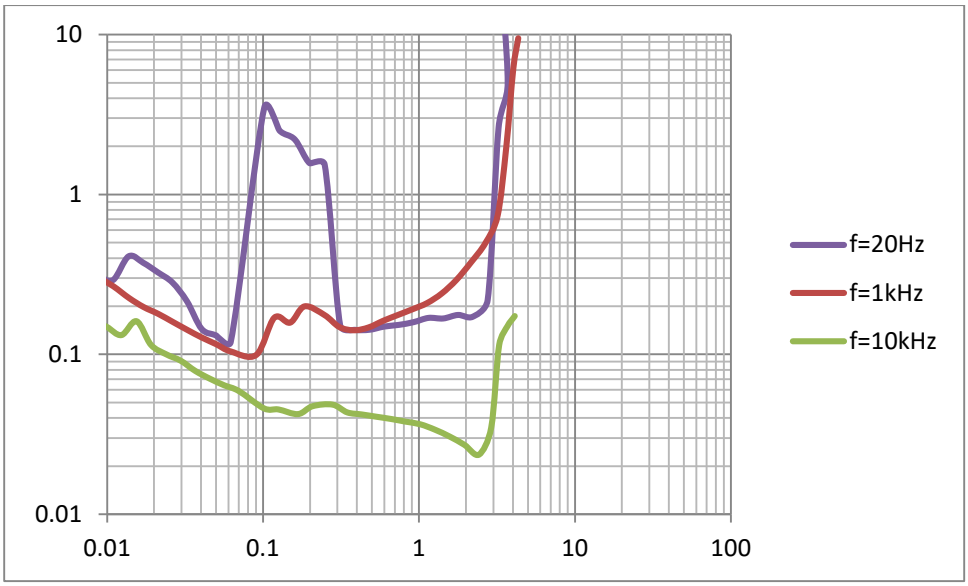
THD+N vs Frequency, Vcc=8V, Rl= 8 BTL



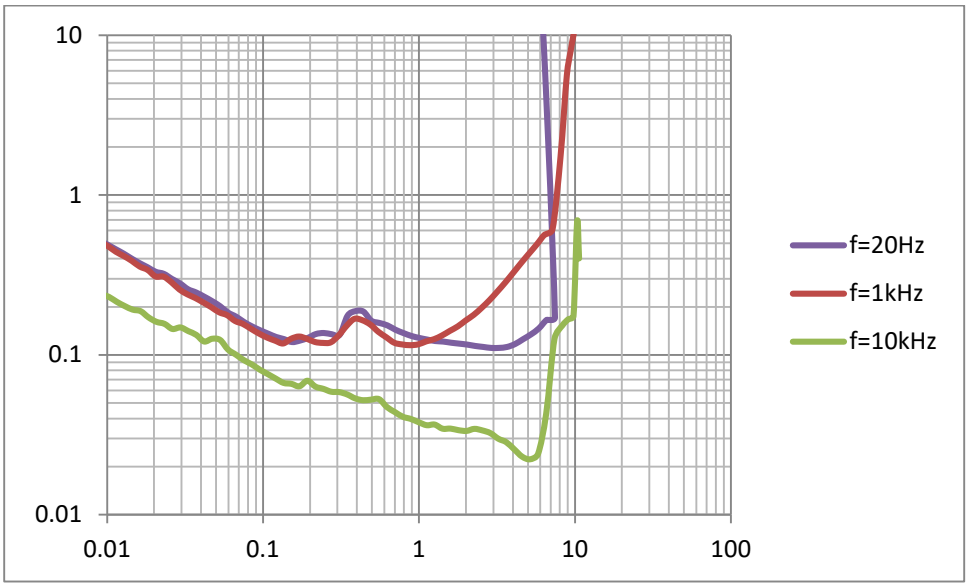
THD+N vs Frequency, Vcc=12V, Rl= 8 BTL



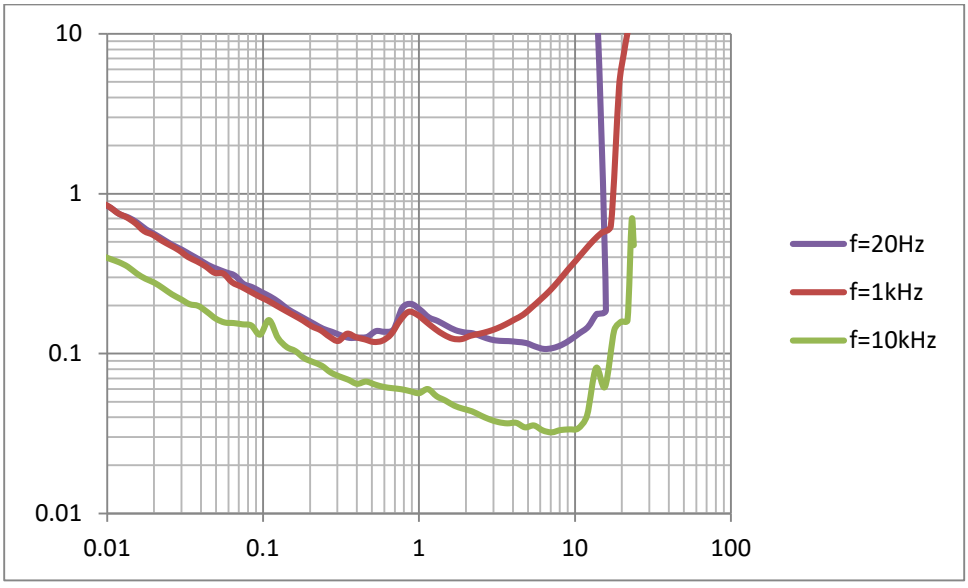
THD+N vs Frequency, Vcc=18V, Rl= 8 BTL



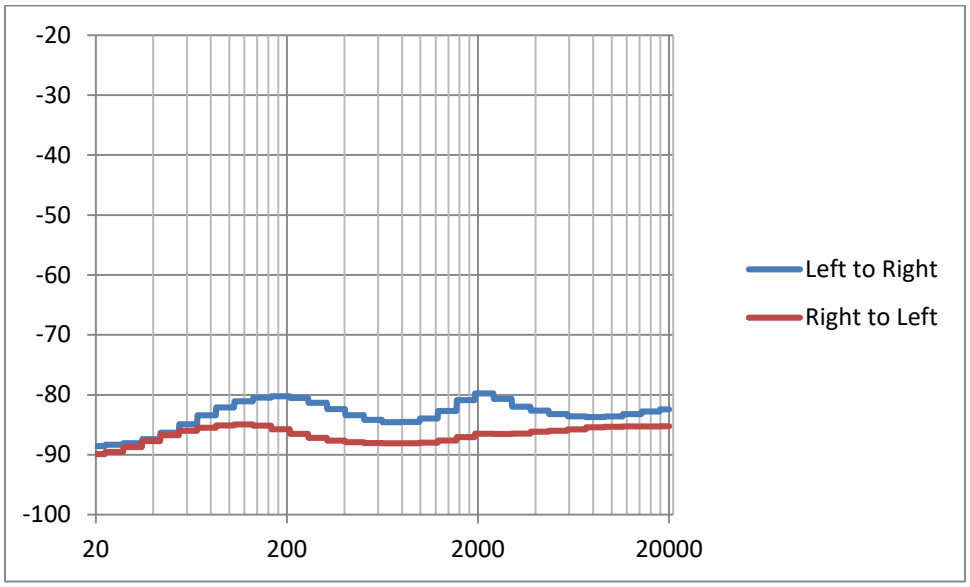
THD+N vs Output Power Vcc=8V, Rl= 8 BTL



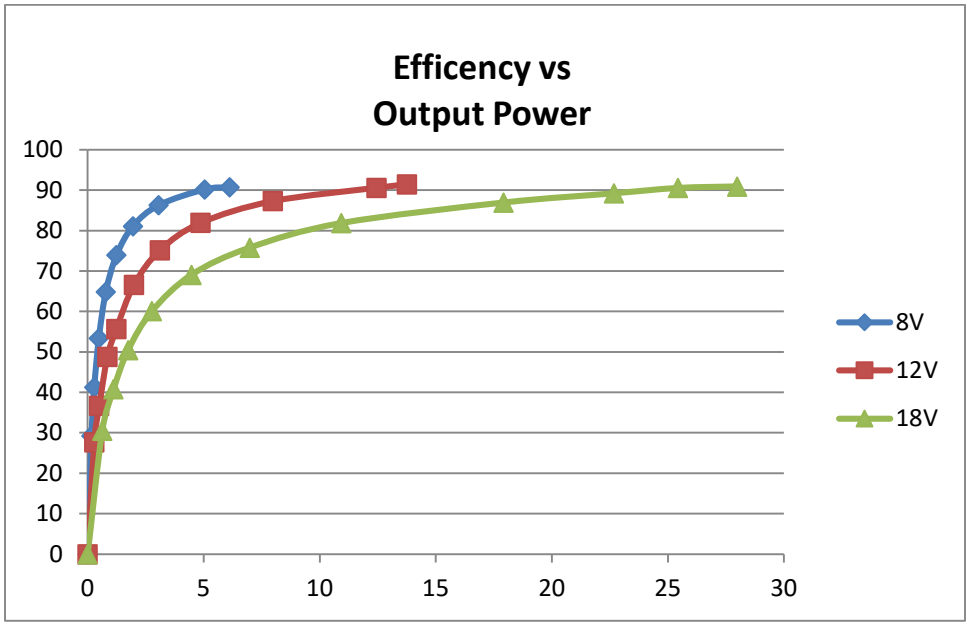
THD+N vs Output Power Vcc=12V, Rl= 8 BTL



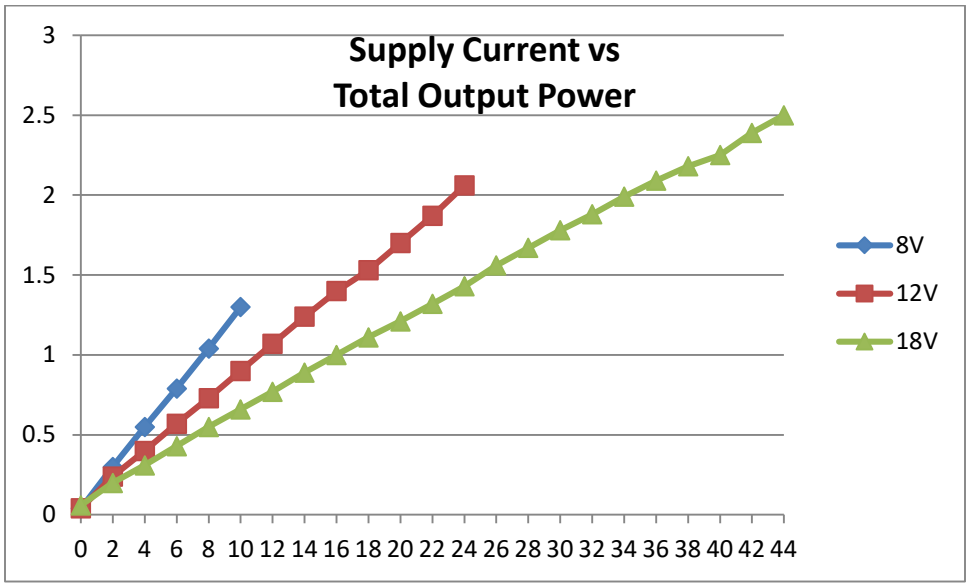
THD+N vs Output Power Vcc=8V, Rl= 8 BTL



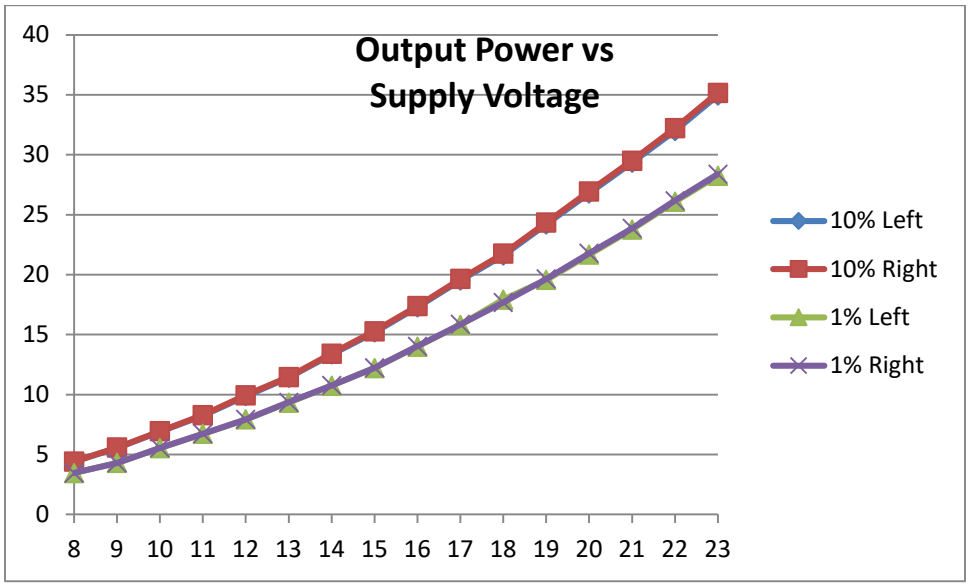
Crosstalk vs Frequency Vcc=18V Rl=4 Po=0.25W BTL



F=1kHz Rl=8 BTL



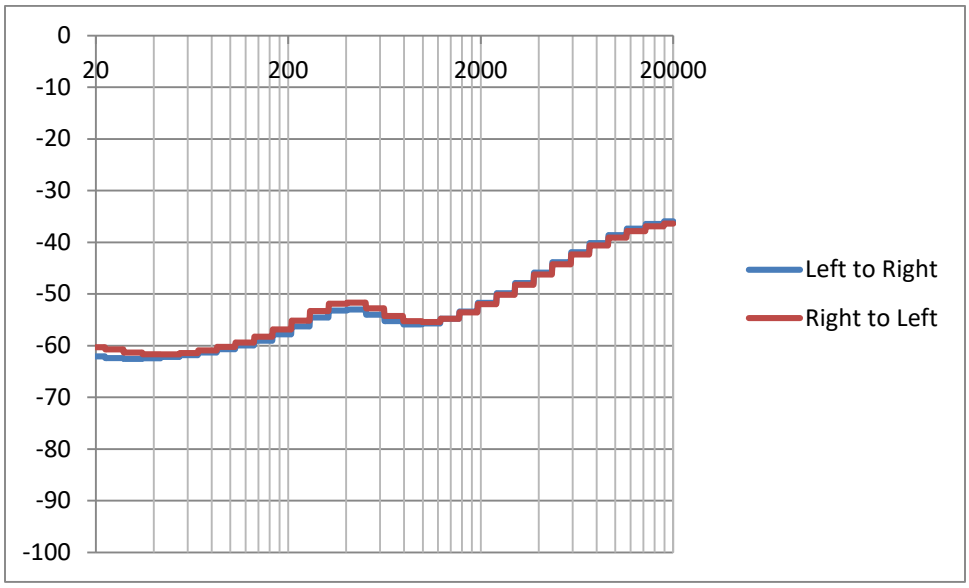
F=1kHz Rl=8 BTL



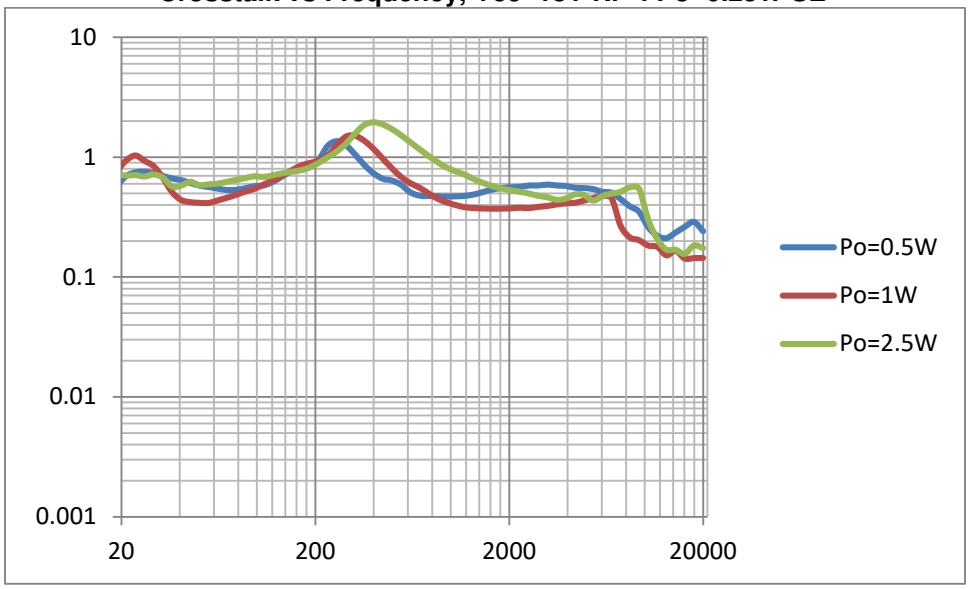
F=1kHz Rl=8 BTL

5 Typical Operating Characteristics

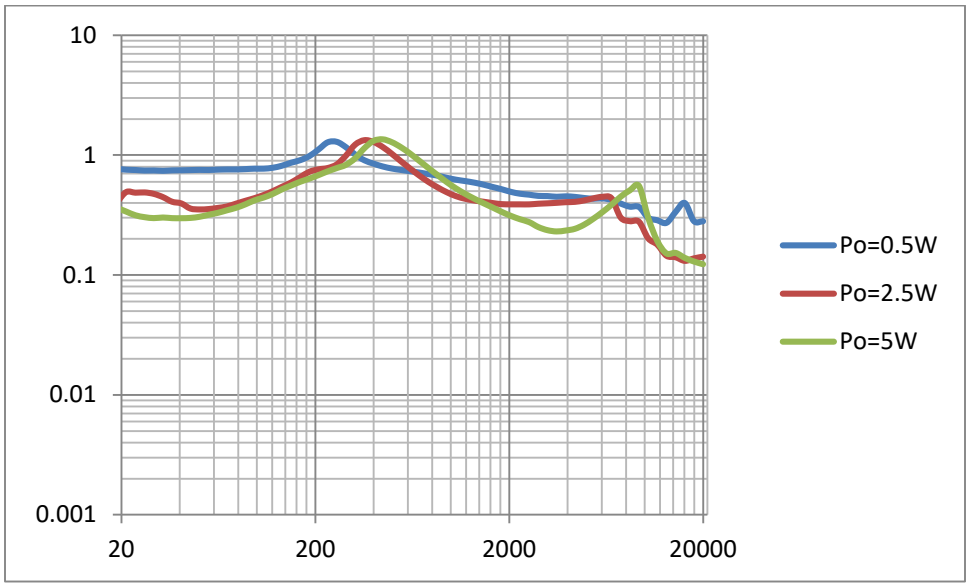
5.1 SE



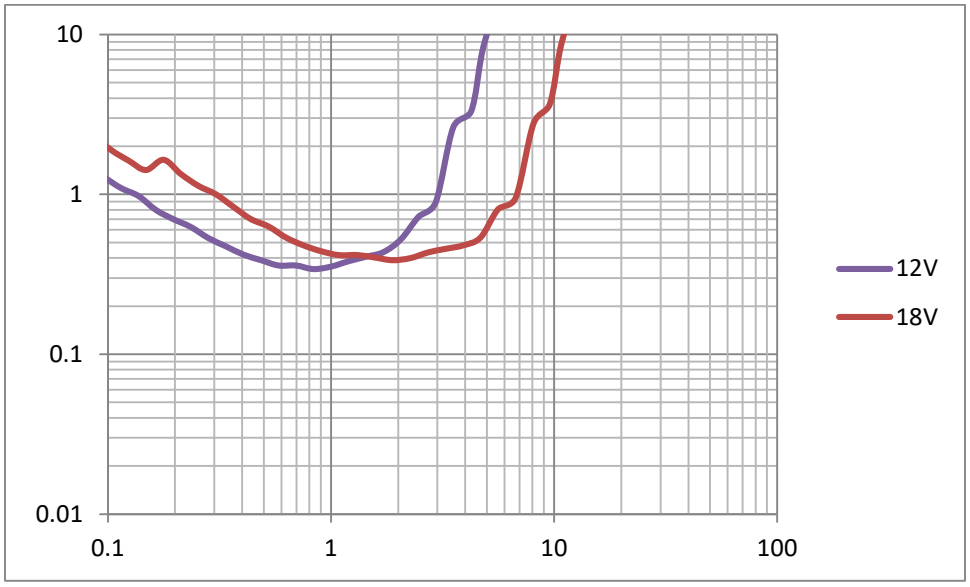
Crosstalk vs Frequency, Vcc=18V Rl=4 Po=0.25W SE



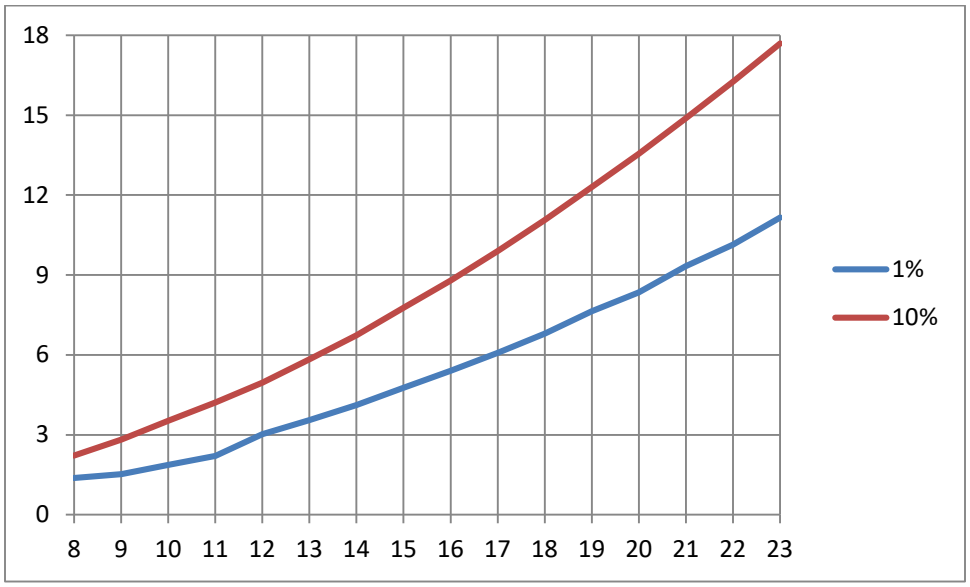
THD+N vs Frequency, Vcc=12V Rl=4 SE



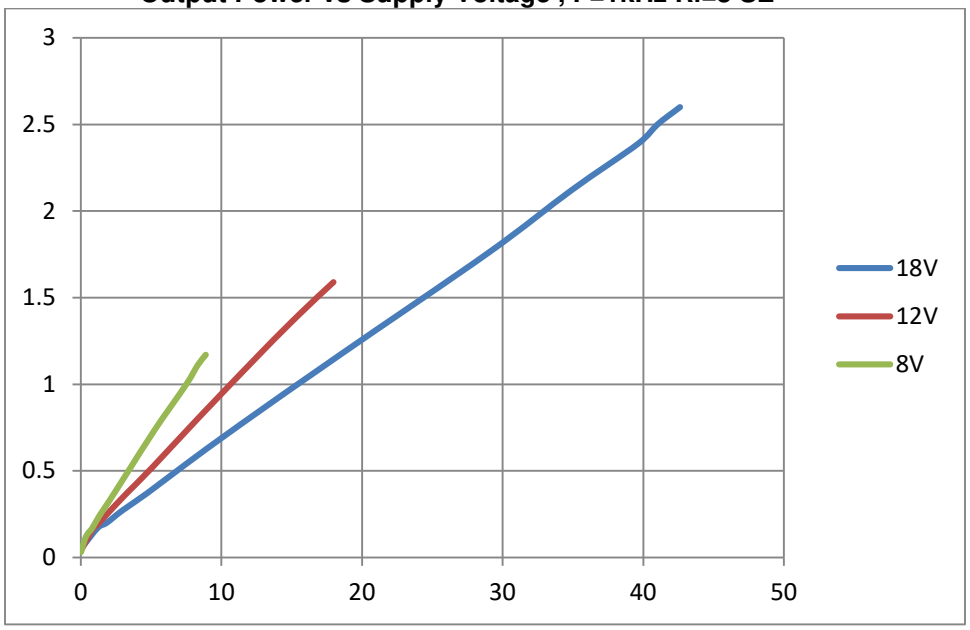
THD+N vs Frequency, Vcc=18V Rl=4 SE



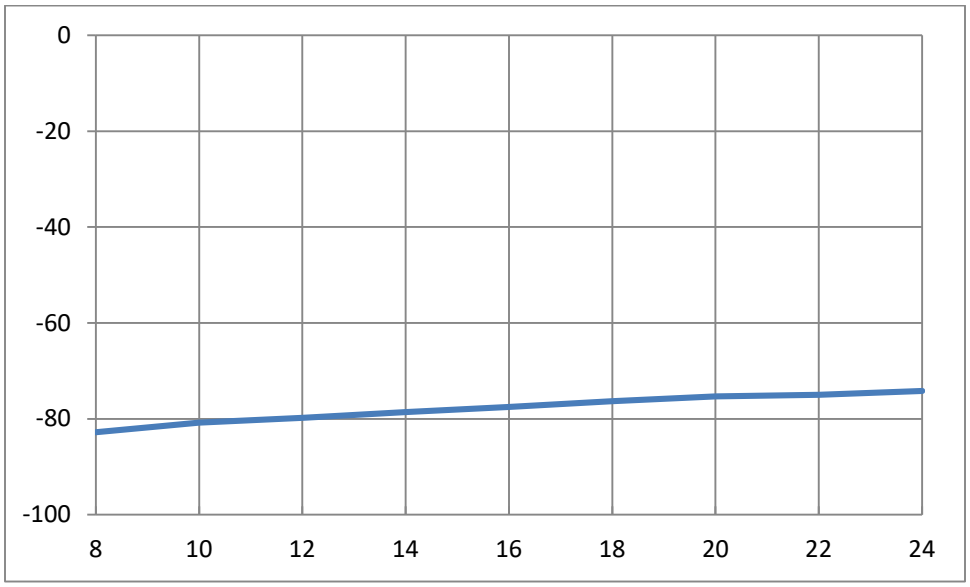
THD+N vs Output Power, F=1kHz Rl=4 SE



Output Power vs Supply Voltage , F=1kHz Rl=8 SE



Supply Current vs Output Power, F=1kHz Rl=4 SE



A-Weighted Noise vs Supply Voltage, F=1kHz Rl=4 SE

6 Special Feature Description

The NAU83P20, in addition to high efficiency, also provides the following fault detection features.

6.1 Device Fault Detection

The NAU83P20 includes device fault detection for three operating scenarios. They are

1. Thermal Overload
2. Short circuit
3. Supply under voltage

6.1.1 Thermal Overload Detection

When the device internal junction temperature reaches 125°C, the NAU83P20 will force the TWARNB digital output low. If the temperature continues to rise to 150°C, the NAU83P20 will force the OTEMPB digital output low. When the device cools down and a safe operating temperature of 125°C has been reached, the TWARNB and OTEMPB digital outputs will return to their default states, high. The processor controlling the NAU83P20 needs to respond to the TWARNB and the OTEMPB signals to ensure that the part operates within the specified temperature range or permanent damage can be caused.

An OTEMPB transition low will also force SDLATB to latch low.

6.1.2 Short Circuit Detection

If a short circuit condition is detected on any of the output drivers the NAU83P20 will force the OCURRB digital output to pulse low. The short circuit threshold is 7A.

An OCURRB transition low will also force SDLATB to latch low. SDLATB may be tied to STBYB, as shown in Figure 2. This will force the output drivers into a high impedance state upon a short circuit condition. SDLATB will remain low until a RESET transition has been performed and the short circuit condition has been removed. It is highly recommended that this configuration be used to prevent damage to the part.

6.1.3 Supply under Voltage Detection

If the supply voltage drops under 3.5V, the NAU83P20 will force the UVOLTB digital output low. UVOLTB digital output will remain low until the supply voltage returns to a level > 4.2V. The processor controlling the NAU83P20 needs to respond to the UVOLTB signal to ensure that the part operates within the specified voltage range or permanent damage can be caused.

An UVOLTB transition low will also force SDLATB to latch low.

6.2 Power up and Power down Control

When the PVDD supply voltage ramps up, the 5V LDO also powers up. The STBYB pin only controls the operation of the 4 half bridge drivers (see Figure 1). When STBYB is low, the 4 half bridge drivers are in the high impedance state. STBYB is high, enables the 4 half bridge drivers. The recommended power up sequence is to hold the STBYB pin low, apply the PVDD supply, wait until the 5V LDO is stable, start driving the PWM input signals and then bring STBYB high. Also perform a RESET transition to reset SDLATB (see also section 9.2.2)

7 Application Information

Differential BTL Application with Modulation Filters and EMI option

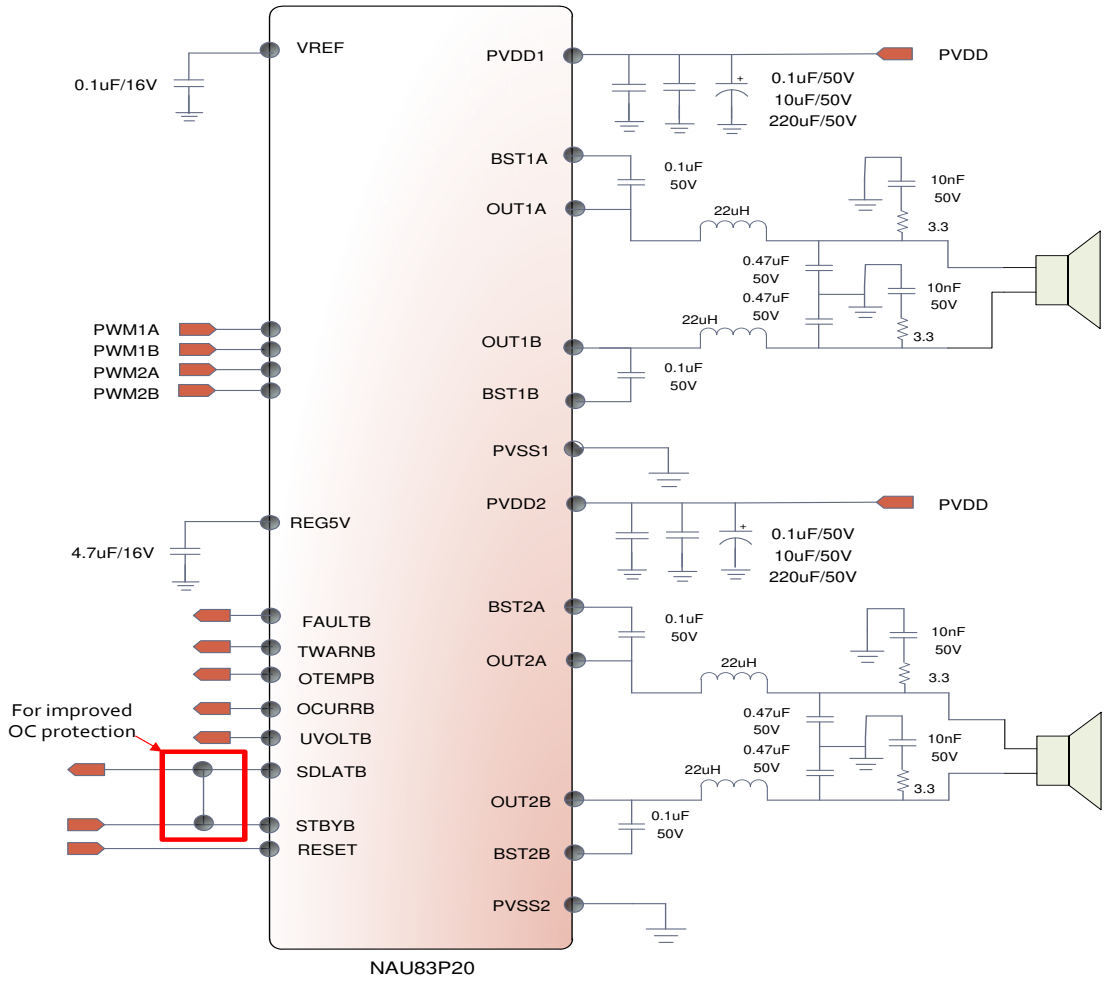


Figure 2: Differential BTL Application with Modulation Filters

Single Ended Application with Modulation Filters and EMI option

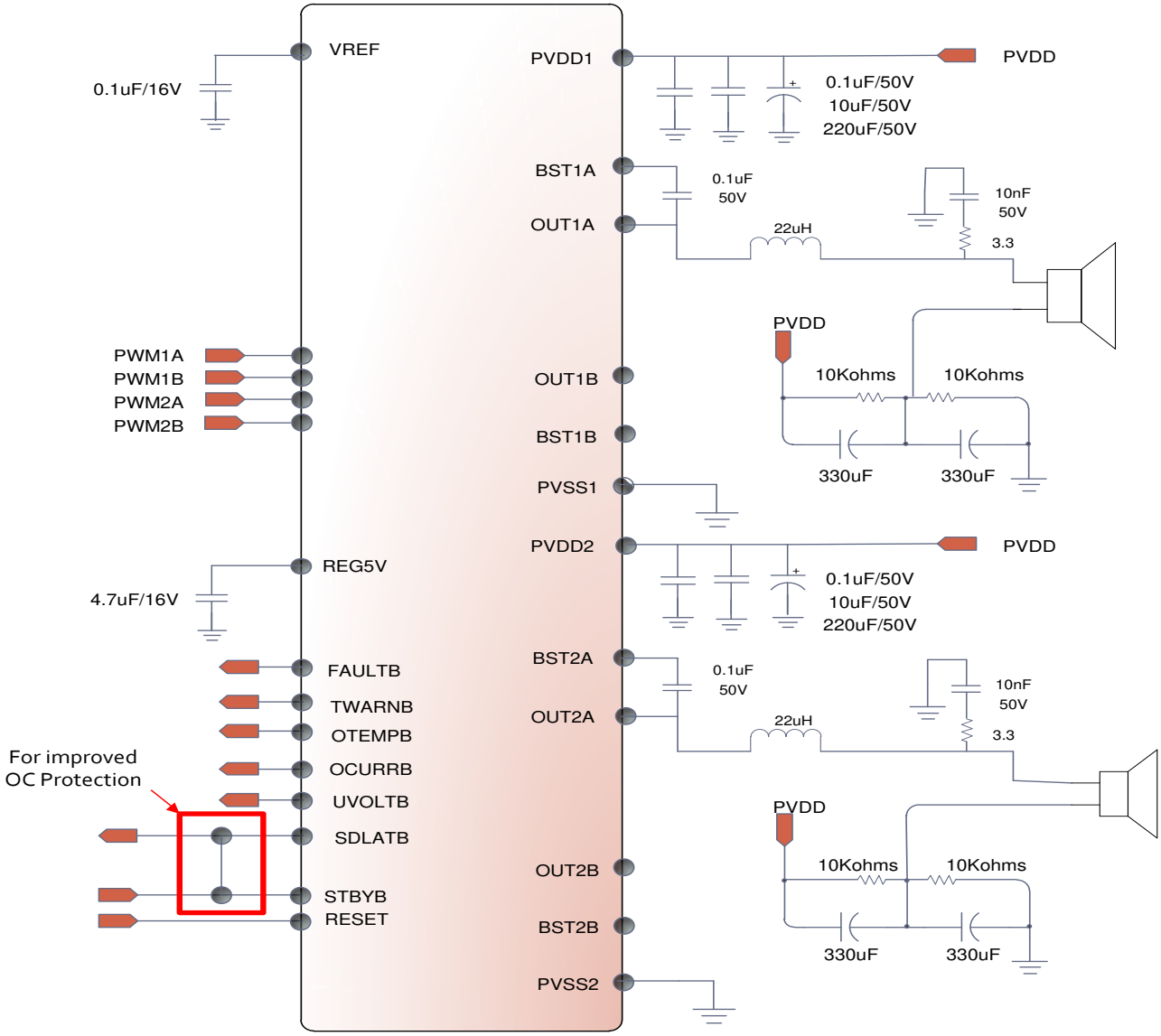


Figure 3: Single Ended Application with Modulation Filters

Sub-Woofer Application with Modulation Filters and EMI option

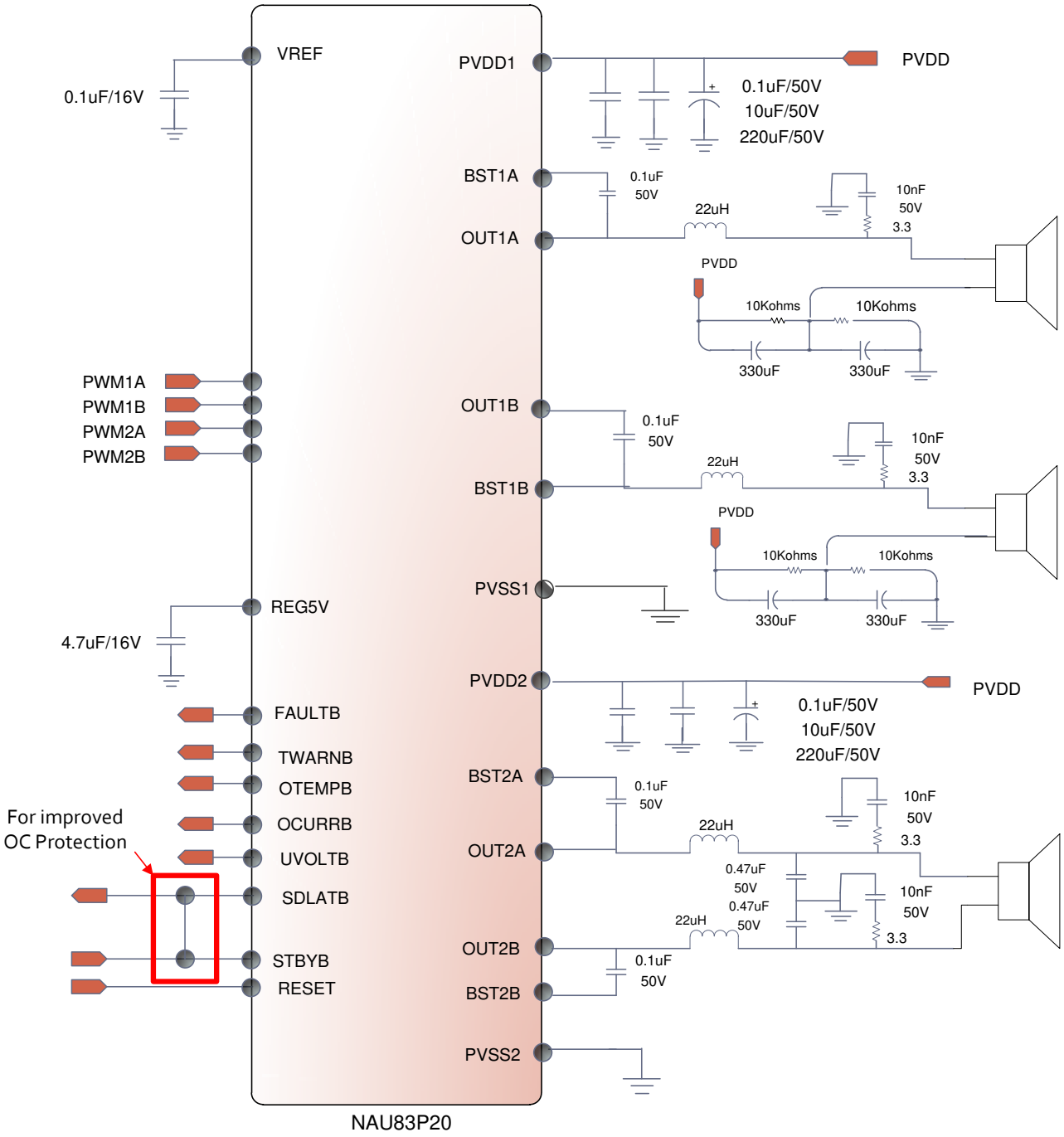


Figure 4: Sub-Woofer Application with Modulation Filters

7.1 Component Selection

7.1.1 Bypass Capacitors

Bypass capacitors are required to remove the ac ripple on the PVDDx pins. The value of these capacitors depends on the length of the PVDDx trace. In most cases, 10uF and 0.1uF are sufficient to ensure optimum performance. In addition, 220uF capacitors should be added to remove the additional ripple on the high current PVDDx inputs.

7.1.2 Bootstrap Circuit (BSTx)

In order for the bootstrap circuit to function correctly, a ceramic capacitor must be added between BSTx and OUTx. In applications with PWM switching frequencies of 300kHz a 0.1uF capacitor is recommended. If the application involves a higher or lower PWM switching frequency, the capacitor size may need to be decreased or increased respectively.

7.1.3 5V LDO

In order for the internal regulator to function more efficiently, a 4.7uF capacitor needs to be placed between the REG5V pin and ground.

7.2 Layout considerations

Good PCB layout and grounding techniques are essential to achieve good audio performance. It is recommended to use low resistance traces for the outputs as these devices are driving low impedance loads. The resistance of the traces has a significant effect on the output power delivered to the load. In order to dissipate more heat, use wide traces for the power and ground lines. In addition, ensure good contact of the exposed pad of the QFN package to GND (see section 9.4.2).

8 Operation

8.1 Power Supplies

The NAU83P20 requires one 4.5-24V supply in order to operate. The boost voltage supplies required by the high-side gate driver is realized by mostly built-in circuitry requiring only a few external capacitors. The power supply should be low output impedance and low noise.

In order to provide high quality electrical and audio characteristics the output stages are identical but independent half-bridges. Each half-bridge has a separate bootstrap power supply pin and voltage regulator for efficient gate drive operation. The supply for the common logic circuits is derived from the internal voltage regulator, which translates the PVDD2 pin supply, allowing for single supply operation.

In order for the bootstrap circuit to function correctly, a ceramic capacitor is added between the BSTx and the OUTx pins. When the output of the power stage is low, the capacitor is charged and when the output is high, the capacitor potential is shifted above the output potential providing a full rail to rail output. Refer to Section 7 for recommended capacitor values.

8.2 System Power Up and Power Down Sequence

8.2.1 Power Up

It is recommended that the STBYB be held low to enter the output drivers into a high impedance state until the PVDDx voltage rises above the under voltage detection threshold of 4.2V. Holding STBYB in a low state while powering up also helps to ensure that the bootstrap capacitors are fully charged before the chip begins operation.

8.2.2 Recommended Power up Sequence

1. With PVDDx Low
2. Hold STBYB LOW
3. Apply Power to PVDDx
4. Wait 10ms for the chip to power up
5. Apply input modulation signal at 50% duty cycle
6. Hold STBYB HIGH
7. The device will begin to modulate

8.2.3 Power Down

The device will remain fully powered on as long as PVDDx remains above the under voltage detection threshold. It is recommended to hold STBYB low during power down; this will prevent clicks and pops.

8.2.4 Recommended Power down Sequence

1. With STBYB and PVDDx High
2. Hold STBYB Low entering the drivers into high impedance state
3. Wait 10ms while the drivers enter high impedance state
4. Remove all input signals
5. Remove power from PVDDx

8.3 Error Reporting

The FAULTB pin is an active-low, open-drain output. The over temperature, over current, and under voltage pins are active-low, open-drain outputs. The function of these pins is to report errors in the chip to the PWM controller, micro controller, or other system control device.

Pin	Causes
FAULTB (FAULTB= 0)	Any low transition on OTEMPB, OCURRB, UVOLTB
OTEMPB (FAULTB= 0)	Device junction temperature above 140°C
OCURRB (FAULTB= 0)	If current drawn from any of the output drivers exceeds 5A
UVOLTB (FAULTB= 0)	PVDDx has fallen below the minimal 3.5V required for chip operation

8.4 Device Exception Handling System

The NAU83P20 has several error reporting signals used for device fault detection. The system has been designed so that it can be easily integrated into a system that will be able to adjust operating parameters in order to allow the device to operate within its specified limits. (see appendix for logic)

There are six signals related to the exception handling system, which are output to device pins:

1. Fault (FAULTB)
2. Temperature Warning (TWARNB)
3. Over Temperature (OTEMPB)
4. Over Current (OCURRB)
5. Under Voltage (UVOLTB)
6. Shutdown Latch (SDLATB)

All 6 signal pins are open drain, active low outputs.

8.4.1 Device Standby and Reset

The STBYB pin controls the half-bridges. Setting STBYB low forces the half-bridges into a high impedance state. The device will also be in a low current state. The STBYB pin can also be used for hard muting the power stage.

For stand-alone fault protection, it is possible to tie the SDLATB pin to STBYB. In this configuration, any fault detection reported by the SDLATB pin going low will force STBYB low, therefore, minimizing any possible damage to the device from over-current issues.

In BTL modes driving the STBYB pin low will enable weak pull down of the half-bridge circuits causing the bootstrap capacitors to charge.

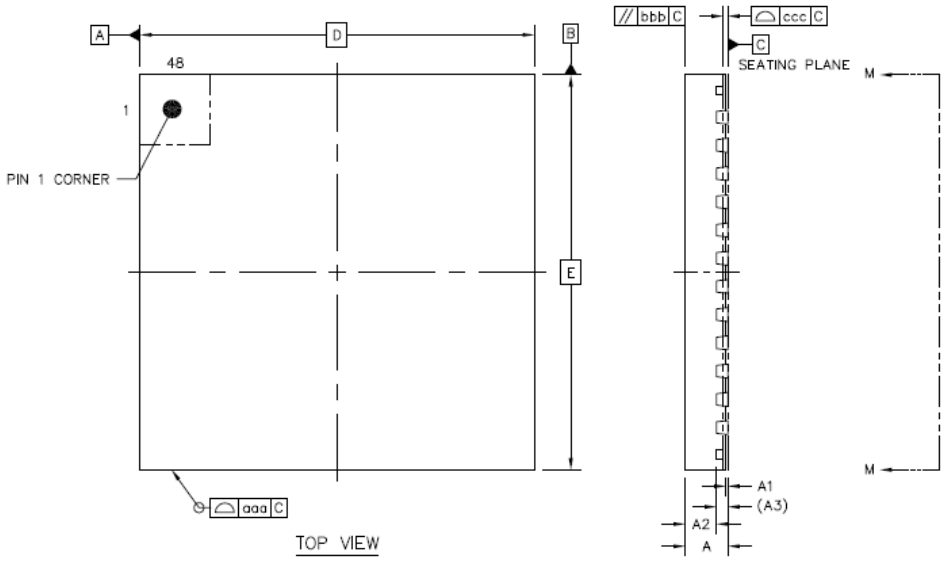
RESET pin resets the SDLATB pin.

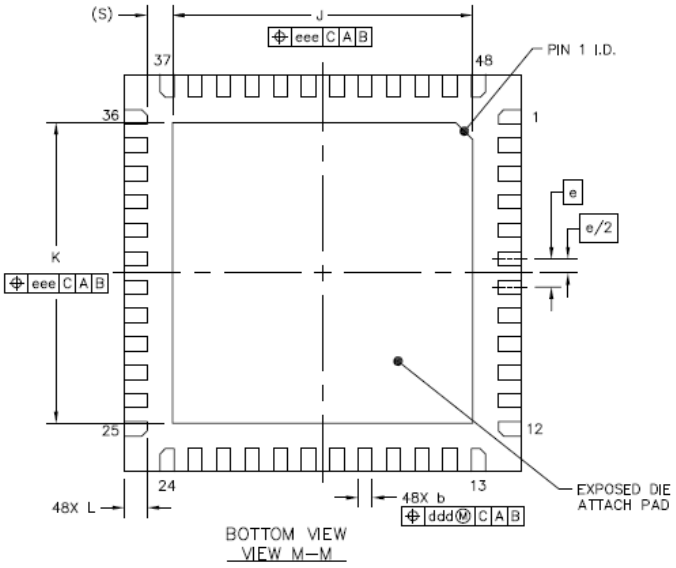
8.4.2 Thermal Information

The QFN-48 package is intended to be interfaced with an exposed heat-sink pad on the underside of the PCB. This can be accomplished by passing plugged thermal vias from pin 49 (exposed pad) of the package through all of the PCB layers to an exposed metal layer on the opposite side. If additional thermal management is required, a heat sink can be attached to this exposed metal layer allowing for additional heat dissipation.

9 Package Dimensions

48-lead plastic QFN; 7X7mm^2, 0.8mm thickness, 0.5mm lead pitch





		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		7 BSC	
	Y	E		7 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	J	5.2	5.3	5.4
	Y	K	5.2	5.3	5.4
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	
		S		0.45 REF	

10 Ordering Information

Part Number	Dimension	Package	Package Material
NAU83P20YGB	7x7 mm	QFN-48	Green

NAU83P20 _ _ B

Package Material:

G = Pb-free Package

Package Type:

Y = 48-Pin QFN Package

11 Revision History

VERSION	DATE	PAGE	DESCRIPTION
NAU83P20 Datasheet Rev1.0	Jan., 2013	NA	Revision1.0
NAU83P20 Datasheet Rev1.1	April, 2013	1, 2, 3,4, 10 12 15 16	Change block diagram Input labels to PWM## Update Single Chip Pin-out Diagram Update Single Chip Pin description Change Fault Protection to Fault Detection and update action description. Remove OC_ADJ and STTIMER descriptions. These are not available. Update Package drawing to QFN48 Saw Type. Change Pkg type designator to Y = QFN
NAU83P20 Datasheet Rev1.3	Oct., 2013	2 7 12 14 All	Package material changed from Pb-free to Green Remove Over Current Resistor Update Signal Ended configuration circuit Updated recommended power up/down sequence Rev A data added. Waiting Rev B to update electrical characteristics.
NAU83P20 Datasheet Rev1.4	August,25,14	All	AC/DC parameters were updated, Changed pin-out by deleting a test pin. Made changes to Application diagrams.
Rev 1.6	Oct, 14, 2014	All	Updated application diagrams, added table contents
Rev 1.7	Oct, 24, 2014	10-18	Updated Performance Graphs
Rev 1.8	Mar 2018	All	Updated pin-out; Updated VDD range and Under-voltage limits; Updated OCURR limit; Updated recommended capacitor values in application diagrams; Added note about tying SDLATB to STBYB for improved S/C detection on page 19; Added Appendix for error handling; Updated Figure titles; Updated pkg information; Removed REG3V references
Rev 1.9	Oct 2018	8	Update VIH/VIL spec
Rev 2.0	Nov 2018	3,4,5 8 23,24	Update Pin Out diagram and Description Table Update typical Overcurrent Response Time Change O/Ps Tri-State to High Z
Rev 2.1	Dec 2018		Removed all reference to Slew Control Update Pin Out diagram and Description Table Added DIE Diagram and Die Pad Coordinates
Rev2.2	Feb 2019		Changes for RevK: Pin-out Die pad Layout Fault detection logic – SDLATB Added ENSLEWB Changes OTP trigger levels Change OCB trigger level
Rev 2.3	Dec 2019		Remove SLEW Update die and pkg drawings to show ENSLEWB as VSS Update spec
Rev 2.4	April 2020		Change ordering number to NAU83P20YGB for new pin-out package drawing

Table 1: Revision History

Appendix: Device Exception Handling System
Fault detection logic:

When a fault is detected, the individual fault pin pulses low and pulses the FAULTB pin low as shown in the error detection scheme shown in Figure 5.

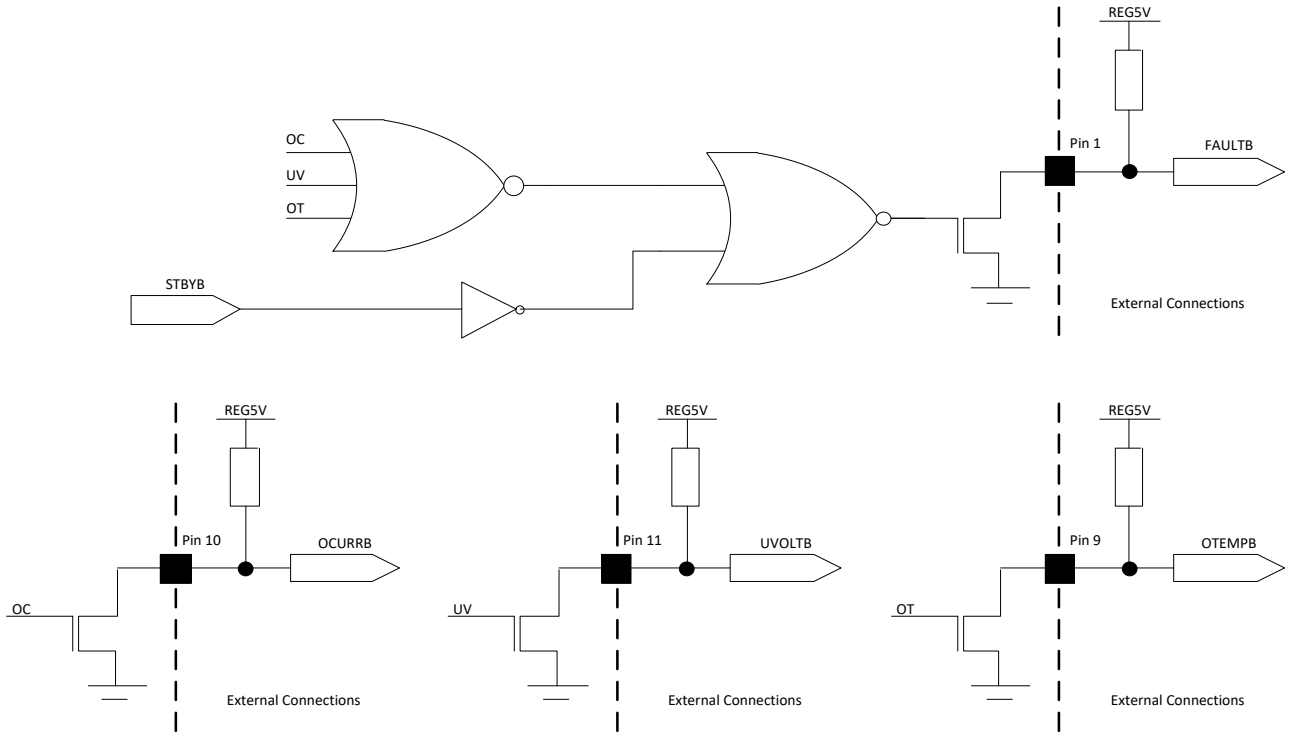


Figure 5: Fault detection Logic

OCURRB Latch:

The Over-current (OCURRB) or Over-Temperature (OTEMPB) or Under-Voltage (UVOLTB) also drive the ShutdownLatchB through a latch, as shown in Figure 6. A positive pulse on the RESET pin clears the ShutdownLatchB.

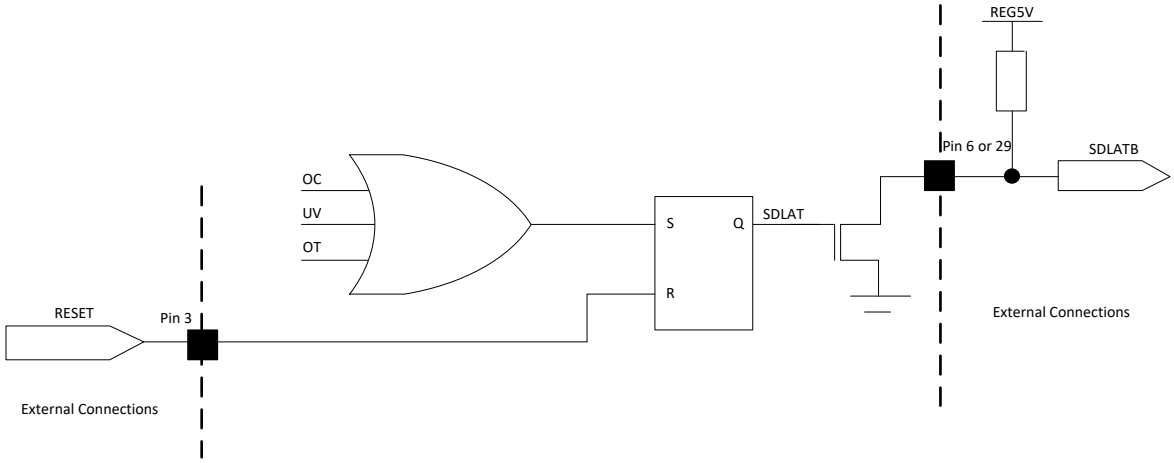


Figure 6: ShutdownLatchB

STBYB Function:

Setting STBYB low forces the half-bridges into a high impedance state.

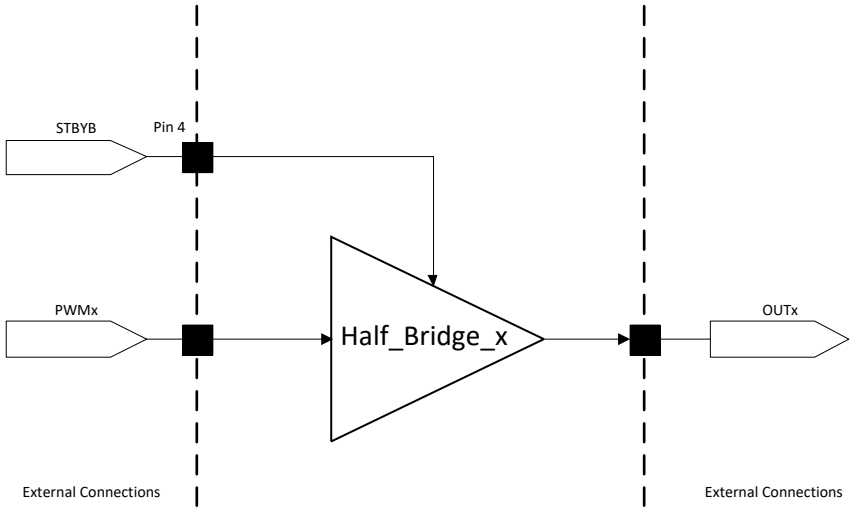


Figure 7: Simplified diagram of STBYB Hi-Z function on the output drivers

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