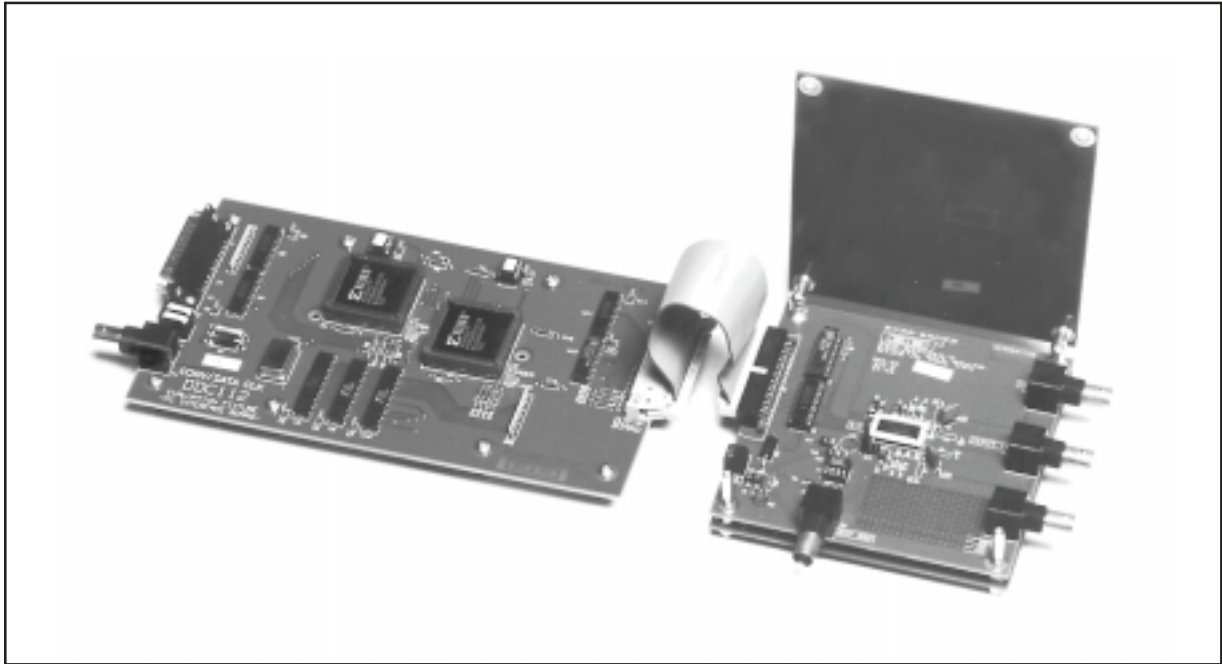**BURR - BROWN ®**

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DEM-DDC112U-C

EVALUATION FIXTURE

FEATURES

- **EASY INSTALLATION AND USE**
- **KEYBOARD AND MOUSE CONTROL**
- **COLLECTS UP TO 32,768 CONVERSIONS**
- **RETRIEVES DATA INTO PC FOR ON-SCREEN, OSCILLOSCOPE-LIKE DISPLAYS**
- **PERFORMS FOURIER TRANSFORMS ON DATA**
- **AUTOMATICALLY DETERMINES FUNDAMENTAL FREQUENCY AND CALCULATES SNR, SNDR, AND SFDR**
- **SAVES AND RETRIEVES DATA TO DISK**
- **SUPPORTS HP LASERJET FOR HARD COPY AND GRAPHIC DISPLAYS**

DESCRIPTION

The DEM-DDC112U-C evaluation fixture is designed for ease of use when evaluating the DDC112 precision integrating analog-to-digital converter. This kit includes a PC interface board and DUT board, allowing for performance evaluation of the DDC112 at the PC. The combination of the PC and the boards provided, makes timing commands, and access to and from the DDC112U DUT board, possible. The PC interface board retrieves up to 32,768 points of data from the DUT to the PC screen. The DEM-DDC112U-C software is mouse-compatible, and provides easy-to-read time or FFT displays of the data points that are retrieved under user control. Data can be saved and retrieved for future reference, or transported to other software applications for further graphical or mathematical analysis. Additionally, a hard copy of the PC screen graphics in time domain, or frequency domain, is easily acquired.

LI-500A
Printed in U.S.A. November, 1999

INSTALLATION

This kit includes the following items:

• DDC112 Evaluation Fixture-PC Interface Board (A2273)

• DEM-DDC112U-C DUT Board (A2326)

• DEM-DDC112U-C PC Software (3 1/2" diskette)

• 25-Pin Ribbon Cable with Connectors (PC Interface Cable)

• 34-Pin Ribbon Cable with Connectors (DUT Cable)

• DEM-DDC112U-C Documentation (LI-500)

• DDC112 Product Data Sheet (PDS-1421)

The additional equipment required to do a complete evaluation of the performance of the DDC112 comprises of:

• IBM-Compatible PC with EGA or VGA Graphics and Parallel Interface Port

• +5VDC Power Supply (300mA maximum current)

• Voltage or Current Signal Source

• Laser Printer (optional)

• PC Software Update (version 2.1) from www.burr-brown.com (optional)

To install the DEM-DDC112U-C evaluation fixture, connect the 25-pin cable between one of the PC's parallel ports and the DDC112 evaluation fixture-PC interface board, as shown in Figure 1. This establishes a communication link between the PC interface board and the PC. Next, connect the 34-pin ribbon cable between the PC interface board and the DEM-DDC112U-C DUT (Device Under Test) board. The 34-pin ribbon cable should lay flat between the PC interface board and DEM-DDC112U-C DUT board. This connection completes the link to the DDC112 being tested. With these connections, the setup configurations for the DDC112 (DUT) can be sent from the PC, and the data can be retrieved from the DDC112 (DUT) to the PC. Verify the power supply is set for +5VDC with a voltmeter, and then turn the power supply off and wire it into the terminal blocks. Connect the +5VDC power supply to J6 of the DEM-DDC112U-C DUT board, and P3 of the DDC112 evaluation fixture-PC interface board.

Finally, verify that the appropriate resistors, shorting bars and/or capacitors are installed in the Z_2, Z_3, Z_4, Z_5, Z_6, and Z_7 sockets on the DDC112U DUT board as discussed in the Theory of Operation section of this data sheet. See Figure 2 for circuit connection details. The factory configuration for these components are:

$$Z_2 = 10M\Omega \qquad Z_5 = \text{Open}$$
$$Z_3 = \text{Open} \qquad Z_6 = 10M\Omega$$
$$Z_4 = \text{Open} \qquad Z_7 = \text{Open}$$

Insert the 3 1/2" diskette into the PC and start the program by typing "DDC112". Optionally, version 2.1 of the software can be downloaded from the web site (www.burr-brown.com). This is described in AB-144 "New Software for the DDC112 Evaluation Fixture." If the software is executed in a Windows environment, it is recommended that other applications are closed. The software will default to the DDC112 setup configuration shown in Table I. When exiting the program, a DDC112.CFG file will be created or updated, storing the last program configuration.

DDC112 Gain	250pC
DDC112 Integration Time	500µs
DDC112 CONV Source	Demo Board (when U7 = 20MHz)
Number of DDC112s Being Tested	1
Data Clock	10MHz
Readback Delay	0µs
DDC Test Mode	On
Number of ~12.5pC Packets Injected per Integration	1
PC Ports	LPT1—PC Interface Board Port LPT2—Hard Copy Port
Display A/B Sides	Separate
Data Points to Retrieve	1024

TABLE I. Default Setting for the DEM-DDC112U-C Software. This default occurs when there is no configuration file (DDC112.CFG) available for reference in the PC directory.
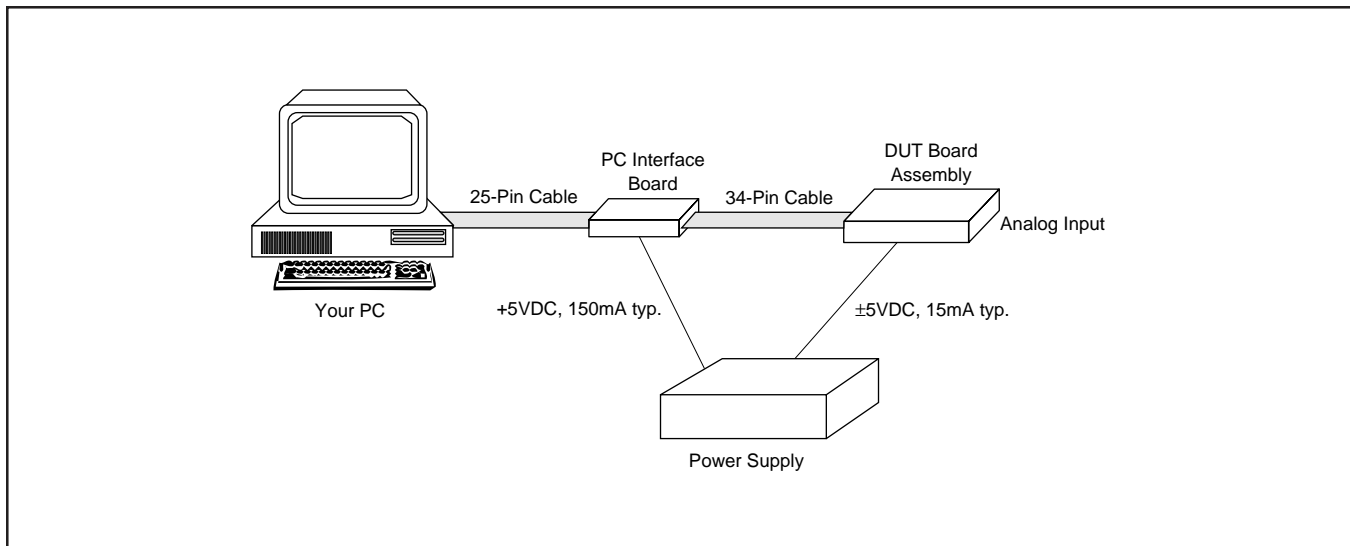

FIGURE 1. DEM-DDC112U-C Evaluation Fixture Connection Diagram.

You are now ready to apply power to the boards and run the first test. The red LED, CR2 on the DEM-DDC112U-C DUT board, should light. Once the two boards have +5VDC applied, execute the **R**efresh command by typing in "alt-R" at the PC. The **R**efresh command can also be found in the **S**etup pull-down menu. This command sends the instruction code default to the DDC112, providing its operating configuration per Table I.

Now retrieve your first data. Note that the inputs to the DDC112 are open. Type "alt-D" to open the **D**ata Menu. Highlight **R**etrieve, and hit return. The next screen that appears allows for changing the graphical display options and the number of data points that are presented. These functions are discussed in the Software section of the data sheet. At this point use the default setting by hitting return.

The DDC112 will perform the specified conversions and return the data to the PC via the interface board. Once the data is retrieved, the software allows for determining the x-axis and y-axis scaling for the data in the time domain. Accept the auto-scale setting by hitting return. A time-scale graph of the data collected will appear on the screen. At the top of the screen, the average should be close to zero. Hit "esc" to leave this screen.

In order to verify full functionality, a signal can be applied to one of the inputs of the DDC112U (DUT). Apply a +5.5VDC signal to Channel 1 of the DDC112 through the connector, P2. Repeat the data retrieval steps outlined above. The data that appears on the screen this time should have an average of approximately one (which is full scale).

THEORY OF OPERATION

The DEM-DDC112U-C evaluation fixture consists of two printed circuit boards, two flat cables (25-pin and 34-pin), and a diskette containing the evaluation software. The two printed circuit boards are the PC interface board and the DUT board.

PC Interface Board—The PC interface board contains the circuitry used to control the DDC112 timing and the interface to the PC (see Figure 11 for circuit diagram, and Figures 15, 16, and 17 for layout artwork.). Full control of the DDC112(s) is accomplished via registers that contain information controlling the DDC112 gain, integration time, data clock rates, number of DDCs, and readback delay. The PC interface board has the capacity to collect 32,728 data words of the DDC112 serial output. Since the DDC112 is a dual A/D converter, each input channel of the DUT is allocated 16,364 data words in the memory section of the PC interface board. The stored data is read via the PC's parallel port.
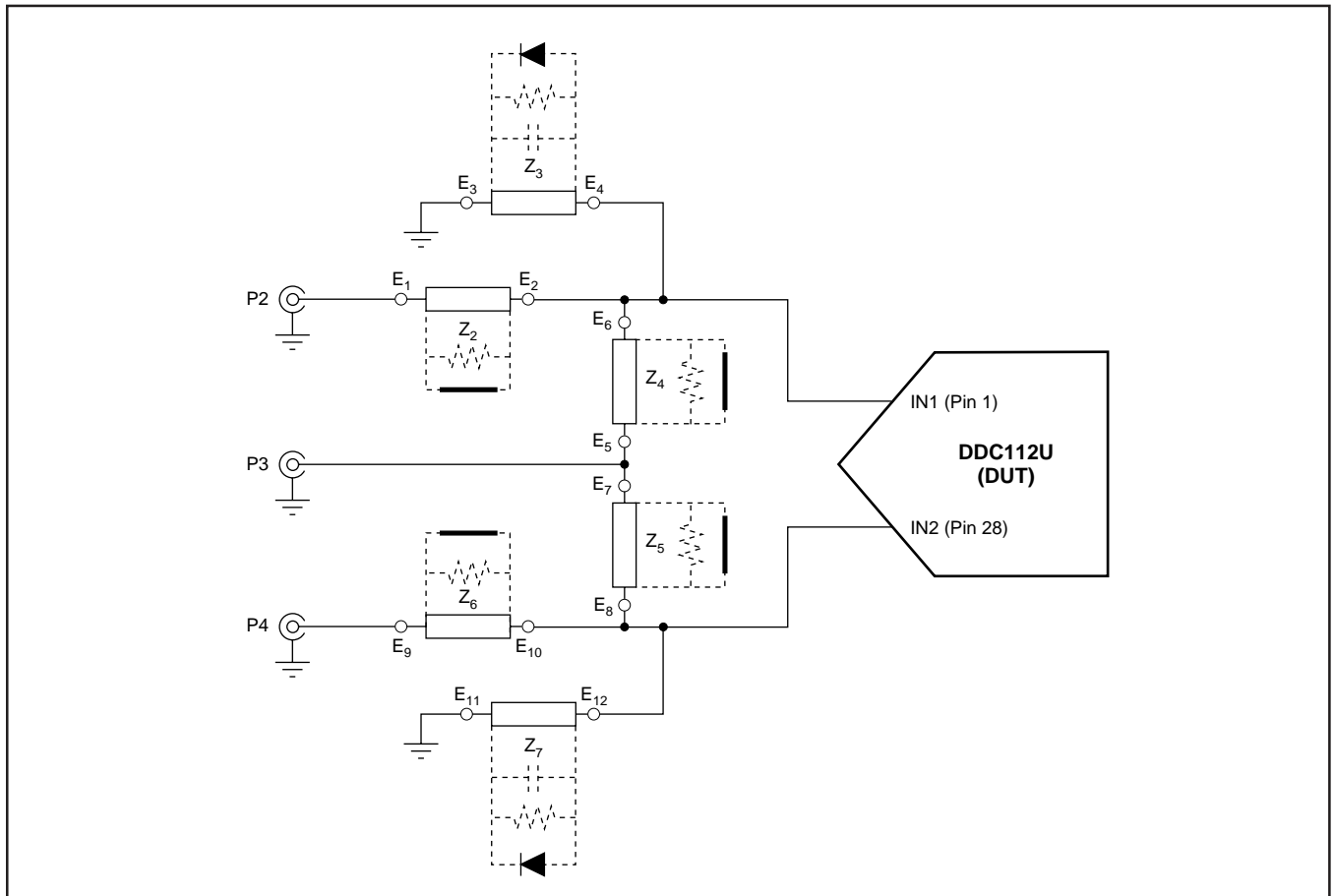

FIGURE 2. Input Structure on the DEM-DDC112U-C DUT Board.

DEM-DDC112U-C

DUT Board: Overview—The DEM-DDC112U-C DUT board contains a socket for one DDC112 to be tested, data buffers, 4.1V reference, decoupling capacitors, sockets for optional input circuits, sockets for optional external gain configurations and an analog breadboard area (see Figure 10 for circuit diagram and Figures 12, 13, and 14 for layout artwork).

The DUT socket (Figure 3) has been selected to allow for easy evaluation of multiple DDC112U parts for part-to-part comparison as well as easy on-board performance evaluation. Multiple parts can be evaluated by removing and reseating the socket's frame. The socket's frame is easily removed by gently dislodging either end with needle-nose pliers, a very small regular screwdriver, or tweezers. Once one end of the socket's frame has been lifted, the entire frame can be removed by lifting the other end. To reinstall the frame, place the DDC112U on top of the socket. Slide one end of the frame in first and then push the other side to snap into place. Alternatively, one can push down on both ends, evenly, until the socket's frame snaps into place. When this is done, make sure the pins are aligned properly. Place the socket's frame over the socket, carefully aligning it with the socket underneath. Repeated removal of the socket's frame may damage the frame. Contact Robinson-Nugent for replacement frames.

This unique socket was also selected to allow on-board performance evaluations. This can be done by desoldering the socket and soldering a DDC112U directly to the board. To do this, the socket's frame must be removed prior to desoldering the socket. Caution should be exercised with this technique because the solder mask will degrade with every cycle of soldering and desoldering.
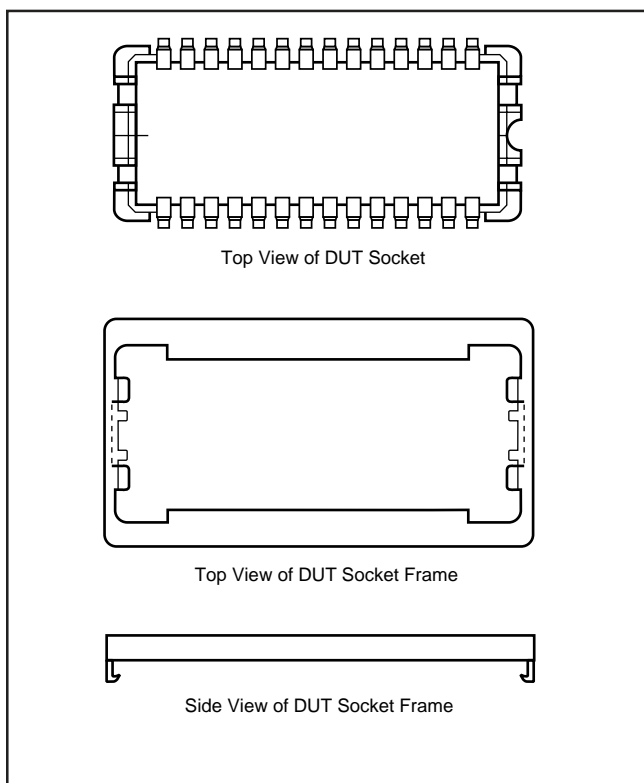
The PC interface board and the DUT board are separate to minimize digital noise effects on the DDC112 being tested, as well as allowing for other DUT boards to be used (i.e., a board with multiple converters). Digital buffers are installed at both ends of the interface to improve the isolation between the boards. The DEM-DDC112U-C DUT board is carefully laid out to insure low noise evaluations. Note that all the digital pins are located on one end of the DDC112U with the analog pins on the other. Care should be taken to keep the digital activity as far away from the analog pins as possible. In particular, pins 9 - 17 of the DDC112U have higher digital activity than the others and should be shielded from the analog functions. Note that the digital return lines are carefully separated on the DEM-DDC112U-C DUT board. The additional ground plane shields on the top and bottom of the DEM-DDC112U-C DUT board are installed with the board to insure that low noise tests are possible. During operation, the lid of the DEM-DDC112U-C DUT board should be closed.

Grounding and shielding practices should be taken into consideration when designing the circuit layout for the DDC112. In the event that the application cannot tolerate the additional shields that the DEM-DDC112U-C DUT board has, an alternative layout is shown in Figure 4. where a PC ground plane is placed around the inputs of the DDC112 (pins 1 and 28). This shield helps minimize coupled noise into the input pins. Additionally, the pins that are used for the external integration capacitors (pins 3, 4, 5, 6, 23, 24, 25 and 26) should be guarded by a ground plane when the external capacitors are used.
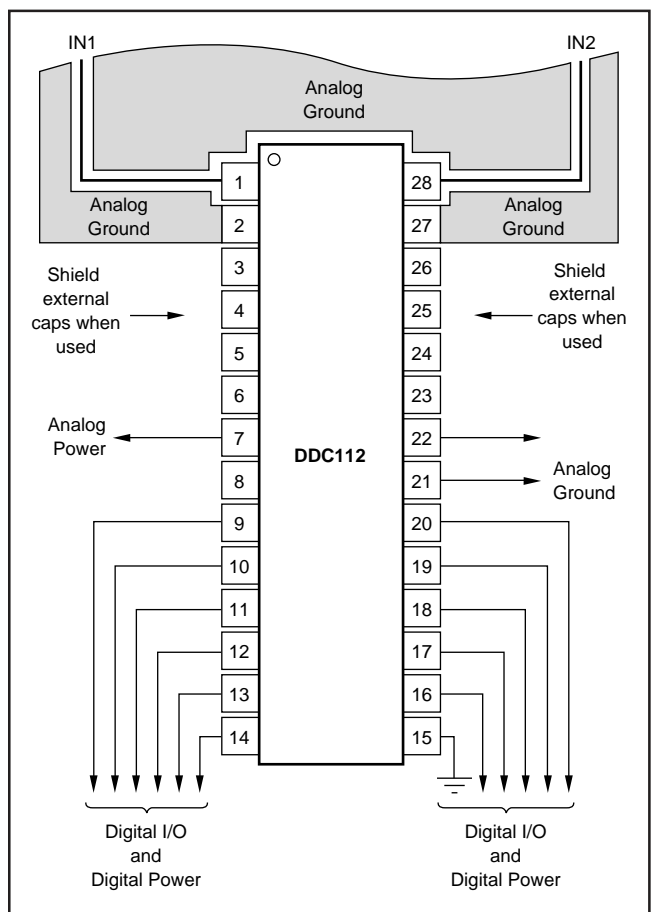
FIGURE 3. Robinson-Nugent Socket for DUT.

FIGURE 4. Recommended Shield for DDC112 Layout Design.

DEM-DDC112U-C

The digital and analog planes are not separate on this demonstration fixture because of the low level of digital activity on the board. Regardless of the power supply strategy, the bypass capacitors should be as close to the device as possible.

DUT Board: Reference Circuit—The 4.096V reference that has been installed on the DEM-DDC112U-C DUT board has been carefully selected because of its low noise performance. The LM4040-4.1 provides a 4.096V (nominal) reference. At the output of the reference, a single pole (3.157Hz) lowpass filter is inserted in the reference signal path. This filter is then followed by an amplifier configured as a buffer. The output of the amplifier has been loaded with 20.1µF of capacitance. This value of capacitance was derived through experimentation. The voltage reference circuit described above has been found to enable the DDC112U to perform at its optimum.

If one wants to evaluate alternative reference circuits, JP1 can be used to jumper in an external reference source through the coax connector, P5, or a user-designed reference circuit from the breadboard. The jumper settings for JP1 are shown in Table II.

JUMPER SETTING	JUMPER SETTING FUNCTION
Position A	Installs the 4.096V on-board reference to the DUT.
Position B	Configures the EXT V_{REF} connector, P5, to the DUT.
Position C	Configures the breadboard V_{REF} bus to the DUT.

TABLE II. Jumper Setting Definitions for JP1 for the Voltage Reference Source for the DDC112.

DUT Board: Optional Component Sockets—Resistor and capacitor sockets are included on the DEM-DDC112U-C DUT board to allow for optional input circuits and easy insertion of the optional external gain capacitors.

Figure 2 shows the topology of the input socket options and coax connectors. With this arrangement, several different input configurations can be implemented on the DDC112 DUT board. As an example, a photosensor can be installed for the IN1 (pin 1 of the DUT) using the E_3 and E_4 sockets. Alternatively, a voltage source could be used to excite the input of the converter by using P2 with a resistor installed in the Z_2 position (E_1 and E_2) sockets. Both of these configurations can be implemented on the IN2 (pin 28) input as well. A DC offset current can be injected into the input through P3. A resistor in the Z_4 position should be inserted if the source from P3 is voltage. A short should be inserted if the source is a current. It can be quickly seen that a variety of configurations can be implemented with this input circuitry configuration. The factory setting for this circuit is:

$$Z_2 = 10M\Omega \qquad Z_5 = Open$$
$$Z_3 = Open \qquad Z_6 = 10M\Omega$$
$$Z_4 = Open \qquad Z_7 = Open$$

External capacitors can be inserted in the C_9, C_{10}, C_{11}, and C_{12} positions, as shown in Figure 5. These external capacitors can be used to set the gain of the DDC112U (DUT) to user specifications rather than to the seven internal gains available. Refer to the "DDC112" portion of this data sheet for more details concerning the appropriate value of these external capacitors. For further detailed information, also refer to the DDC112 Product Data Sheet. For best performance, the leads of the capacitors should be as short as possible on $C_9 = C_{10}$ and $C_{11} = C_{12}$.
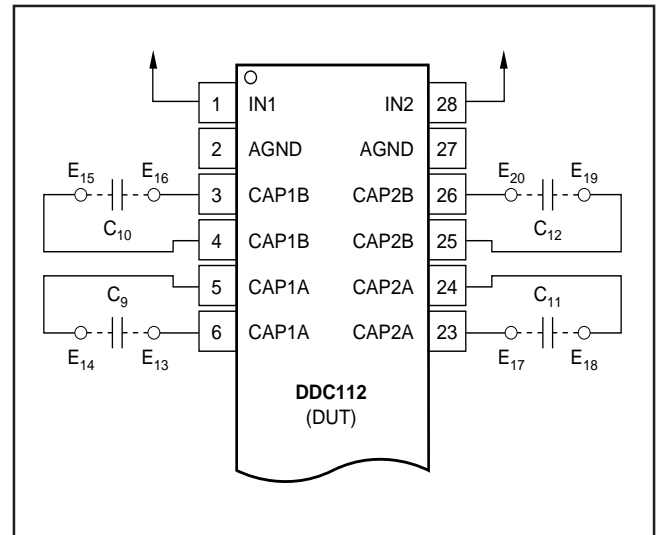

FIGURE 5. External Gain Capacitor Socket Configuration for the DUT Board.

DUT Board: CONV Input—There are three CONV options for the DEM-DDC112U-C evaluation fixture. In all three cases, the PC interface board uses the 20MHz clock oscillator (U7). The first clock option for the DEM-DDC112U-C DUT board is to use the 20MHz clock oscillator on the PC interface board. This clock is divided by two so that the DDC112U (DUT) has a 10MHz clock applied to pin 10 of the DUT. In all cases, the CONV source to the DDC112 is set in software (see the Software Setup/Timing section of this data sheet for more details). If "Demo Board" is selected, the CONV command is generated by the demo board. If "external" is selected, the CONV command is accessed from P1. The external CONV command can be synchronized with the system clock by selecting "Ext. syncd to clk." The external clock should be synchronized for the best noise performance.

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DDC112

The DDC112 is a dual input precision, wide dynamic range, charge digitizing A/D converter with 20-bit resolution (Figure 6). Low level current output devices, such as photosensors, can be directly connected to its input. The most stringent accuracy requirements of many unipolar output sensor applications occur at low signal levels. The DDC112 combines the functions of current to voltage conversion, integration, programmable full scale, A/D conversion, and digital filtering to produce precision, wide dynamic range results. Oversampling and digital filtering reduce system noise dramatically. Correlated double sampling captures and eliminates steady state and conversion cycle dependent offset and switching errors that are not eliminated with conventional analog circuits.

The DDC112 continuously integrates the input signal by incorporating one dual integrator (A and B) per input channel. The output of the dual integrators are multiplexed into the A/D converter. In operation, one side of each input integrates the input charge, while the other side is being converted by the delta-sigma A/D converter and reset. This operation is shown in Figure 7. Another unique feature of the DDC112 is the option of external integrating capacitors. This options allows a user-programmable full-scale range. On the DEM-DDC112U-C evaluation fixture, sockets are provided on the DUT board (E_{13} - E_{20}) to allow for easy insertion of these optional capacitors.
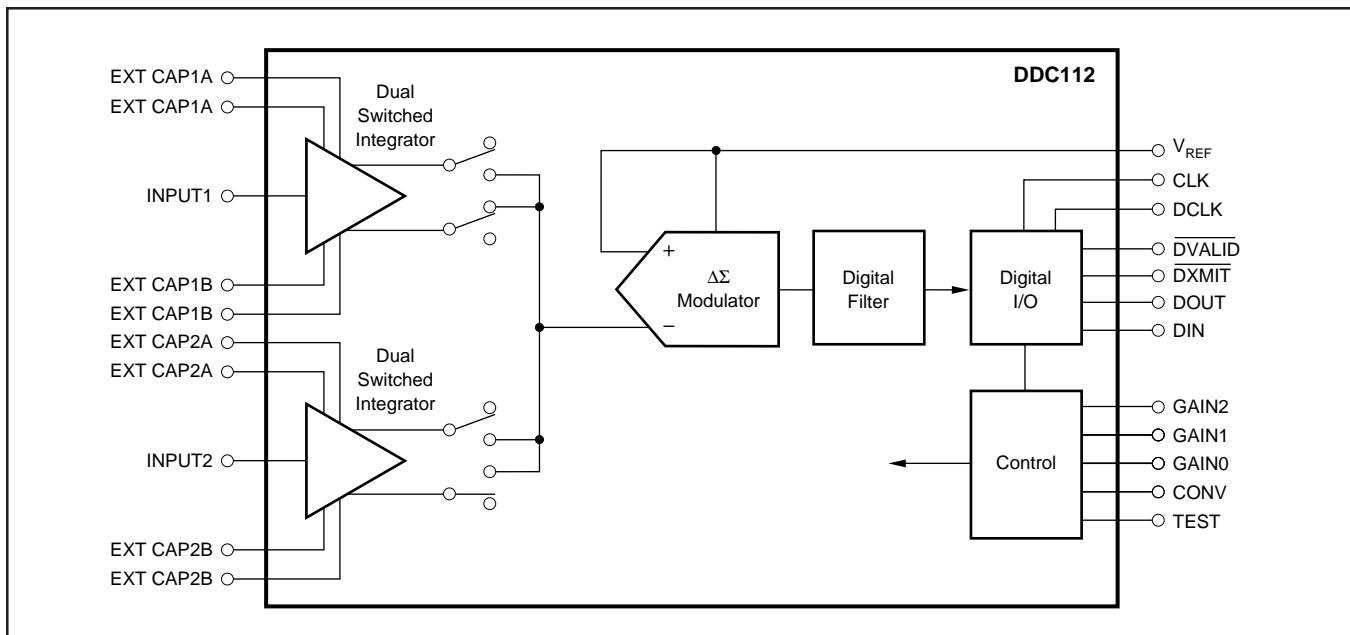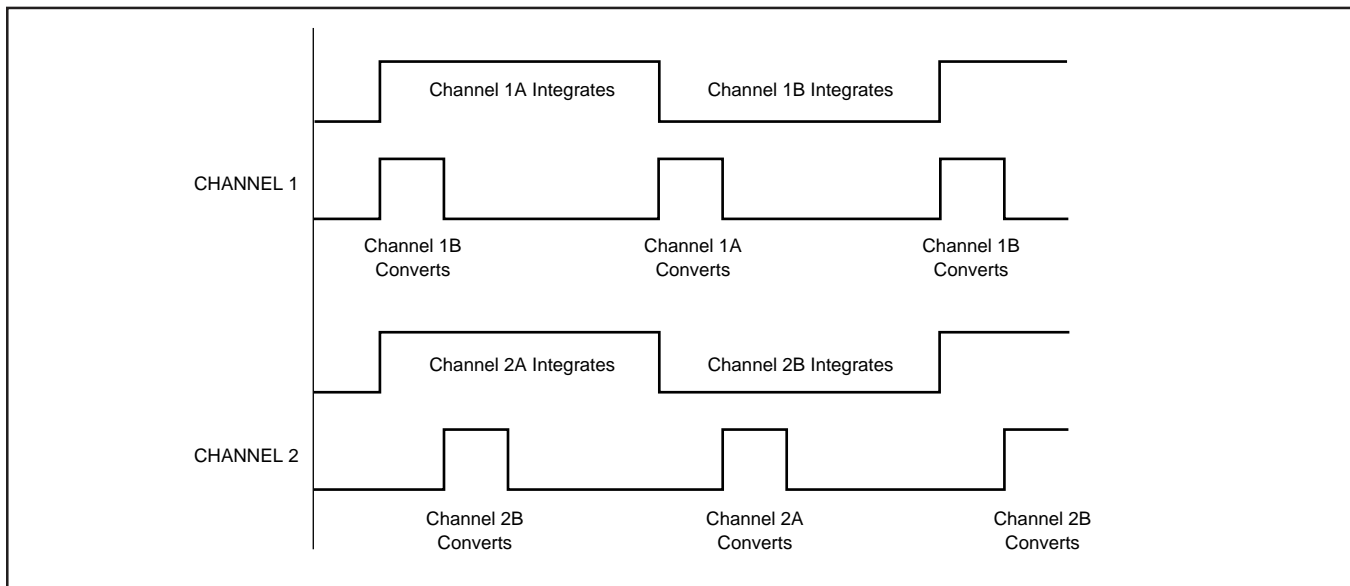

FIGURE 6. DDC112 Functional Block Diagram.

FIGURE 7. Integration/Conversion Timing of a Dual DDC112 A/D Converter.

The gain of the DDC112 can be programmed to seven predetermined values through the software. Likewise, one can install four external capacitors (C_9, C_{10}, C_{11}, and C_{12}) and design in their own gain setting. The gain options that are available are summarized in Table III.

INPUT RANGE Q_{IN} RANGE (pC)	INTEGRATION CAPACITOR (Nominal) C_{INT} (pF)
–0.2 to 50	12.5 (internal)
–0.4 to 100	25.0 (internal)
–0.6 to 150	37.5 (internal)
–0.8 to 200	50.0 (internal)
–1.0 to 250	62.5 (internal)
–1.2 to 300	75.0 (internal)
–1.4 to 350	87.5 (internal)
–4.0 to 1000	250 (external)

TABLE III. Input Ranges vs Gain Settings for the DDC112. In this Example, the Integration Time is 1ms.

Assuming a 10MHz system clock (pin 10 of the DUT), the relationship between the integration time, input current, and input charge is summarized in the formulas below:

$$T_{INT} = Q_{IN}/I_{IN} \text{ (max)}$$

$$(T_{INT}/C_{INT}) = (V_{REF}/I_{IN} \text{ (max)})$$

$$C_{INT} = Q_{IN}/(V_{REF} - 0.1V)$$

where, T_{INT} = Integration Time

Q_{IN} = Input Charge in Columns

I_{IN} = Input Current in Amperes

The dual switched integrators of the A/D converter utilize a differential input topology, with the non-inverting input internally tied to V_{REF}. This allows the digitizer to operate from a single supply. Prior to the beginning of each integration, the integrator is reset to V_{REF}. Additionally, the offset, offset drift, noise, and kT/C errors are corrected at that time. A low noise, voltage reference of 4.096V (nominal) provides the best performance from the DDC112. The reference that is designed for the DEM-DDC112U-C DUT board is implemented with a LM4040 (4.1V reference), a lowpass R/C filter and single supply operational amplifier (U3). The operational amplifier is loaded with multiple capacitors in an effort to further reduce reference noise and ripple.

A digital filter in the DDC112 passes a low noise, high resolution digital output to the serial I/O register. Since the serial I/O register is independent of the DDC112 conversion process, the output of multiple DDC112 units can be connected together in series to minimize interconnections.

The DDC112 integrates on one side of the dual switched integrator while it digitizes the other side (as illustrated in Figure 7). In the event that the integration time is less than the amount of time required to digitize Channel 1 and Channel 2, the DDC112 will change to a non-continuous mode. In this mode, the integration is not continuous and the device will appear to skip integrations. The limiting factor in these situations will be the time it takes to digitize the signals (Channel 1 and Channel 2).

SOFTWARE FEATURES

The pop down menus are activated with the mouse or by typing the first letter of a desired category with the Alt key down. For instance, to access the **S**etup menu, type "Alt-S". Once the desired pop-down menu appears on the screen, menu selections can be made with the up and down arrows and a carriage return or by typing the highlighted letter. The tab key and left and right arrows can be used to move inside the menu categories. The **R**efresh command, "Alt-R", should be used immediately after power-up of the PC interface board and DUT board, or if there is a power supply disturbance to the boards. If the **R**efresh command is not used, data will be invalid.

The three main pop-down menus are **S**etup, **D**ata, and **A**nalysis. The setup menu allows for accessing the commands that will initialize the DDC112 to desired gain, control the conversion timing, control the data clock rate, set the multiple device option, initiate the DDC test signal, select the PC interface board port and printer port, and refresh (or reset) the setup conditions of the DDC112.

SETUP MENU

The **S**etup menu performs six functions, all of which control the configuration of the test setup for the DDC112 test. The six functions are listed and described below:

Gain

Timing

D**a**ta Transfer

DDC Test **M**ode

PC **P**orts

Refresh

Gain—To configure the DDC112 into the appropriate gain setting, the DDC112 receives a 3-bit parallel word from the PC interface board. This 3-bit word is downloaded into pins 18, 19 and 20 of the DUT. The pins control the variable gain by selecting the internal feedback capacitance value or external capacitors for the input integrators. Refer to the product data sheet for details about the DDC112 operation versus these gain options.

Timing—There are two items that can be programmed in this menu. The DDC112 integration time can be programmed to one tenth of a micro second. This timing refers to the integration time required for one half of a complete, side A plus side B conversion. If the time that is programmed in this screen is less than the amount of time that is required to digitize the opposite two channels (per Figure 7), the demonstration fixture will automatically switch into a non-continuous mode. Refer to the product data sheet for details about the DDC112 operation for continuous versus non-continuous modes.

The second item that is programmed from this screen is the conversion signal. Three options are available; Demo Board, External, and Ext. syncd to clk. If the "Demo Board" option is selected, the convert command comes from the PC inter-

face board. By default, the convert command is synchronized to the PC interface board. The second convert option available is the "External" option. In this case, an external convert signal must be transmitted from the CONV/DATA CLK connector (P1). With this option, the DDC112 receives the input convert command from P1 directly. This is not synchronized with the 20MHz clock oscillator on the PC interface board. The third option is "Ext. syncd to clk". In this configuration, a convert command from the connector, P1, is once again used for the DDC112, however, it is synchronized with a D-type flip-flop on the PC interface board clock. Of the three options, the best noise performance can be achieved with option one or option three.

Data Transfer—The Data Transfer menu allows for programming the number of DDCs under evaluation, the data clock frequency and the data readback delay.

The PC interface board can accommodate several DDC112s at one time. If this option is required during the evaluation, the number of DDCs can be programmed into the evaluation software in this screen. If more than one DDC112U is tested, a new DUT board must be built to accommodate multiple parts. The default value for this entry is 1.

The speed of the readback is controlled by the data clock frequency (pin 11 of the DUT). This speed can be programmed to a value of 10MHz, 1.25MHz, 2.5MHz or 5MHz. Additionally, an external data clock signal can be connected to P1 of the PC interface board. Since P1 can also be used to implement an external convert command, one or the other must be chosen. The software will warn the user if this condition is violated. In the case where an external data clock is used with P1, that clock frequency will be sent directly to the DDC112U on the DUT board. Overall, the 10MHz setting for this value will give the best performance.

Finally, the data readback delay can be determined with the third programmable value in this screen. This option changes the time delay from the falling edge of Data Valid (pin 17 of the DDC112U-DUT) to the initiation of the data transmit to a larger number than 0µs. The inquisitive user will find that there is actually a 2µs to 3µs readback delay that was unavoidable in the implementation of the evaluation fixture design.

DDC Test Mode—This test mode can be used to determine if the proper gain has been implemented on the board. This mode allows for controlling the amount of charge injected into the input(s) of the converter and can readback the digital outcome of that experiment.

PC Ports—The communication port for the PC interface board to the computer and the printer port is set in this area. The PC interface must be connected to a parallel port. The graphs generated by the software can be sent to a printer through the same port or preferably, a second port. If the same port is used for the PC interface cable and the printer cable, the data must be collected with the PC interface cable connected.

The output to the printer is a bit map. An HP LaserJet is the recommended printer. A graph can also be stored as a file on the disk for future printing. The default print file name is DDC112.PRT. This can be changed by the user. Stored plot files are printed from the DOS environment by typing "Print <filename>". All settings on the PC **P**ort screen are saved after exiting the program, except for the graphics print file name.

Refresh—The **R**efresh command should be used immediately after power-up or if there is a power supply disturbance to the boards. THis command sends the setup informationto the DDC112 and PC interface board. If the **R**efresh command is not used, the data that is collected during a test will be invalid. The "F1" key will implement a refresh while in the graphics mode (Time or FFT).

DATA MENU

The **D**ata menu performs three functions which control the collection, storage, or retrieval of the data. The three functions are:

Retrieve
Save to File
Read **F**ile

Each function is described below:

Retrieve—The ouput data from the DDC112 on the DUT board is continuously read, and that data stored in the RAM memory on the PC interface board. The **R**etrieve command brings the latest data from the PC interface board to PC RAM memory for graphical evaluation. The graphical evaluation tools are available in this section of the software after the data retrieval process has been completed. These graphical evaluation tools, Time plots, and FFT analysis are also available in the analysis section.

The **R**etrieve screen, also initiated by pressing F1, allows for specifying how the data from the DDC112 will be presented and the number of data points that will be taken during the DDC112 test. The first option offered in this screen is "Display A/D Sides". This option provides the opportunity to view the time and FFT plots of sides A and B of each DDC112 input channel separately or to view the data points collected from side A and B of each single channel together. If "Separate" option is chosen, the data will be presented in four separate screens (as indicated at the top of the of each plot). Each plot can be viewed with the "**P**rev" or "**N**ext" options at the bottom of the plot screen. In all cases, side "A" is graphically represented in white fonts and side "B" is graphically represented in blue.

One can also determine the number of data points that will be collected from the first "**R**etrieve" Screen. If the combination of "Separate" (as described above) and 1024 data points is selected, 4096 data points will be retrieved, 2048 for each channel or 1024 for each DDC112 side of each channel. If the combination of "Together" and 1024 data points is selected, 2048 data points will be retrieved, 1024 for each channel. The PC interface board RAM is able to store up to 32,768 of the most recently collected data points. If the "other" option is chosen (a user-selected number of data points collected that do not match the predefined menu options), FFT analysis is not available.

If the user has configured more than one DDC112 to be tested in the Data Transfer screen, the maximum number of data points per device is divided by the number of devices; ie., if four DDC112s are being tested in the separate graphical mode, the maximum number of data points for each DDC112 will be 32,768/4 or 2048 data points.

After the data is collected, the user is given the option to select plot scales. Auto-scale will attempt to give an optimal data fit. To continue to the plot screen, click on "Plot" or press return. An example of the plot screen in the time domain is shown in Figure 8. The title of the screen identifies the type of plot displayed (time or frequency), which side and channel data is being displayed, and if multiple DDC112s were tested. In the time domain, the x-axis unit of measure is samples (time domain). The y-axis is the normalized data output (1 = fullscale in a 20-bit system). Any data point falling between 0 and 1 on the y-axis can be translated into the equivalent digital word with the formula:

$$\text{digital word} = ((\text{numeric value on screen}) \cdot 1{,}044{,}479) + 4096$$

In the frequency domain, the x-axis unit of measure is frequency, and y-axis is magnitude, where 0dB = fullscale.
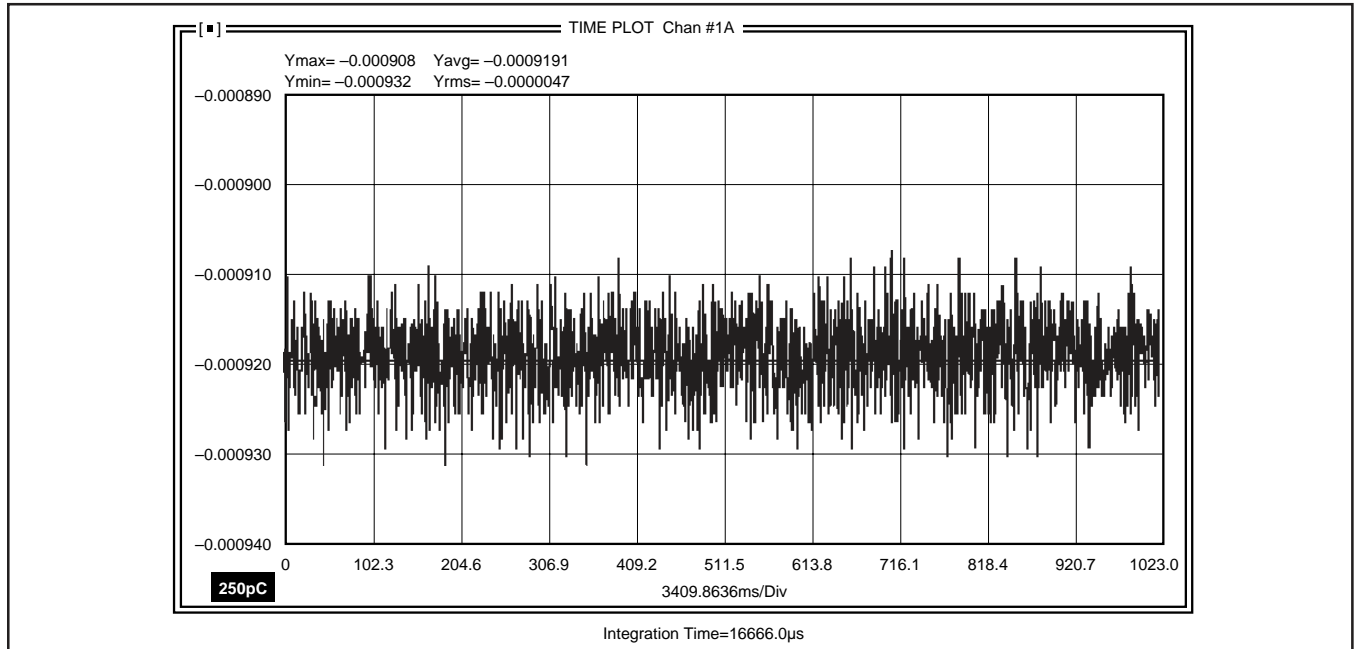

FIGURE 8. Time Domain Plot of Channel 1A. X-Axis Represents Sample Number, Y-Axis is Normalized Digital Output in Decimal Form.
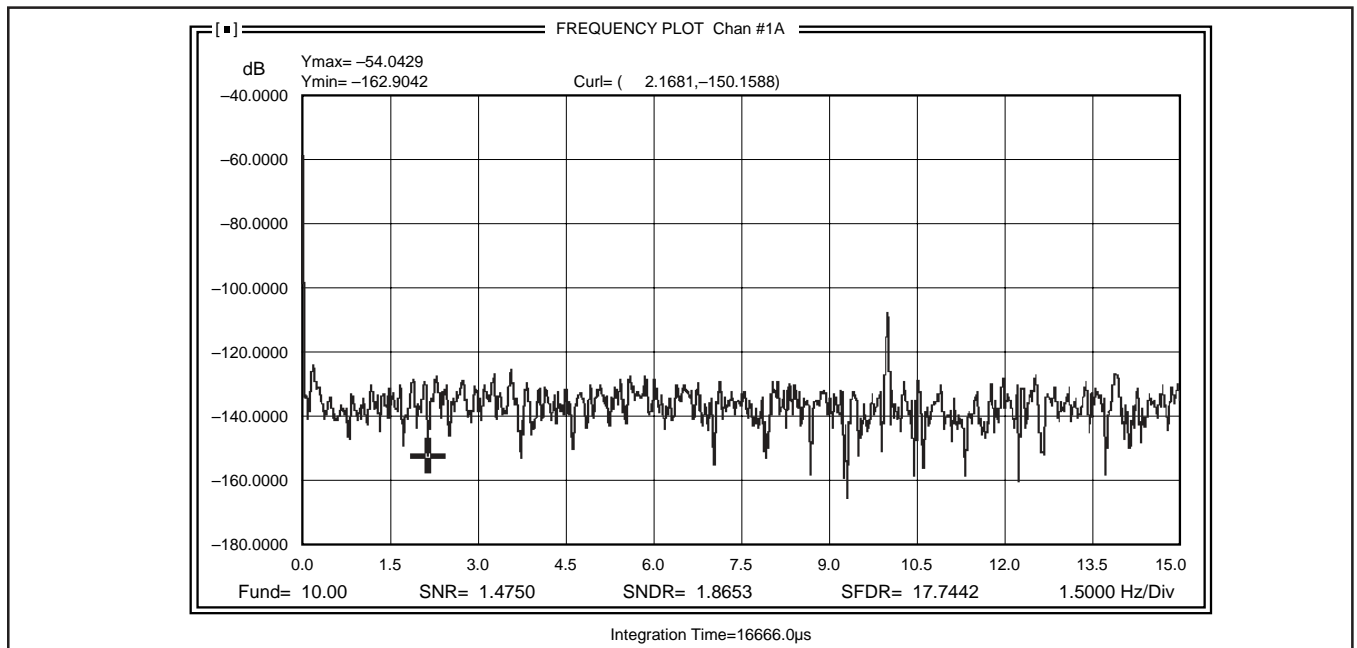

FIGURE 9. FFT Plot of Data Shown in Figure 8.

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Along the bottom of the screen, several options are available. If the data is displayed in the time domain, the **R**etrieve option allows for retrieval of the most current data from the PC interface board. The **D**isplay option toggles the data presentation between dots and lines connecting the data points. The **S**cale option allows for setting x- and y-axis scales. The **P**rev and **N**ext option allows for viewing each DDC112's data output, as defined at the beginning of the retrieval process. **Y**-auto will re-scale the y-axis to a best-fit range. The cur**1** and cur**2** activate cursors to determine exact values of data points as numerically displayed at the top of the screen. Movement of the cursors is effected by place and drag of the mouse or arrow and Ctrl-arrow operation. Also, the cursor will jump in steps of 10 if the shift key is held down with the cursor key. An **F**FT option is available with seven windowing options. After FFT calculations are performed, the data is plotted in the frequency domain. An example of the frequency domain plots is shown in Figure 9.

Save to File—This utility allows for saving current test data and test setup in ASCI format on a PC disk. It is recommended that all data files be stored with the *.DDC format. Files stored through this utility cannot be printed into plots from the DOS environment, but can be loaded into spread sheet software with graphics utilities. If a printed plot is required, refer to the PC Ports section of this data sheet for detailed instructions.

Read File—This utility allows for the reading of files on the disk containing saved data and setup information.

ANALYSIS MENU

The **A**nalysis menu performs four functions, all on existing data in the PC memory. The four functions are:

Time Plot

FFT

Freq Plot

Hard Copy

Each function is described below.

Time Plot—The time plot utility gives a time representation of the data. The plot utility is the same utility described in the **R**etrieve section of this data sheet.

FFT—The FFT utility gives the options of a Hamming, Hanning, Blackman, Blackman-Harris, Continuous 5th Derivative, Triangle or Rectangle evaluation of the data.

The Continuous 5th Derivative window is a cosine window derivative where:

$$window = 0.3125 - 0.46875\cos(2\pi n/N) + 0.1875 \cos(4\pi n/N) - 0.03125\cos(6\pi n/N)$$

This window provides a good balance between spectral resolution and side lobe peaks.

The SNR and SINAD calculations include the ability for the user to define the spectral resolution of the fundamental and harmonics in the FFT. The user specifies the width of the spectral peaks (30 bins is the default resolution). Since the signal will have spectral spreading from the FFT, this allows correct measurement of the signal power while preventing the signal power from being mistaken as noise power. One half of the resolution term is used to skip past the FFT's DC component when calculating SNR and SINAD.

For the bandwidth selected, the SNR calculates the rms signal power divided by the rms noise power. The signal power is the power in the bins between $\pm 1/2$ the spectral resolution from the fundamental bin. The noise power is summed as the noise in all other bins except for harmonics and the DC components' bins. As for the fundamental, the spectral resolution term is used to skip the signal's harmonics when summing noise power. The SNR noise power summation is "corrected" by multiplying the sum by the ratio of all bins in the bandwidth, divided by the bins counted as noise without harmonics, DC or signal.

For the bandwidth selected, the SINAD calculation is the rms square root of the signal power divided by the rms noise and distortion power. The signal power is the power in the bins between $\pm 1/2$ the spectral resolution from the fundamental bin. The noise distortion power is the power in all other bins except for the DC component's bins. The SINAD noise and distortion power summation is "corrected" by multiplying the sum by the ratio of all bins in the bandwidth, divided by the bins counted as noise and harmonics without DC or signal.

The spurious free dynamic range (SFDR) is calculated as the magnitude of the fundamental bin divided by the peak magnitude of the next highest bin in the bandwidth selected (ignoring DC and the fundamental's spectral spreading). For this measurement to be exactly correct and consistent, the fundamental should be located on bin exactly. That is, the input sinewave signal should be coherent with the exact integral number of cycles per time sample.
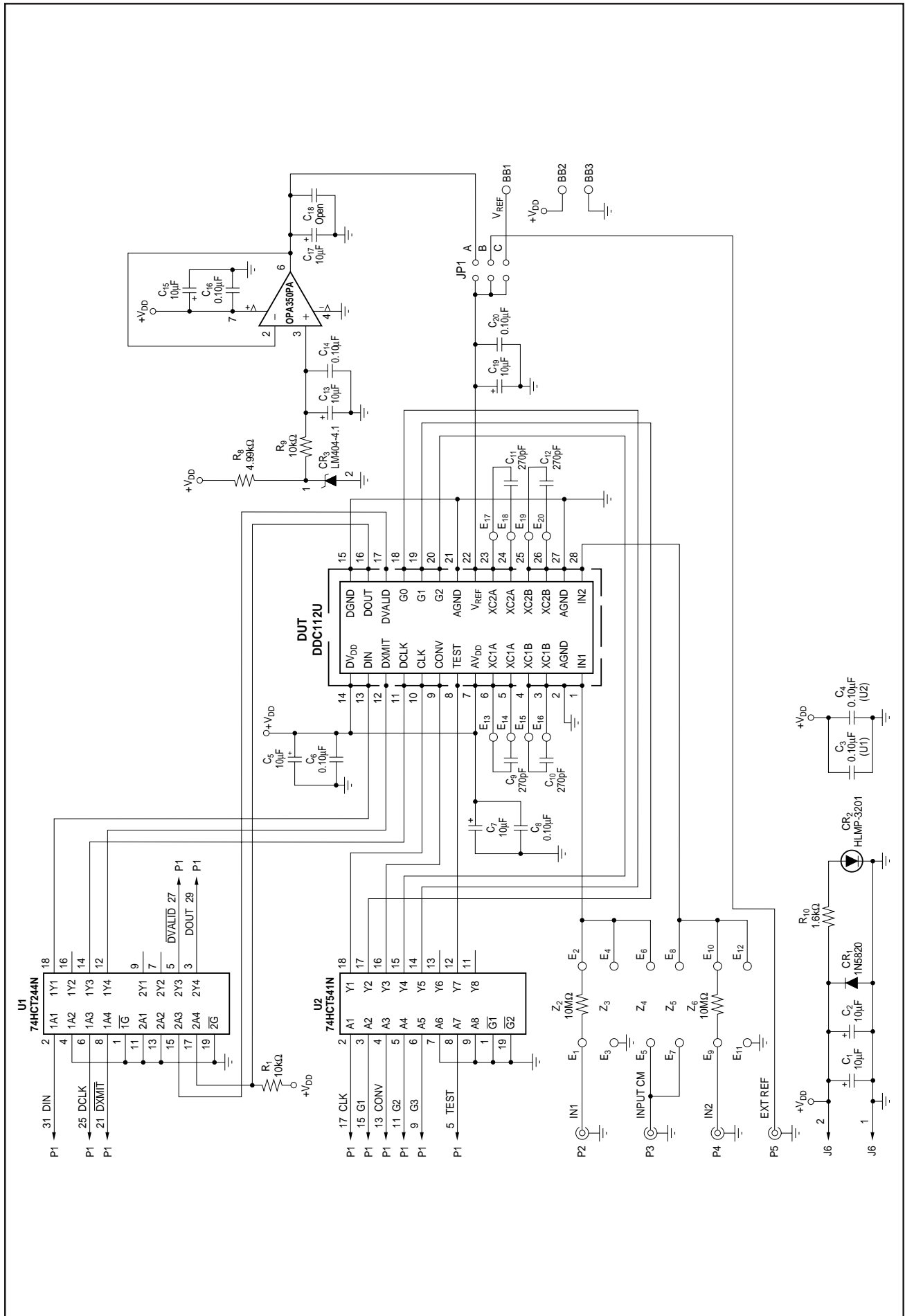
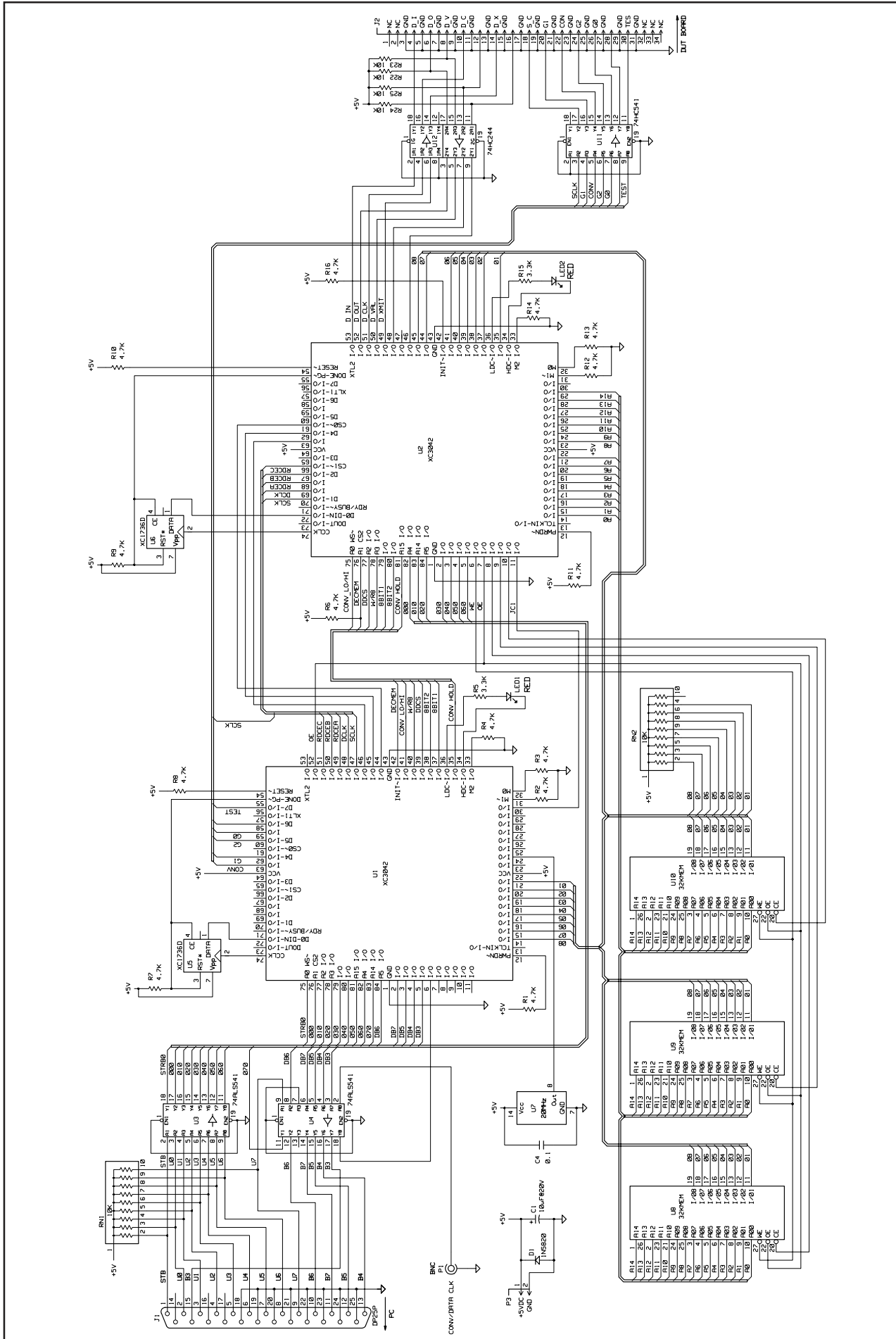FIGURE 10. Circuit Diagram of DEM-DDC112U-C DUT Board.

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FIGURE 11. Circuit Diagram for DEM-DDC112U-C PC Interface Board.
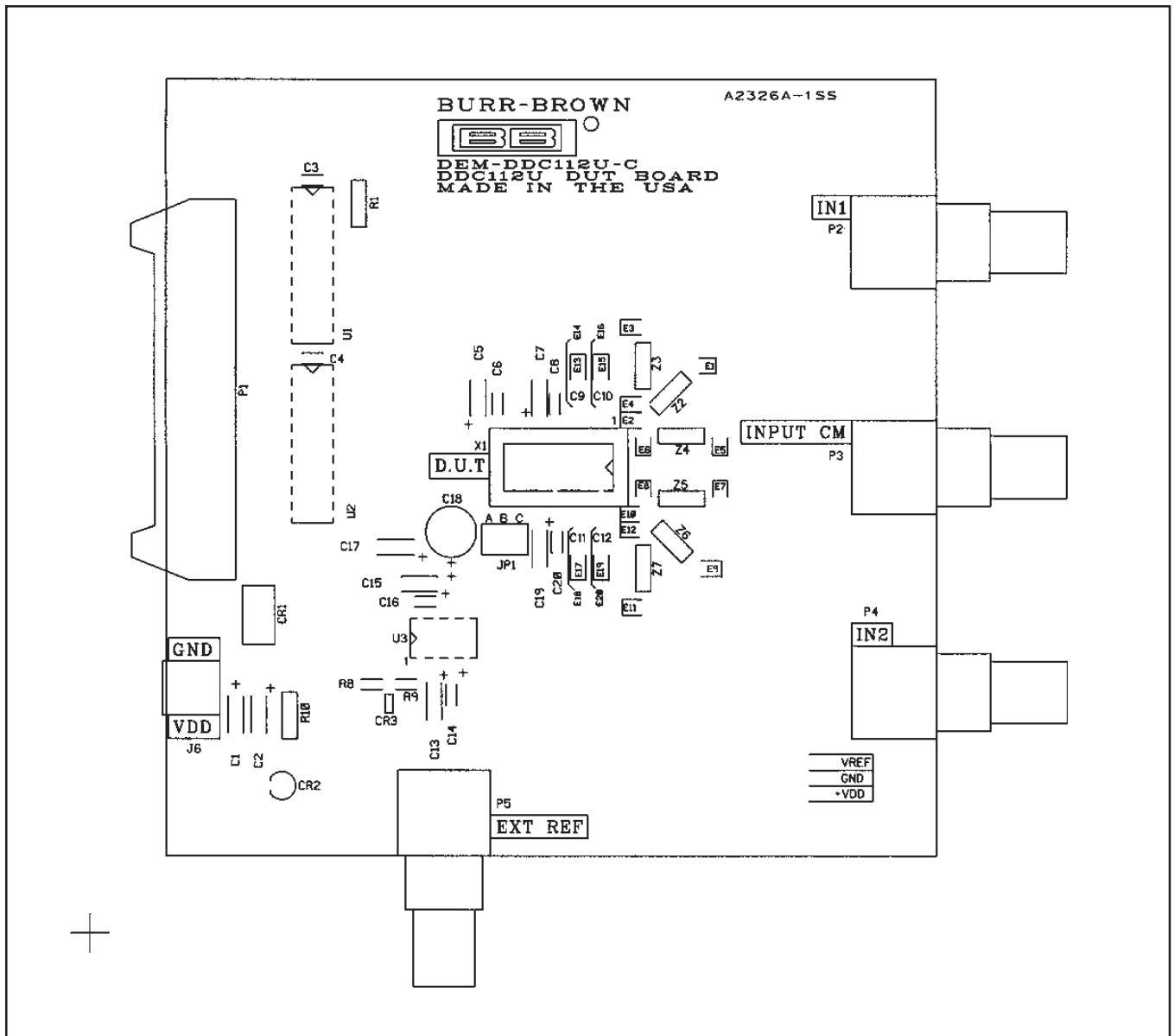
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FIGURE 12. Silkscreen for DEM-DDC112U-C DUT Board.
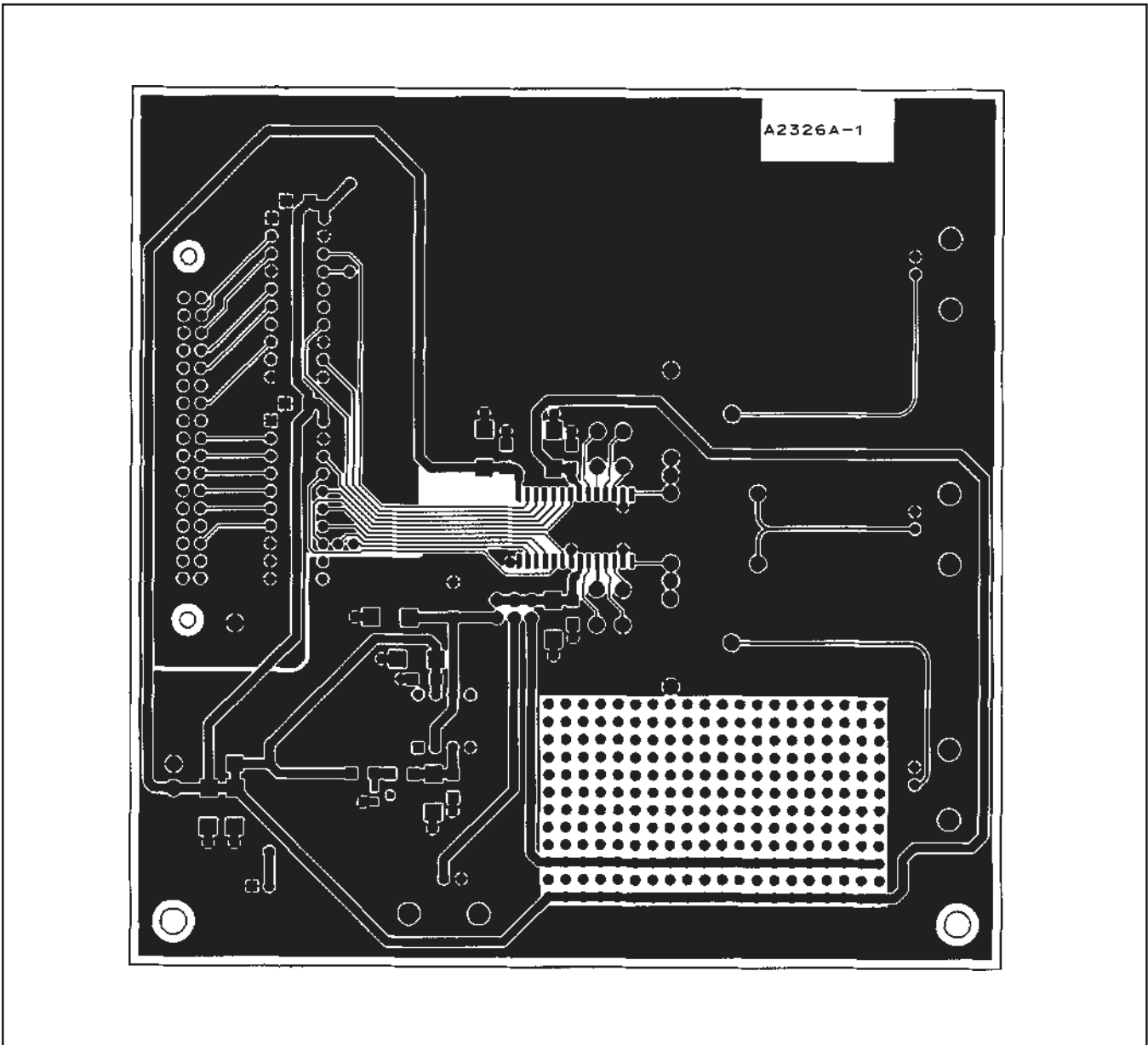
DEM-DDC112U-C

FIGURE 13. Top Layer of DEM-DDC112U-C DUT Board.

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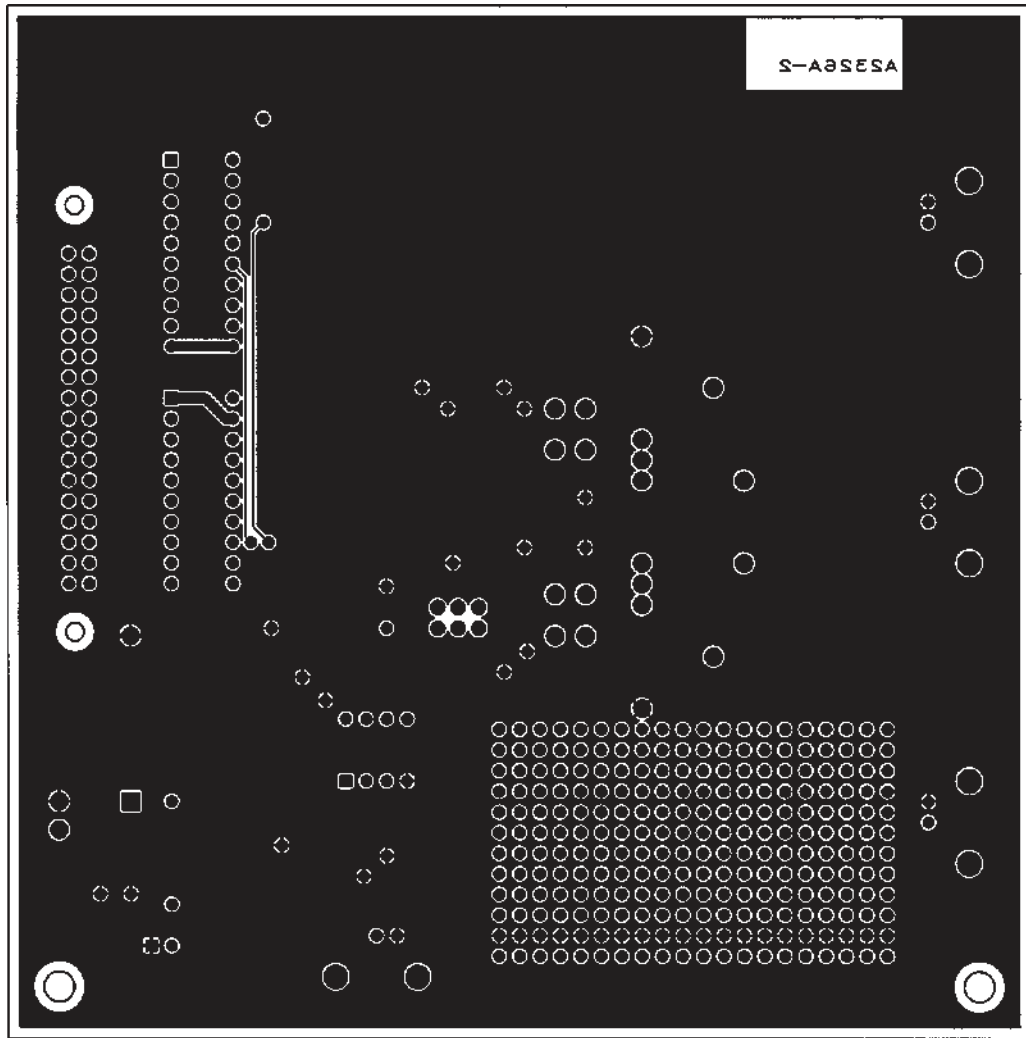
FIGURE 14. Bottom Layer of DEM-DDC112U-C DUT Board.

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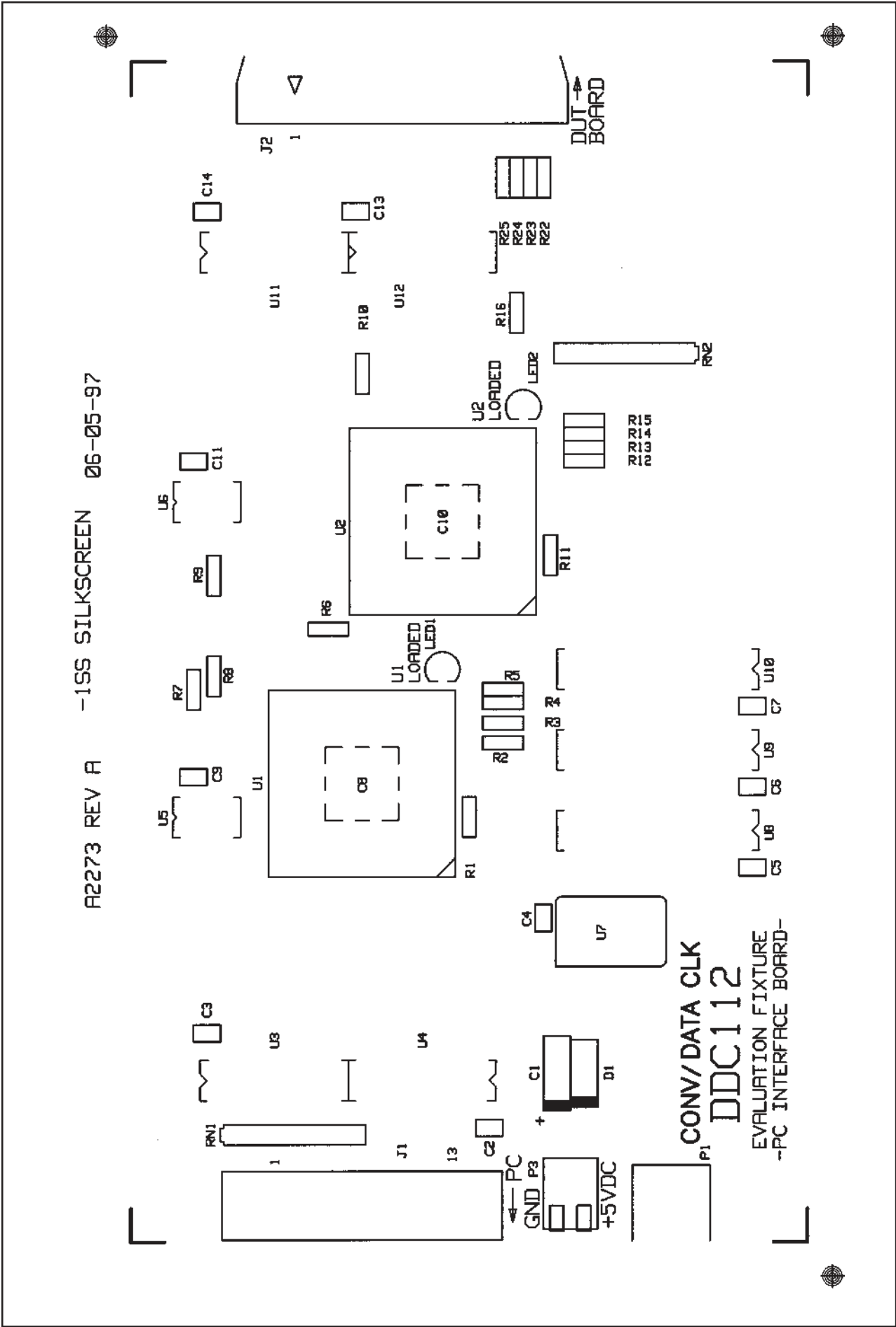
FIGURE 15. Silkscreen for DEM-DDC112U-C PC Interface Board.

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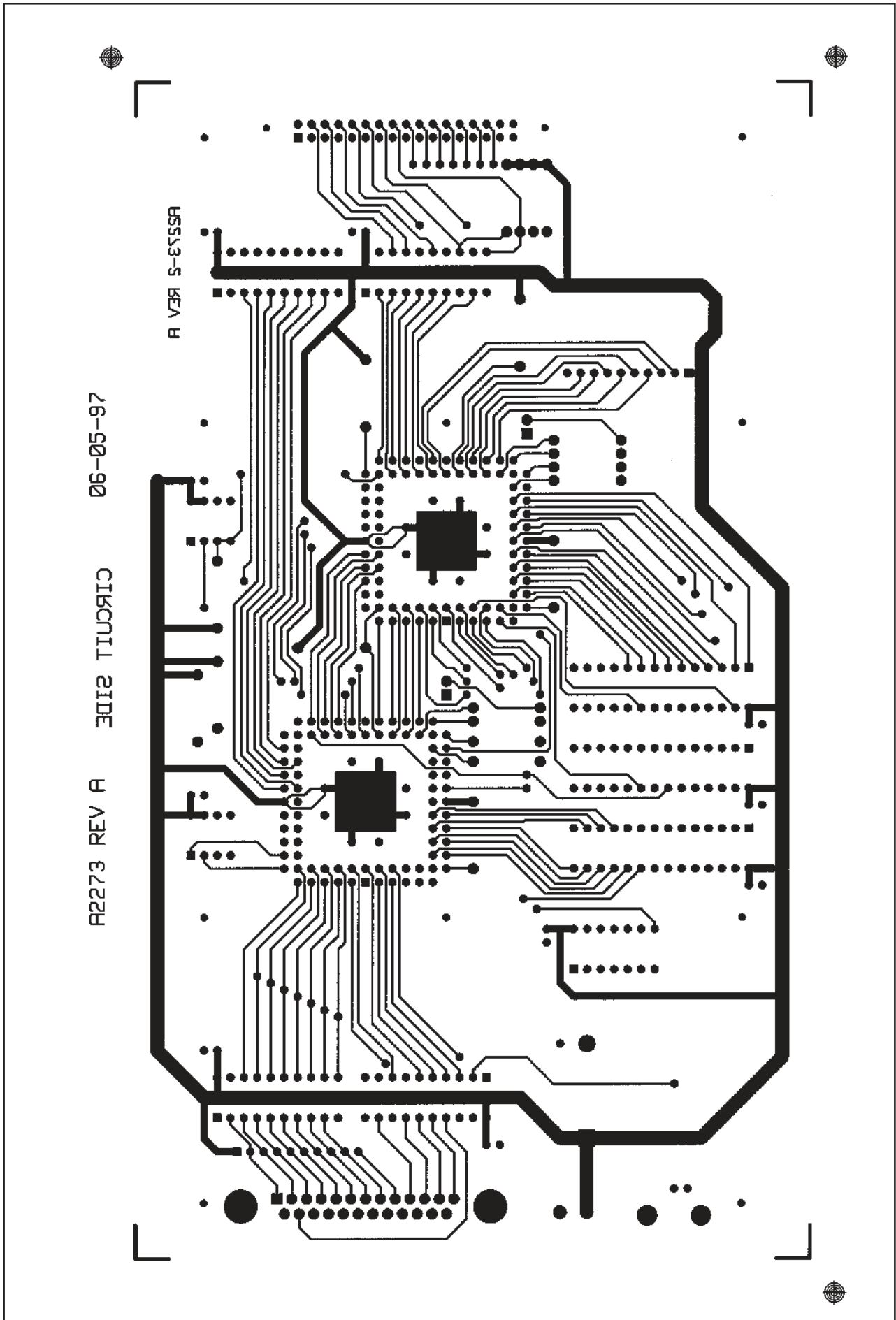
FIGURE 16. Bottom Layer of DEM-DDC112U-C PC Interface Board.

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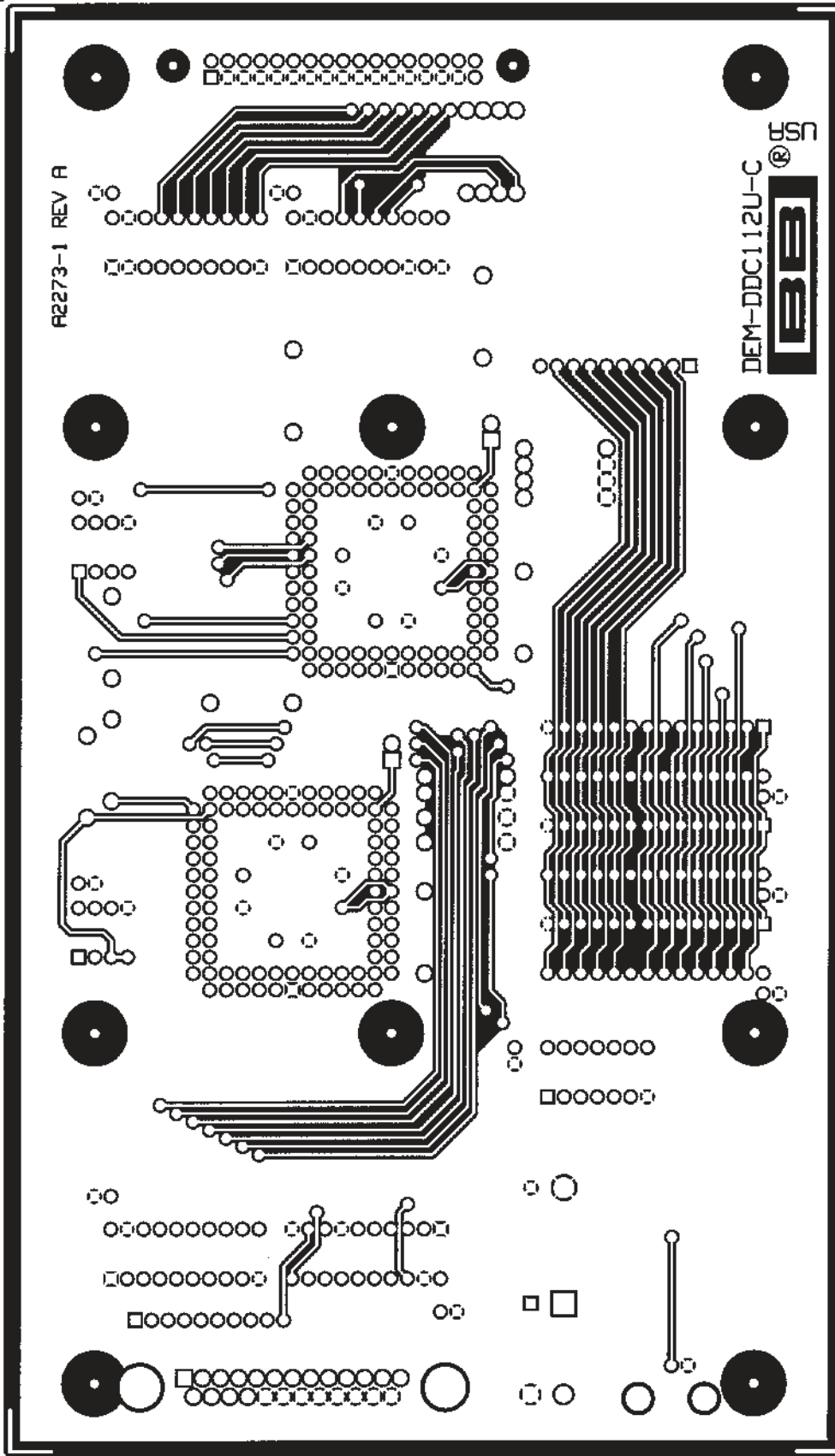
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FIGURE 17 . Top Layer of DEM-DDC112U-C PC Interface Board.

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PARTS LIST—PC INTERFACE BOARD

PART LOCATION	NO. PER KIT	PART NUMBER	VENDOR	DESCRIPTION
	1	A2273	Burr-Brown	DDC112 Evaluation Fixture-PC Interface Board
U1, U2	2	XC3042-70-PLCC84	Xilinx	Programmable Gate Array
U1, U2 (Sockets)	2	PCS-084A-1	Augat	84-pin PLCC Socket
C_8, C_{10}	2	503AHL	Rogers	Decoupling Capacitors for Xilinx
U5, U6	2	XC1736DPD8C	Xilinx	Gate Array Control Prom
U5, U6 (Sockets)	2	508-AG11D-E-S		8-pin Single Wide DIP Socket
U8, U9, U10	3	IDT71256SA15TP	IDT	8 x 32K Memory
U12	1	74HCT244N	TI	Digital Buffers
U3, U4, U11	3	74HCT541N	TI	Digital Buffers
J1	1	747842-6	AMP	25-pin Male Right Angle D Connector with Hold Down Clip
J2	1	3431-1202	3M	34-pin Male Ribbon Connector
To Connect DUT Board	1	3414-6034	3M	34-pin Wiremount Socket
LED 1, LED 2	2	CMD5453	Chicago Miniature	LED (2V, 20mA)
U7	1	CTX119-ND	Digi-Key	20MHz Clock Oscillator, (CTS)
P1	1	227161-2	AMP	BNC Right Angle, PC Mount Connectors
RN_1, RN_2	2	CSC10A-01-103F		10-pin SIP Resistor Network (10kΩ, 9R, 1C)
R_1 - R_{16}	16	RN55C4751F		4.7kΩ Resistor, 1%
R_{22} - R_{25}	4	RN55C1002F		10kΩ Resistor, 1%
D1	1	IN5820		1W Diode
C_2 - C_7, C_9, C_{11}, C_{13}, C_{14}	10	RFE121X7R104K050V	0.1 Inch spacing	0.1μF Capacitors
C_1	1	T110B106K020AS	Kermet	10μF Polarized Capacitors, 20V, 10%
P3	1	2SV-02	AUGAT/RDI	Terminal Block
Legs	8	313-6487-016	E.F. Johnson	1/2 Inch Hex Spacer, 6-32 Thread
To Attach Legs	8			0.25 Inch Round Head Screw, 6-32 Thread

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PARTS LIST—DUT BOARD

PART LOCATION	NO. PER KIT	PART NUMBER	VENDOR	DESCRIPTION
	1	A2326	Burr-Brown	DDC112 DUT Board
U1	1	74HCT244N	TI	Octal Digital Buffer
U2	1	74HCT541N	TI	Octal Digital Buffer
U1, U2 (Sockets)	2	520-AG11D-ES	Augat	20-pin DIP Socket
P4 (Tops)	1	31165102	RIACON	2-pin Terminal Block Top, 3.5mm Center
P4 (Pins)	1	31024102	RIACON	2-pin Terminal Block Pins, 3.5mm Centers
X1	1	DDC112U	Burr-Brown	Two-Channel A/D Converter
X1 (Socket, Socket Top)	1	SOP-28B0SMT-TT	Robinson-Nugent	SMT SOP Socket, 0.375" Row Spacing, Body and Frame
U3	1	OPA350PA	Burr-Brown	Operational Amplifier
U3 (Socket)	1	508-AG11D-ES	Augat	8-pin DIP Socket
CR3	1	LM4040AIM-4.1	National Semiconductor	4.1 Voltage Reference, SOT-23 Package
P1	1	IDH-34LP-SR3-TG	Robinson-Nugent	Right Angle, 17x2 Connector
P2 - P5	4	227161-2	AMP	Right Angle BNC Connector
J6 (Pins)	1	31024102	RIACON	2-pin Terminal Block Pins, 3.5mm Centers
J6 (Tops)	1	31165102	RIACON	2-pin Terminal Block Tops, 3.5mm Centers
CR1	1	IN5820	Motorola	Shottsky Diode, 3A
CR2		HLMP-3201	Hewlett-Packard	Red LED
C_1, C_2, C_5, C_7, C_{13}, C_{15}, C_{17}, C_{19}	8	293D106X9020C2T	Sprague	10μF, 20V, SM Capacitors
C_3, C_4, C_6, C_8, C_{14}, C_{16}, C_{20}	7	C1206C104K5RAC3972	Kemet	0.1μF SM Capacitors
C_9, C_{10}, C_{11}, C_{12}	4	C315C271J1G5CA	Kemet	270pF, 100V, Capacitors
C_{18}	1	Open	Open	Open
R_1	1	RN55C1002	Dale	10kΩ, 1%, 1/8W Resistor
Z_3, Z_4, Z_5, Z_7	4	Open	Open	Open
Z_2, Z_6	2	MK632, 10M	Caddock	10MΩ, 1%, Resistor
R_8	1	CRCW124991F	Dale	4.99kΩ, 1%, 1/8W SM Chip Resistor
R_9	1	CRCW12061002F	Dale	10kΩ, 1%, 1/8W SM Chip Resistor
R_{10}	1	RN55C1621F	Dale	1.62kΩ, 1%, 1/8W Resistor
E1 - E20	20	50863-5	AMP	Resistor Sockets, Hotlite Socket .0, "E" Point 0.062 Drill
JP1 (Pins)	1	TSW-103-07-T-D	Samtec	3x2 Jumper Headers
JP1 (Tops)	1	SNT-100-BK-T	Samtec	Jumper Top (JP1, Position A)
Legs	4	313-6487-008	E.F. Johnson	1/4 Inch Hex Spacer, 6-32 Thread
To Separate Bottom Ground Plane from DUT Board	4	313-6487-008	E.F. Johnson	1/4 Inch Hex Spacer, 6-32 Thread
To Separate Top Ground Plane from DUT Board	2	555-7003-044	Concord	3/4 Inch Hinged Spacer, 6-32 Thread
To Separate Top Ground Plane from DUT Board	2	542-7612	Concord	3/4 Inch Spacer, 6-32 Thread
To Connect Three Boards	4			0.75 Inch Round Head Screw, 6-32 Thread
To Connect Top	2			0.25 Inch Round Head Screw, 6-32 Thread

CABLES

PART LOCATION	NO. PER KIT	PART NUMBER	VENDOR	DESCRIPTION
Between PC and Interface Board	8 Feet			25-Line Ribbon Cable
Between PC and Interface Board	1	8325-6060	3M	25-Pin Female Connector
Between PC and Interface Board	1	8225-6060	3M	25-Pin Male Connector
Between Interface Board and DUT Board	6 Inches			34-Line Ribbon Cable
Between Interface Board and DUT Board	2	3414-6034	3M	34-Pin Female Connector

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