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April 2014

# FQA62N25C

## N-Channel QFET<sup>®</sup> MOSFET

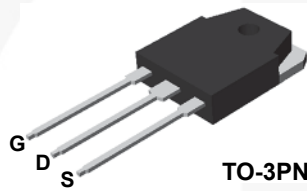
250 V, 62 A, 35 mΩ

### Description

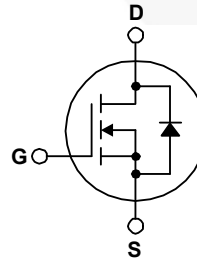
This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

### Features

- 62 A, 250 V,  $R_{DS(on)} = 35 \text{ m}\Omega$  (Max.) @  $V_{GS} = 10 \text{ V}$ ,  $I_D = 31 \text{ A}$
- Low Gate Charge (Typ. 100 nC)
- Low  $C_{rss}$  (Typ. 63.5 pF)
- 100% Avalanche Tested



TO-3PN



### Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FQA62N25C	Unit
$V_{DSS}$	Drain-Source Voltage	250	V
$I_D$	Drain Current - Continuous ( $T_C = 25^\circ\text{C}$ )	62	A
	- Continuous ( $T_C = 100^\circ\text{C}$ )	39	A
$I_{DM}$	Drain Current - Pulsed (Note 1)	248	A
$V_{GSS}$	Gate-Source Voltage	$\pm 30$	V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	2300	mJ
$I_{AR}$	Avalanche Current (Note 1)	62	A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	29.8	mJ
$dv/dt$	Peak Diode Recovery $dv/dt$ (Note 3)	5.5	V/ns
$P_D$	Power Dissipation ( $T_C = 25^\circ\text{C}$ )	298	W
	- Derate above $25^\circ\text{C}$	2.38	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
$T_L$	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ\text{C}$

### Thermal Characteristics

Symbol	Parameter	FQA62N25C	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	0.42	$^\circ\text{C}/\text{W}$
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink, Typ.	0.24	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	40	$^\circ\text{C}/\text{W}$

FQA62N25C — N-Channel QFET<sup>®</sup> MOSFET

## Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQA62N25C	FQA62N25C	TO-3PN	Tube	N/A	N/A	30 units

## Electrical Characteristics T<sub>c</sub> = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
<b>Off Characteristics</b>						
B <sub>V</sub> DSS	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	250	--	--	V
ΔB <sub>V</sub> DSS / ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, Referenced to 25°C	--	0.28	--	V/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 250 V, V <sub>GS</sub> = 0 V	--	--	10	μA
		V <sub>DS</sub> = 200 V, T <sub>C</sub> = 125°C	--	--	100	μA
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = 30 V, V <sub>DS</sub> = 0 V	--	--	100	nA
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	V <sub>GS</sub> = -30 V, V <sub>DS</sub> = 0 V	--	--	-100	nA

### On Characteristics

V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2.0	--	4.0	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 31 A	--	0.029	0.035	Ω
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 40 V, I <sub>D</sub> = 31 A	--	55	--	S

### Dynamic Characteristics

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz	--	4830	6280	pF
C <sub>oss</sub>	Output Capacitance		--	945	1230	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		--	63.5	83	pF

### Switching Characteristics

t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 125 V, I <sub>D</sub> = 62 A, R <sub>G</sub> = 25 Ω  (Note 4)	--	75	160	ns
t <sub>r</sub>	Turn-On Rise Time		--	395	800	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		--	245	500	ns
t <sub>f</sub>	Turn-Off Fall Time		--	335	680	ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> = 200 V, I <sub>D</sub> = 62 A, V <sub>GS</sub> = 10 V  (Note 4)	--	100	130	nC
Q <sub>gs</sub>	Gate-Source Charge		--	25.5	--	nC
Q <sub>gd</sub>	Gate-Drain Charge		--	39	--	nC

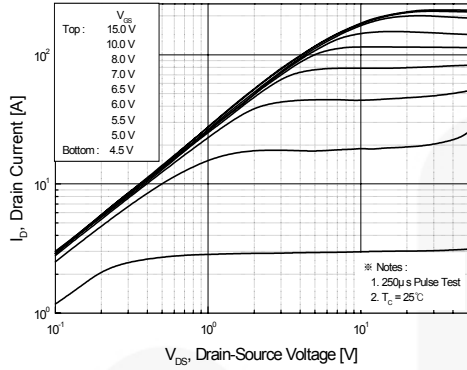
### Drain-Source Diode Characteristics and Maximum Ratings

I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current	--	--	62	A	
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current	--	--	248	A	
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 62 A	--	--	1.5	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 62 A,	--	340	--	ns
Q <sub>rr</sub>	Reverse Recovery Charge	dI <sub>F</sub> / dt = 100 A/μs	--	4.77	--	μC

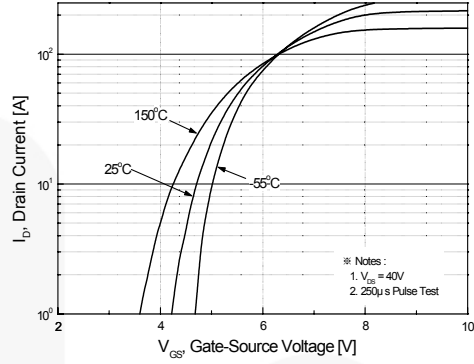
#### Notes:

1. Repetitive rating : pulse-width limited by maximum junction temperature.
2. L = 0.96 mH, I<sub>AS</sub> = 62 A, V<sub>DD</sub> = 50 V, R<sub>G</sub> = 25 Ω, starting T<sub>J</sub> = 25°C.
3. I<sub>SD</sub> ≤ 62 A, di/dt ≤ 300 A/μs, V<sub>DD</sub> ≤ B<sub>V</sub>DSS, starting T<sub>J</sub> = 25°C.
4. Essentially independent of operating temperature.

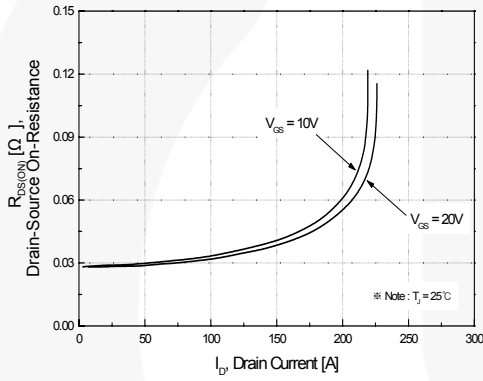
**Typical Performance Characteristics**



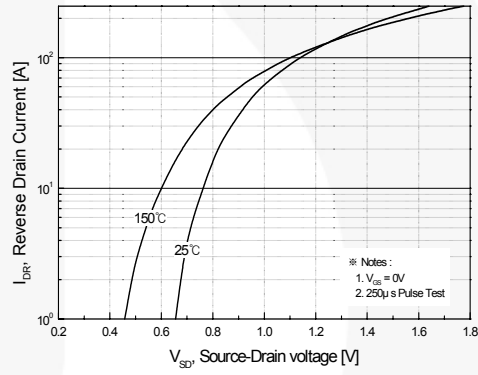
**Figure 1. On-Region Characteristics**



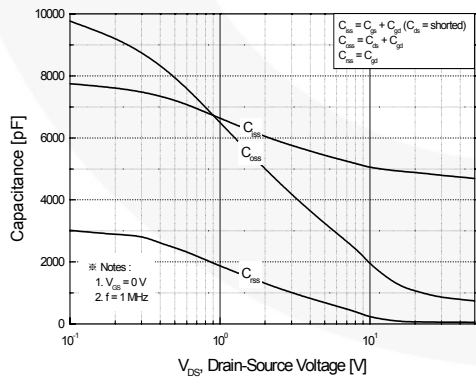
**Figure 2. Transfer Characteristics**



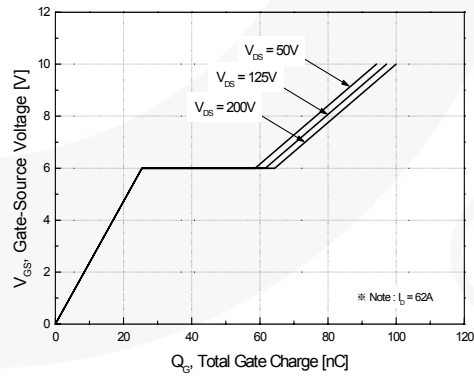
**Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage**



**Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature**

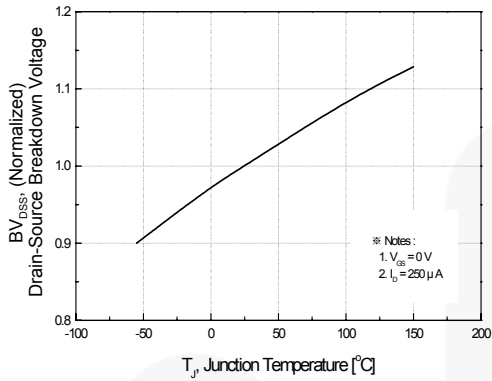


**Figure 5. Capacitance Characteristics**

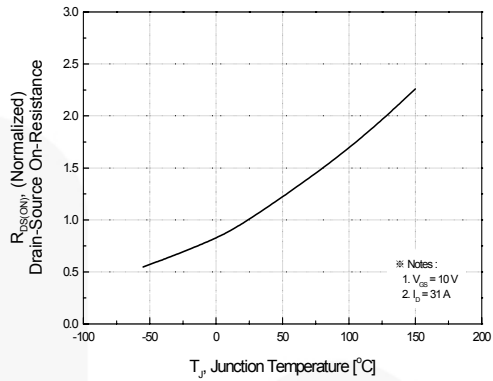


**Figure 6. Gate Charge Characteristics**

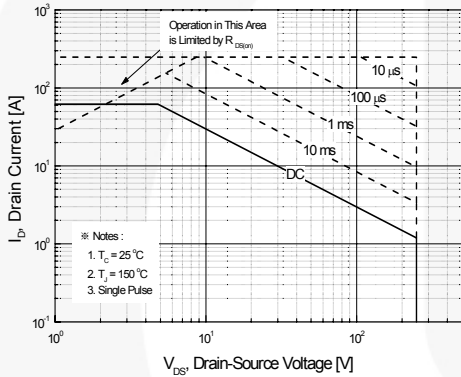
**Typical Performance Characteristics** (Continued)



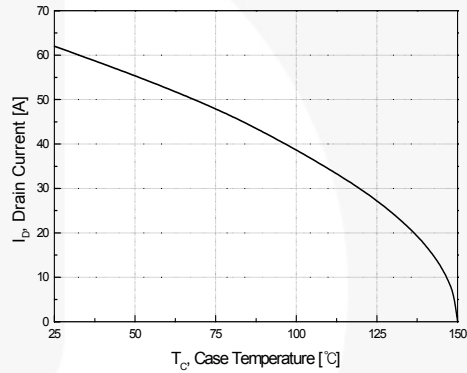
**Figure 7. Breakdown Voltage Variation vs Temperature**



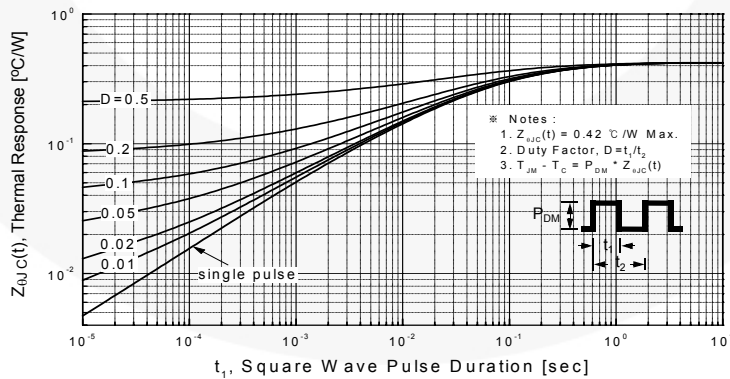
**Figure 8. On-Resistance Variation vs Temperature**



**Figure 9. Maximum Safe Operating Area**



**Figure 10. Maximum Drain Current vs Case Temperature**



**Figure 11. Transient Thermal Response Curve**

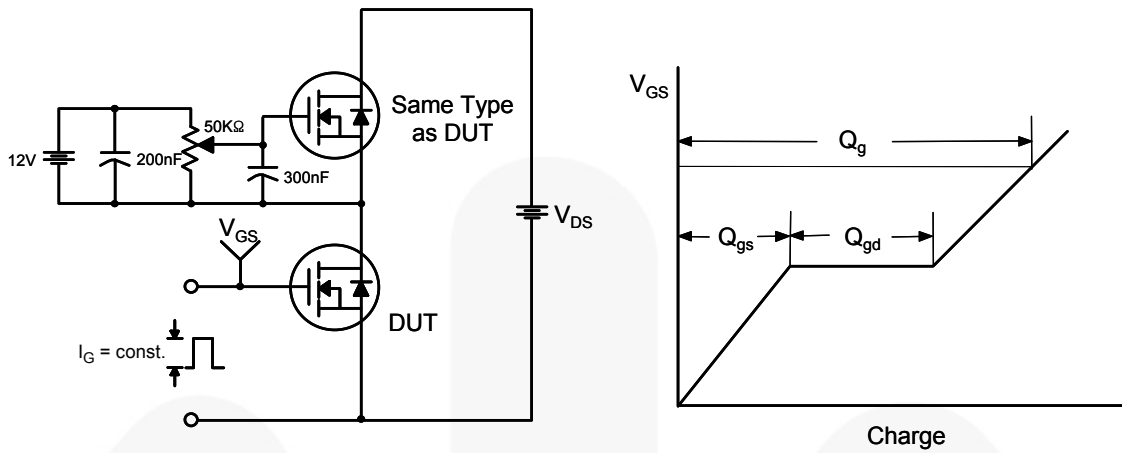


Figure 12. Gate Charge Test Circuit & Waveform

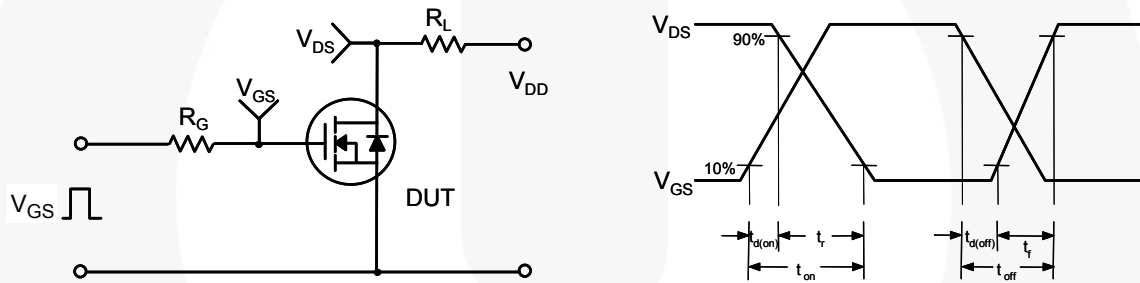


Figure 13. Resistive Switching Test Circuit & Waveforms

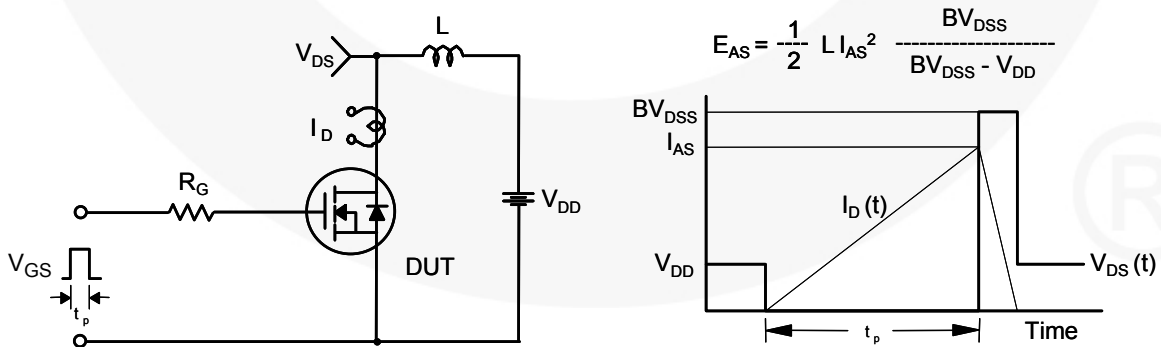


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

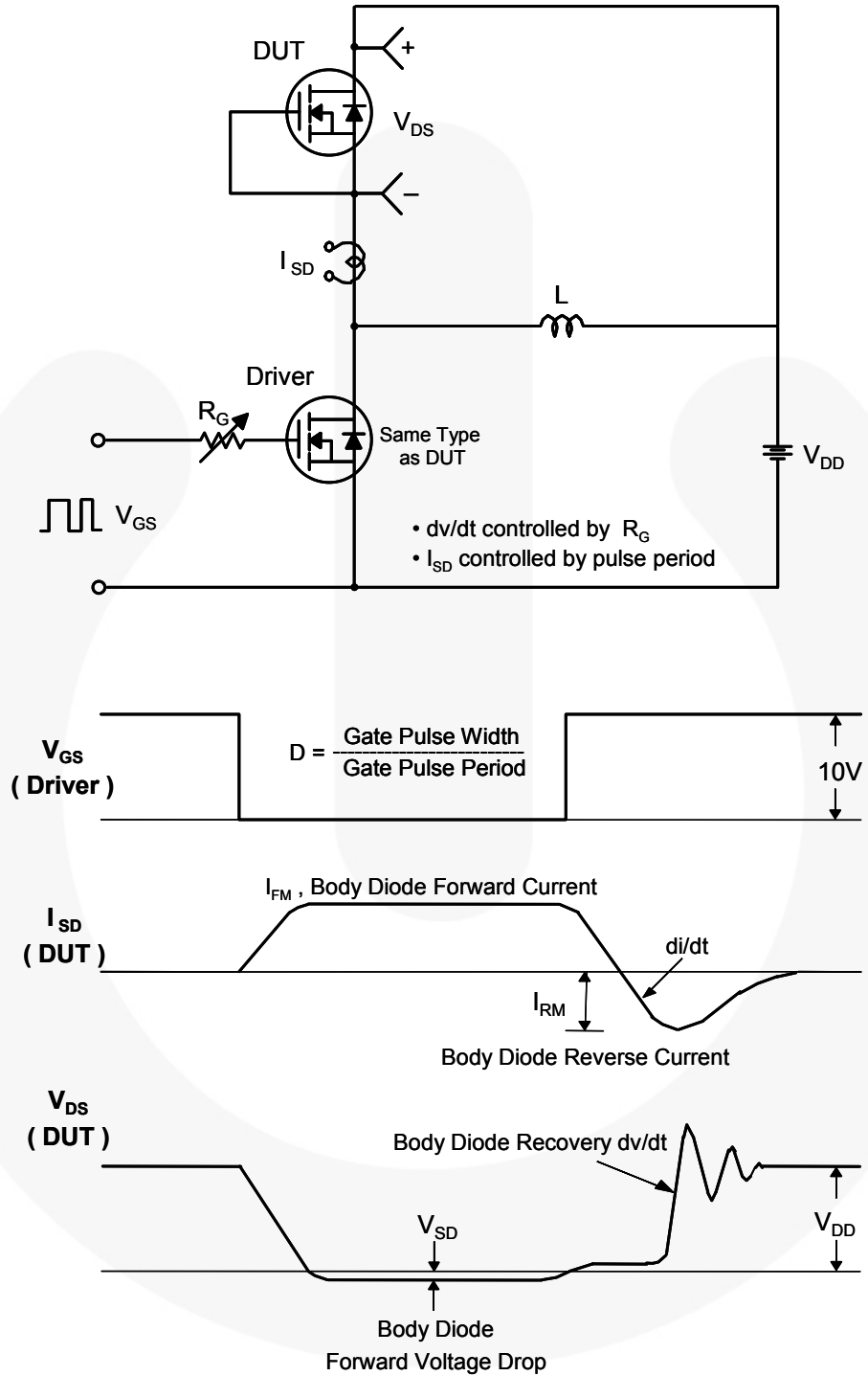
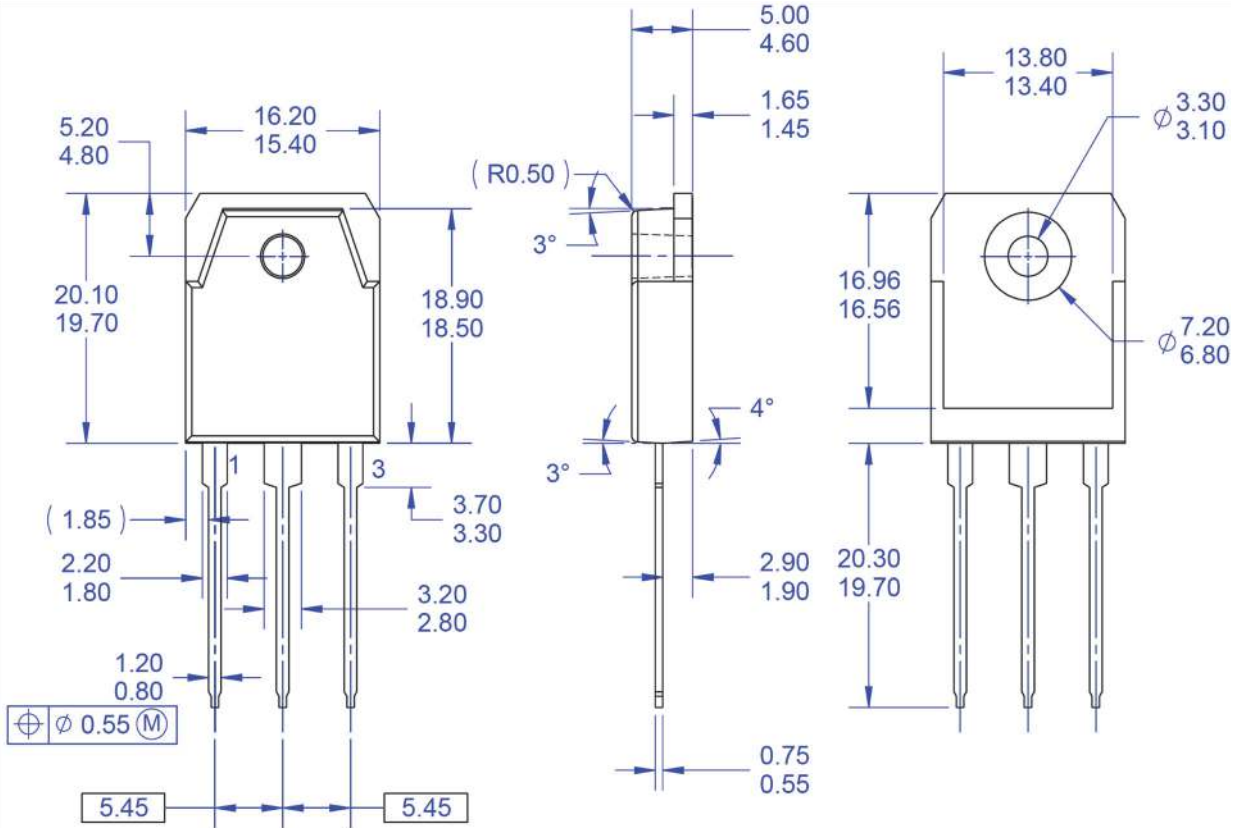


Figure 15. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms

## Mechanical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED

- THIS PACKAGE CONFORMS TO EIAJ SC-65 PACKAGING STANDARD.
- ALL DIMENSIONS ARE IN MILLIMETERS.
- DIMENSION AND TOLERANCING PER ASME14.5-2009.
- DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- DRAWING FILE NAME: TO3PN03AREV1.
- FAIRCHILD SEMICONDUCTOR.

**Figure 16. TO3PN, 3-Lead, Plastic, EIAJ SC-65**

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