

## FEATURES

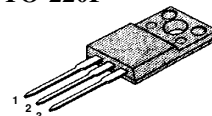
- Avalanche Rugged Technology
- Rugged Gate Oxide Technology
- Lower Input Capacitance
- Improved Gate Charge
- Extended Safe Operating Area
- Lower Leakage Current : 25  $\mu$ A (Max.) @  $V_{DS} = 700V$
- Low  $R_{DS(ON)}$  : 1.552  $\Omega$  (Typ.)

$$BV_{DSS} = 700 V$$

$$R_{DS(on)} = 1.8 \Omega$$

$$I_D = 4 A$$

### TO-220F



1.Gate 2. Drain 3. Source

## Absolute Maximum Ratings

Symbol	Characteristic	Value	Units
$V_{DSS}$	Drain-to-Source Voltage	700	V
$I_D$	Continuous Drain Current ( $T_C=25^\circ C$ )	4	A
	Continuous Drain Current ( $T_C=100^\circ C$ )	2.5	
$I_{DM}$	Drain Current-Pulsed	24	A
$V_{GS}$	Gate-to-Source Voltage ①	$\pm 30$	V
$E_{AS}$	Single Pulsed Avalanche Energy ②	560	mJ
$I_{AR}$	Avalanche Current ①	4	A
$E_{AR}$	Repetitive Avalanche Energy ①	4	mJ
dv/dt	Peak Diode Recovery dv/dt ③	2.5	V/ns
$P_D$	Total Power Dissipation ( $T_C=25^\circ C$ )	40	W
	Linear Derating Factor	0.32	
$T_J, T_{STG}$	Operating Junction and Storage Temperature Range	- 55 to +150	$^\circ C$
$T_L$	Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5-seconds	300	

## Thermal Resistance

Symbol	Characteristic	Typ.	Max.	Units
$R_{\theta_{JC}}$	Junction-to-Case	--	3.13	$^\circ C/W$
$R_{\theta_{JA}}$	Junction-to-Ambient	--	62.5	

## Electrical Characteristics (T<sub>C</sub>=25 °C unless otherwise specified)

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	700	--	--	V	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA
ΔBV/ΔT <sub>J</sub>	Breakdown Voltage Temp. Coeff.	--	0.79	--	V/ °C	I <sub>D</sub> =250μA <b>See Fig 7</b>
V <sub>GS(th)</sub>	Gate Threshold Voltage	2.0	--	4.0	V	V <sub>DS</sub> =5V, I <sub>D</sub> =250μA
I <sub>GSS</sub>	Gate-Source Leakage , Forward	--	--	100	nA	V <sub>GS</sub> =30V
	Gate-Source Leakage , Reverse	--	--	-100		V <sub>GS</sub> =-30V
I <sub>DSS</sub>	Drain-to-Source Leakage Current	--	--	25	μA	V <sub>DS</sub> =700V
		--	--	250		V <sub>DS</sub> =560V, T <sub>C</sub> =125 °C
R <sub>DS(on)</sub>	Static Drain-Source On-State Resistance	--	--	1.8	Ω	V <sub>GS</sub> =10V, I <sub>D</sub> =2A ④*
g <sub>fs</sub>	Forward Transconductance	--	3.22	--	Ω	V <sub>DS</sub> =50V, I <sub>D</sub> =2A ④
C <sub>iss</sub>	Input Capacitance	--	920	1200	pF	V <sub>GS</sub> =0V, V <sub>DS</sub> =25V, f =1MHz <b>See Fig 5</b>
C <sub>oss</sub>	Output Capacitance	--	100	115		
C <sub>rfs</sub>	Reverse Transfer Capacitance	--	45	55		
t <sub>d(on)</sub>	Turn-On Delay Time	--	18	45	ns	V <sub>DD</sub> =350V, I <sub>D</sub> =6A, R <sub>G</sub> =11.5§ <b>See Fig 13</b> ④ ⑤
t <sub>r</sub>	Rise Time	--	23	55		
t <sub>d(off)</sub>	Turn-Off Delay Time	--	76	160		
t <sub>f</sub>	Fall Time	--	26	60		
Q <sub>g</sub>	Total Gate Charge	--	51	67	nC	V <sub>DS</sub> =560V, V <sub>GS</sub> =10V, I <sub>D</sub> =6A <b>See Fig 6 &amp; Fig 12</b> ④ ⑤
Q <sub>gs</sub>	Gate-Source Charge	--	8.3	--		
Q <sub>gd</sub>	Gate-Drain("Miller") Charge	--	23.1	--		

## Source-Drain Diode Ratings and Characteristics

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
I <sub>S</sub>	Continuous Source Current	--	--	4	A	Integral reverse pn-diode in the MOSFET
I <sub>SM</sub>	Pulsed-Source Current ①	--	--	24		
V <sub>SD</sub>	Diode Forward Voltage ④	--	--	1.4	V	T <sub>J</sub> =25 °C, I <sub>S</sub> =4A, V <sub>GS</sub> =0V
t <sub>rr</sub>	Reverse Recovery Time	--	440	--	ns	T <sub>J</sub> =25 °C, I <sub>F</sub> =6A
Q <sub>rr</sub>	Reverse Recovery Charge	--	4.05	--	μC	di <sub>F</sub> /dt=100A/μs ④

### Notes ;

- ① Repetitive Rating : Pulse Width Limited by Maximum Junction Temperature
- ② L=65mH, I<sub>AS</sub>=4A, V<sub>DD</sub>=50V, R<sub>G</sub>=27Ω, Starting T<sub>J</sub>=25 °C
- ③ I<sub>SD</sub>≤6A, di/dt≤140A/μs, V<sub>DD</sub>≤BV<sub>DSS</sub>, Starting T<sub>J</sub>=25 °C
- ④ Pulse Test : Pulse Width = 250 μs, Duty Cycle ≤2%
- ⑤ Essentially Independent of Operating Temperature

Fig 1. Output Characteristics

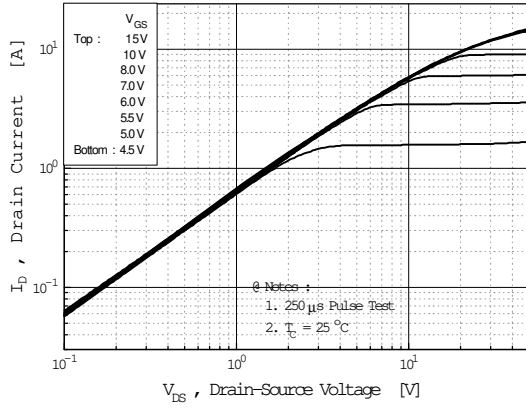


Fig 2. Transfer Characteristics

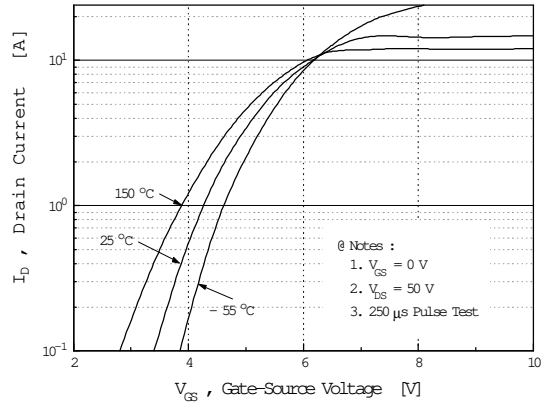


Fig 3. On-Resistance vs. Drain Current

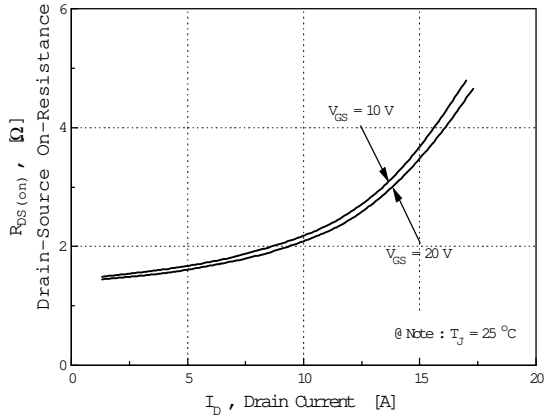


Fig 4. Source-Drain Diode Forward Voltage

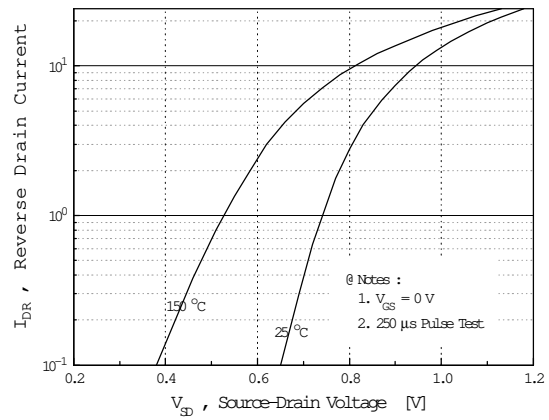


Fig 5. Capacitance vs. Drain-Source Voltage

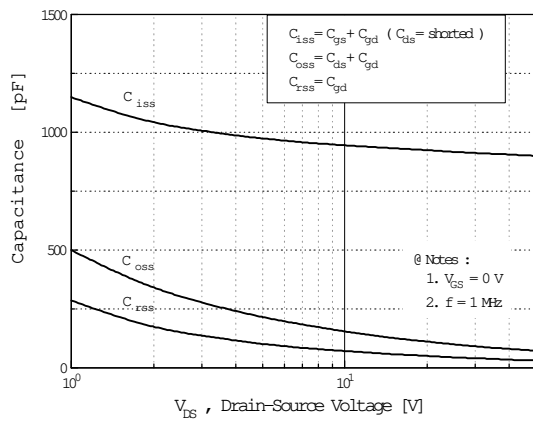
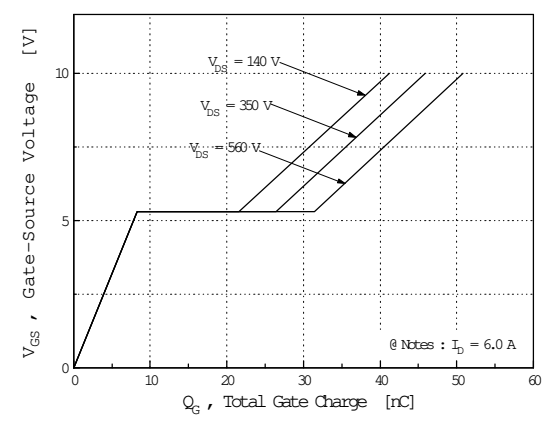
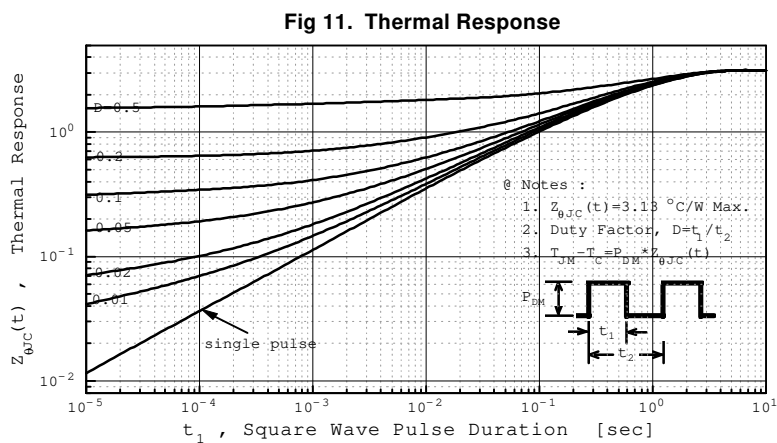
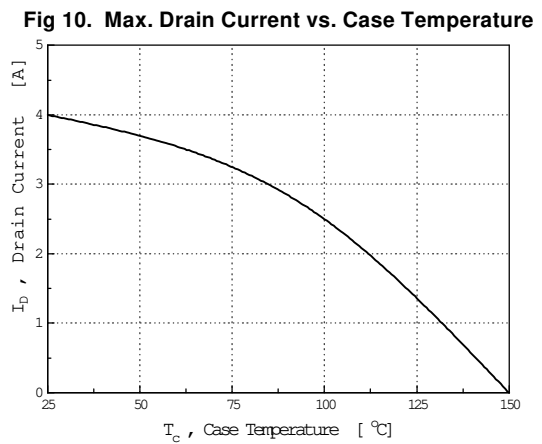
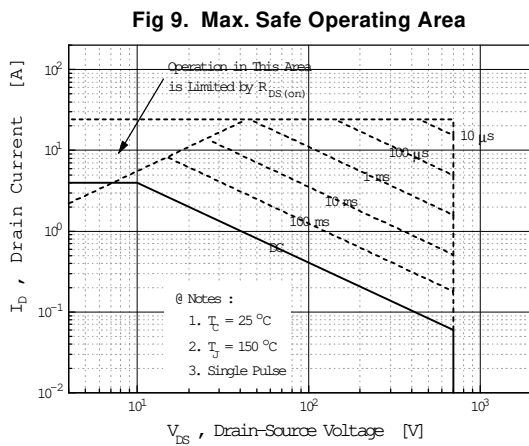
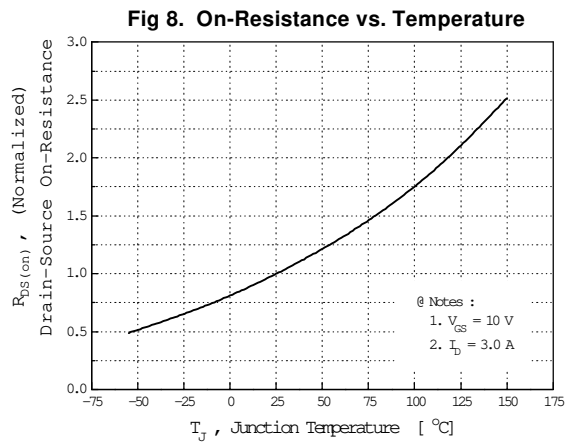
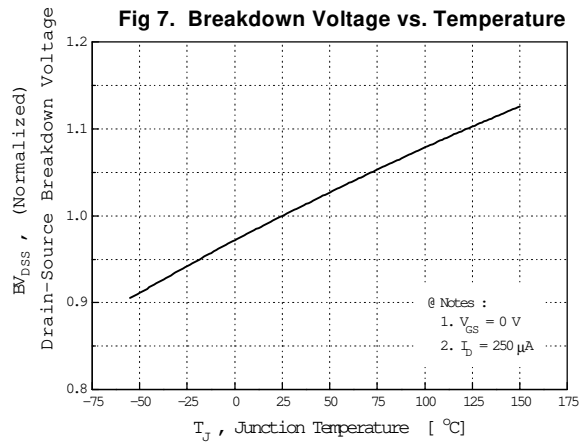


Fig 6. Gate Charge vs. Gate-Source Voltage

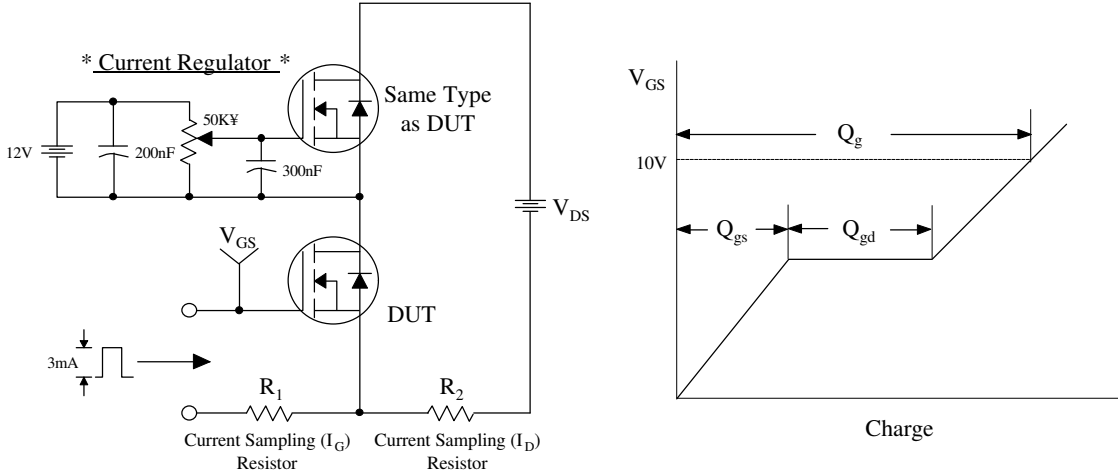


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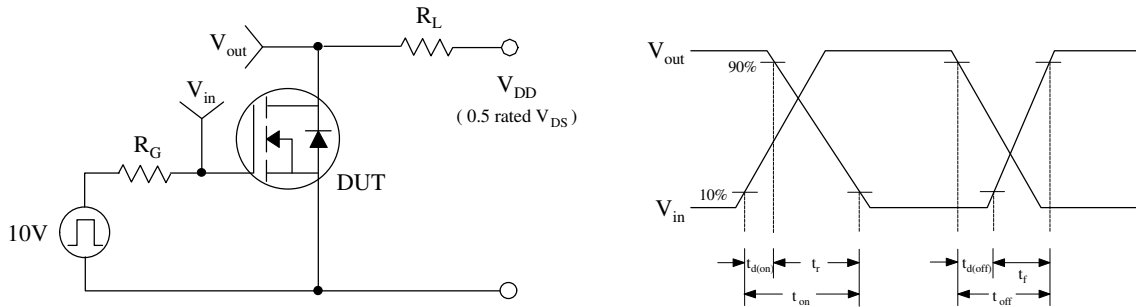
N-C HANNEL  
POWER MOSFET



**Fig 12. Gate Charge Test Circuit & Waveform**



**Fig 13. Resistive Switching Test Circuit & Waveforms**



**Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms**

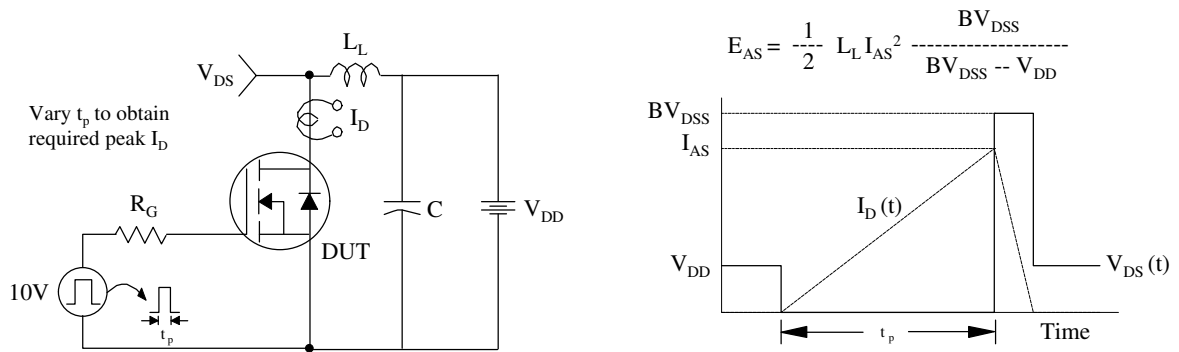
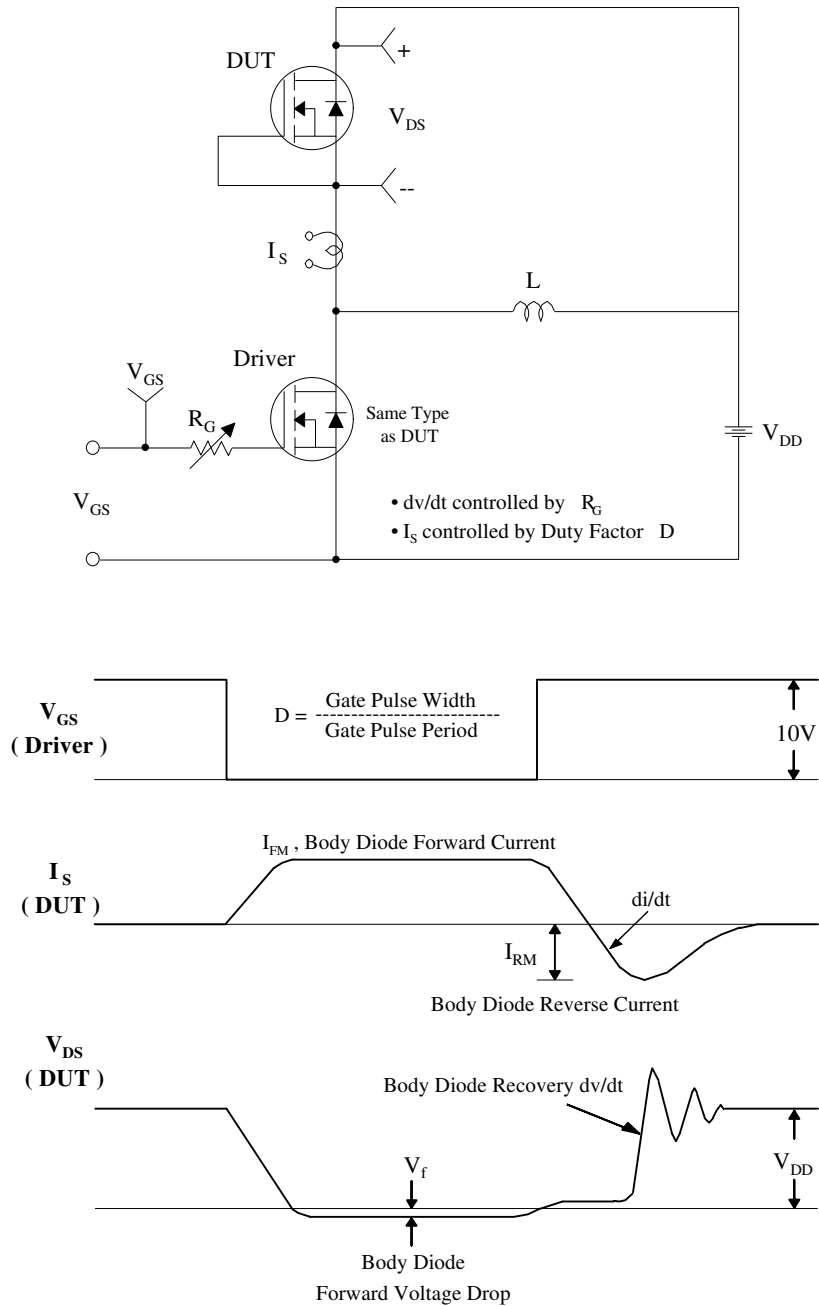


Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



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