



Optimized Reconfigurable Cell Array (ORCA) ATT2Cxx Series Field-Programmable Gate Arrays

Features

- High-performance, cost-effective 0.5 μm technology (four-input look-up table delay less than 3.6 ns)
- High density (up to 43,200 usable, logic-only gates, or 99,400 gates including RAM)
- Up to 480 user I/Os
- Fast on-chip user SRAM: 64 bits/logic block
- Nibble-oriented architecture for implementing 4-, 8-, 16-, 32-bit (or wider) bus structures
- Innovative, abundant, and hierarchical nibble-oriented routing resources that allow automatic use of internal gates for all device densities without sacrificing performance
- Four 16-bit look-up tables and four latches/flip-flops per logic block
- Internal fast carry for arithmetic functions
- TTL or CMOS input thresholds programmable per pin
- Individually programmable drive capability: 12 mA sink/6 mA source or 6 mA sink/3 mA source
- Built-in boundary scan (*IEEE 1149.1*)
- Low power consumption from submicron CMOS process
- Full PCI-bus compliance
- Supported by industry-standard CAE tools for design entry, synthesis, and simulation
- ORCA Foundry Development System support

Description

The Lucent Technologies Optimized Reconfigurable Cell Array (ORCA) series is the second generation of SRAM-based field-programmable gate arrays (FPGAs) from Lucent. The ORCA 2C FPGA series provides seven CMOS FPGAs ranging in complexity from 4,800 to 43,200 usable gates in a variety of packages, speed grades, and temperature ranges. Table 1 lists the usable gates for the 0.5 μm ORCA 2C series FPGAs.

The ORCA series FPGA consists of two basic elements: programmable logic cells (PLCs) and programmable input/output cells (PICs). An array of PLCs is surrounded by PICs. Each PLC contains a programmable function unit (PFU). The PLCs and PICs also contain routing resources and configuration RAM. All logic is done in the PFU. Each PFU contains four 16-bit look-up tables (LUTs) and four latches/flip-flops (FFs).

The PLC architecture provides a balanced mix of logic and routing which allows a higher utilized gate/PFU than alternative architectures. The routing resources carry logic signals between PFUs and I/O pads. The routing in the PLC is symmetrical about the horizontal and vertical axes. This improves routability by allowing a signal to be routed into the PLC from any direction.

Table 1. ORCA 2C Series FPGAs

| Device | Usable Gates* | Latches/ Flip-Flops | Max User RAM Bits | User I/Os | Array Size |
|--------|---------------|------------------------|-------------------------|--------------|---------------|
| 2C04 | 4,800—11,000 | 400 | 6,400 | 160 | 10 x 10 |
| 2C06 | 6,900—15,900 | 576 | 9,216 | 192 | 12 x 12 |
| 2C08 | 9,400—21,600 | 784 | 12,544 | 224 | 14 x 14 |
| 2C10 | 12,300—28,300 | 1024 | 16,384 | 256 | 16 x 16 |
| 2C12 | 15,600—35,800 | 1296 | 20,736 | 288 | 18 x 18 |
| 2C15 | 19,200—44,200 | 1600 | 25,600 | 320 | 20 x 20 |
| 2C26 | 27,600—63,600 | 2304 | 36,864 | 384 | 24 x 24 |
| 2C40 | 43,200—99,400 | 3600 | 57,600 | 480 | 30 x 30 |

* The first number in the usable gates column assumes 48 gates per PFU for logic-only designs. The second number assumes 30% of a design is RAM. PFUs used as RAM are counted at 4 gates per bit, with each PFU capable of implementing a 16 x 4 RAM (or 256 gates) per PFU.

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Description (continued)

The ORCA Foundry Development System is used to process a design from a netlist to a configured FPGA. Lucent provides interfaces and libraries to popular CAE tools for design entry and simulation.

The FPGA's functionality is determined by internal configuration RAM. The FPGA's internal initialization/configuration circuitry loads the configuration data at powerup or under system control. The RAM is loaded by using one of several configuration modes. The configuration data resides externally in an EEPROM, EPROM, or ROM on the circuit board, or any other storage media. Serial ROMs provide a simple, low pin count method for configuring FPGAs.

ORCA Foundry Development System Overview

The ORCA Foundry Development System interfaces to front-end design entry tools and provides the tools to produce a configured FPGA. In the design flow, the user defines the functionality of the FPGA at two points in the design flow: at design entry and at the bit stream generation stage.

Following design entry, the development system's map, place, and route tools translate the netlist into a routed FPGA. Its bit stream generator is then used to generate the configuration data which is loaded into the FPGA's internal configuration RAM. When using the bit stream generator, the user selects options that affect the functionality of the FPGA. Combined with the front-end tools, ORCA Foundry produces configuration data that implements the various logic and routing options discussed in this data sheet.

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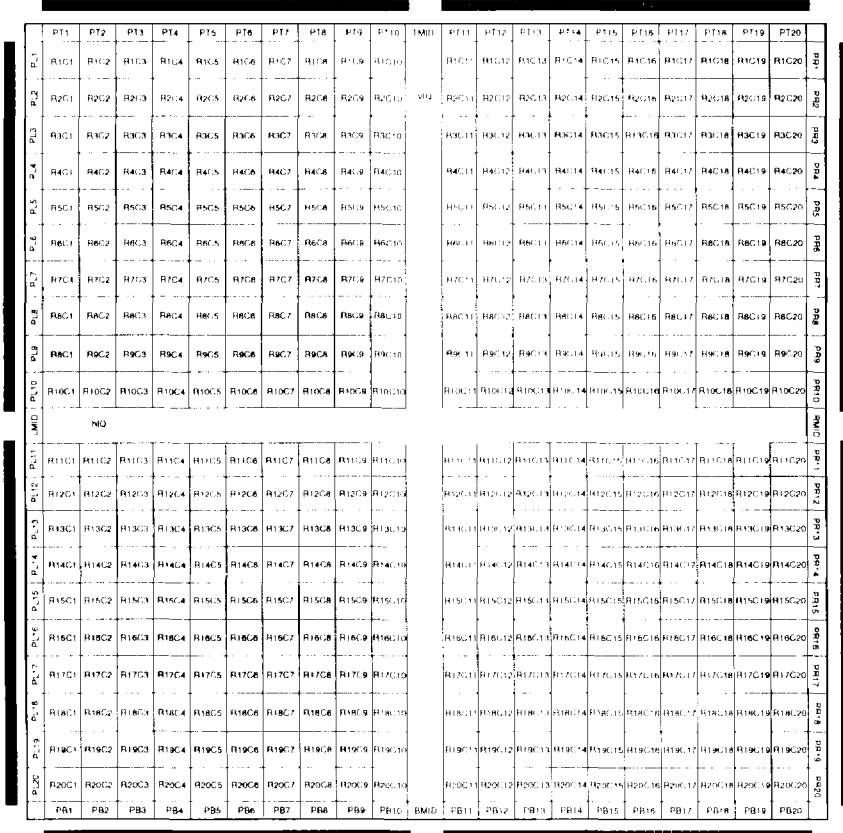


Figure 1. ATT2C15 Array

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Architecture

The ORCA Series FPGA is comprised of two basic elements: PLCs and PICs. Figure 1 shows an array of programmable logic cells (PLCs) surrounded by programmable input/output cells (PICs). The ATT2C15 has PLCs arranged in an array of 20 rows and 20 columns. PICs are located on all four sides of the FPGA between the PLCs and the IC edge. The location of a PLC is indicated by its row and column so that a PLC in the second row and third column is R2C3. PICs are indicated similarly, with PT (top) and PB (bottom) designating rows and PL (left) and PR (right) designating columns, followed by a number. The routing resources and configuration RAM are not shown, but the interquad routing blocks (hIQ, vIQ) present in the 2C series are shown.

Each PIC contains the necessary I/O buffers to interface to bond pads. The PICs also contain the routing resources needed to connect signals from the bond pads to/from PLCs. The PICs do not contain any user-accessible logic elements, such as flip-flops.

Combinatorial logic is done in look-up tables (LUTs) located in the PFU. The PFU can be used in different modes to meet different logic requirements. The LUT's configurable medium-/large-grain architecture can be used to implement from one to four combinatorial logic functions. The flexibility of the LUT to handle wide input functions as well as multiple smaller input functions maximizes the gate count/PFU.

Programmable Logic Cells

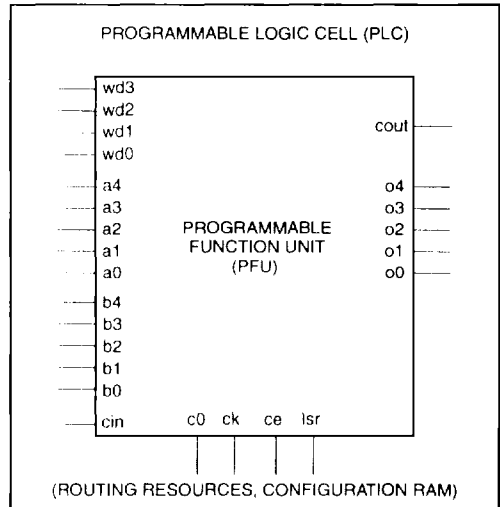
The programmable logic cell (PLC) consists of a programmable function unit (PFU) and routing resources. All PLCs in the array are identical. The PFU, which contains four LUTs and four latches/FFs for logic implementation, is discussed in the next section.

Programmable Function Unit

The programmable function units (PFUs) are used for logic. The PFU has 19 external inputs and six outputs and can operate in several modes. The functionality of the inputs and outputs depends on the operating mode.

The PFU uses three input data buses (a[4:0], b[4:0], wd[3:0]), four control inputs (c0, ck, ce, lsr), and a carry input (cin); the last is used for fast arithmetic functions. There is a 5-bit output bus (o[4:0]) and a carry-out (cout).

Figure 2 and Figure 3 show high-level and detailed views of the ports in the PFU, respectively. The ports are referenced with a two- to four-character suffix to a PFU's location. As mentioned, there are two 5-bit input data buses (a[4:0] and b[4:0]) to the LUT, one 4-bit input data bus (wd[3:0]) to the latches/FFs, and an output data bus (o[4:0]).



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Figure 2. PFU Ports

The PFU is used in a variety of modes, as illustrated in Figures 4 through 11, and it is these specific modes that are most relevant to PFU functionality.

The PFU does combinatorial logic in the LUT and sequential logic in the latches/FFs. The LUT is static random access memory (SRAM) and can be used for read/write or read-only memory. Table 2 lists the basic operating modes of the LUT. The operating mode affects the functionality of the PFU input and output ports and internal PFU routing.

Programmable Logic Cells (continued)

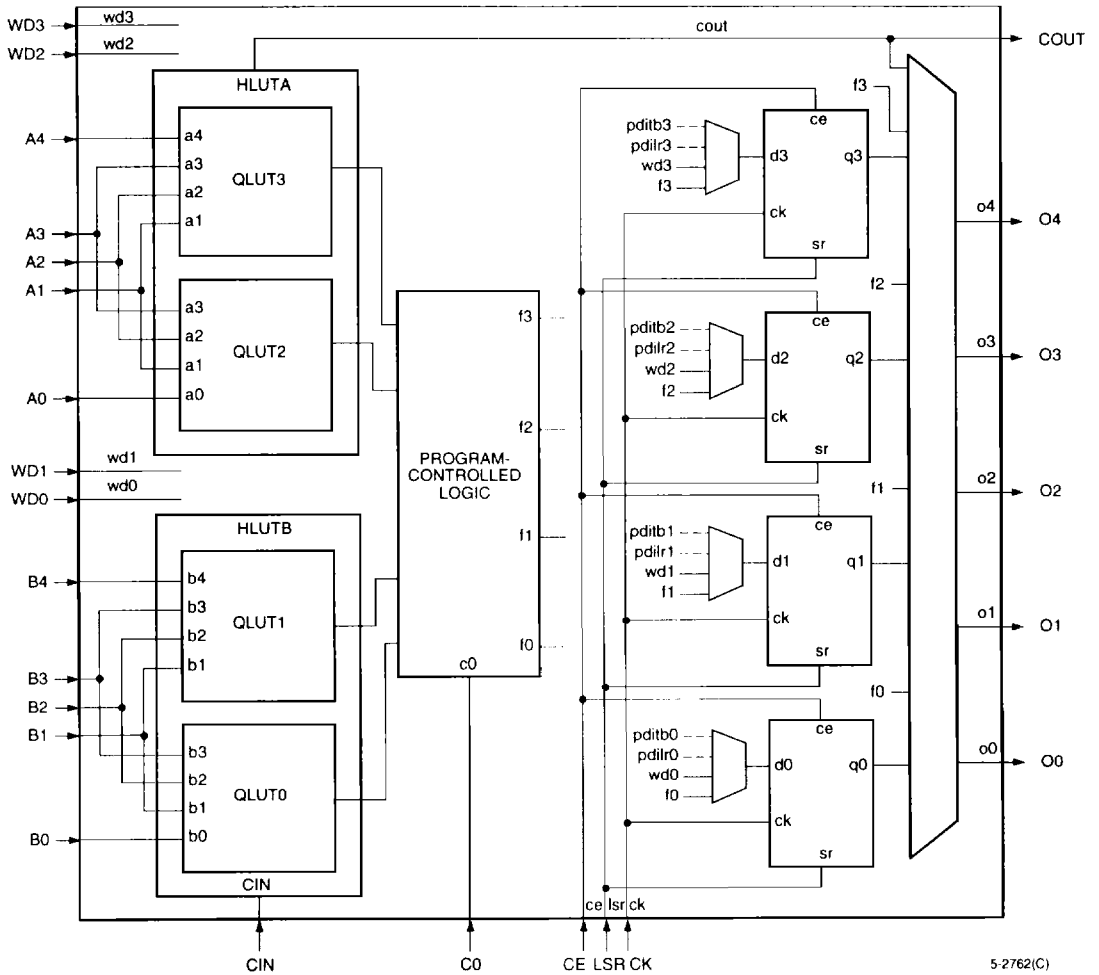


Figure 3. Simplified PFU Diagram

For example, in some operating modes, the wd[3:0] inputs are direct data inputs to the PFU latches/FFs. In the dual 16 x 2 memory mode, the same wd[3:0] inputs are used as a 4-bit data input bus into LUT memory.

Figure 3 shows the four latches/FFs and the 64-bit look-up table (LUT) in the PFU. Each latch/FF can accept data from the LUT. Alternately, the latches/FFs can accept direct data from wd[3:0], eliminating the LUT delay if no combinatorial function is needed.

The LUT outputs can bypass the latches/FFs, which reduces the delay out of the PFU. The pdilr[3:0] and pditb[3:0] inputs allow fast input from an I/O pad to the latches/FFs in the two closest PLCs perpendicular to the PIC containing the I/O pad. It is possible to use the LUT and latches/FFs more or less independently. For example, the latches/FFs can be used as a 4-bit shift register, and the LUT can be used to detect when a register has a particular pattern in it.

Programmable Logic Cells (continued)

PFU Control Inputs

The four control inputs to the PFU are clock (ck), local set/reset (l_{sr}), clock enable (ce), and c0. The ck, ce, and l_{sr} inputs control the operation of all four latches in the PFU. An active-low global set/reset (gsrn) signal is also available to the latches/FFs in every PFU. Their operation is discussed briefly here, and in more detail in the Latches/Flip-Flops section. The polarity of the control inputs can be inverted.

The ck input is distributed to each PFU from a vertical or horizontal net. The ce input inhibits the latches/FFs from responding to data inputs. The ce input can be disabled, always enabling the clock. Each latch/FF can be independently programmed to be a set or reset by the l_{sr} and the global set/reset (gsrn) signals. Each PFU's l_{sr} input can be configured as synchronous or asynchronous. The gsrn signal is always asynchronous. The l_{sr} signal applies to all four latches/FFs in a PFU. The l_{sr} input can be disabled (the default). The asynchronous set/reset is dominant over clocked inputs.

The c0 input is used as an input in combinatorial logic functions and as a carry input. It is used as an input into special PFU logic gates in wide input functions. The c0 input can be disabled (the default).

Look-Up Table Operating Modes

The LUT can be configured to operate in one of three general modes:

- Combinatorial logic mode
- Ripple mode
- Memory mode

The combinatorial logic mode uses a 64-bit look-up table (LUT) to implement Boolean functions. The two 5-bit logic inputs, a[4:0] and b[4:0], and the c0 input are used as LUT inputs. The use of these ports changes based on the PFU operating mode.

Table 2. Look-Up Table Operating Modes

| Mode | Function |
|------|--|
| F4A | Two functions of four inputs, some inputs shared (QLUT2/QLUT3) |
| F4B | Two functions of four inputs, some inputs shared (QLUT0/QLUT1) |
| F5A | One function of five inputs (HLUTA) |
| F5B | One function of five inputs (HLUTB) |
| MA | 16 x 2 memory (HLUTA) |
| MB | 16 x 2 memory (HLUTB) |
| R | Ripple—LUT |

For combinatorial logic, the LUT can be used to do any single function of six inputs, any two functions of five inputs, or four functions of four inputs (with some inputs shared), and three special functions based on the two five-input functions and c0.

The functionality of the LUT is determined by its operating mode. The entries in Table 2 show the basic modes of operation for combinatorial logic, ripple, and memory functions in the LUT. Depending on the operating mode, the LUT can be divided into sub-LUTs. The LUT is comprised of two 32-bit half look-up tables, HLUTA and HLUTB. Each half look-up table (HLUT) is comprised of two quarter look-up tables (QLUTs). HLUTA consists of QLUT2 and QLUT3, while HLUTB consists of QLUT0 and QLUT1. The outputs of QLUT0, QLUT1, QLUT2, and QLUT3 are f0, f1, f2, and f3, respectively.

If the LUT is configured to operate in the ripple mode, it cannot be used for basic combinatorial logic or memory functions. In modes other than the ripple mode, combinations of operating modes are possible. For example, the LUT can be configured as a 16 x 2 RAM in one HLUT and a five-input combinatorial logic function in the second HLUT. This can be done by configuring HLUTA in the MA mode and HLUTB in the F5B mode (or vice versa).

F4A/F4B Mode — Two Four-Input Functions

Each HLUT can be used to implement two four-input combinatorial functions, but the total number of inputs into each HLUT cannot exceed five. The two QLUTs within each HLUT share three inputs. In HLUTA, the a1, a2, and a3 inputs are shared by QLUT2 and QLUT3. Similarly, in HLUTB, the b1, b2, and b3 inputs are shared by QLUT0 and QLUT1. The four outputs are f0, f1, f2, and f3. The use of the LUT for four functions of up to four inputs each is given in Figure 4.

Programmable Logic Cells (continued)

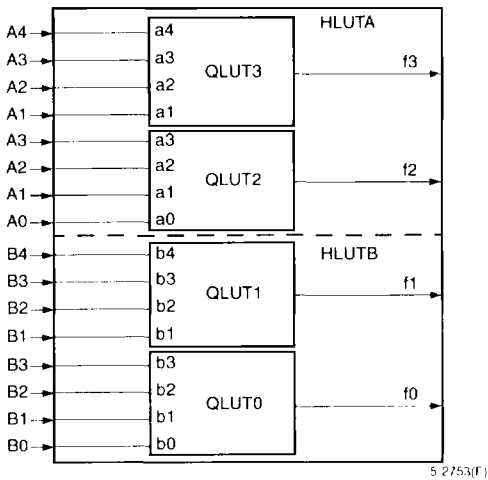


Figure 4. F4 Mode—Four Functions of Four Input Variables

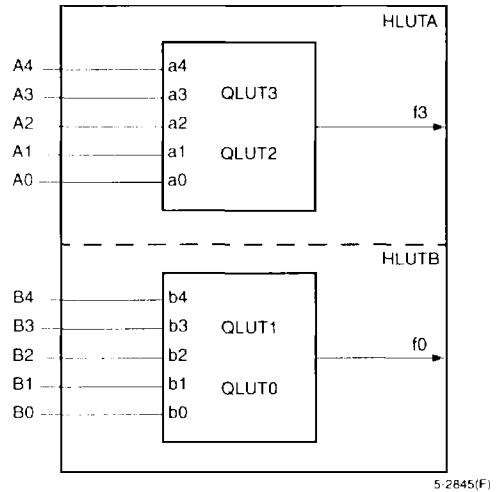


Figure 5. F5 Mode—Two Functions of Five Input Variables

F5A/F5B Mode—One Five-Input Variable Function

Each HLUT can be used to implement any five-input combinational function. The input ports are a[4:0] and b[4:0], and the output ports are f0 and f3. One five or less input function is input into a[4:0], and the second five or less input function is input into b[4:0]. The results are routed to the latch/FF d0 and latch/FF d3 inputs, or directly to the outputs o0 and o3. The use of the LUT for two independent functions of up to five inputs is given in Figure 5. In this case, the LUT is configured in the F5A and F5B modes. As a variation, the LUT can do one function of up to five input variables and two four-input functions using F5A and F4B modes or F4A and F5B modes.

F5M and F5X Modes — Special Function Modes

The PFU contains logic to implement two special function modes which are variations on the F5 mode. As with the F5 mode, the LUT implements two independent five-input functions. Figure 6 and Figure 7 show the schematics for F5M and F5X modes. The F5X and F5M functions differ from the basic F5A/F5B functions in that there are three logic gates which have inputs from the LUT. In some cases, this can be used for faster and/or wider logic functions. The HLUTs operate as in the F5 mode, providing outputs on f0 and f3. The resulting output is then input into a NAND and either a multiplexer in F5M mode or an exclusive OR in F5X mode.

As shown, two of the three inputs into the NAND, XOR, and MUX gates, f0 and f3, are from the LUT. The third input is from the c0 input into PFU. The output of the special function (either XOR or MUX) is f1. Since the XOR and multiplexer share the f1 output, the F5X and F5M modes are mutually exclusive. The output of the NAND is f2.

To use either the F5M or F5X functions, the LUT must be in the F5A/F5B mode. In both the F5X and F5M functions, the outputs of the five-input combinational functions, f0 and f3, are also usable simultaneously with the logic gate outputs.

The output of the multiplexer is:
 $f1 = (HLUTA \times c0) + (HLUTB \times \bar{c0})$

$f1 = (f3 \times c0) + (f0 \times \bar{c0})$

The output of the exclusive OR is:

$f1 = HLUTA \oplus HLUTB \oplus c0$

$f1 = f3 \oplus f0 \oplus c0$

The output of the NAND is:

$f2 = \overline{HLUTA \times HLUTB \times c0}$

$f2 = \overline{f3 \times f0 \times c0}$

Programmable Logic Cells (continued)

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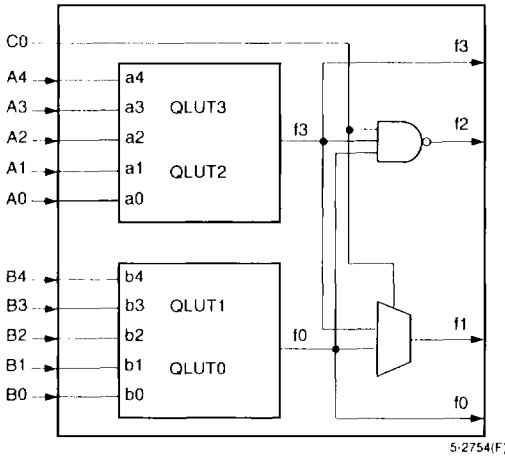


Figure 6. F5M Mode—Multiplexed Function of Two Independent Five-Input Variable Functions

F5M Mode — One Six-Input Variable Function

The LUT can be used to implement any function of six input variables. As shown in Figure 8, five input signals are routed into both the a[4:0] and b[4:0] ports, and the c0 port is used for the sixth input. The output port is f1.

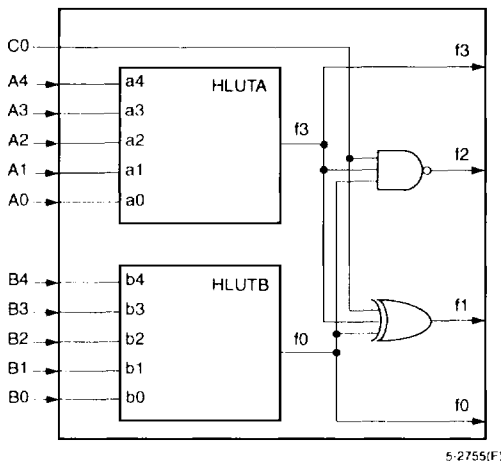


Figure 7. F5X Mode—Exclusive OR Function of Two Independent Five-Input Variable Functions

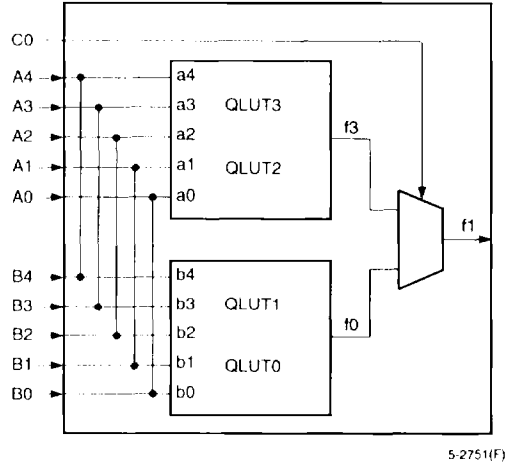


Figure 8. F5M Mode—One Six-Input Variable Function

Ripple Mode

The LUT can do nibble-wide ripple functions with high-speed carry logic. The QLUTs each have a dedicated carry-out net to route the carry to/from the adjacent QLUT. Using the internal carry circuits, fast arithmetic and counter functions can be implemented in one PFU. Similarly, each PFU has carry-in and carry-out ports for fast carry routing between adjacent PFUs.

The ripple mode is generally used in operations on two 4-bit buses. Each QLUT has two operands and a ripple input, and provides a result and ripple (generally carry) output. A single bit is rippled from the previous QLUT and is used as input into the current QLUT. For QLUT0, the ripple input is from the PFU cin port. The cin data can come from either the fast carry routing or the PFU input b4, or it can be tied to logic 1 or logic 0.

The result output and ripple output are calculated by using generate/propagate circuitry. In ripple mode, the two operands are input into a[3:0] and b[3:0]. The four results bits, one per QLUT, are f[3:0] (see Figure 9). The ripple output from QLUT3 can be routed to dedicated carry-out circuitry into any of four adjacent PLCs, or it can be placed on the o4 PFU output, or both. This allows for cascading PLCs in the ripple mode so that nibble-wide ripple functions can be easily expanded to any length. If an up/down counter or adder/subtractor is needed, the control signal is input on a4.

Programmable Logic Cells (continued)

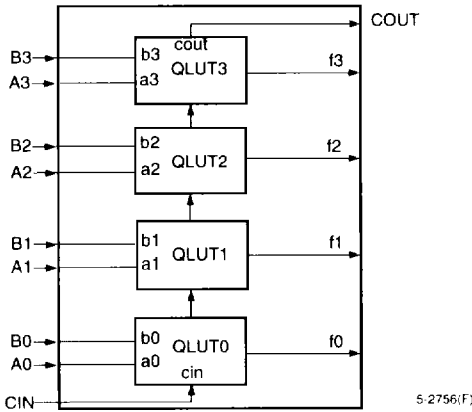


Figure 9. Ripple Mode

Each QLUT generates two separate outputs. One of the two outputs selects whether the carry-in is to be propagated to the carry-out of the current QLUT or if the carry-out needs to be generated. The resulting output is placed on the QLUT output. The result bit is created in one half of the QLUT from a single bit from each input bus along with the ripple input bit. These inputs are also used to create the programmable propagate.

Memory Modes — MA and MB Modes

The LUT in the PFU can be configured as either read/write or read-only memory. A read/write address (a[3:0],b[3:0]), write data (wd[1:0], wd[3:2]), and two write enable (wea, web) ports are used for memory. In memory mode, each HLUT can be used as a 16 x 2 memory. Each HLUT is configured independently, allowing functions such as 16 x 4 memory or a 16 x 2 memory in one HLUT and a logic function of five input variables or less in the other HLUT.

Figure 10 illustrates the use of the LUT for a 16 x 4 memory. When the LUTs are used as memory, there are independent address, input data, and output data buses. If the LUT is used as a 16 x 4 read/write memory, the a[3:0] and b[3:0] ports are address inputs. The a4 and b4 ports are write-enable (we) signals. The wd[3:0] inputs are the data inputs. The f[3:0] data outputs can be routed out on the o[4:0] PFU outputs or to the latch/FFs d[3:0] inputs.

To increase memory address locations (e.g., 32 x 4), two or more PLCs can be used. The address and write data inputs for the two PLCs are tied together (bit by bit) and the data outputs are routed through a 3-statable BIDI and then tied together (bit by bit).

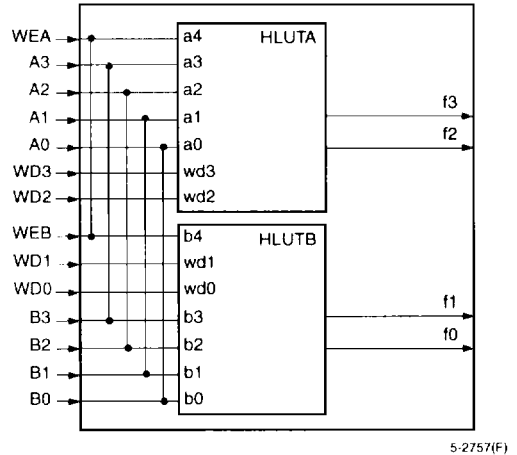


Figure 10. MA/MB Mode—16 x 4 RAM

The write enable and read enable for each PLC is created from an extended address. The read enable is connected to the 3-state enable input to the BIDs for a given PLC and then used to enable the 4 bits of data from a PLC onto the read data bus.

To increase the memory's word size (e.g., 16 x 8), two or more PLCs are used again. The address and write enable of the PLCs are tied together, and the data is different for each PLC. Increasing both the address locations and word size is done by using a combination of these two techniques.

The LUT can be used for both memory and a combinatorial logic function simultaneously. Figure 11 shows the use of a LUT implementing a 16 x 2 RAM (HLUTA) and any function of up to five input variables (HLUTB).

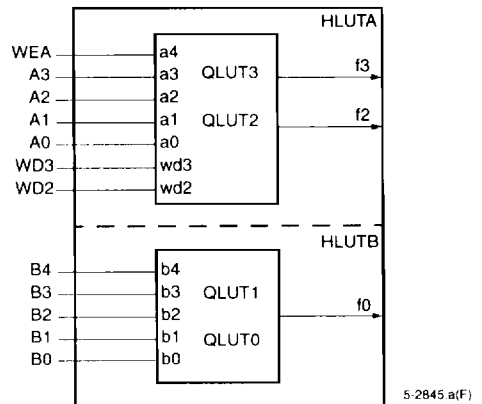


Figure 11. MA/F5 Mode—16 x 2 Memory and One Function of Five Input Variables

Programmable Logic Cells (continued)

Latches/Flip-Flops

The four latches/FFs in the PFU can be used in a variety of configurations. In some cases, the configuration options apply to all four latches/FFs in the PFU. For other options, each latch/FF is independently programmable.

Table 3 summarizes these latch/FF options. The latches/FFs can be configured as either positive or negative level sensitive latches, or positive or negative edge-triggered flip-flops. All latches/FFs in a given PFU share the same clock, and the clock to these latches/FFs can be inverted. The input into each latch/FF is from either the corresponding QLUT output ($f[3:0]$) or the direct data input ($wd[3:0]$). For latches/FFs located in the two outer rings of PLCs, additional inputs are possible. These additional inputs are fast paths from I/O pads located in PICs perpendicular to the PLCs. If the latch/FF is not located in the two outer rings of the PLCs, the latch/FF input can also be tied to logic 0, which is the default. The four latch/FF outputs, $q[3:0]$, can be placed on the five PFU outputs, $o[4:0]$.

Table 3. Configuration RAM Controlled Latch/Flip-Flop Operation

| Function | Options |
|---|---|
| Functionality Common to All Latch/FFs in PFU | |
| LSR Operation | Asynchronous or Synchronous |
| Clock Polarity | Noninverted or Inverted |
| Front-End Select | Direct ($wd[3:0]$) or from LUT ($f[3:0]$) |
| Functionality Set Individually in Each Latch/FF in PFU | |
| Latch/FF Mode | Latch or Flip-Flop |
| Set/Reset Mode | Set or Reset |

The four latches/FFs in a PFU share the clock (ck), clock enable (ce), and local set/reset (lsr) inputs. When ce is disabled, each latch/FF retains its previous value when clocked, unless there is an asynchronous set/reset. Both the clock enable and lsr inputs can be inverted to be active-low.

The set/reset operation of the latch/FF is controlled by two parameters: reset mode and set/reset value. When the global ($gsrn$) or local set/reset (lsr) are active, the storage element operates normally as a latch or FF. The reset mode is used to select a synchronous or asynchronous lsr operation. If synchronous, lsr is enabled if clock enable (ce) is active. The clock enable is supported on FFs, not latches. The clock enable function is implemented by using a two-input multiplexer on the FF input, with one input being the

previous state of the FF and the other input being the new data applied to the FF. The select of this two-input multiplexer is clock enable (ce), which selects either the new data or the previous state. When ce is inactive, the FF output does not change when the clock edge arrives.

The global reset ($gsrn$) is only asynchronous, and it sets/resets all latches/FFs in the FPGA based upon the set/reset configuration bit for each latch/FF. The set/reset value determines whether $gsrn$ and lsr are set or reset inputs. The set/reset value is independent for each latch/FF.

If the local set/reset is not needed, the latch/FF can be configured to have a data front-end select. Two data inputs are possible in the front-end select mode, with the lsr signal used to select which data input is used. The data input into each latch/FF is from the output of its associated QLUT $f[3:0]$ or direct from $wd[3:0]$, bypassing the LUT. In the front-end data select mode, both signals are available to the latches/FFs.

For PLCs that are in the two outside rows or columns of the array, the latch/FFs can have two inputs in addition to the f and wd inputs mentioned above. One input is from an I/O pad located at the PIC closest to either the left or right of the given PLC (if the PLC is in the left two columns or right two columns of the array). The other input is from an I/O pad located at the closest PIC either above or below the given PLC (if the PLC is in the top or the bottom two rows). It should be noted that both inputs are available for a 2 x 2 array of PLCs in each corner of the array. For the entire array of PLCs, if either or both of these inputs is unavailable, the latch/FF can be tied to a logic 0 instead.

To speed up the interface between signals external to the FPGA and the latches/FFs, there are direct paths from latch/FF outputs to the I/O pads. This is done for each PLC that is adjacent to a PIC. The latches/FFs can be configured in three modes:

1. Local synchronous set/reset: the input into the PFU's lsr port is used to synchronously set or reset each latch/FF.
2. Local asynchronous set/reset: the input into lsr asynchronously sets or resets each latch/FF.
3. Latch/FF with front-end select: the data select signal (actually lsr) selects the input into the latches/FFs between the LUT output and direct data in.

For all three modes, each latch/FF can be independently programmed as either set or reset. Each latch/FF in the PFU is independently configured to operate as either a latch or flip-flop. Figure 12 provides the logic functionality of the front-end select, global set/reset, and local set/reset operations.

2

Programmable Logic Cells (continued)

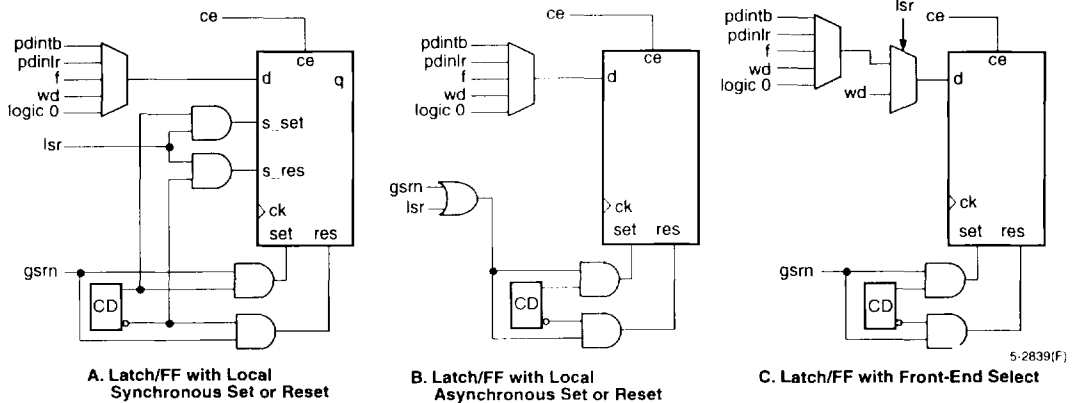


Figure 12. Latch/FF Set/Reset Configurations

PLC Routing Resources

Generally, the ORCA Foundry Development System is used to automatically route interconnections. Interactive routing with the ORCA Foundry design editor (EPIC) is also available for design optimization. To use EPIC for interactive layout, an understanding of the routing resources is needed and is provided in this section.

The routing resources consist of switching circuitry and metal interconnect segments. Generally, the metal lines which carry the signals are designated as routing nodes (R-nodes). The switching circuitry connects the routing nodes, providing one or more of three basic functions: signal switching, amplification, and isolation. A net running from a PFU or PIC output (source) to a PLC or PIC input (destination) consists of one or more R-nodes, connected by switching circuitry designated as configurable interconnect points (CIPs).

The following sections discuss PLC, PIC, and interquad routing resources. This section discusses the PLC switching circuitry, intra-PLC routing, inter-PLC routing, and clock distribution.

Configurable Interconnect Points

The process of connecting R-nodes uses three basic types of switching circuits: two types of configurable interconnect points (CIPs) and bidirectional buffers (BIDs). The basic element in CIPs is one or more pass transistors, each controlled by a configuration RAM bit. The two types of CIPs are the mutually exclusive (or multiplexed) CIP and the independent CIP.

A mutually exclusive set of CIPs contains two or more CIPs, only one of which can be on at a time. An independent CIP has no such restrictions and can be on independent of the state of other CIPs. Figure 13 shows an example of both types of CIPs.

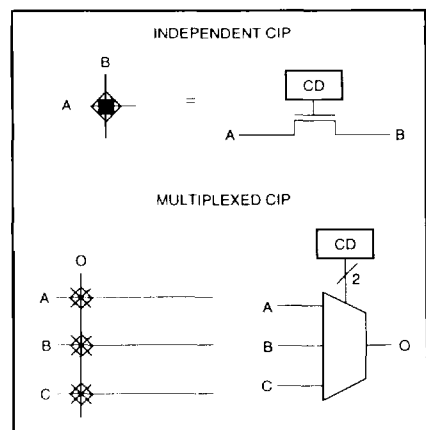


Figure 13. Configurable Interconnect Point

Programmable Logic Cells (continued)

3-Statable Bidirectional Buffers

Bidirectional buffers provide isolation as well as amplification for signals routed a long distance. Bidirectional buffers are also used to drive signals directly onto either vertical or horizontal xL and xH R-nodes (to be described later in the inter-PLC routing section). BIDIs are also used to indirectly route signals through the switching R-nodes. Any number from zero to eight BIDIs can be used in a given PLC.

The BIDIs in a PLC are divided into two nibble-wide sets of four (BIDI and BIDIH). Each of these sets has a separate BIDI controller that can have an application net connected to its TRI input, which is used to 3-state enable the BIDIs. Although only one application net can be connected to both BIDI controllers, the sense of this signal (active-high, active-low, or ignored) can be configured independently. Therefore, one set can be used for driving signals, the other set can be used to create 3-state buses, both sets can be used for 3-state buses, and so forth.

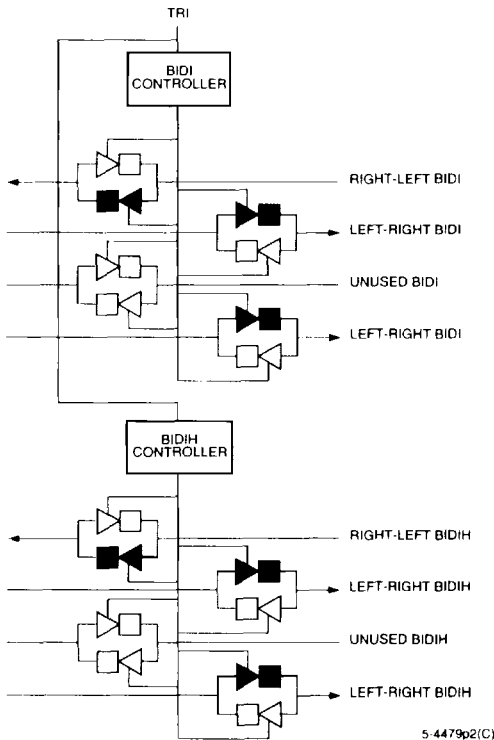


Figure 14. 3-Statable Bidirectional Buffers

Intra-PLC Routing

The function of the intra-PLC routing resources is to connect the PFU's input and output ports to the routing resources used for entry to and exit from the PLC. These are nets for providing PFU feedback, turning corners, or switching from one type of routing resource to another.

PFU Input and Output Ports. There are nineteen input ports to each PFU. The PFU input ports are labelled a[4:0], b[4:0], wd[3:0], c0, ck, lsr, cin, and ce. The six output ports are o[4:0] and cout. These ports correspond to those described in the PFU section.

Switching R-Nodes. There are four sets of switching R-nodes in each PLC, one in each corner. Each set consists of five switching elements, labelled sul[4:0], sur[4:0], sl[4:0], and slr[4:0], for the upper-left, upper-right, lower-left, and lower-right sections of the PFUs, respectively. The switching R-nodes connect to the PFU inputs and outputs as well as the BIDI and BIDIH R-nodes, to be described later. They also connect to both the horizontal and vertical x1 and x4 R-nodes (inter-PLC routing resources, described below) in their specific corner.

One of the four sets of switching R-nodes can be connected to a set of switching R-nodes in each of the four adjacent PLCs or PICs. This allows direct routing of up to five signals without using inter-PLC routing.

BIDI/BIDIH R-Nodes. There are two sets of bidirectional R-nodes in the PLC, each set consisting of four bidirectional buffers. They are designated BIDI and BIDIH and have similar functionality. The BIDI R-nodes are used in conjunction with the xL R-nodes, and the BIDIH R-nodes are used in conjunction with the xH R-nodes. Each side of the four BIDIs in the PLC is connected to a BIDI R-node on the left (BL[3:0]) and on the right (BR[3:0]). These R-nodes can be connected to the xL R-nodes through CIPs, with BL[3:0] connected to the vertical xL R-nodes and BR[3:0] connected to the horizontal xL R-nodes. Both BL[3:0] and BR[3:0] have CIPs which connect to the switching R-nodes.

Similarly, each side of the four BIDIHs is connected to a BIDIH R-node: BLH[3:0] on the left and BRH[3:0] on the right. These R-nodes can also be connected to the xH R-nodes through CIPs, with BLH[3:0] connected to the vertical xH R-nodes and BRH[3:0] connected to the horizontal xH R-nodes. Both BLH[3:0] and BRH[3:0] have CIPs which connect to the switching R-nodes.

CIPs are also provided to connect the BIDIH and BIDI R-nodes together on each side of the BIDIs. For example, BLH3 can connect to BL3, while BRH3 can connect to BR3.

2

Programmable Logic Cells (continued)

Inter-PLC Routing Resources

The inter-PLC routing is used to route signals between PLCs. The R-nodes occur in groups of four, and differ in the numbers of PLCs spanned. The x1 R-nodes span one PLC, the x4 R-nodes span four PLCs, the xH R-nodes span one-half the width (height) of the PLC array, and the xL R-nodes span the width (height) of the PLC array. All types of R-nodes run in both horizontal and vertical directions. Table 4 shows the groups of inter-PLC R-nodes in each PLC. In the table, there are two rows/columns each for x1 and x4 lines. In the design editor, the horizontal x1 and x4 R-nodes are located above and below the PFU. Similarly, the vertical segments are located on each side. The xL and xH R-nodes only run below and to the left of the PFU. The indexes specify individual R-nodes within a group. For example, the vx4[2] R-node runs vertically to the left of the PFU, spans four PLCs, and is the third line in the 4-bit wide bus.

Table 4. Inter-PLC Routing Resources

| Horizontal R-Nodes | Vertical R-Nodes | Distance Spanned |
|--------------------|------------------|------------------|
| hx1[3:0] | vx1[3:0] | One PLC |
| hx1[7:4] | vx1[7:4] | One PLC |
| hx4[3:0] | vx4[3:0] | Four PLCs |
| hx4[7:4] | vx4[7:4] | Four PLCs |
| hxL[3:0] | vxL[3:0] | PLC Array |
| hxH[3:0] | vxH[3:0] | 1/2 PLC Array |
| ckl, ckr | ckt, ckb | PLC Array |

Figure 15 shows the inter-PLC routing within one PLC. Figure 16 provides a global view of inter-PLC routing resources across multiple PLCs.

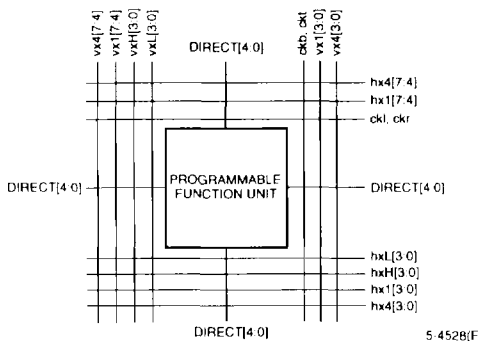


Figure 15. Single PLC View of Inter-PLC R-Nodes

x1 R-Nodes. There are a total of 16 x1 R-nodes per PLC: eight vertical and eight horizontal. Each of these is subdivided into nibble-wide buses: hx1[3:0], hx1[7:4], vx1[3:0], and vx1[7:4]. An x1 line is one PLC long. If a net is longer than one PLC, an x1 R-node can be lengthened to n times its length by turning on n - 1 CIPs. A signal is routed onto an x1 R-node via the switching R-nodes.

x4 R-Nodes. There are four sets of four x4 R-nodes, for a total of 16 x4 R-nodes per PLC. They are hx4[3:0], hx4[7:4], vx4[3:0], and vx4[7:4]. Each set of x4 R-nodes is twisted each time it passes through a PLC, and one of the four is broken with a CIP. This allows a signal to be routed for a length of four cells in any direction on a single line without additional CIPs. The x4 R-nodes can be used to route any nets that require minimum delay. A longer net is routed by connecting two x4 R-nodes together by a CIP. The x4 R-nodes are accessed via the switching R-nodes.

xL R-Nodes. The long xL R-nodes run vertically and horizontally the height and width of the array, respectively. There are a total of eight xL R-nodes per PLC: four horizontal (hxL[3:0]) and four vertical (vxL[3:0]). Each PLC column has four xL lines, and each PLC row has four xL R-nodes. Each of the xL R-nodes connects to the two PICs at either end. The ATT2C12, which consists of a 18 x 18 array of PLCs, contains 72 vxL and 72 hxL R-nodes. They are intended primarily for global signals which must travel long distances and require minimum delay and/or skew, such as clocks.

There are three methods for routing signals onto the xL R-nodes. In each PLC, there are two long line drivers: one for a horizontal xL R-node, and one for a vertical xL R-node. Using the long line drivers produces the least delay. The xL R-nodes can also be driven directly by PFU outputs using the BIDI R-nodes. In the third method, the xL R-nodes are accessed by the bidirectional buffers, again using the BIDI R-nodes.

Programmable Logic Cells (continued)

xH R-nodes. Four by half (xH) R-nodes run horizontally and four xH R-nodes run vertically in each row and column in the array. These R-nodes travel a distance of one-half the PLC array before being broken in the middle of the array, where they connect to the interquad block (discussed later). They also connect at the periphery of the FPGA to the PICs, like the xL R-nodes. The xH R-nodes do not twist like xL R-nodes, allowing nibble-wide buses to be routed easily.

Two of the three methods of routing signals onto the xL R-nodes can also be used for the xH R-nodes. A special xH line driver is not supplied for the xH R-nodes.

Clock R-Nodes. For a very fast and low-skew clock (or other global signal tree), clock R-nodes run the entire height and width of the PLC array. There are two horizontal clock R-nodes per PLC row (CKL, CKR) and two vertical clock R-nodes per PLC column (CKT, CKB). The source for these clock R-nodes can be any of the four I/O buffers in the PIC. The horizontal clock R-nodes in a row (CKL and CKR) are driven by the left and right PICs, respectively. The vertical clock R-nodes in a column (CKT, CKB) are driven by the top and bottom PICs, respectively.

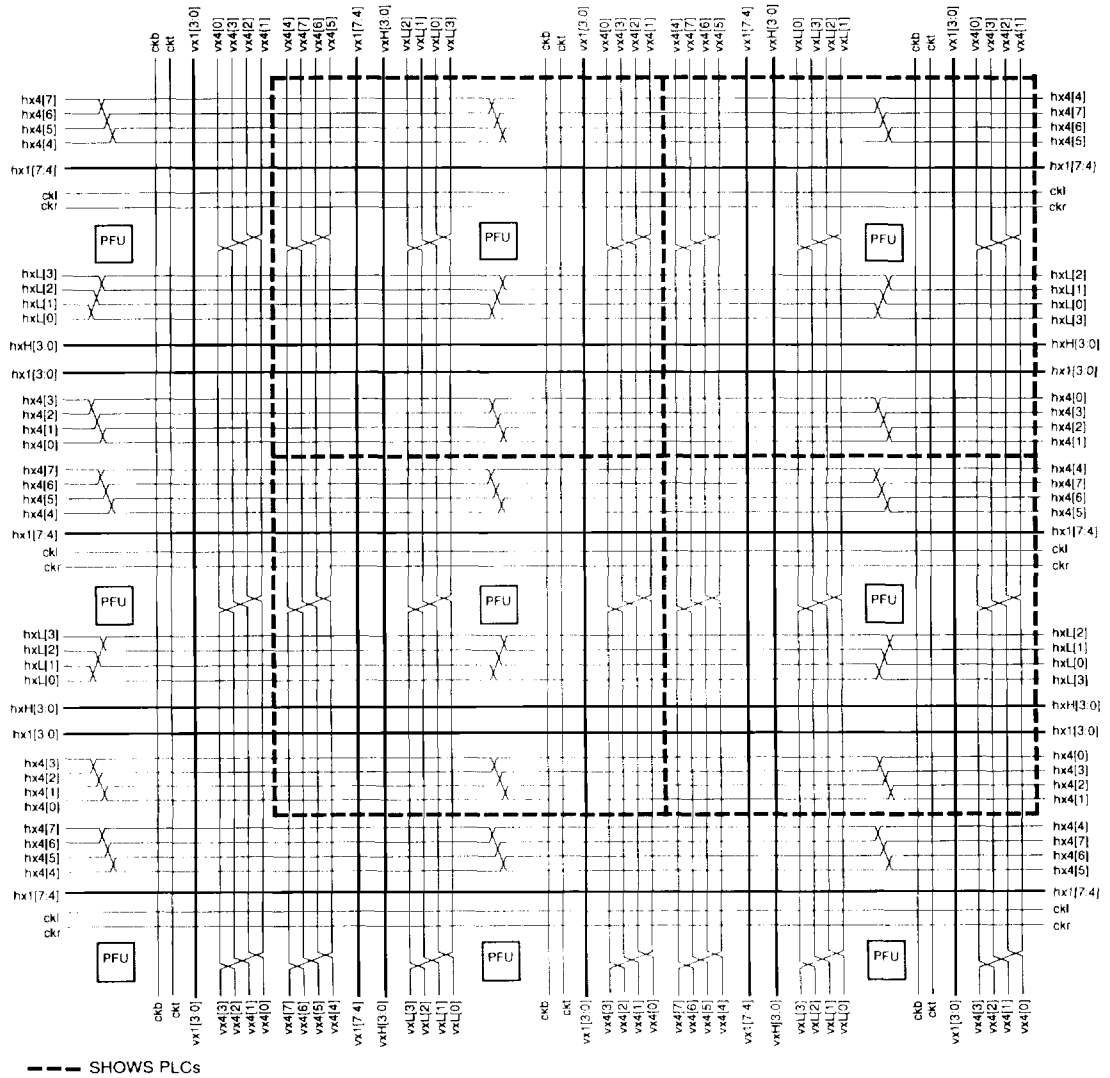
The clock R-nodes are designed to be a clock spine. In each PLC, there is a fast connection available from the clock R-node to the long-line driver (described earlier). With this connection, one of the clock R-nodes in each PLC can be used to drive one of the four xL R-nodes perpendicular to it, which, in turn, creates a clock tree. This feature is discussed in detail in the clock distribution section.

Minimizing Routing Delay

The CIP is an active element used to connect two R-nodes. As an active element, it adds significantly to the resistance and capacitance of a net, thus increasing the net's delay. The advantage of the x1 R-node over a x4 R-node is routing flexibility. A net from PLC db to PLC cb is easily routed by using x1 R-nodes. As more CIPs are added to a net, the delay increases. To increase speed, routes that are greater than two PLCs away are routed on the x4 R-nodes because a CIP is located only in every fourth PLC. A net which spans eight PLCs requires seven x1 R-nodes and six CIPs. Using x4 R-nodes, the same net uses two R-nodes and one CIP.

All routing resources in the PLC can carry 4-bit buses. In order for data to be used at a destination PLC that is in data path mode, the data must arrive unscrambled. For example, in data path operation, the least significant bit 0 must arrive at either a[0] or b[0]. If the bus is to be routed by using either x4 or xL R-nodes (both of which twist as they propagate), the bus must be placed on the appropriate lines at the source PLC so that the data arrives at the destination unscrambled. The switching R-nodes provide the most efficient means of connecting adjacent PLCs. Signals routed with these R-nodes have minimum propagation delay.

Programmable Logic Cells (continued)



5.2841(C)2C

Figure 16. Multiple PLC View of Inter-PLC Routing

Programmable Logic Cells (continued)

PLC Architectural Description

Figure 17 is an architectural drawing of the PLC which reflects the PFU, the R-nodes, and the CIPs. A discussion of each of the letters in the drawing follows.

A. These are switching R-nodes which give the router flexibility. In general switching theory, the more levels of indirection there are in the routing, the more routable the network is. The switching R-nodes can also connect to adjacent PLCs.

The switching R-nodes provide direct connections to PLCs directly to the top, bottom, left, and right, without using other routing resources. The ability to disable this connection between PLCs is provided so that each side of these connections can be used exclusively as switching R-nodes in their respective PLC.

B. These CIPs connect the x1 routing. These are located in the middle of the PLC to allow the block to connect to either the left end of the horizontal x1 R-node from the right or the right end of the horizontal x1 R-node from the left, or both. By symmetry, the same principle is used in the vertical direction. The x1 lines are not twisted, making them suitable for data paths.

C. This set of CIPs is used to connect the x1 and x4 nets to the switching R-nodes or to other x1 and x4 nets. The CIPs on the major diagonal allow data to be transmitted from x1 nets to the switching R-nodes without being scrambled. The CIPs on the major diagonal also allow unscrambled data to be passed between the x1 and x4 nets.

In addition to the major diagonal CIPs for the x1 lines, other CIPs provide an alternative entry path into the PLC in case the first one is already used. The other CIPs are arrayed in two patterns, as shown. Both of these patterns start with the main diagonal, but the extra CIPs are arrayed on either a parallel diagonal shifted by one or shifted by two (modulo the size of the vertical bus (5)). This allows any four application nets incident to the PLC corner to be transferred to the five switching R-nodes in that corner. Many patterns of five nets can also be transferred.

D. The x4 R-nodes are twisted at each PLC. One of the four x4 lines is broken with a CIP, which allows a signal to be routed a distance of four PLCs in any direction on a single R-node without an intermediate CIP. The x4 R-nodes are less populated with CIPs than the x1 lines to increase their speed. A CIP can be enabled to extend an x4 R-node four more PLCs, and so on.

For example, if an application signal is routed onto hx4[4] in a PLC, it appears on hx4[5] in the PLC to the right. This signal step-up continues until it reaches hx4[7], two PLCs later. At this point, the user can break the connection or continue the signal for another four PLCs.

E. These symbols are bidirectional buffers (BIDIs). There are four BIDIs per PLC, and they provide signal amplification as needed to decrease signal delay. The BIDIs are also used to transmit signals on xL lines.

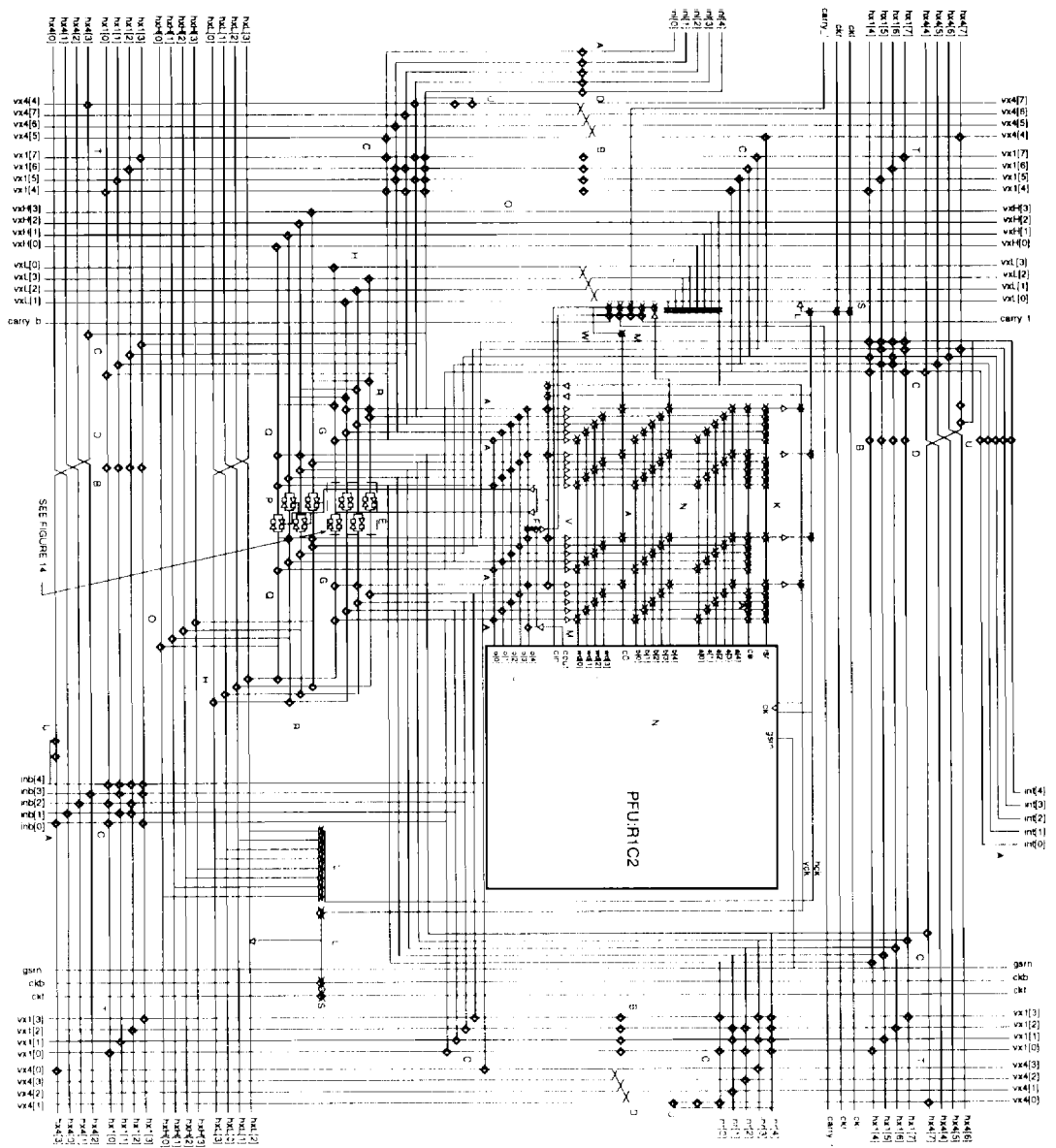
F. These are the BIDI and BIDIH controllers. The 3-state control signal can be disabled. They can be configured as active-high or active-low independently of each other.

G. This set of CIPs allows a BIDI to get or put a signal from one set of switching R-nodes on each side. The BIDIs can be accessed by the switching R-nodes. These CIPs allow a nibble of data to be routed through the BIDIs and continue to a subsequent block. They also provide an alternative routing resource to improve routability.

H. These CIPs are used to take data from/to the BIDIs to/from the xL R-nodes. These CIPs have been optimized to allow the BIDI buffers to drive the large load usually seen when using xL R-nodes.

I. Each latch/FF can accept data: from a LUT output; from a direct data input signal from general routing; or, as in the case of PLCs located in the two rows (columns) adjacent to PICs, directly from the pad. In addition, the LUT outputs can bypass the latches/FFs completely and output data on the general routing resources. The four inputs shown are used as the direct input to the latches/FFs from general routing resources. If the LUT is in memory mode, the four inputs wd[3:0] are the data input to the memory.

Programmable Logic Cells (continued)



5-4479(C)

Figure 17. PLC Architecture

Programmable Logic Cells (continued)

J. Any five of the eight output signals can be routed out of the PLC. The eight signals are the four LUT outputs (f0, f1, f2, and f3) and the four latch/FF outputs (q0, q1, q2, and q3). This allows the user to access all four latch/FF outputs, read the present state and next state of a latch/FF, build a 4-bit shift register, etc. Each of the outputs can drive any number of the five PFU outputs. The speed of a signal can be increased by dividing its load among multiple PFU output drivers.

K. These lines deliver the auxiliary signals clock enable and set/reset to the latches/FFs. All four of the latches/FFs share these signals.

L. This is the clock input to the latches/FFs. Any of the horizontal and vertical xH or xL lines can drive the clock of the PLC latches/FFs. Long line drivers are provided so that a PLC can drive one xL R-node in the horizontal direction and one xL R-node in the vertical direction. The xL lines in each direction exhibit the same properties as x4 lines, except there are no CIPs. The clock R-nodes (ckl, ckr, ckt, and ckb) and multiplexers/drivers are used to connect to the xL R-nodes for low-skew, low-delay global signals.

The long lines run the length or width of the PLC array. They rotate to allow four PLCs in one row or column to generate four independent global signals. These lines do not have to be used for clock routing. Any highly used application net can use this resource, especially one requiring low skew.

M. These R-nodes are used to route the fast carry signal to/from the neighboring four PLCs. The carry-out (cout) of the PFU can also be routed out of the PFU onto the fifth output (o4). The carry-in (cin) signal can also be supplied by the b4 input to the PFU.

N. These are the 11 logic inputs to the LUT. The a[4:0] inputs are provided into HLUTA, and the b[4:0] inputs are provided into HLUTB. The c0 input bypasses the main LUT and is used in the pfumux, pfuxor, and pfunand functions (F5M, F5X modes). Since this input bypasses the LUT, it can be used as a fast path around the LUT, allowing the implementation of fast, wide combinatorial functions. The c0 input can be disabled or inverted.

O. The xH R-nodes run one-half the length (width) of the array before being broken by a CIP.

P. The BIDIHs are used to access the xH R-nodes.

Q. The BIDIH R-nodes are used to connect the BIDIHs to the xsw R-nodes, the xH R-nodes, or the BIDI R-nodes.

R. These CIPs connect the BIDI R-nodes and the BIDIH R-nodes.

S. These are clock R-nodes (ckt, ckb, ckl, and ckr) with the multiplexers and drivers to connect to the xL R-nodes.

T. These CIPs connect x1 R-nodes which cross in each corner to allow turns on the x1 R-nodes without using the xsw R-nodes.

U. These CIPs connect x4 R-nodes and xsw R-nodes, allowing nets that run a distance that is not divisible by four to be routed more efficiently.

V. This routing structure allows any PFU output, including LUT and latch/FF outputs, to be placed on o4 and be routed onto the fast carry routing.

W. This routing structure allows the fast carry routing to be routed onto the c0 PFU input.

Programmable Input/Output Cells

The programmable input/output cells (PICs) are located along the perimeter of the device. Each PIC interfaces to four bond pads and contains the necessary routing resources to provide an interface between I/O pads and the PLCs. Each PIC is composed of input buffers, output buffers, and routing resources as described below. Table 5 provides an overview of the programmable functions in an I/O cell. Figure 18 is a simplified diagram of the functionality of the ORCA series I/O cells.

Table 5. Input/Output Cell Options

| Input | Option |
|-----------------|-------------------------------|
| Input Levels | TTL/CMOS |
| Input Speed | Fast/Delayed |
| Float Value | Pull-up/Pull-down/None |
| Direct-in to FF | Fast/Delayed |
| Output | Option |
| Output Drive | 12 mA/6 mA or 6 mA/3 mA |
| Output Speed | Fast/Slewlim/Sinklim |
| Output Source | FF Direct-out/General Routing |
| Output Sense | Active-high/-low |
| 3-State Sense | Active-high/-low (3-state) |

Inputs

Each I/O can be configured to be either an input, an output, or bidirectional I/O. Inputs can be configured as either TTL or CMOS compatible. To allow zero hold time on PLC latches/FFs, the input signal can be delayed. Pull-up or pull-down resistors are available on inputs to minimize power consumption.

A fast path from the input buffer to the clock R-nodes is also provided. Any one of the four I/O pads on any PIC can be used to drive the clock R-node generated in that PIC.

To reduce the time required to input a signal into the FPGA, a dedicated path (pdin) from the I/O pads to the PFU flip-flops is provided. Like general input signals, this signal can be configured as normal or delayed. The delayed direct input can be selected independently from the delayed general input. If the fast clock routing is selected from a given I/O pad, then the direct input signal is automatically delayed, decreasing the delay of the fast clock.

Inputs should have transition times of less than 500 ns and should not be left floating. If an input can float, a pull-up or pull-down should be enabled. Floating inputs increase power consumption, produce oscillations, and increase system noise. The inputs have a typical hysteresis of approximately 280 mV to reduce sensitivity to input noise. The PIC contains input circuitry which provides protection against latch-up and electrostatic discharge.

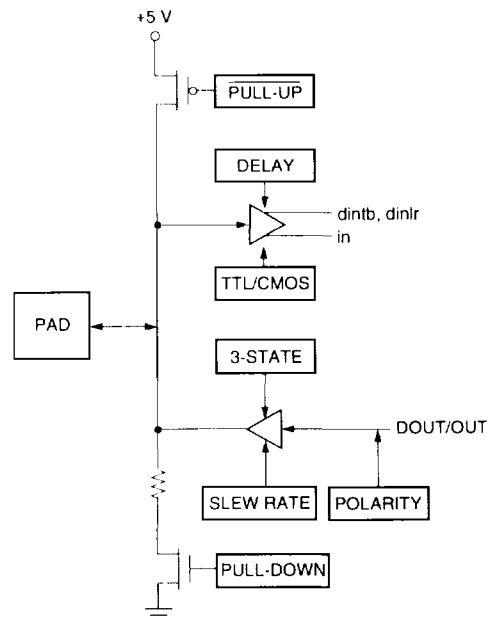


fig. 19(M)2C

Figure 18. Simplified Diagram of Programmable I/O Cell

Programmable Input/Output Cells

(continued)

Outputs

The PIC's output drivers have programmable drive capability and slew rates. Three propagation delays (fast, slewlim, sinklim) are available on output drivers. The sinklim mode has the longest propagation delay and is used to minimize system noise and minimize power consumption. The fast and slewlim modes allow critical timing to be met.

The drive current is 12 mA sink/6 mA source for the slewlim and fast output speed selections and 6 mA sink/3 mA source for the sinklim output. Two adjacent outputs can be interconnected to increase the output sink current to 24 mA.

All outputs that are not speed critical should be configured as sinklim to minimize power and noise. The number of outputs that switch simultaneously in the same direction should be limited to minimize ground bounce. To minimize ground bounce problems, locate heavily loaded output buffers near the ground pads. Ground bounce is generally a function of the driving circuits, traces on the PCB, and loads and is best determined with a circuit simulation.

Outputs can be inverted, and 3-state control signals can be active-high or active-low. An open-drain output may be obtained by using the same signal for driving the output and 3-state signal nets so that the buffer output is enabled only by a low. At powerup, the output drivers are in slewlim mode, and the input buffers are configured as TTL-level compatible with a pull-up. If an output is not to be driven in the selected configuration mode, it is 3-stated.

Global 3-State Functionality

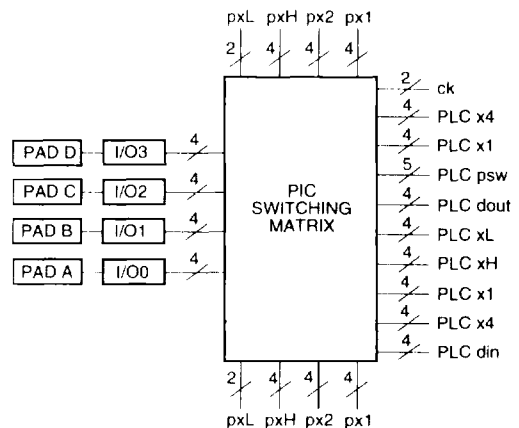
To increase the testability of the ORCA Series FPGAs, the global 3-state function (*ts_all*) disables the device. The *ts_all* signal is driven from either an external pin or an internal signal. Before and during configuration, the *ts_all* signal is driven by the input pad *RD_CFGN*. After configuration, the *ts_all* signal can be disabled, driven from the *RD_CFGN* input pad, or driven by a general routing signal in the upper-right corner. Before configuration, *ts_all* is active-low; after configuration, the sense of *ts_all* can be inverted. The following occur when *ts_all* is activated:

1. All of the user I/O output buffers are 3-stated, the user I/O input buffers are pulled up (with the pull-down disabled), and the input buffers are configured with TTL input thresholds.
2. The *TDO/RD_DATA* output buffer is 3-stated.
3. The *RD_CFGN*, *RESET*, and *PRGM* input buffers remain active with a pull-up.
4. The *DONE* output buffer is 3-stated and the input buffer is pulled-up.

PIC Routing Resources

The PIC routing is designed to route 4-bit wide buses efficiently. For example, any four consecutive I/O pads can have both their input and output signals routed into one PLC. Using only PIC routing, either the input or output data can be routed to/from a single PLC from/to any eight pads in a row.

The connections between PLCs and the I/O pad are provided by two basic types of routing resources. These are routing resources internal to the PIC and routing resources used for PIC-PLC connection. Figure 19 and Figure 20 show a high-level and detailed view of these routing resources.



5-4504(C)2C

Figure 19. Simplified PIC Routing Diagram

Programmable Input/Output Cells

(continued)

The PIC's name is represented by a two-letter designation to indicate on which side of the device it is located followed by a number to indicate in which row or column it is located. The first letter, P, designates that the cell is a PIC and not a PLC. The second letter indicates the side of the array where the PIC is located. The four sides are left (L), right (R), top (T), and bottom (B). The individual I/O pad is indicated by a single letter (either A, B, C, or D) placed at the end of the PIC name. As an example, PL10A indicates a pad located on the left side of the array in the tenth row.

Each PIC has four pads and each pad can be configured as an input, an output (3-statable), a direct output, or a bidirectional I/O. When the pads are used as inputs, the external signals are provided to the internal circuitry at in[3:0]. When the pads are used to provide direct inputs to the latches/FFs, they are connected through din[3:0]. When the pads are used as outputs, the internal signals connect to the pads through out[3:0]. When the pads are used as direct outputs, the output from the latches/flip-flops in the PLCs to the PIC is designated dout[3:0]. When the outputs are 3-statable, the 3-state enable signals are ts[3:0].

Routing Resources Internal to the PIC

For inter-PIC routing, the PIC contains fourteen R-nodes used to route signals around the perimeter of the FPGA. Figure 19 shows these lines running vertically for a PIC located on the left side. Figure 20 shows the R-nodes running horizontally for a PIC located at the top of the FPGA.

pxL R-Nodes. Each PIC has two pxL R-nodes, labelled pxL[1:0]. Like the xL R-nodes of the PLC, the pxL R-nodes span the entire edge of the FPGA.

pxH R-Nodes. Each PIC has four pxH R-nodes, labelled pxH[3:0]. Like the xH R-nodes of the PLC, the pxH R-nodes span 1/2 the edge of the FPGA.

px2 R-Nodes. There are four px2 R-nodes in each PIC, labelled px2[3:0]. The px2 R-nodes pass through two adjacent PICs before being broken. These are used to route nets around the perimeter a distance of two or more PICs.

px1 R-Nodes. Each PIC has four px1 R-nodes, labelled px1[3:0]. The px1 R-nodes are one PIC long and are extended to adjacent PICs by enabling CIPs.

Programmable Input/Output Cells

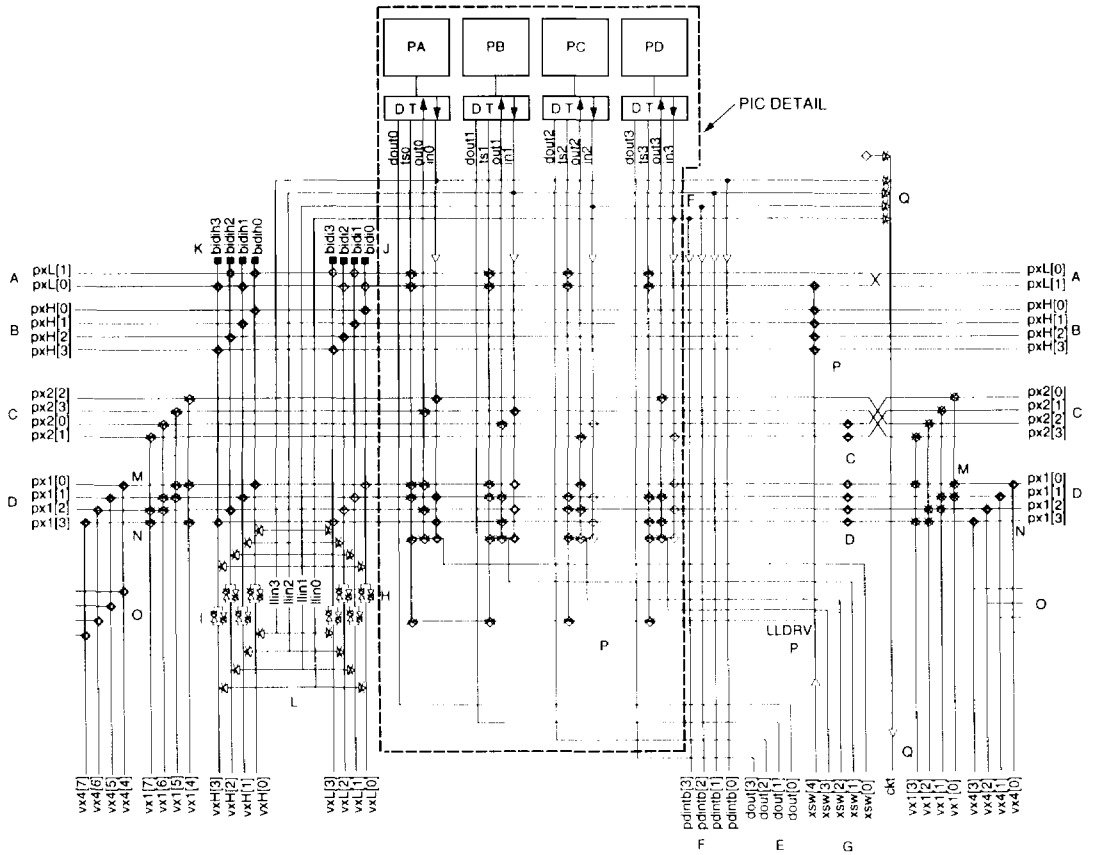
(continued)

PIC Architectural Description

The PIC architecture given in Figure 20 is described using the following letter references. The figure depicts a PIC at the top of the array, so inter-PIC routing is horizontal and the indirect PIC-PLC routing is horizontal to vertical. In some cases, letters are provided in more than one location to indicate the path of an R-node.

- 2**
- A.** As in the PLCs, the PIC contains a set of R-nodes which run the length (width) of the array. The pxL R-nodes connect in the corners of the array to other pxL R-nodes. The pxL R-nodes also connect to the PIC BIDI, PIC BIDIH, and LLDRV R-nodes. As in the PLC xL R-nodes, the pxH R-nodes twist as they propagate through the PICs.
 - B.** As in the PLCs, the PIC contains a set of R-nodes which run one-half the length (width) of the array. The pxH R-nodes connect in the corners and in the middle of the array perimeter to other pxH R-nodes. The pxH R-nodes also connect to the PIC BIDI, PIC BIDIH, and LLDRV R-nodes. As in the PLC xH R-nodes, the pxH R-nodes do not twist as they propagate through the PICs.
 - C.** The px2[3:0] R-nodes span a length of two PICs before intersecting with a CIP. The CIP allows the length of a path using px2 R-nodes to be extended two PICs.
 - D.** The px1[3:0] R-nodes span a single PIC before intersecting with a CIP. The CIP allows the length of a path using px1 R-nodes to be extended by one PIC.
 - E.** These are four dedicated direct output R-nodes connected to the output buffers. The dout[3:0] signals go directly from a PLC latch/FF to an output buffer, minimizing the latch/FF to pad propagation delay.
 - F.** This is a direct path from the input pad to the PLC latch/flip-flops in the two rows (columns) adjacent to PICs. This input allows a reduced setup time. Direct inputs from the top and bottom PIC rows are pdintb[3:0]. Direct inputs from the left and right PIC columns are pdinr[3:0].
 - G.** The out[3:0], ts[3:0], and in[3:0] signals for each I/O pad can be routed directly to the adjacent PLC's switching R-nodes.
 - H.** The four TRIDI buffers allow connections from the pads to the PLC xL R-nodes. The TRIDIs also allow connections between the PLC xL R-nodes and the pBIDI R-nodes, which are described in **J** below.
 - I.** The four TRIDIH buffers allow connections from the pads to the PLC xH R-nodes. The TRIDIHs also allow connections between the PLC xH R-nodes and the pBIDIH R-nodes, which are described in **K** below.
 - J.** The pBIDI R-nodes (bidi[3:0]) connect the pxL R-nodes, pxH R-nodes, and the px1 R-nodes. These are bidirectional in that the path can be from the pxL, pxH, or px1 R-nodes to the xL R-nodes, or from the xL R-nodes to the pxL, pxH, or px1 R-nodes.
 - K.** The pBIDIH R-nodes (bidih[3:0]) connect the pxL R-nodes, pxH R-nodes, and the px1 R-nodes. These are bidirectional in that the path can be from the pxL, pxH, or px1 R-nodes to the xH R-nodes, or from the xH R-nodes to the pxL, pxH, or px1 R-nodes.
 - L.** The llin[3:0] R-nodes provide a fast connection from the I/O pads to the xL and xH R-nodes.
 - M.** This set of CIPs allows the eight x1 R-nodes (four on each side) of the PLC perpendicular to the PIC to be connected to either the px1 or px2 R-nodes in the PIC.
 - N.** This set of CIPs allows the eight x4 R-nodes (four on each side) of the PLC perpendicular to the PIC to be connected to the px1 R-nodes. This allows fast access to/from the I/O pads from/to the PLCs.
 - O.** All four of the PLC x4 R-nodes in a group connect to all four of the PLC x4 R-nodes in the adjacent PLC through a CIP. (This differs from the Lucent ORCA 1C Series in which two of the x4 R-nodes in adjacent PLCs are directly connected without any CIPs.)
 - P.** The long line driver (LLDRV) R-node can be driven by the xsw4 switching R-node of the adjacent PLC. To provide connectivity to the pads, the LLDRV R-node can also connect to any of the four pxH or to one of the pxL R-nodes. The 3-state enable (ts[i]) for all four I/O pads can be driven by xsw4, pxH, or pxL R-nodes.
 - Q.** For fast clock routing, one of the four I/O pads in each PIC can be selected to be driven onto a dedicated clock R-node. The clock R-node spans the length (width) of the PLC array. This dedicated clock R-node is typically used as a clock spine. In the PLCs, the spine is connected to an xL R-node to provide a clock branch in the perpendicular direction. Since there is another clock R-node in the PIC on the opposite side of the array, only one of the I/O pads in a given row (column) can be used to generate a global signal in this manner, if all PLCs are driven by the signal.

Programmable Input/Output Cells (continued)



5-2843(C)2C

Figure 20. PIC Architecture

Programmable Input/Output Cells

(continued)

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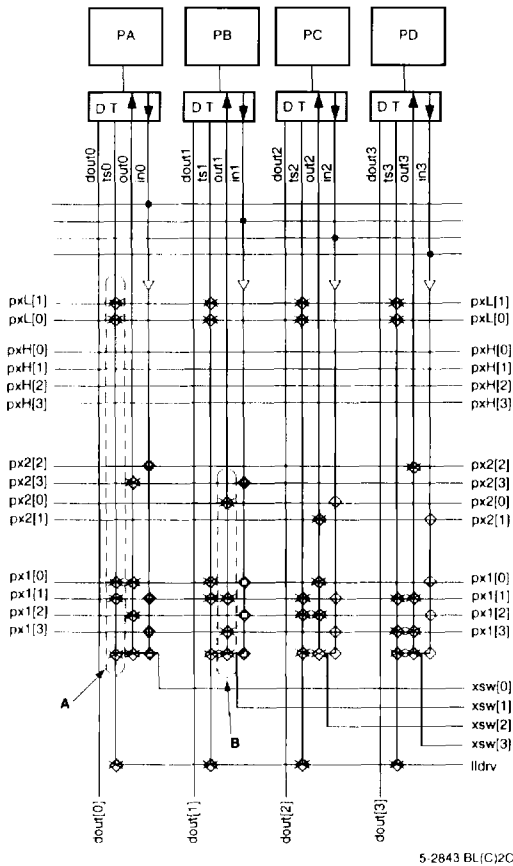


Figure 21. PIC Detail

PLC-PIC Routing Resources

There is no direct connection between the inter-PIC R-nodes and the PLC R-nodes. All connections to/from the PLC must be done through the connecting R-nodes which are perpendicular to the R-nodes in the PIC. The use of perpendicular and parallel R-nodes will be clearer if the PLC and PIC architectures (Figure 17 and Figure 20) are placed side by side. Twenty-nine R-nodes in the PLC can be connected to the fifteen R-nodes in the PIC.

Multiple connections between the PIC px1 R-nodes and the PLC x1 R-nodes are available. These allow buses placed in any arbitrary order on the I/O pads to be unscrambled when placed on the PLC x1 R-nodes. Connections are also available between the PIC px2 R-nodes and the PLC x1 R-nodes.

There are eight tridirectional (four TRIDI/four TRIDIH) buffers in each PIC; they can do the following:

- Drive a signal from an I/O pad onto one of the adjacent PLC's xL or xH R-nodes
- Drive a signal from an I/O pad onto one of the two pxL or four pxH R-nodes in the PIC
- Drive a signal from the PLC xL or xH R-nodes onto one of the two pxL or four pxH R-nodes in the PIC
- Drive a signal from the PIC pxL or pxH R-nodes onto one of the PLC xL or xH R-nodes

Figure 21 shows paths to and from pads and the use of MUX CIPs to connect R-nodes. Detail A shows six MUX CIPs for the pad P0 used to construct the net for the 3-state signal. In the MUX CIP, one of six R-nodes is connected to an R-node to form the net. In this case, the ts0 signal can be driven by either of the two pxLs, px1[0], px1[1], xsw[0], or the lldrv R-nodes. Detail B shows the four MUX CIPs used to drive the P1 output. The source R-node for out1 is either xsw[1], px1[1], px1[3], or px2[2].

Interquad Routing

In the ORCA 2C Series devices, the PLC array is split into four equal quadrants. In between these quadrants, routing has been added to route signals between the quadrants, especially to the quadrant in the opposite corner. The two types of interquad blocks, vertical and horizontal, are pitch matched to PICs. Vertical interquad blocks (vIQ) run between quadrants on the left and right, while horizontal interquad blocks (hIQ) run

between top and bottom quadrants. Since hIQ and vIQ blocks have the same logic, only the hIQ block is described below.

The interquad routing connects xL and xH R-nodes. It does not affect local routing (xsw, x1, x4, fast carry), so local routing is the same, whether PLC-PLC connections cross quadrants or not. There are no connections to the local R-nodes in the interquad blocks. Figure 22 presents a (not to scale) view of interquad routing.

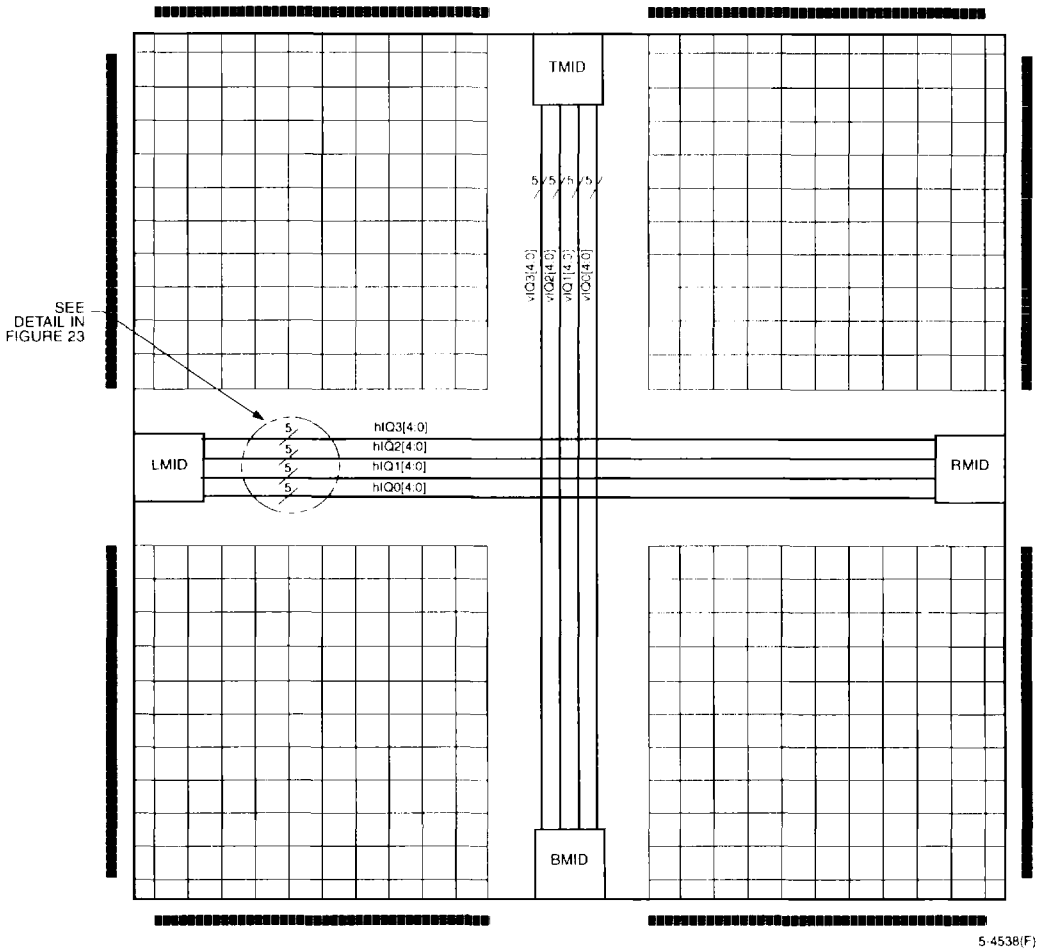


Figure 22. Interquad Routing

5-4538(F)

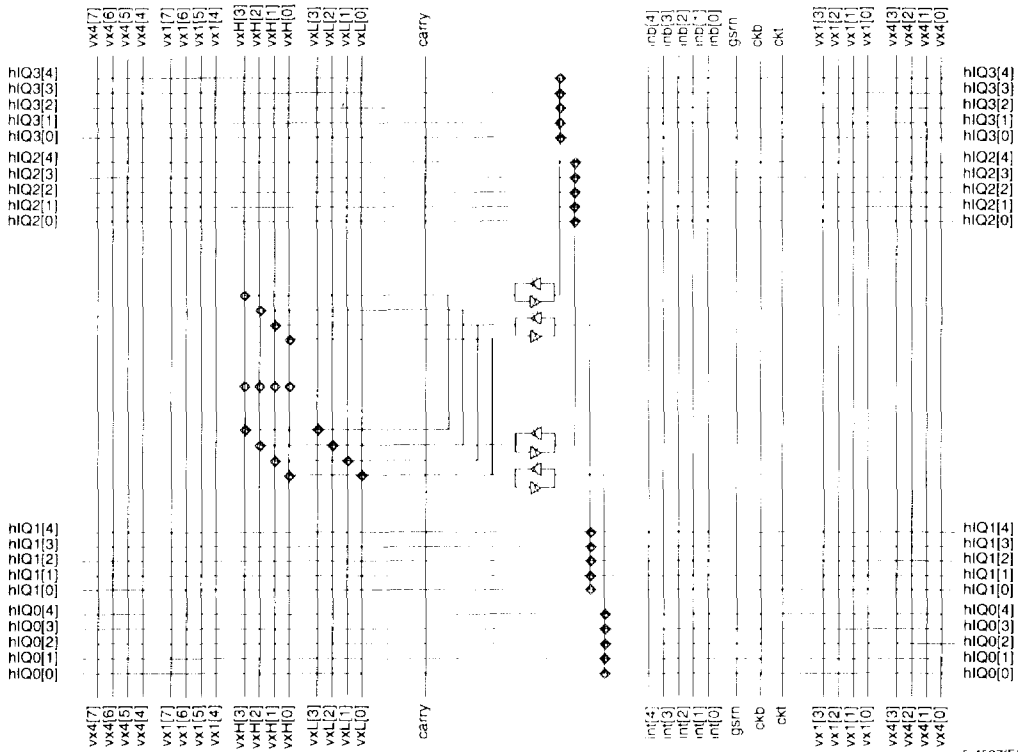
Interquad Routing (continued)

In the hIQ block in Figure 23, the xH R-nodes from one quadrant connect through a CIP to its counterpart in the opposite quadrant, creating a path that spans the PLC array. Since a passive CIP is used to connect the two xH R-nodes, a 3-state signal can be routed on the two xH R-nodes in the opposite quadrants, and then they can be connected through this CIP.

2

In the hIQ block, the 20 hIQ R-nodes span the array in a horizontal direction. The 20 hIQ R-nodes consist of four groups of five R-nodes each. To effectively route

nibble-wide buses, each of these sets of five R-nodes can connect to only one of the bits of the nibble for both the xH and xL. For example, hIQ0 R-nodes can only connect to the xH0 and xL0 R-nodes, and the hIQ1 R-nodes can connect only to the xH1 and xL1 R-nodes, etc. Buffers are provided for routing signals from the xH and xL R-nodes onto the hIQ R-nodes and from the hIQ R-nodes onto the xH and xL R-nodes. Therefore, a connection from one quadrant to another can be made using only two xH R-nodes (one in each quadrant) and one interquad R-node.



5 4537(F)

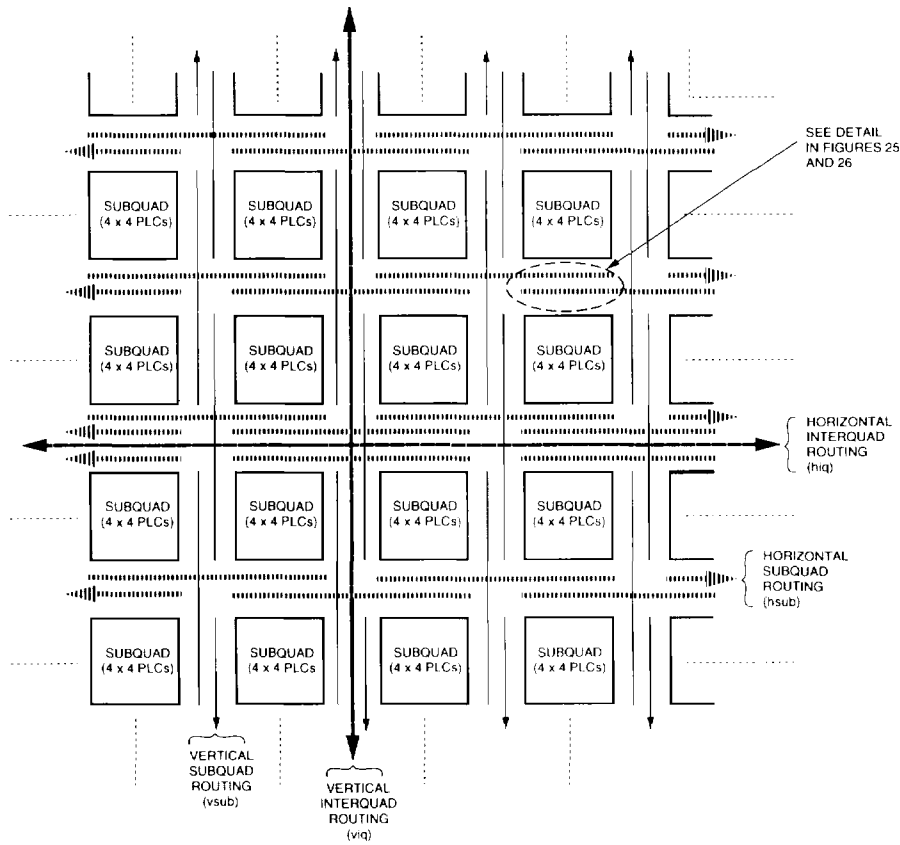
Figure 23. hIQ Block Detail

Interquad Routing (continued)

ATT2C40 Subquad Routing

In the ORCA ATT2C40, each quadrant of the device is split into smaller arrays of PLCs called subquads. Each of these subquads is made of a 4 x 4 array of PLCs (for a total of 16 per subquadrant), except at the outer edges of array, which have less than 16 PLCs per subquad. New routing resources, called subquad R-nodes, have been added between each adjacent pair of subquads to enhance the routability of the ATT2C40. A portion of the center of the ATT2C40 array is shown in Figure 24, including the subquad blocks containing a 4 x 4 array of PLCs, the interquad routing R-nodes, and the subquad routing R-nodes.

All of the inter-PLC routing resources discussed previously continue to be routed between a PLC and its adjacent PLC, even if the two adjacent PLCs are in different subquad blocks. Since the PLC routing has not been modified for the ATT2C40 architecture, this means that all of the same routing connections are possible for the ATT2C40 as for any other ORCA 2C Series device. In this way, the ATT2C40 is upwardly compatible when compared with the other 2C Series devices. As the inter-PLC routing runs between subquad blocks, it crosses the new subquad R-nodes. When this happens, CIPs are used to connect the subquad R-nodes to the x4 and/or the xH R-nodes which lie along the other axis of the PLC array.



5-4200(C)

Figure 24. Subquad Blocks and Subquad Routing

Interquad Routing (continued)

The x4 and xH R-nodes make the only connections to the subquad R-nodes; therefore, the array remains symmetrical and homogeneous. Since each subquad is made from a 4 x 4 array of PLCs, the distance between sets of subquad R-nodes is four PLCs, which is also the distance between the breaks of the x4 R-nodes. Therefore, each x4 R-node will cross exactly one set of subquad R-nodes. Since all x4 R-nodes make the same connections to the subquad R-nodes that they cross, all x4 R-nodes in the array have the same connectivity, and the symmetry of the routing is preserved. Since all xH R-nodes cross the same number of subquad blocks, the symmetry is maintained for the xH R-nodes as well.

The new subquad R-nodes travel a length of eight PLCs (seven PLCs on the outside edge) before they are broken. Unlike other inter-PLC R-nodes, they cannot be connected end-to-end. As shown in Figure 24, some of the horizontal (vertical) subquad R-nodes have connectivity to the subquad to the left of (above) the current subquad, while others have connectivity to the subquad to the right (below). This allows connections to/from the current subquad from/to the PLCs in all subquads that surround it.

Between all subquads, including in the center of the array, there are three groups of subquad R-nodes where each group contains four R-nodes. Figure 25 shows the connectivity of these three groups of subquad R-nodes (hsub) to the vx4 and vxH R-nodes running between a vertical pair of PLCs. Between each vertical pair of subquad blocks, four of the blocks shown in Figure 25 are used, one for each pair of vertical PLCs.

The first two groups, depicted as A and B, have connectivity to only one of the two sets of x4 R-nodes between pairs of PLCs. Since they are very lightly loaded, they are very fast. The third group, C, connects to both groups of x4 R-nodes between pairs of PLCs, as well as all of the xH R-nodes between pairs of PLCs, providing high flexibility. The connectivity for the vertical subquad routing (vsub) is the same as described above for the horizontal subquad routing, when rotated onto the other axis.

At the center row and column of each quadrant, a fourth group of subquad R-nodes has been added. These subquad R-nodes only have connectivity to the xH R-nodes. The xH R-nodes are also broken at this point, which means that each xH R-node travels one-half of the quadrant (i.e., one-quarter of the device) before it is broken by a CIP. Since the xH R-nodes can be connected end-to-end, the resulting line can be

either one-quarter, one-half, three-quarters, or the entire length of the array. The connectivity of the xH R-nodes and this fourth group of subquad R-nodes, indicated as D, are detailed in Figure 26. Again, the connectivity for the vertical subquad routing (vsub) is the same as the horizontal subquad routing, when rotated onto the other axis.

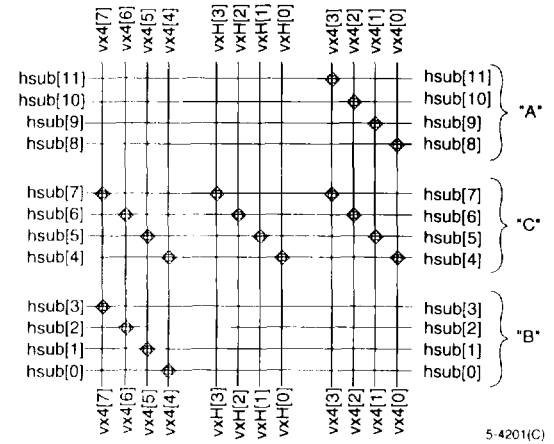


Figure 25. Horizontal Subquad Routing Connectivity

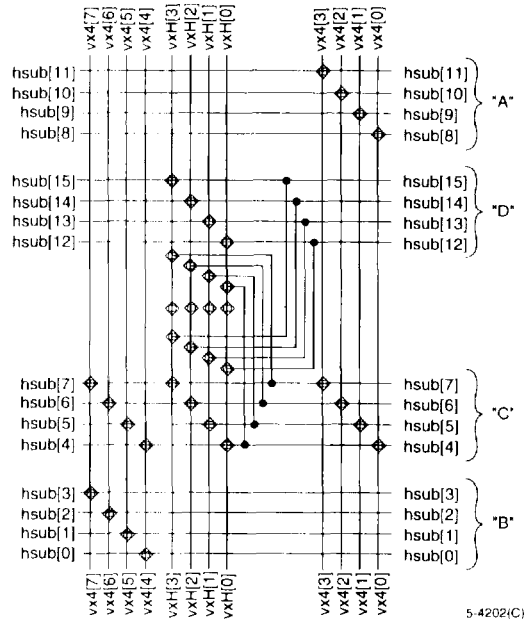


Figure 26. Horizontal Subquad Routing Connectivity (Half Quad)

Interquad Routing (continued)

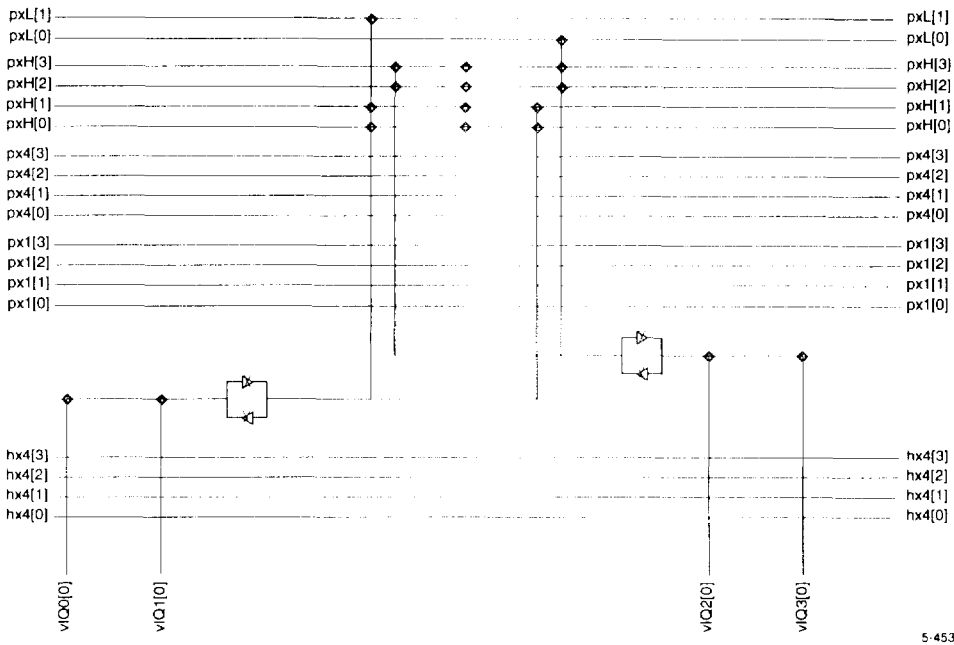


Figure 27. Top (TMID) Routing

PIC Interquad (MID) Routing

Between the PICs in each quadrant, there is also connectivity between the PIC routing and the interquad routing. These blocks are called LMID (left), TMID (top), RMID (right), and BMID (bottom). The TMID routing is shown in Figure 27. As with the hIQ and viQ blocks, the only connectivity to the PIC routing is to the global pxH and pxL R-nodes.

The pxH R-nodes from the one quadrant can be connected through a CIP to its counterpart in the opposite quadrant, providing a path that spans the array of PICs. Since a passive CIP is used to connect the two pxH R-nodes, a 3-state signal can be routed on the two pxH R-nodes in the opposite quadrants, and then connected through this CIP. As with the hIQ and viQ blocks, CIPs and buffers allow nibble-wide connections between the interquad R-nodes, the xH R-nodes, and the xL R-nodes.

Programmable Corner Cells

Programmable Routing

The programmable corner cell (PCC) contains the circuitry to connect the routing of the two PICs in each corner of the device. The PIC px1 and px2 R-nodes are directly connected together from one PIC to another. The PIC pxL R-nodes are connected from one block to another through tridirectional buffers. Four CIPs in each corner connect the four pxH R-nodes from each side of the device.

Special-Purpose Functions

In addition to routing functions, special-purpose functions are located in each FPGA corner. The upper-left PCC contains connections to the boundary-scan logic. The upper-right PCC contains connections to the read-back logic and the connectivity to the global 3-state signal (*ts_all*). The lower-left PCC contains connections to the internal oscillator.

The lower-right PCC contains connections to the start-up and global reset logic. During configuration, the *RESET* input pad always initiates a configuration abort, as described in the FPGA States of Operation section. After configuration, the global set/reset signal (*gsrn*) can either be disabled (the default), directly connected to the *RESET* input pad, or sourced by a lower-right corner signal. If the *RESET* input pad is not used as a global reset after configuration, this pad can be used as a normal input pad. During start-up, the release of the global set/reset, the release of the I/Os, and the release of the external *DONE* signal can each be timed individually based upon the start-up clock. The start-up clock can come from *CCLK* or it can be routed into the start-up block using the lower-right corner routing resources. More details on start-up can be found in the FPGA States of Operation section.

Clock Distribution Network

The *ORCA 2C* series clock distribution scheme uses primary and secondary clocks. This provides the system designer with additional flexibility in assigning clock input pins.

One advantage is that board-level clock traces routed to the FPGA are shorter. On a PC board, the added length of high-speed clock traces routed to dedicated clock input pins can significantly increase the parasitic impedances. The primary advantage of the *ORCA* clock distribution is the availability of a large number of clocks, since all I/O pins are configurable as clocks.

Primary Clock

The primary clock distribution is shown in Figure 28. If the clock signal is from an I/O pad, it can be driven onto a clock R-node. The clock R-nodes do not provide clock signals directly to the PFU; they act as clock spines from which clocks are branched to xL R-nodes. The xL R-nodes then feed the clocks to PFUs. A multiplexer in each PLC is used to transition from the clock spine to the branch.

For a clock spine in the horizontal direction, the inputs into the multiplexer are the two R-nodes from the left and right PICs (*ckl* and *ckr*) and the local clock R-node from the perpendicular direction (*hck*). This signal is then buffered and driven onto one of the vertical xL R-nodes, forming the branches. The same structure is used for a clock spine in the vertical direction. In this case, the multiplexer selects from R-nodes from the top and bottom PICs (*ckt*, *ckb*, and *vck*) and drives the signal onto one of the horizontal xL R-nodes.

Figure 28 illustrates the distribution of the low-skew primary clock to a large number of loads using a main spine and branches. Each row (column) has two dedicated clock R-nodes originating from PICs on opposite sides of the array. The clock is input from the pads to the dedicated clock R-node *ckt* to form the clock spine (see Figure 28, Detail A). From the clock spine, net branches are routed using horizontal xL lines. Clocks into PLCs are tapped from the xL R-nodes, as shown in Figure 28, Detail B.

Clock Distribution Network (continued)

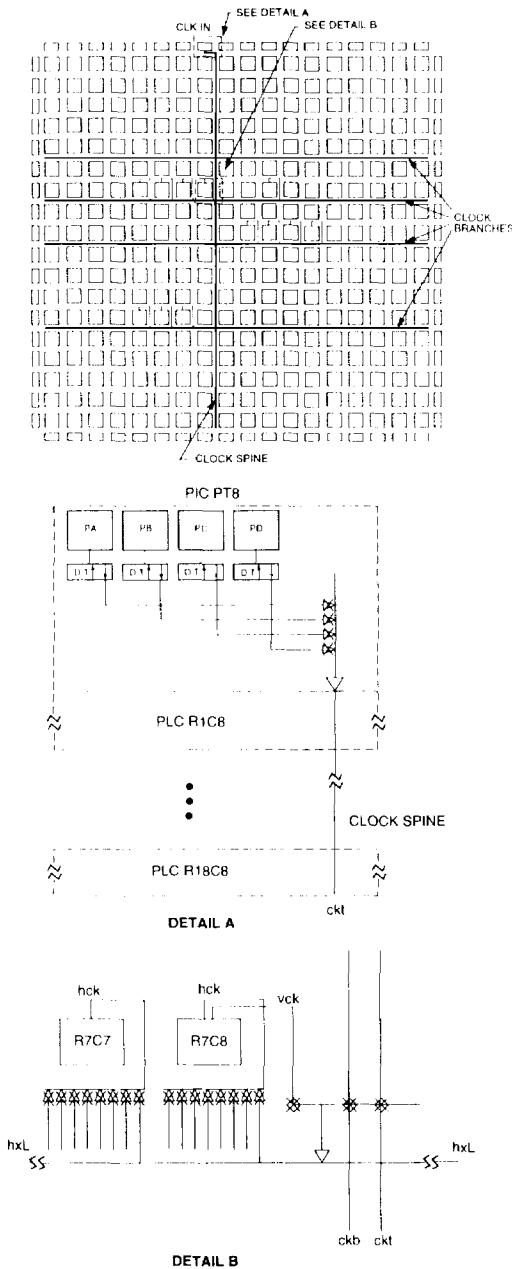


Figure 28. Primary Clock Distribution

Secondary Clock

There are times when a primary clock is either not available or not desired, and a secondary clock is needed. For example:

- Only one input pad per PIC can be placed on the clock routing. If a second input pad in a given PIC requires global signal routing, a secondary clock route must be used.
- Since there is only one branch driver in each PLC for either direction (vertical and horizontal), both clock R-nodes in a particular row or column (ckl and ckr, for example) cannot drive a branch. Therefore, two clocks should not be placed into I/O pads in PICs on the opposite sides of the same row or column if global clocks are to be used.
- Since the clock R-nodes can only be driven from input pads, internally generated clocks should use secondary clock routing.

Figure 29 illustrates the secondary clock distribution. If the clock signal originates from either the left or right side of the FPGA, it can be routed through the TRIDI buffers in the PIC onto one of the adjacent PLC's horizontal xL R-nodes. If the clock signal originates from the top or bottom of the FPGA, the vertical xL R-nodes are used for routing. In either case, an xL R-node is used as the clock spine. In the same manner, if a clock is only going to be used in one quadrant, the xH R-nodes can be used as a clock spine. The routing of the clock spine from the input pads to the vxL (vxH) using the BIDIs (BIDIHs) is shown in Figure 29, Detail A.

In each PLC, a low-skew connection through a long line driver can be used to connect a horizontal xL R-node to a vertical xL R-node or vice versa. As shown in Figure 29, Detail B, this is used to route the branches from the clock spine. If the clock spine is a vertical xL R-node, then the branches are horizontal xL R-nodes and vice versa. The clock is then routed into each PLC from the xL R-node clock branches.

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Clock Distribution Network (continued)

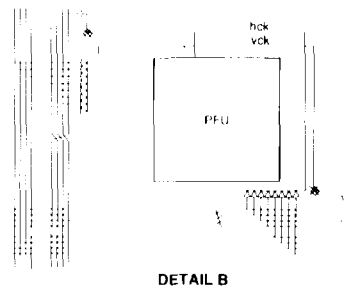
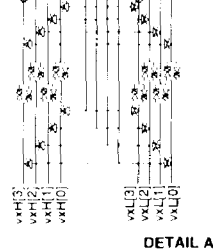
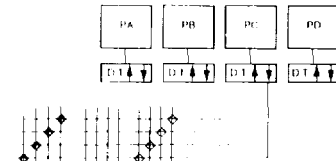
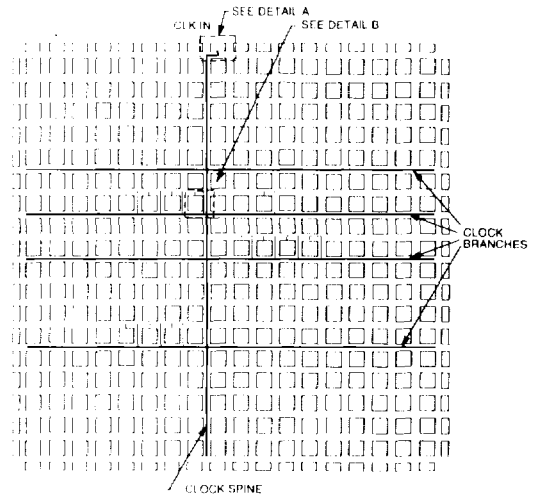
To minimize skew, the PLC clock input for all PLCs must be connected to the branch xL R-nodes, not the spine xL R-node. Even in PLCs where the clock is routed from the spine to the branches, the clock should be routed back into the PLC from the clock branch.

If the clock is to drive only a limited number of loads, the PFUs can be connected directly to the clock spine. In this case, all flip-flops driven by the clock must be located in the same row or column.

2

Alternatively, the clock can be routed from the spine to the branches by using the BIDIs instead of the long line drivers. This results in added delay in the clock net, but the clock skew is approximately equal to the clock routed using the long line drivers. This method can be used to create a clock that is used in only one quadrant. The xH R-nodes act as a clock spine, which is then routed to perpendicular xH R-nodes (the branches) using the BIDIHs.

Clock signals, such as the output of a counter, can also be generated in PLCs and routed onto an xL R-node, which then acts as a clock spine. Although the clock can be generated in any PLC, it is recommended that the clock be located as close to the center of the FPGA as possible to minimize clock skew.



5-4481(C)2C

Figure 29. Secondary Clock Distribution

FPGA States of Operation

Prior to becoming operational, the FPGA goes through a sequence of states, including initialization, configuration, and start-up. This section discusses these three states. Figure 30 outlines the FPGA states.

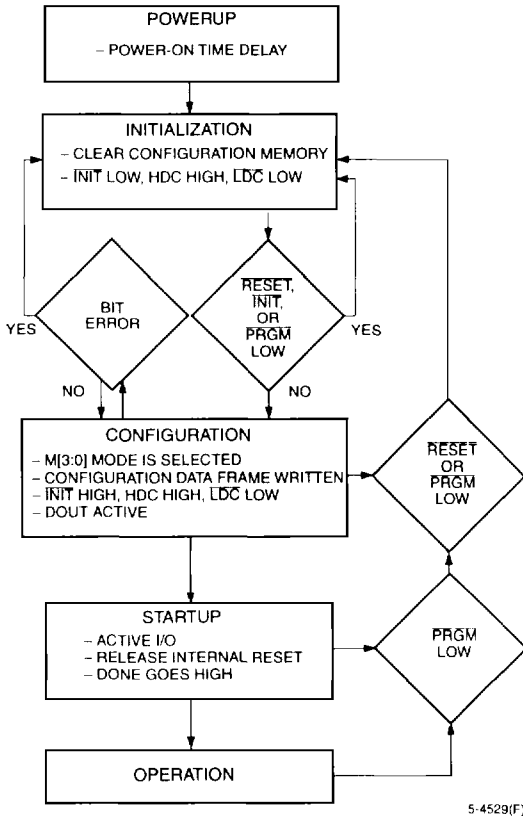


Figure 30. FPGA States of Operation

Initialization

Upon powerup, the device goes through an initialization process. First, an internal power-on-reset circuit is triggered when power is applied. When VDD reaches the voltage at which portions of the FPGA begin to operate (2.5 V to 3 V), the I/Os are configured based on the configuration mode, as determined by the mode select inputs M[2:0]. A time-out delay is initiated when VDD reaches between 3.0 V and 4.0 V to allow the power supply voltage to stabilize. The INIT and DONE outputs are low. At powerup, if VDD does not rise from 2.0 V to VDD in less than 25 ms, the user should delay configuration by inputting a low into INIT, PRGM, or RESET until VDD is greater than the recommended minimum operating voltage (4.75 V for commercial devices).

At the end of initialization, the default configuration option is that the configuration RAM is written to a low state. This prevents shorts prior to configuration. As a configuration option, after the first configuration (i.e., at reconfiguration), the user can reconfigure without clearing the internal configuration RAM first.

The active-low, open-drain initialization signal INIT is released and must be pulled high by an external resistor when initialization is complete. To synchronize the configuration of multiple FPGAs, one or more INIT pins should be wire-ANDed. If INIT is held low by one or more FPGAs or an external device, the FPGA remains in the initialization state. INIT can be used to signal that the FPGAs are not yet initialized. After INIT goes high for two internal clock cycles, the mode lines are sampled and the FPGA enters the configuration state.

The high during configuration (HDC), low during configuration (LDC), and DONE signals are active outputs in the FPGA's initialization and configuration states. HDC, LDC, and DONE can be used to provide control of external logic signals such as reset, bus enable, or PROM enable during configuration. For parallel master configuration modes, these signals provide PROM enable control and allow the data pins to be shared with user logic signals.

If configuration has begun, an assertion of RESET or PRGM initiates an abort, returning the FPGA to the initialization state. The PRGM and RESET pins must be pulled back high before the FPGA will enter the configuration state. During the start-up and operating states, only the assertion of PRGM causes a reconfiguration.

FPGA States of Operation (continued)

In the master configuration modes, the FPGA is the source of configuration clock (CCLK). In this mode, the initialization state is extended to ensure that, in daisy-chain operation, all daisy-chained slave devices are ready. Independent of differences in clock rates, master mode devices remain in the initialization state an additional six internal clock cycles after *INIT* goes high.

2

When configuration is initiated, a counter in the FPGA is set to 0 and begins to count configuration clock cycles applied to the FPGA. As each configuration data frame is supplied to the FPGA, it is internally assembled into data words. Each data word is loaded into the internal configuration memory. The configuration loading process is complete when the internal length count equals the loaded length count in the length count field, and the required end of configuration frame is written.

All I/Os operate as TTL inputs during configuration. All I/Os that are not used during the configuration process are 3-stated with internal pull-ups. During configuration, the PLC latch/FFs are held set/reset and the internal BiDi buffers are 3-stated. The TRIDs in the PICs are not 3-stated. The combinatorial logic begins to function as the FPGA is configured. Figure 31 shows the general waveform of the initialization, configuration, and start-up states.

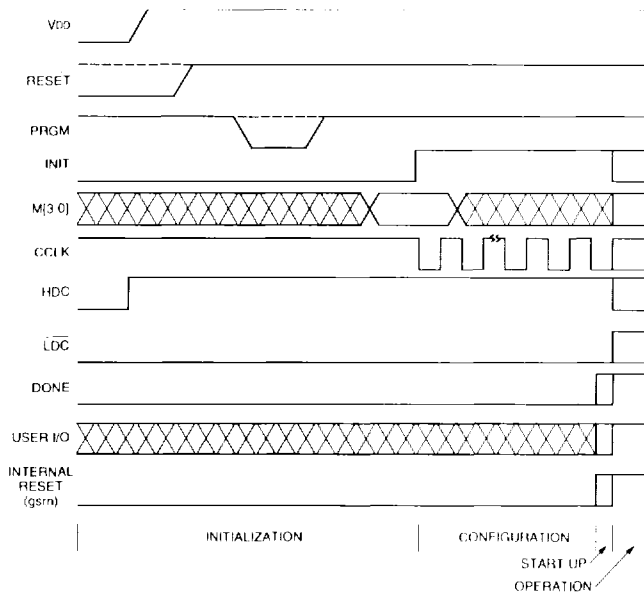
Configuration

The ORCA Series FPGA functionality is determined by the state of internal configuration RAM. This configuration RAM can be loaded in a number of different modes. In these configuration modes, the FPGA can act as a master or a slave of other devices in the system. The decision as to which configuration mode to use is a system design issue. The next section discusses configuration in detail, including the configuration data format and the configuration modes used to load the configuration data in the FPGA.

Start-Up

After configuration, the FPGA enters the start-up phase. This phase is the transition between the configuration and operational states.

This begins when the number of CCLKs received after *INIT* goes high is equal to the value of the length count field in the configuration frame and when the end of configuration frame has been written. The system design issue in the start-up phase is to ensure the user I/Os become active without inadvertently activating devices in the system or causing bus contention. A second system design concern is the timing of the release of global set/reset of the PLC latches/FFs.



5-4482(C)2C

Figure 31. Initialization/Configuration/Start-Up Waveforms

FPGA States of Operation (continued)

There are configuration options which control the relative timing of three events: DONE going high, release of the set/reset of internal FFs, and user I/Os becoming active. Figure 32 shows the start-up timing for both the ORCA and ATT3000 Series FPGAs. The system designer determines the relative timing of the I/Os becoming active, DONE going high, and the release of the set/reset of internal FFs. In the ORCA Series FPGA, the three events can occur in any arbitrary sequence. This means that they can occur before or after each other, or they can occur simultaneously. The default is for DONE to go high first. This allows configuration sources to be disconnected so that there is no bus contention when the I/Os become active in later cycles. The FFs are set/reset one cycle after DONE goes high so that operation begins in a known state. The DONE output is an open drain and may include an optional internal pull-up resistor to accommodate wired ANDing. The open-drain DONE outputs from multiple FPGAs can be ANDed and used as an active-high ready signal, an active-low PROM enable, or a reset to other portions of the system.

There is also a synchronous start-up mode where start-up does not begin until DONE goes high. The enabling of the FPGA outputs and the set/reset of the internal flip-flops can be triggered or delayed from the rising edge of DONE. Start-up can be delayed by holding the DONE signal low in the synchronous start-up mode. If the DONE signals of multiple FPGAs are tied together, with all in the synchronous start-up mode, start-up does not begin until all of the FPGAs are configured. Normally, the three events are triggered by CCLK. As a configuration option, the three events can be triggered by a user clock, UCLK. This allows start-up to be synchronized by a known system clock. When the user clock option is enabled, the user can still hold DONE low to delay start-up. This allows the synchronization of the start-up of multiple FPGAs. In addition to controlling the FPGA during start-up, additional start-up techniques to avoid contention include using isolation devices between the FPGA and other circuits in the system, reassigning I/O locations, and maintaining I/Os as 3-stated outputs until contentions are resolved.

Reconfiguration

To reconfigure the FPGA when the device is operating in the system, a low pulse is input into PRGM. The configuration data in the FPGA is cleared, and the I/Os not used for configuration are 3-stated. The FPGA then samples the mode select inputs and begins reconfiguration. When reconfiguration is complete, DONE is released, allowing it to be pulled high.

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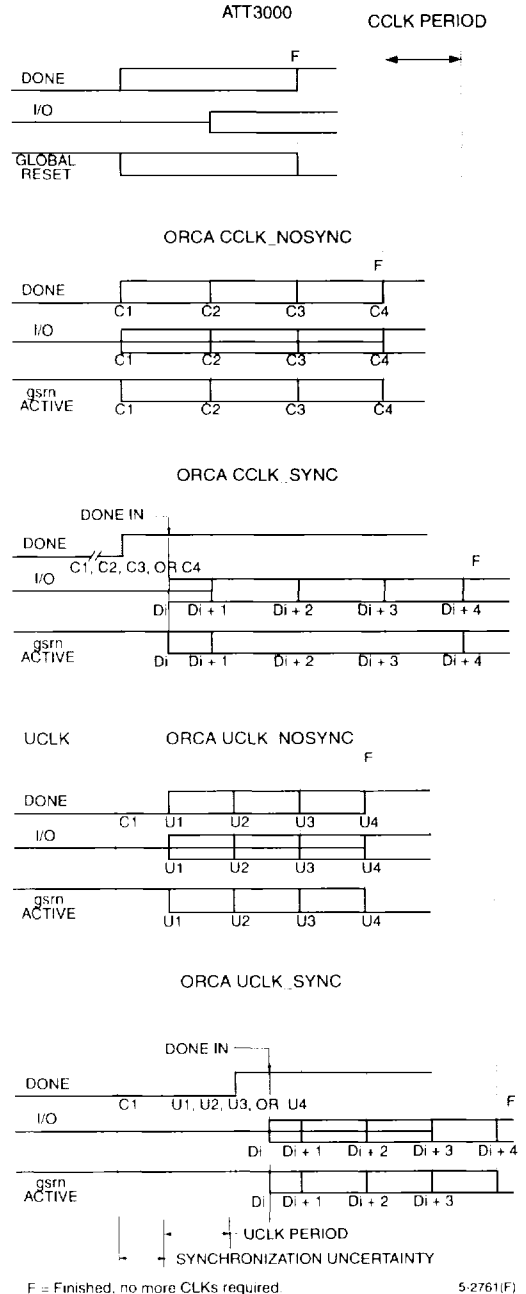


Figure 32. Start-Up Waveform

Configuration Data Format

This section discusses using the *ORCA* Foundry Development System to generate configuration RAM data and then provides the details of the configuration frame format.

Using *ORCA* Foundry to Generate Configuration RAM Data

2

The configuration data defines the I/O functionality, logic, and interconnections. The bit stream is generated by the development system. The bit stream created by the bit stream generation tool is a series of 1s and 0s used to write the FPGA configuration RAM. The bit stream can be loaded into the FPGA using one of the configuration modes discussed later. In the bit stream generator, the designer selects options which affect the FPGA's functionality. Using the output of bit stream generator, *circuit.bit*, the development system's download tool can load the configuration data into the *ORCA* series FPGA evaluation board from a PC or workstation. Alternatively, a user can program a PROM (such as the ATT1700 Series Serial ROMs or standard EPROMs) and load the FPGA from the PROM. The development system's PROM programming tool produces a file in *.mks* or *.exo* format.

Configuration Data Frame

A detailed description of the frame format is shown in Figure 33. The header frame begins with a series of 1s and a preamble of 0010, followed by a 24-bit length count field representing the total number of configuration clocks needed to complete the loading of the FPGAs. Following the header frame is an optional ID frame. This frame contains data used to determine if the bit stream is being loaded to the correct type of *ORCA* FPGA (e.g., is a bit stream generated for an ATT2C15 actually being sent to an ATT2C15?). It has a secondary function of optionally enabling the parity checking logic for the rest of the data frames.

The configuration data frames follow, with each frame starting with a 0 start bit and ending with three or more 1 stop bits. Following the start bit of each frame are four control bits: program bit, set to 1 if this is a data frame; compress bit, set to 1 if this is a compressed frame; and the *opar* and *epar* parity bits, to be discussed in the Bit Stream Error Checking section. An 11-bit address field (that determines which column in the FPGA is to be written) is followed by alignment and write control bits. For uncompressed frames, the data bits needed to write one column in the FPGA are next. For compressed frames, the data bits from the previous frame are sent to a different FPGA column, as specified by the new address bits; therefore, new data bits are not required. When configuration of the current FPGA is finished, an end-of-configuration frame (where the program bit is set to 0) is sent to the FPGA. The length and number of data frames and information about the PROM size for the 2C series FPGAs are given in Table 6.

Configuration Data Format (continued)

Table 6. Configuration Frame Size

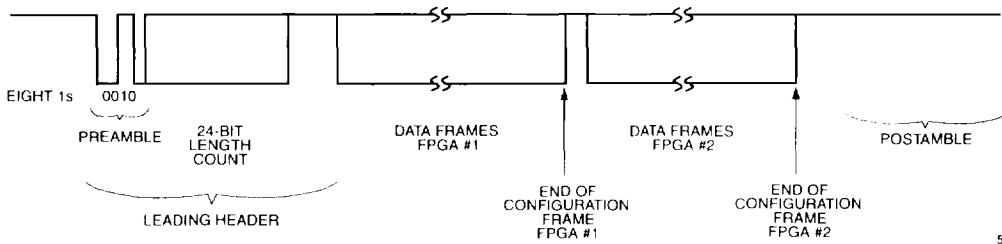
| Device | 2C04 | 2C06 | 2C08 | 2C10 | 2C12 | 2C15 | 2C26 | 2C40 |
|---|--------|--------|---------|---------|---------|---------|---------|---------|
| # of Frames | 480 | 568 | 656 | 744 | 832 | 920 | 1096 | 1378 |
| Data Bits/Frame | 110 | 130 | 150 | 170 | 190 | 210 | 250 | 316 |
| Configuration Data (# of frames x # of data bits/frame) | 52,800 | 73,840 | 98,400 | 126,480 | 158,080 | 193,200 | 274,000 | 435,448 |
| Maximum Total # Bits/Frame (align bits, 1 write bit, 8 stop bits) | 136 | 160 | 176 | 200 | 216 | 240 | 280 | 344 |
| Maximum Configuration Data (# bits x # of frames) | 65,280 | 90,880 | 115,456 | 148,800 | 179,712 | 220,800 | 306,880 | 474,032 |
| Maximum PROM Size (bits) (add 48-bit header, ID frame, and 40-bit end of configuration frame) | 65,504 | 91,128 | 115,720 | 149,088 | 180,016 | 221,128 | 307,248 | 474,464 |

The data frames for all the 2C series devices are given in Table 7. An alignment field is required in the slave parallel mode for the uncompressed format. The alignment field (shown by [A]) is a series of 0s: five for the 2C06, 2C10, 2C15, and 2C26; three for the 2C40; and one for the 2C04, 2C08, and 2C12. The alignment field is not required in any other mode.

Table 7. Configuration Data Frames

| | |
|----------------|---|
| ATT2C04 | |
| Uncompressed | 010 opar epar [addr10:0] [A]1[Data109:0]111 |
| Compressed | 011 opar epar [addr10:0] 111 |
| ATT2C06 | |
| Uncompressed | 010 opar epar [addr10:0] [A]1[Data129:0]111 |
| Compressed | 011 opar epar [addr10:0] 111 |
| ATT2C08 | |
| Uncompressed | 010 opar epar [addr10:0] [A]1[Data149:0]111 |
| Compressed | 011 opar epar [addr10:0] 111 |
| ATT2C10 | |
| Uncompressed | 010 opar epar [addr10:0] [A]1[Data169:0]111 |
| Compressed | 011 opar epar [addr10:0] 111 |
| ATT2C12 | |
| Uncompressed | 010 opar epar [addr10:0] [A]1[Data189:0]111 |
| Compressed | 011 opar epar [addr10:0] 111 |
| ATT2C15 | |
| Uncompressed | 010 opar epar [addr10:0] [A]1[Data209:0]111 |
| Compressed | 011 opar epar [addr10:0] 111 |
| ATT2C26 | |
| Uncompressed | 010 opar epar [addr10:0] [A]1[Data249:0]111 |
| Compressed | 011 opar epar [addr10:0] 111 |
| ATT2C40 | |
| Uncompressed | 010 opar epar [addr10:0] [A]1[Data315:0]111 |
| Compressed | 011 opar epar [addr10:0] 111 |

Configuration Data Format (continued)



5-4530(F)

Figure 33. Serial Configuration Data Format

| | | |
|--|-------------------------|---|
| Header | 11111111 | Leading header — 4 bits minimum dummy bits |
| | 0010 | Preamble |
| | 24-Bit Length Count | Configuration frame length |
| | 1111 | Trailing header — 4 bits minimum dummy bits |
| ID Frame (Optional) | 0 | Frame start |
| | P—1 | Must be set to 1 to indicate data frame |
| | C—0 | Must be set to 0 to indicate uncompressed |
| | Opar, Epar | Frame parity bits |
| | Addr[10:0] = 1111111111 | ID frame address |
| | Prty_En | Set to 1 to enable parity |
| | Reserved [42:0] | Reserved bits set to 0 |
| | ID | 20-bit part ID |
| Configuration Data Frame (repeated for each data frame) | 111 | Three or more stop bits (high) to separate frames |
| | 0 | Frame start |
| | P—1 or 0 | 1 indicates data frame; 0 indicates all frames are written |
| | C—1 or 0 | Uncompressed — 0 indicates data and address are supplied; Compressed — 1 indicates only address is supplied |
| | Opar, Epar | Frame parity bits |
| | Addr[10:0] | Column address in FPGA to be written |
| | A | Alignment bit (different number of 0s needed for each part) |
| | 1 | Write bit — used in uncompressed data frame |
| End of Configuration | Data Bits | Needed only in an uncompressed data frame |
| | 111 | One or more stop bits (high) to separate frames |
| End of Configuration | 0010011111111111 | 16 bits—00 indicates all frames are written |
| Postamble | 111111..... | Additional 1s |

Note: For slave parallel mode, the byte containing the preamble must be 11110010. The number of leading header dummy bits must be $(n * 8) + 4$, where n is any nonnegative integer and the number of trailing dummy bits must be $(n * 8)$, where n is any positive integer. The number of stop bits/frame for slave parallel mode must be $(x * 8)$, where x is a positive integer. Note also that the bit stream generator tool supplies a bit stream which is compatible with all configuration modes, including slave parallel mode.

Figure 34. Configuration Frame Format and Contents

Bit Stream Error Checking

There are three different types of bit stream error checking performed in the ORCA 2C FPGAs: ID frame, frame alignment, and parity checking.

An optional ID data frame can be sent to a specified address in the FPGA. This ID frame contains a unique code for the part it was generated for which is compared within the FPGA. Any differences are flagged as an ID error.

Every data frame in the FPGA begins with a start bit set to 0 and three or more stop bits set to 1. If any of the three previous bits were a 0 when a start bit is encountered, it is flagged as a frame alignment error.

Parity checking is also done on the FPGA for each frame, if it has been enabled by setting the `prty_en` bit to 1 in the ID frame. Two parity bits, `opar` and `epar`, are used to check the parity of bits in alternating bit positions to even parity in each data frame. If an odd number of ones is found for either the even bits (starting with the start bit) or the odd bits (starting with the program bit), then a parity error is flagged.

When any of the three possible errors occur, the FPGA is forced into the INIT state, forcing `INIT` low. The FPGA will remain in this state until either the `RESET` or `PRGM` pins are asserted.

FPGA Configuration Modes

There are eight methods for configuring the FPGA. Seven of the configuration modes are selected on the M0, M1, and M2 inputs. The eighth configuration mode is accessed through the boundary-scan interface. A fourth input, M3, is used to select the frequency of the internal oscillator, which is the source for CCLK in some configuration modes. The nominal frequencies of the internal oscillator are 1.25 MHz and 10 MHz. The 1.25 MHz frequency is selected when the M3 input is unconnected or driven to a high state.

There are three basic FPGA configuration modes: master, slave, and peripheral. The configuration data can be transmitted to the FPGA serially or in parallel bytes. As a master, the FPGA provides the control signals out to strobe data in. As a slave device, a clock is generated externally and provided into CCLK. In the peripheral mode, the FPGA acts as a microprocessor peripheral. Table 8 lists the functions of the configuration mode pins.

Table 8. Configuration Modes

| M2 | M1 | M0 | CCLK | Configuration Mode | Data |
|----|----|----|----------|--------------------|----------|
| 0 | 0 | 0 | Output | Master | Serial |
| 0 | 0 | 1 | Input | Slave Parallel | Parallel |
| 0 | 1 | 0 | Reserved | | |
| 0 | 1 | 1 | Input | Sync Peripheral | Parallel |
| 1 | 0 | 0 | Output | Master (up) | Parallel |
| 1 | 0 | 1 | Output | Async Peripheral | Parallel |
| 1 | 1 | 0 | Output | Master (down) | Parallel |
| 1 | 1 | 1 | Input | Slave | Serial |

Master Parallel Mode

The master parallel configuration mode is generally used to interface to industry-standard byte-wide memory such as the 2764 and larger EPROMs. Figure 35 provides the connections for master parallel mode. The FPGA outputs an 18-bit address on A[17:0] to memory and reads one byte of configuration data on the rising edge of RCLK. The parallel bytes are internally serialized starting with the least significant bit, D0.

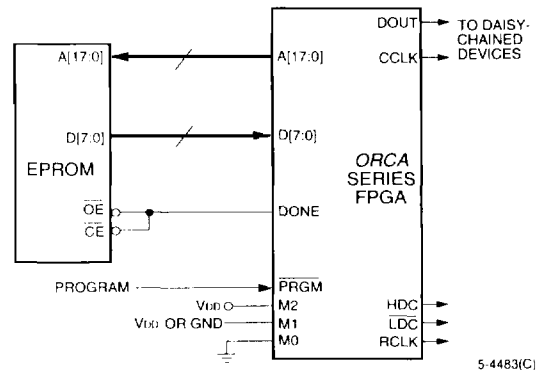


Figure 35. Master Parallel Configuration Schematic

There are two parallel master modes: master up and master down. In master up, the starting memory address is 00000 Hex and the FPGA increments the address for each byte loaded. In master down, the starting memory address is 3FFFF Hex and the FPGA decrements the address.

One master mode FPGA can interface to the memory and provide configuration data on DOUT to additional FPGAs in a daisy chain. The configuration data on DOUT is provided synchronously with the falling edge of CCLK. The frequency of the CCLK output is eight times that of RCLK.

FPGA Configuration Modes (continued)

Master Serial Mode

2

In the master serial mode, the FPGA loads the configuration data from an external serial ROM. The configuration data is either loaded automatically at start-up or on a PRGM command to reconfigure. The ATT1700 and ATT1700A Series can be used to configure the FPGA in the master serial mode. This provides a simple four-pin interface in an eight-pin package. The ATT1736, ATT1765, and ATT17128 serial ROMs store 32K, 64K, and 128K bits, respectively.

Configuration in the master serial mode can be done at powerup and/or upon a configure command. The system or the FPGA must activate the serial ROM's RESET/OE and CE inputs. At powerup, the FPGA and serial ROM each contain internal power-on reset circuitry that allows the FPGA to be configured without the system providing an external signal. The power-on reset circuitry causes the serial ROM's internal address pointer to be reset. After powerup, the FPGA automatically enters its initialization phase.

The serial ROM/FPGA interface used depends on such factors as the availability of a system reset pulse, availability of an intelligent host to generate a configure command, whether a single serial ROM is used or multiple serial ROMs are cascaded, whether the serial ROM contains a single or multiple configuration programs, etc. Because of differing system requirements and capabilities, a single FPGA/serial ROM interface is generally not appropriate for all applications.

Data is read in the FPGA sequentially from the serial ROM. The DATA output from the serial ROM is connected directly into the DIN input of the FPGA. The CCLK output from the FPGA is connected to the CLOCK input of the serial ROM. During the configuration process, CCLK clocks one data bit on each rising edge.

Since the data and clock are direct connects, the FPGA/serial ROM design task is to use the system or FPGA to enable the RESET/OE and CE of the serial ROM(s). There are several methods for enabling the serial ROM's RESET/OE and CE inputs. The serial ROM's RESET/OE is programmable to function with RESET active-high and OE active-low or RESET active-low and OE active-high.

In Figure 36, serial ROMs are cascaded to configure multiple daisy-chained FPGAs. The host generates a 500 ns low pulse into the FPGA's PRGM input. The FPGA's INIT input is connected to the serial ROMs' RESET/OE input, which has been programmed to

function with RESET active-low and OE active-high. The FPGA DONE is routed to the CE pin. The low on DONE enables the serial ROMs. At the completion of configuration, the high on the FPGA's DONE disables the serial ROM.

Serial ROMs can also be cascaded to support the configuration of multiple FPGAs or to load a single FPGA when configuration data requirements exceed the capacity of a single serial ROM. After the last bit from the first serial ROM is read, the serial ROM outputs CE low and 3-states the DATA output. The next serial ROM recognizes the low on CE input and outputs configuration data on the DATA output. After configuration is complete, the FPGA's DONE output into CE disables the serial ROMs.

This FPGA/serial ROM interface is not used in applications in which a serial ROM stores multiple configuration programs. In these applications, the next configuration program to be loaded is stored at the ROM location that follows the last address for the previous configuration program. The reason the interface in Figure 36 will not work in this application is that the low output on the INIT signal would reset the serial ROM address pointer, causing the first configuration to be reloaded.

In some applications, there can be contention on the FPGA's DIN pin. During configuration, DIN receives configuration data, and after configuration, it is a user I/O. If there is contention, an early DONE at start-up (selected in ORCA Foundry) may correct the problem. An alternative is to use LDC to drive the serial ROM's CE pin. In order to reduce noise, it is generally better to run the master serial configuration at 1.25 MHz (M3 pin tied high), rather than 10 MHz, if possible.

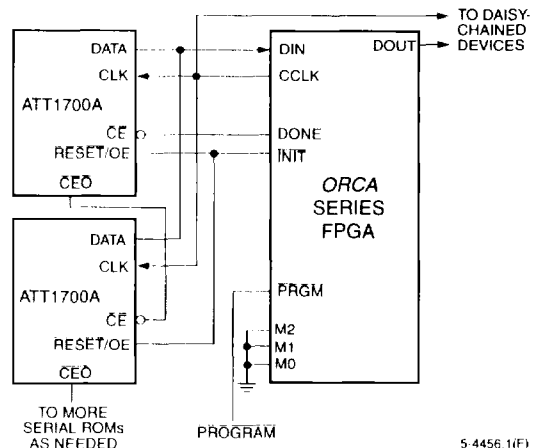


Figure 36. Master Serial Configuration Schematic

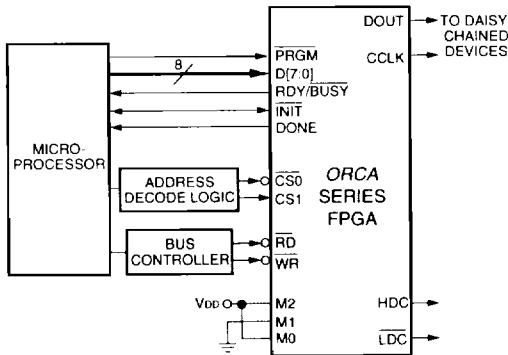
5-4456 1(F)

FPGA Configuration Modes (continued)

Asynchronous Peripheral Mode

Figure 37 shows the connections needed for the asynchronous peripheral mode. In this mode, the FPGA system interface is similar to that of a microprocessor-peripheral interface. The microprocessor generates the control signals to write an 8-bit byte into the FPGA. The FPGA control inputs include active-low CS0 and active-high CS1 chip selects and a write WR input. The chip selects can be cycled or maintained at a static level during the configuration cycle. Each byte of data is written into the FPGA's D[7:0] input pins.

The FPGA provides a RDY/BUSY status output to indicate that another byte can be loaded. A low on RDY/BUSY indicates that the double-buffered hold/shift registers are not ready to receive data. The shortest time RDY/BUSY is low occurs when a byte is loaded into the hold register and the shift register is empty, in which case the byte is immediately transferred to the shift register. The longest time for RDY/BUSY to remain low occurs when a byte is loaded into the holding register and the shift register has just started shifting configuration data into configuration RAM. The RDY/BUSY status is also available on the D7 pin by enabling the chip selects, setting WR high, and setting RD low.



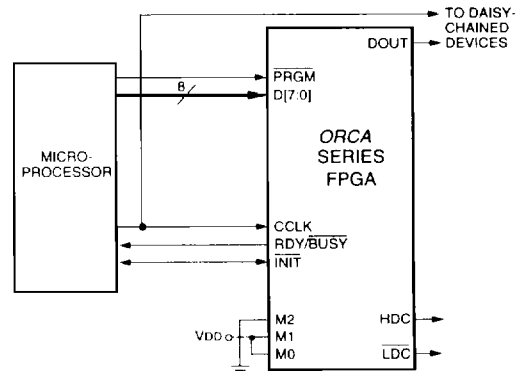
5-4484(C)

Figure 37. Asynchronous Peripheral Configuration Schematic

Synchronous Peripheral Mode

In the synchronous peripheral mode, byte-wide data is input into D[7:0] on the rising edge of the CCLK input. The first data byte is clocked in on the second CCLK after INIT goes high. Subsequent data bytes are clocked in on every eighth rising edge of CCLK. The RDY/BUSY signal is an output which acts as an acknowledge. RDY/BUSY goes high one CCLK after data is clocked and, after one CCLK cycle, returns low. The process repeats until all of the data is loaded into the FPGA. The data begins shifting on DOUT 1.5 cycles after it is loaded in parallel. It requires additional CCLKs after the last byte is loaded to complete the shifting. Figure 38 shows the connections for synchronous peripheral mode.

As with master modes, the peripheral modes can be used as the lead FPGA for a daisy chain of slave FPGAs.



5-4486(C)

Figure 38. Synchronous Peripheral Configuration Schematic

FPGA Configuration Modes (continued)

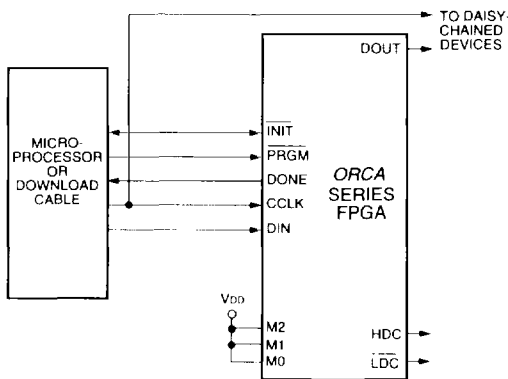
Slave Serial Mode

The slave serial mode is primarily used when multiple FPGAs are configured in a daisy chain. The serial slave mode is also used on the FPGA evaluation board which interfaces to the download cable. A device in the slave serial mode can be used as the lead device in a daisy chain. Figure 39 shows the connections for the slave serial configuration mode.

2

The configuration data is provided into the FPGA's DIN input synchronous with the configuration clock CCLK input. After the FPGA has loaded its configuration data, it retransmits the incoming configuration data on DOUT. CCLK is routed into all slave serial mode devices in parallel.

Multiple slave FPGAs can be loaded with identical configurations simultaneously. This is done by loading the configuration data into the DIN inputs in parallel.



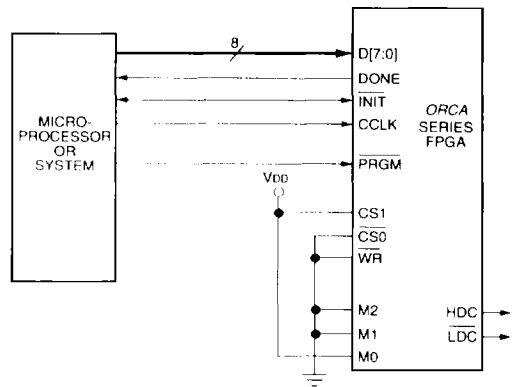
5-4485(C)

Figure 39. Slave Serial Configuration Schematic

Slave Parallel Mode

The slave parallel mode is essentially the same as the slave serial mode except that 8 bits of data are input on pins D[7:0] for each CCLK cycle. Due to 8 bits of data being input per CCLK cycle, the DOUT pin does not contain a valid bit stream for slave parallel mode. As a result, the lead device cannot be used in the slave parallel mode in a daisy-chain configuration.

Figure 40 is a schematic of the connections for the slave parallel configuration mode. WR and CS0 are active-low chip select signals, and CS1 is an active-high chip select signal. These chip selects allow the user to configure multiple FPGAs in slave parallel mode using an 8-bit data bus common to all of the FPGAs. These chip selects can then be used to select the FPGA(s) to be configured with a given bit stream, but once an FPGA has been selected, it cannot be deselected until it has been completely programmed.



5-4487(C)

Figure 40. Slave Parallel Configuration Schematic

FPGA Configuration Modes (continued)

Daisy Chain

Multiple FPGAs can be configured by using a daisy chain of the FPGAs. Daisy chaining uses a lead FPGA and one or more FPGAs configured in slave serial mode. The lead FPGA can be configured in any mode except slave parallel mode. (Daisy chaining is not available with the boundary-scan ram_w instruction, discussed later.)

All daisy-chained FPGAs are connected in series. Each FPGA reads and shifts the preamble and length count in on positive CCLK and out on negative CCLK edges.

An upstream FPGA which has received the preamble and length count outputs a high on DOUT until it has received the appropriate number of data frames so that downstream FPGAs do not receive frame start bits (0s). After loading and retransmitting the preamble and length count to a daisy chain of slave devices, the lead device loads its configuration data frames. The loading of configuration data continues after the lead device has received its configuration data if its internal frame bit counter has not reached the length count. When the configuration RAM is full and the number of bits received is less than the length count field, the FPGA shifts any additional data out on DOUT.

The configuration data is read into DIN of slave devices on the positive edge of CCLK, and shifted out DOUT on the negative edge of CCLK. Figure 41 shows the connections for loading multiple FPGAs in a daisy-chain configuration.

The generation of CCLK for the daisy-chained devices which are in slave serial mode differs depending on the configuration mode of the lead device. A master parallel mode device uses its internal timing generator to produce an internal CCLK at eight times its memory address rate (RCLK). The asynchronous peripheral mode device outputs eight CCLKs for each write cycle. If the lead device is configured in either synchronous peripheral or a slave mode, CCLK is routed to the lead device and to all of the daisy-chained devices.

The development system can create a composite configuration bit stream for configuring daisy-chained FPGAs. The frame format is a preamble, a length count for the total bit stream, multiple concatenated data frames, an end-of-configuration frame per device, a postamble, and an additional fill bit per device in the serial chain.

As seen in Figure 41, the INIT pins for all of the FPGAs are connected together. This is required to guarantee that powerup and initialization will work correctly. In general, the DONE pins for all of the FPGAs are also connected together as shown to guarantee that all of the FPGAs enter the start-up state simultaneously. This may not be required, depending upon the start-up sequence desired.

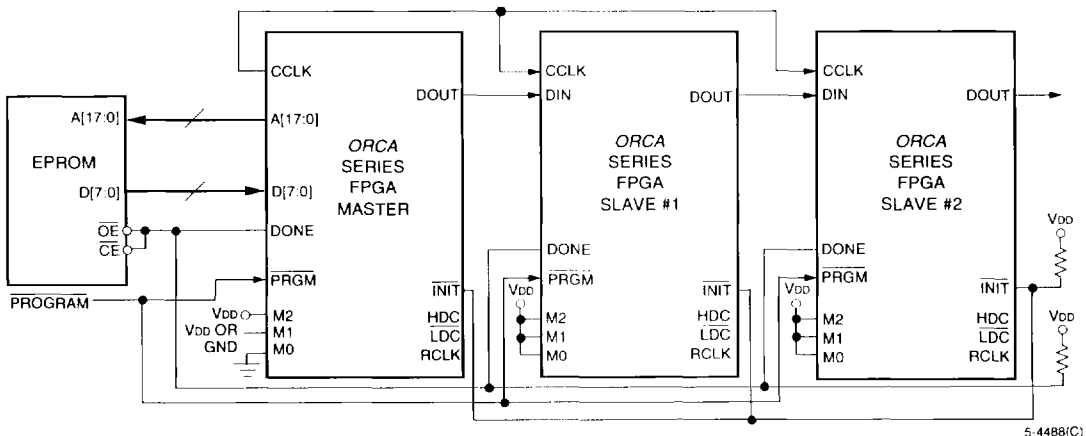


Figure 41. Daisy-Chain Configuration Schematic

Readback

Readback is used to read back the configuration data and, optionally, the state of the PFU outputs. A readback operation can be done while the FPGA is in normal system operation. The readback operation cannot be daisy chained. To use readback, the user selects options in the bit stream generator in the *ORCA* Foundry development system.

2

Table 9 provides readback options selected in the bit stream generator tool. The table provides the number of times that the configuration data can be read back. This is intended primarily to give the user control over the security of the FPGA's configuration program. The user can prohibit readback (0), allow a single readback (1), or allow unrestricted readback (U).

The pins used for readback are readback data (RD_DATA), read configuration (RD_CFGN), and configuration clock (CCLK). A readback operation is initiated by a high-to-low transition on RD_CFGN. The RD_CFGN input must remain low during the readback operation. The readback operation can be restarted at frame 0 by setting the RD_CFGN pin high, applying at least two rising edges of CCLK, and then applying RD_CFGN low again. One bit of data is shifted out on RD_DATA on the rising edge of CCLK. The first start bit of the readback frame is transmitted out on the first rising edge of CCLK after RD_CFGN is input low.

It should be noted that the RD_DATA output pin is also used as the dedicated boundary-scan output pin, TDO. If this pin is being used as TDO, the RD_DATA output from readback can be routed internally to any other pin desired. The RD_CFGN input pin is also used to control the global 3-state (ts_all) function. Before and during configuration, the ts_all signal is always driven by the RD_CFGN input and readback is disabled. After configuration, the selection as to whether this input drives the readback or global 3-state function is determined by a set of bit stream options. If used as the RD_CFGN input for readback, the internal ts_all input can be routed internally to be driven by any input pin.

The readback frame contains the configuration data and the state of the internal logic. During readback, the value of all five PFU outputs can be captured. The following options are allowed when doing a capture of the PFU outputs.

1. Do not capture data (the data written to the RAMs, usually 0, will be read back).
2. Capture data upon entering readback.
3. Capture data based upon a configurable signal internal to the FPGA. If this signal is tied to logic 0, capture RAMs are written continuously, which is equivalent to ATT3000 Series capture.
4. Capture data on either options 2 or 3 above.

The readback frame has a similar, but not identical, format to the configuration frame. This eases a bitwise comparison between the configuration and readback data. The readback data is not inverted. Every data frame has one low start bit and one high stop bit. The preamble, including the length count field, is not part of the readback frame. The readback frame contains states in locations not used in the configuration. These locations need to be masked out when comparing the configuration and readback frames. The development system optionally provides a readback bit stream to compare to readback data from the FPGA.

Table 9. Readback Options

| Option | Function |
|--------|--|
| 0 | Inhibit Readback |
| 1 | Allow One Readback Only |
| U | Allow Unrestricted Number of Readbacks |

Boundary Scan

The increasing complexity of integrated circuits (ICs) and IC packages has increased the difficulty of testing printed-circuit boards (PCBs). To address this testing problem, the *IEEE* standard 1149.1 - 1990 (*IEEE* Standard Test Access Port and Boundary-Scan Architecture) is implemented in the *ORCA* series of FPGAs. It allows users to efficiently test the interconnection between integrated circuits on a PCB as well as test the integrated circuit itself. The *IEEE* 1149.1 standard is a well-defined protocol that ensures interoperability among boundary-scan (BSCAN) equipped devices from different vendors.

The *IEEE* 1149.1 standard defines a test access port (TAP) that consists of a four-pin interface with an optional reset pin for boundary-scan testing of integrated circuits in a system. The *ORCA* Series FPGA provides four interface pins: test data in (TDI), test mode select (TMS), test clock (TCK), and test data out (TDO). The PRGM pin used to reconfigure the device also resets the boundary-scan logic.

The user test host serially loads test commands and test data into the FPGA through these pins to drive outputs and examine inputs. In the configuration shown in Figure 42, where boundary scan is used to test ICs, test data is transmitted serially into TDI of the first BSCAN device (U1), through TDO/TDI connections between BSCAN devices (U2 and U3), and out TDO of the last BSCAN device (U4). In this configuration, the TMS and TCK signals are routed to all boundary-scan ICs in parallel so that all boundary-scan components operate in the same state. In other configurations, multiple scan paths are used instead of a single ring. When multiple scan paths are used, each ring is independently controlled by its own TMS and TCK signals.

Figure 43 provides a system interface for components used in the boundary-scan testing of PCBs. The three major components shown are the test host, boundary-scan support circuit, and the devices under test (DUTs). The DUTs shown here are *ORCA* Series FPGAs with dedicated boundary-scan circuitry. The test host is normally one of the following: automatic test equipment (ATE), a workstation, a PC, or a microprocessor.

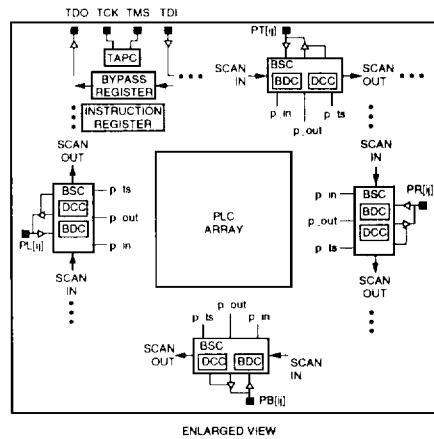
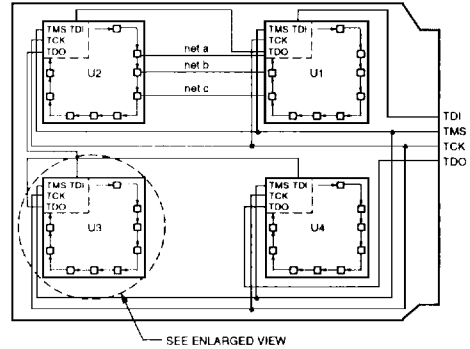


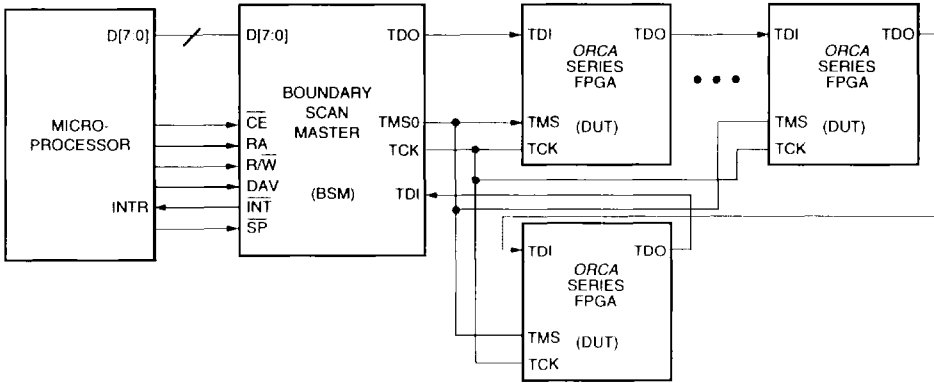
Fig.34 a(M)

Key: BSC = boundary-scan cell, BDC = bidirectional data cell, and DCC = data control cell.

Figure 42. Printed-Circuit Board with Boundary-Scan Circuitry

Boundary Scan (continued)

2



1BSI(C)

Figure 43. Boundary-Scan Interface

The boundary-scan support circuit shown in Figure 43 is the Lucent 497AA Boundary-Scan Master (BSM). The BSM off-loads tasks from the test host to increase test throughput. To interface between the test host and the DUTs, the BSM has a general microprocessor interface and provides parallel-to-serial/serial-to-parallel conversion, as well as three 8K data buffers. The BSM also increases test throughput with a dedicated automatic test pattern generator and with compression of the test response with a signature analysis register. The PC-based Lucent boundary-scan test card/software allows a user to quickly prototype a boundary-scan test setup.

Boundary-Scan Instructions

The ORCA Series boundary-scan circuitry is used for three mandatory IEEE 1149.1 tests (EXTEST, SAMPLE/PRELOAD, BYPASS) and four Lucent-defined instructions. The 3-bit wide instruction register supports the eight instructions listed in Table 10.

Table 10. Boundary-Scan Instructions

| Code | Instruction |
|------|-------------------|
| 000 | EXTEST |
| 001 | PLC Scan Ring 1 |
| 010 | RAM Write (RAM_W) |
| 011 | Reserved |
| 100 | SAMPLE/PRELOAD |
| 101 | PLC Scan Ring 2 |
| 110 | RAM Read (RAM_R) |
| 111 | BYPASS |

The external test (EXTEST) instruction allows the interconnections between ICs in a system to be tested for opens and stuck-at faults. If an EXTEST instruction is performed for the system shown in Figure 42, the connections between U1 and U2 (shown by nets a, b, and c) can be tested by driving a value onto the given nets from one device and then determining whether the same value is seen at the other device. This is determined by shifting 2 bits of data for each pin (one for the output value and one for the 3-state value) through the BSR until each one aligns to the appropriate pin. Then, based upon the value of the 3-state signal, either the I/O pad is driven to the value given in the BSR, or the BSR is updated with the input value from the I/O pad, which allows it to be shifted out TDO.

The SAMPLE instruction is useful for system debugging and fault diagnosis by allowing the data at the FPGA's I/Os to be observed during normal operation. The data for all of the I/Os is captured simultaneously into the BSR, allowing them to be shifted-out TDO to the test host. Since each I/O buffer in the PICs is bidirectional, two pieces of data are captured for each I/O pad: the value at the I/O pad and the value of the 3-state control signal.

There are four Lucent-defined instructions. The PLC scan rings 1 and 2 (PSR1, PSR2) allow user-defined internal scan paths using the PLC latches/FFs. The RAM Write Enable (RAM_W) instruction allows the user to serially configure the FPGA through TDI. The RAM_Read Enable (RAM_R) allows the user to read back RAM contents on TDO after configuration.

Boundary Scan (continued)

ORCA Boundary-Scan Circuitry

The ORCA Series boundary-scan circuitry includes a test access port controller (TAPC), instruction register (IR), boundary-scan register (BSR), and bypass register. It also includes circuitry to support the four Lucent-defined instructions.

Figure 44 shows a functional diagram of the boundary-scan circuitry that is implemented in the ORCA series. The input pins' (TMS, TCK, and TDI) locations vary depending on the part, and the output pin is the dedicated TDO/RD_DATA output pad. Test data in (TDI) is the serial input data. Test mode select (TMS) controls the boundary-scan test access port controller (TAPC). Test clock (TCK) is the test clock on the board.

The BSR is a series connection of boundary-scan cells (BSCs) around the periphery of the IC. Each I/O pad on the FPGA, except for CCLK, DONE, and the boundary-scan pins (TCK, TDI, TMS, and TDO), is included in the BSR. The first BSC in the BSR (connected to TDI) is

located in the first PIC I/O pad on the left of the top side of the FPGA (PTA PIC). The BSR proceeds clockwise around the top, right, bottom, and left sides of the array. The last BSC in the BSR (connected to TDO) is located on the top of the left side of the array (PLA3).

The bypass instruction uses a single FF which resynchronizes test data that is not part of the current scan operation. In a bypass instruction, test data received on TDI is shifted out of the bypass register to TDO. Since the BSR (which requires a two FF delay for each pad) is bypassed, test throughput is increased when devices that are not part of a test operation are bypassed.

The boundary-scan logic is enabled before and during configuration. After configuration, a configuration option determines whether or not boundary-scan logic is used.

The 32-bit boundary-scan identification register contains the manufacturer's ID number, unique part number, and version, but is not implemented in the ORCA series of FPGAs. If boundary scan is not used, TMS, TDI, and TCK become user I/Os, and TDO is 3-stated or used in the readback operation.

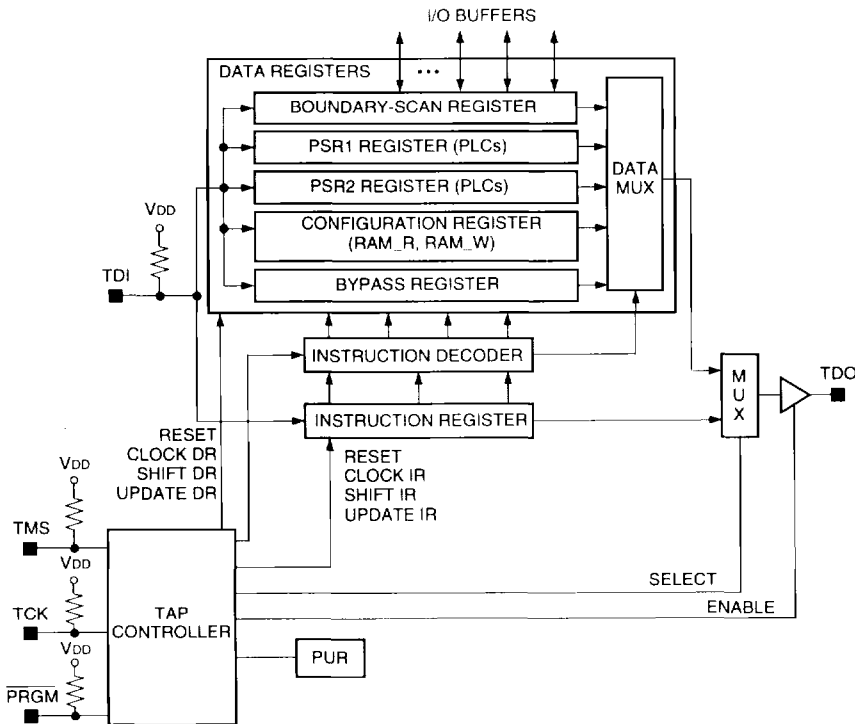


Figure 44. ORCA Series Boundary-Scan Circuitry Functional Diagram

5-2840(C)2C

Boundary Scan (continued)

ORCA Series TAP Controller (TAPC)

The ORCA Series TAP controller (TAPC) is a 1149.1 compatible test access port controller. The 16 JTAG state assignments from the IEEE 1149.1 specification are used. The TAPC is controlled by TCK and TMS. The TAPC states are used for loading the IR to allow three basic functions in testing: providing test stimuli (Update DR), test execution (Run Test/Idle), and obtaining test responses (Capture DR). The TAPC allows the test host to shift in and out both instructions and test data/results. The inputs and outputs of the TAPC are provided in the table below. The outputs are primarily the control signals to the instruction register and the data register.

2

Table 11. TAP Controller Input/Outputs

| Symbol | I/O | Function |
|------------|-----|-----------------------------------|
| TMS | I | Test Mode Select |
| TCK | I | Test Clock |
| PUR | I | Powerup Reset |
| PRGM | I | BSCAN Reset |
| TRESET | O | Test Logic Reset |
| Select | O | Select IR (High); Select DR (Low) |
| Enable | O | Test Data Out Enable |
| Capture DR | O | Capture/Parallel Load DR |
| Capture IR | O | Capture/Parallel Load IR |
| Shift DR | O | Shift Data Register |
| Shift IR | O | Shift Instruction Register |
| Update DR | O | Update/Parallel Load DR |
| Update IR | O | Update/Parallel Load IR |

The TAPC generates control signals which allow capture, shift, and update operations on the instruction and data registers. In the capture operation, data is loaded into the register. In the shift operation, the captured data is shifted out while new data is shifted in. In the update operation, either the instruction register is loaded for instruction decode, or the boundary-scan register is updated for control of outputs.

The test host generates a test by providing input into the ORCA Series TMS input synchronous with TCK. This sequences the TAPC through states in order to perform the desired function on the instruction register or a data register. Figure 45 provides a diagram of the state transitions for the TAPC. The next state is determined by the TMS input value.

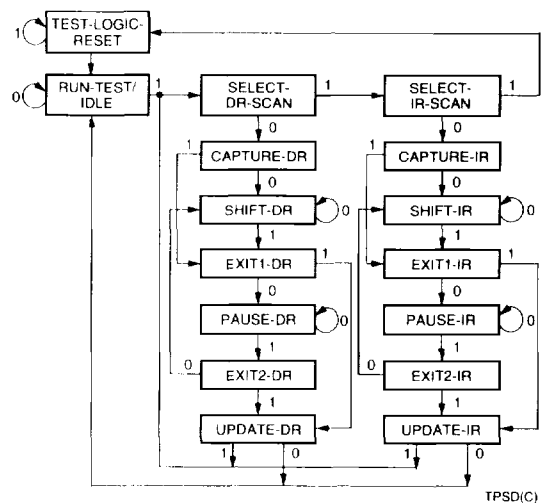


Figure 45. TAP Controller State Transition Diagram

Boundary Scan (continued)

Boundary-Scan Cells

Figure 46 is a diagram of the boundary-scan cell (BSC) in the ORCA series PICs. There are four BSCs in each PIC: one for each pad, except as noted above. The BSCs are connected serially to form the BSR. The BSC controls the functionality of the in, out, and 3-state signals for each pad.

The BSC allows the I/O to function in either the normal or test mode. Normal mode is defined as when an output buffer receives input from the PLC array and provides output at the pad or when an input buffer provides input from the pad to the PLC array. In the test mode, the BSC executes a boundary-scan operation, such as shifting in scan data from an upstream BSC in the BSR, providing test stimuli to the pad, capturing test data at the pad, etc.

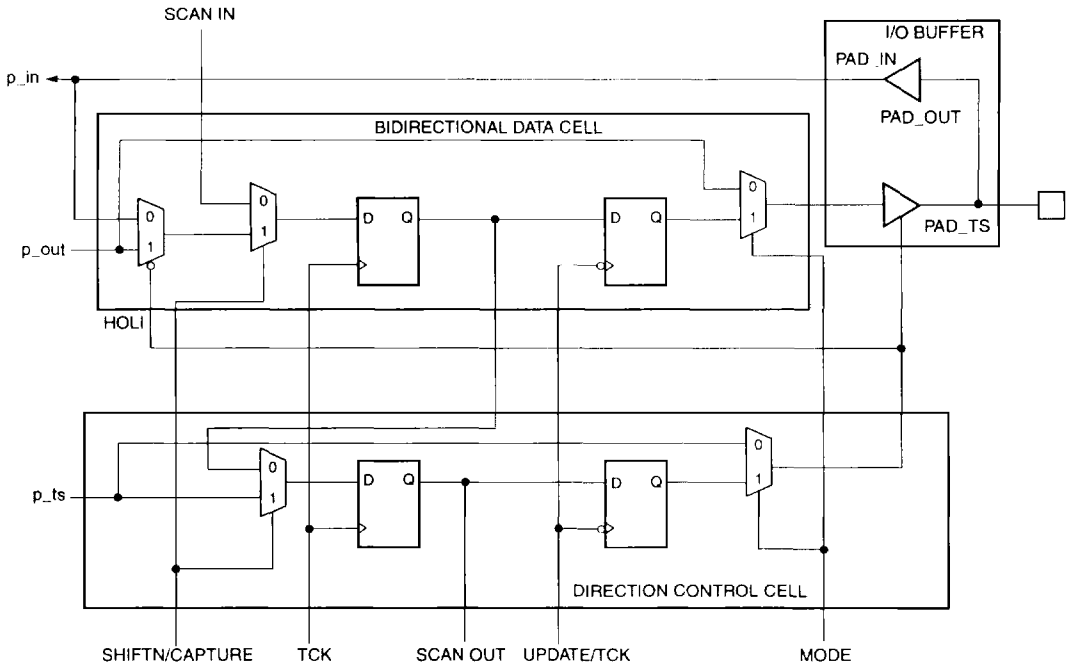
The primary functions of the BSC are shifting scan data serially in the BSR and observing input (p_in), output (p_out), and 3-state (p_ts) signals at the pads. The BSC consists of two circuits: the bidirectional data cell is used to access the input and output data, and the

direction control cell is used to access the 3-state value. Both cells consist of a flip-flop used to shift scan data which feeds a flip-flop to control the I/O buffer. The bidirectional data cell is connected serially to the direction control cell to form a boundary-scan shift register.

The TAPC signals (capture, update, shiftn, treset, and TCK) and the MODE signal control the operation of the BSC. The bidirectional data cell is also controlled by the high out/low in (HOLI) signal generated by the direction control cell. When HOLI is low, the bidirectional data cell receives input buffer data into the BSC. When HOLI is high, the BSC is loaded with functional data from the PLC.

The MODE signal is generated from the decode of the instruction register. When the MODE signal is high (EXTEST), the scan data is propagated to the output buffer. When the MODE signal is low (BYPASS or SAMPLE), functional data from the FPGA's internal logic is propagated to the output buffer.

The boundary-scan description language (BSDL) is provided for each device in the ORCA series of FPGAs. The BSDL is generated from a device profile, pinout, and other boundary-scan information.



5-2844(F)

Figure 46. Boundary-Scan Cell

Boundary Scan (continued)

2

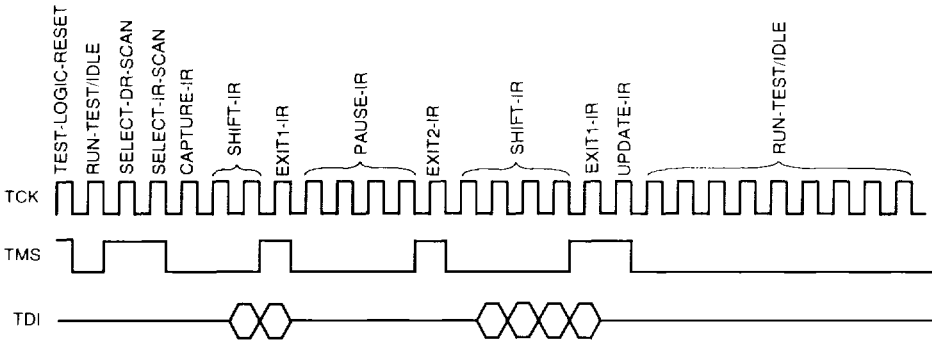


Fig 5.3(C)

Figure 47. Instruction Register Scan Timing Diagram

Boundary-Scan Timing

To ensure race-free operation, data changes on specific clock edges. The TMS and TDI inputs are clocked in on the rising edge of TCK, while changes on TDO occur on the falling edge of TCK. In the execution of an EXTEST instruction, parallel data is output from the BSR to the FPGA pads on the falling edge of TCK. The maximum frequency allowed for TCK is 10 MHz.

Figure 47 shows timing waveforms for an instruction scan operation. The diagram shows the use of TMS to sequence the TAPC through states. The test host (or BSM) changes data on the falling edge of TCK, and it is clocked into the DUT on the rising edge.

ORCA Timing Characteristics

To define speed grades, the ORCA Series part number designation (see Table 45) uses a single-digit number to designate a speed grade. This number is not related to any single ac parameter. Higher numbers indicate a faster set of timing parameters. The actual speed sorting is based on testing the delay in a path consisting of an input buffer, combinatorial delay through all PLCs in a row, and an output buffer. Other tests are then done to verify other delay parameters, such as routing delays, setup times to FFs, etc.

The most accurate timing characteristics are reported by the timing analyzer in the ORCA Foundry Development System. A timing report provided by the development system after layout divides path delays into logic and routing delays. The timing analyzer can also provide logic delays prior to layout. While this allows routing budget estimates, there is wide variance in routing delays associated with different layouts.

The logic timing parameters noted in the Electrical Characteristics section of this data sheet are the same as those in the design tools. In the PFU timing given in Table 30, symbol names are generally a concatenation of the PFU operating mode (as defined in Table 2) and the parameter type. The wildcard character (*) is used in symbol names to indicate that the parameter applies to any sub-LUT. The setup, hold, and propagation delay parameters, defined below, are designated in the symbol name by the SET, HLD, and DEL characters, respectively.

ORCA Timing Characteristics

(continued)

The values given for the parameters are the same as those used during production testing and speed binning of the devices. The junction temperature and supply voltage used to characterize the devices are listed in the delay tables. Actual delays at nominal temperature and voltage for best-case processes can be much better than the values given.

Table 12 and Table 13 provide approximate power supply and junction temperature derating for commercial and industrial devices. The delay values in this data sheet and reported by ORCA Foundry are shown as **1.00** in the tables. The method for determining the maximum junction temperature is defined in the Thermal Characteristics section. Taken cumulatively, the range of parameter values for best-case vs. worst-case processing, supply voltage, and junction temperature can approach 3 to 1.

Table 12. Derating for Commercial Devices

| T _J (°C) | Power Supply Voltage | | |
|------------------------|----------------------|-------|--------|
| | 4.75 V | 5.0 V | 5.25 V |
| 0 | 0.79 | 0.77 | 0.75 |
| 25 | 0.83 | 0.81 | 0.79 |
| 85 | 1.00 | 0.97 | 0.95 |
| 100 | 1.05 | 1.03 | 1.00 |
| 125 | 1.14 | 1.11 | 1.08 |

Table 13. Derating for Industrial Devices

| T _J (°C) | Power Supply Voltage | | | | |
|------------------------|----------------------|--------|-------|--------|-------|
| | 4.5 V | 4.75 V | 5.0 V | 5.25 V | 5.5 V |
| -40 | 0.70 | 0.69 | 0.67 | 0.65 | 0.64 |
| 0 | 0.79 | 0.77 | 0.75 | 0.73 | 0.72 |
| 25 | 0.83 | 0.81 | 0.79 | 0.77 | 0.76 |
| 85 | 1.00 | 0.97 | 0.95 | 0.92 | 0.91 |
| 100 | 1.05 | 1.02 | 1.00 | 0.97 | 0.95 |
| 125 | 1.14 | 1.11 | 1.08 | 1.05 | 1.03 |

In addition to supply voltage, process variation, and operating temperature, circuit and process improvements of the ORCA series FPGAs over time will result in significant improvement of the actual performance over those listed for a speed grade. Even though lower speed grades may still be available, the distribution of yield to timing parameters may be several speed bins higher than that designated on a product brand. Design practices need to consider best-case timing parameters (e.g., delays = 0), as well as worst-case timing.

The routing delays are a function of fan-out and the capacitance associated with the CIPs and metal interconnect in the path. The number of logic elements that can be driven (or fan-out) by PFUs is unlimited, although the delay to reach a valid logic level can exceed timing requirements. It is difficult to make accurate routing delay estimates prior to design compilation based on fan-out. This is because the CAE software may delete redundant logic inserted by the designer to reduce fan-out, and/or it may also automatically reduce fan-out by net splitting.

The waveform test points are given in the Measurement Conditions section of this data sheet. The timing parameters given in the electrical characteristics tables in this data sheet follow industry practices, and the values they reflect are described below.

Propagation Delay — the time between the specified reference points. The delays provided are the worst case of the t_{phh} and t_{pll} delays for noninverting functions, t_{plh} and t_{phl} for inverting functions, and t_{phz} and t_{plz} for 3-state enable.

Setup Time — the interval immediately preceding the transition of a clock or latch enable signal, during which the data must be stable to ensure it is recognized as the intended value.

Hold Time — the interval immediately following the transition of a clock or latch enable signal, during which the data must be held stable to ensure it is recognized as the intended value.

3-state Enable — the time from when a ts[3:0] signal becomes active and the output pad reaches the high-impedance state.

Estimating Power Dissipation

The total operating power dissipated is estimated by summing the standby (IDD5B), internal, and external power dissipated. The internal and external power is the power consumed in the PLCs and PICs, respectively. In general, the standby power is small and may be neglected. The total operating power is as follows:

$$P_T = \Sigma P_{PLC} + \Sigma P_{PIC}$$

The internal operating power is made up of two parts: clock generation and PFU output power. The PFU output power can be estimated based upon the number of PFU outputs switching when driving an average fan-out of two:

$$P_{PFU} = 0.19 \text{ mW/MHz}$$

For each PFU output that switches, 0.19 mW/MHz needs to be multiplied times the frequency (in MHz) that the output switches. Generally, this can be estimated by using one-half the clock rate, multiplied by some activity factor; for example, 20%.

The power dissipated by the clock generation circuitry is based upon three parts: the fixed clock power, the power/clock branch row or column, and the clock power dissipated in each PFU that uses this particular clock. Therefore, the clock power can be calculated for the three parts using the following equations:

2C04 Clock Power

$$P = [0.64 \text{ mW/MHz} + (0.22 \text{ mW/MHz} - \text{Branch}) (\# \text{ Branches}) + (0.025 \text{ mW/MHz} - \text{PFU}) (\# \text{ PFUs})] f_{CLK}$$

For a quick estimate, the worst-case (typical circuit) 2C04 Clock Power \approx 4.1 mW/MHz.

2C06 Clock Power

$$P = [0.65 \text{ mW/MHz} + (0.26 \text{ mW/MHz} - \text{Branch}) (\# \text{ Branches}) + (0.025 \text{ mW/MHz} - \text{PFU}) (\# \text{ PFUs})] f_{CLK}$$

For a quick estimate, the worst-case (typical circuit) 2C06 Clock Power \approx 5.6 mW/MHz.

2C08 Clock Power

$$P = [0.66 \text{ mW/MHz} + (0.29 \text{ mW/MHz} - \text{Branch}) (\# \text{ Branches}) + (0.025 \text{ mW/MHz} - \text{PFU}) (\# \text{ PFUs})] f_{CLK}$$

For a quick estimate, the worst-case (typical circuit) 2C08 Clock Power \approx 7.2 mW/MHz.

2C10 Clock Power

$$P = [0.67 \text{ mW/MHz} + (0.33 \text{ mW/MHz} - \text{Branch}) (\# \text{ Branches}) + (0.025 \text{ mW/MHz} - \text{PFU}) (\# \text{ PFUs})] f_{CLK}$$

For a quick estimate, the worst-case (typical circuit) 2C10 Clock Power \approx 9.2 mW/MHz.

2C12 Clock Power

$$P = [0.69 \text{ mW/MHz} + (0.37 \text{ mW/MHz} - \text{Branch}) (\# \text{ Branches}) + (0.025 \text{ mW/MHz} - \text{PFU}) (\# \text{ PFUs})] f_{CLK}$$

For a quick estimate, the worst-case (typical circuit) 2C12 Clock Power \approx 11.4 mW/MHz.

2C15 Clock Power

$$P = [0.70 \text{ mW/MHz} + (0.40 \text{ mW/MHz} - \text{Branch}) (\# \text{ Branches}) + (0.025 \text{ mW/MHz} - \text{PFU}) (\# \text{ PFUs})] f_{CLK}$$

For a quick estimate, the worst-case (typical circuit) 2C15 Clock Power \approx 13.7 mW/MHz.

2C26 Clock Power

$$P = [0.71 \text{ mW/MHz} + (0.47 \text{ mW/MHz} - \text{Branch}) (\# \text{ Branches}) + (0.025 \text{ mW/MHz} - \text{PFU}) (\# \text{ PFUs})] f_{CLK}$$

For a quick estimate, the worst-case (typical circuit) 2C26 Clock Power \approx 19.2 mW/MHz.

2C40 Clock Power

$$P = [0.75 \text{ mW/MHz} + (0.57 \text{ mW/MHz} - \text{Branch}) (\# \text{ Branches}) + (0.025 \text{ mW/MHz} - \text{PFU}) (\# \text{ PFUs})] f_{CLK}$$

For a quick estimate, the worst-case (typical circuit) 2C40 Clock Power \approx 29.1 mW/MHz.

The power dissipated in a PIC is the sum of the power dissipated in the four I/Os in the PIC. This consists of power dissipated by inputs and ac power dissipated by outputs. The power dissipated in each I/O depends on whether it is configured as an input, output, or input/output. If an I/O is operating as an output, then there is a power dissipation component for P_{IN}, as well as P_{OUT}. This is because the output feeds back to the input.

Estimating Power Dissipation

(continued)

The power dissipated by a TTL input buffer is estimated as:

$$P_{TTL} = 1.8 \text{ mW} + 0.20 \text{ mW/MHz}$$

The power dissipated by a CMOS input buffer is estimated as:

$$P_{CMOS} = 0.20 \text{ mW/MHz}$$

The ac power dissipation from an output or bidirectional is estimated by the following:

$$P_{OUT} = (C_L + 9 \text{ pF}) \times V_{DD}^2 \times F \text{ Watts}$$

where the unit for C_L is farads, and the unit for F is Hz.

As an example of estimating power dissipation, suppose that a fully utilized 2C15 has an average of three outputs for each of the 400 PFUs, that all 20 clock branches are used, that 150 of the 400 PFUs have FFs clocked at 40 MHz, and that the PFU outputs have an average activity factor of 20%.

Twenty TTL-configured inputs, 20 CMOS-configured inputs, 32 outputs driving 30 pF loads, and 16 bidirectional I/Os driving 50 pF loads are also generated from the 40 MHz clock with an average activity factor of 20%. The worst-case power dissipation is estimated as follows:

$$\begin{aligned} P_{PFU} &= 400 \times 3 (0.19 \text{ mW/MHz} \times 20 \text{ MHz} \times 20\%) \\ &= 912 \text{ mW} \end{aligned}$$

$$\begin{aligned} P_{CLK} &= [0.70 \text{ mW/MHz} + (0.40 \text{ mW/MHz} - \text{Branch}) \\ &\quad (20 \text{ Branches}) \\ &\quad + (0.025 \text{ mW/MHz} - \text{PFU}) (150 \text{ PFUs}) [40 \text{ MHz}]] \\ &= 498 \text{ mW} \end{aligned}$$

$$\begin{aligned} P_{TTL} &= 20 \times [1.8 \text{ mW} + (0.20 \text{ mW/MHz} \times 20 \text{ MHz} \times \\ &\quad 20\%)] \\ &= 52 \text{ mW} \end{aligned}$$

$$\begin{aligned} P_{CMOS} &= 20 \times [0.20 \text{ mW} \times 20 \text{ MHz} \times 20\%] \\ &= 16 \text{ mW} \end{aligned}$$

$$\begin{aligned} P_{OUT} &= 30 \times [(30 \text{ pF} + 9 \text{ pF}) \times 5.5252 \times 20 \text{ MHz} \times 20\%] \\ &= 129 \text{ mW} \end{aligned}$$

$$\begin{aligned} P_{BID} &= 16 \times [(50 \text{ pF} + 9 \text{ pF}) \times 5.5252 \times 20 \text{ MHz} \times 20\%] \\ &= 104 \text{ mW} \end{aligned}$$

$$TOTAL = 1.71 \text{ W}$$

Pin Information

Table 14. Pin Descriptions

| Symbol | I/O | Description |
|-----------------------------|-----|---|
| Dedicated Pins | | |
| VDD | — | Positive power supply. |
| GND | — | Ground supply. |
| RESET | I | During configuration, RESET forces the restart of configuration and a pull-up is enabled. After configuration, RESET can be used as a general FPGA input or as a direct input, which causes all PLC latches/FFs to be asynchronously set/reset. |
| CCLK | I | In the master and asynchronous peripheral modes, CCLK is an output which strobes configuration data in. In the slave or synchronous peripheral mode, CCLK is input synchronous with the data on DIN or D[7:0]. |
| DONE | I/O | DONE is a bidirectional pin with an optional pull-up resistor. As an active-low, open-drain output, it indicates that configuration is complete. As an input, a low level on DONE delays FPGA start-up after configuration. |
| PRGM | I | PRGM is an active-low input that forces the restart of configuration and resets the boundary-scan circuitry. This pin always has an active pull-up. |
| RD_CFGN | I | If readback is enabled, after configuration, a high-to-low transition on RD_CFGN initiates a readback of configuration data, including PFU output states, starting with frame address 0. During configuration, this is an active-low input that activates the TS_ALL function and 3-states all the I/O. This same functionality can be selected after configuration as well. This pin always has an active pull-up. |
| RD_DATA/TDO | O | RD_DATA/TDO is a dual-function pin. If used for readback, RD_DATA provides configuration data out. If used in boundary scan, TDO is test data out. |
| Special-Purpose Pins | | |
| RDY/BUSY | O | During configuration in peripheral mode, RDY/BUSY indicates another byte can be written to the FPGA. If a read operation is done when the device is selected, the same status is also available on D7 in asynchronous peripheral mode. After configuration, the pin is a user-programmable I/O. |
| RCLK | O | During the master parallel configuration mode, RCLK is a read output signal to an external memory. This output is not normally used. After configuration, this pin is a user-programmable I/O pin. |
| DIN | I | During slave serial or master serial configuration modes, DIN accepts serial configuration data synchronous with CCLK. During parallel configuration modes, DIN is the D0 input. During configuration, a pull-up is enabled, and after configuration, this pin is a user-programmable I/O pin. |
| M0, M1, M2 | I | M0—M2 are used to select the configuration mode. See Table 8 for the configuration modes. During configuration, a pull-up is enabled, and after configuration, the pins are user-programmable I/O. |
| M3 | I | M3 is used to select the speed of the internal oscillator during configuration. When M3 is low, the oscillator frequency is 10 MHz. When M3 is high, the oscillator is 1.25 MHz. During configuration, a pull-up is enabled, and after configuration, this pin is a user-programmable I/O pin. |

Pin Information (continued)

Table 14. Pin Descriptions (continued)

| Symbol | I/O | Description |
|------------------|-----|---|
| TDI, TCK, TMS | I | If boundary scan is used, these pins are Test Data In, Test Clock, and Test Mode Select inputs. If boundary scan is not selected, all boundary-scan functions are inhibited once configuration is complete, and these pins are user-programmable I/O pins. Even if boundary scan is not used, either TCK or TMS must be held at logic 1 during configuration. Each pin has a pull-up enabled during configuration. |
| HDC | O | High During Configuration is output high until configuration is complete. It is used as a control output indicating that configuration is not complete. After configuration, this pin is a user-programmable I/O pin. |
| LDC | O | Low During Configuration is output low until configuration is complete. It is used as a control output indicating that configuration is not complete. After configuration, this pin is a user-programmable I/O pin. |
| INIT | I/O | INIT is a bidirectional signal before and during configuration. During configuration, a pull-up is enabled, but an external pull-up resistor is recommended. As an active-low open-drain output, INIT is held low during power stabilization and internal clearing of memory. As an active-low input, INIT holds the FPGA in the wait-state before the start of configuration. After configuration, the pin is a user-programmable I/O pin. |
| CS0, CS1, WR, RD | I | CS0, CS1, WR, RD are used in the asynchronous peripheral configuration modes. The FPGA is selected when CS0 is low and CS1 is high. When selected, a low on the write strobe, WR, loads the data on D[7:0] inputs into an internal data buffer. WR, CS0, and CS1 are also used as chip selects in the slave parallel mode. A low on RD changes D7 into a status output. As a status indication, a high indicates ready and a low indicates busy. WR and RD should not be used simultaneously. If they are, the write strobe overrides. During configuration, a pull-up is enabled, and after configuration, the pins are user-programmable I/O pins. |
| A[17:0] | O | During master parallel configuration mode, A[17:0] address the configuration EPROM. During configuration, a pull-up is enabled, and after configuration, the pins are user-programmable I/O pins. |
| D[7:0] | I | During master parallel, peripheral, and slave parallel configuration modes, D[7:0] receive configuration data and each pin has a pull-up enabled. After configuration, the pins are user-programmable I/O pins. |
| DOUT | O | During configuration, DOUT is the serial data output that can drive the DIN of daisy-chained slave LCA devices. Data out on DOUT changes on the falling edge of CCLK. After configuration, DOUT is a user-programmable I/O pin. |

Pin Information (continued)**Package Compatibility**

The package pinouts are consistent across ORCA Series FPGAs. This allows a designer to select a package based on I/O requirements and change the FPGA without relaying out the printed-circuit board. The change might be to a larger FPGA, if additional functionality is needed, or a smaller FPGA to decrease unit cost.

Table 15 provides the number of user I/Os available for Lucent ORCA Series FPGAs for each available package. Each package has six dedicated configuration pins.

Tables 16—25 provide the package pin and pin function for the ORCA 2C Series FPGAs and packages. The bond pad name is identified in the PIC nomenclature used in the ORCA Foundry design editor.

When the number of FPGA bond pads exceeds the number of package pins, bond pads are unused. When the number of package pins exceeds the number of bond pads, package pins are left unconnected (no connects).

For each package in the 2C Series, Tables 16—25 provide package pin functionality and the bond pad connection. When a package pin is to be left as a no connect for a specific die, it is indicated as a note in the bond pad column for the FPGA. The tables provide no information on unused pads.

Table 15. ORCA 2C Series FPGA I/Os Summary

| Device | 84-Pin PLCC | 100-Pin TQFP | 144-Pin TQFP | 160-Pin MQFP | 208-Pin SQFP/ SQFP- PQ2 | 240-Pin SQFP/ SQFP- PQ2 | 256-Pin PBGA | 304-Pin SQFP/ SQFP- PQ2 | 364- Pin CPGA | 428-Pin CPGA |
|----------------|----------------|-----------------|-----------------|-----------------|----------------------------------|----------------------------------|-----------------|----------------------------------|---------------------|-----------------|
| ATT2C04 | | | | | | | | | | |
| User I/Os | 64 | 77 | 114 | 130 | 160 | — | — | — | — | — |
| VDD/VSS | 14 | 17 | 24 | 24 | 31 | — | — | — | — | — |
| ATT2C06 | | | | | | | | | | |
| User I/Os | 64 | 77 | 114 | 130 | 171 | 192 | — | — | — | — |
| VDD/VSS | 14 | 17 | 24 | 24 | 31 | 42 | — | — | — | — |
| ATT2C08 | | | | | | | | | | |
| User I/Os | 64 | — | — | 130 | 171 | 192 | 221 | 224 | — | — |
| VDD/VSS | 14 | — | — | 24 | 31 | 40 | 27 | 46 | — | — |
| ATT2C10 | | | | | | | | | | |
| User I/Os | 64 | — | — | 130 | 171 | 192 | 223 | 252 | — | — |
| VDD/VSS | 14 | — | — | 24 | 31 | 40 | 27 | 46 | — | — |
| ATT2C12 | | | | | | | | | | |
| User I/Os | — | — | — | — | 171 | 192 | 223 | 252 | 288 | — |
| VDD/VSS | — | — | — | — | 31 | 42 | 27 | 46 | 38 | — |
| ATT2C15 | | | | | | | | | | |
| User I/Os | — | — | — | — | 171 | 192 | — | 252 | 320 | — |
| VDD/VSS | — | — | — | — | 31 | 42 | — | 46 | 38 | — |
| ATT2C26 | | | | | | | | | | |
| User I/Os | — | — | — | — | 171 | 192 | — | 252 | — | 384 |
| VDD/VSS | — | — | — | — | 31 | 42 | — | 46 | — | 38 |
| ATT2C40 | | | | | | | | | | |
| User I/Os | — | — | — | — | 171 | 192 | — | 252 | — | 384 |
| VDD/VSS | — | — | — | — | 31 | 42 | — | 46 | — | 38 |

Pin Information (continued)

Table 16. ATT2C04, ATT2C06, ATT2C08, and ATT2C10 84-Pin PLCC Pinout

| Pin | 2C04 Pad | 2C06 Pad | 2C08 Pad | 2C10 Pad | Function | Pin | 2C04 Pad | 2C06 Pad | 2C08 Pad | 2C10 Pad | Function |
|-----|--------------|--------------|--------------|--------------|--------------|-----|----------|----------|----------|----------|--------------|
| 1 | VSS | VSS | VSS | VSS | VSS | 43 | VSS | VSS | VSS | VSS | VSS |
| 2 | PT5A | PT6A | PT7A | PT8A | I/O-D2 | 44 | PB6A | PB7A | PB8A | PB9A | I/O |
| 3 | VSS | VSS | VSS | VSS | VSS | 45 | VSS | VSS | VSS | VSS | VSS |
| 4 | PT4D | PT5D | PT6D | PT7D | I/O-D1 | 46 | PB7A | PB8A | PB9A | PB10A | I/O |
| 5 | PT4A | PT5A | PT6A | PT7A | I/O-D0/DIN | 47 | PB7D | PB8D | PB9D | PB10D | I/O |
| 6 | PT3A | PT4A | PT5A | PT6A | I/O-DOOUT | 48 | PB8A | PB9A | PB10A | PB11A | I/O-HDC |
| 7 | PT2D | PT3D | PT4D | PT5D | I/O | 49 | PB9A | PB10A | PB11A | PB12A | I/O-LDC |
| 8 | PT2A | PT3A | PT4A | PT4A | I/O-TDI | 50 | PB9D | PB10D | PB11D | PB13A | I/O |
| 9 | PT1D | PT2A | PT3A | PT3A | I/O-TMS | 51 | PB10A | PB11A | PB12C | PB13D | I/O-INIT |
| 10 | PT1A | PT1A | PT1A | PT1A | I/O-TCK | 52 | PB10D | PB12A | PB13D | PB15D | I/O |
| 11 | RD_DATA /TDO | RD_DATA /TDO | RD_DATA /TDO | RD_DATA /TDO | RD_DATA /TDO | 53 | DONE | DONE | DONE | DONE | DONE |
| 12 | VDD | VDD | VDD | VDD | VDD | 54 | RESET | RESET | RESET | RESET | RESET |
| 13 | VSS | VSS | VSS | VSS | VSS | 55 | PRGM | PRGM | PRGM | PRGM | PRGM |
| 14 | PL1C | PL1A | PL2D | PL2D | I/O-A0 | 56 | PR10A | PR12A | PR14A | PR16A | I/O-M0 |
| 15 | PL1A | PL2A | PL3A | PL3A | I/O-A1 | 57 | PR10D | PR11A | PR12A | PR14A | I/O |
| 16 | PL2D | PL3D | PL4D | PL4A | I/O-A2 | 58 | PR9A | PR10A | PR11A | PR13B | I/O-M1 |
| 17 | PL2A | PL3A | PL4A | PL5A | I/O-A3 | 59 | PR9D | PR10D | PR11D | PR12B | I/O |
| 18 | PL3A | PL4A | PL5A | PL6A | I/O-A4 | 60 | PR8A | PR9A | PR10A | PR11A | I/O-M2 |
| 19 | PL4D | PL5D | PL6D | PL7D | I/O-A5 | 61 | PR7A | PR8A | PR9A | PR10A | I/O-M3 |
| 20 | PL4A | PL5A | PL6A | PL7A | I/O-A6 | 62 | PR7D | PR8D | PR9D | PR10D | I/O |
| 21 | PL5A | PL6A | PL7A | PL8A | I/O-A7 | 63 | PR6A | PR7A | PR8D | PR9D | I/O |
| 22 | VDD | VDD | VDD | VDD | VDD | 64 | VDD | VDD | VDD | VDD | VDD |
| 23 | PL6A | PL7A | PL8A | PL9A | I/O-A8 | 65 | PR5A | PR6A | PR7A | PR8A | I/O |
| 24 | VSS | VSS | VSS | VSS | VSS | 66 | VSS | VSS | VSS | VSS | VSS |
| 25 | PL7D | PL8D | PL9D | PL10D | I/O-A9 | 67 | PR4A | PR5A | PR6A | PR7A | I/O |
| 26 | PL7A | PL8A | PL9A | PL10A | I/O-A10 | 68 | PR4D | PR5D | PR6D | PR7D | I/O |
| 27 | PL8A | PL9A | PL10A | PL11A | I/O-A11 | 69 | PR3A | PR4A | PR5A | PR6A | I/O-CS1 |
| 28 | PL9D | PL10D | PL11D | PL12D | I/O-A12 | 70 | PR2A | PR3A | PR4A | PR5A | I/O-CS0 |
| 29 | PL9A | PL10A | PL11A | PL13D | I/O-A13 | 71 | PR2D | PR3D | PR4D | PR4D | I/O |
| 30 | PL10D | PL11A | PL12A | PL14C | I/O-A14 | 72 | PR1A | PR2A | PR3A | PR3A | I/O-RD |
| 31 | PL10A | PL12A | PL14A | PL16A | I/O-A15 | 73 | PR1D | PR1A | PR2A | PR2A | I/O-WR |
| 32 | CCLK | CCLK | CCLK | CCLK | CCLK | 74 | RD_CFGN | RD_CFGN | RD_CFGN | RD_CFGN | RD_CFGN |
| 33 | VDD | VDD | VDD | VDD | VDD | 75 | VDD | VDD | VDD | VDD | VDD |
| 34 | VSS | VSS | VSS | VSS | VSS | 76 | VSS | VSS | VSS | VSS | VSS |
| 35 | PB1A | PB1A | PB1A | PB1A | I/O-A16 | 77 | PT10C | PT12A | PT13D | PT15D | I/O-RDY/RCLK |
| 36 | PB1D | PB2A | PB3A | PB3B | I/O-A17 | 78 | PT9D | PT11A | PT12C | PT13D | I/O-D7 |
| 37 | PB2A | PB3A | PB3D | PB4D | I/O | 79 | PT9C | PT10D | PT11D | PT13A | I/O |
| 38 | PB2D | PB3D | PB4D | PB5D | I/O | 80 | PT9A | PT10A | PT11B | PT12B | I/O-D6 |
| 39 | PB3A | PB4A | PB5A | PB6A | I/O | 81 | PT8A | PT9A | PT10A | PT11A | I/O-D5 |
| 40 | PB4A | PB5A | PB6A | PB7A | I/O | 82 | PT7D | PT8D | PT9D | PT10D | I/O |
| 41 | PB4D | PB5D | PB6D | PB7D | I/O | 83 | PT7A | PT8A | PT9A | PT10A | I/O-D4 |
| 42 | PB5A | PB6A | PB7A | PB8A | I/O | 84 | PT6A | PT7A | PT8A | PT9A | I/O-D3 |

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Pin Information (continued)

Table 17. ATT2C04 and ATT2C06 100-Pin TQFP Pinout

| Pin | 2C04 Pad | 2C06 Pad | Function | Pin | 2C04 Pad | 2C06 Pad | Function |
|-----|----------|----------|----------|-----|----------|----------|--------------|
| 1 | VDD | VDD | VDD | 43 | PB8C | PB9C | I/O |
| 2 | VSS | VSS | VSS | 44 | PB8D | PB9D | I/O |
| 3 | PL1C | PL1A | I/O-A0 | 45 | PB9A | PB10A | I/O-LDC |
| 4 | PL1A | PL2A | I/O-A1 | 46 | PB9D | PB10D | I/O |
| 5 | PL2D | PL3D | I/O-A2 | 47 | PB10A | PB11A | I/O-INIT |
| 6 | PL2A | PL3A | I/O-A3 | 48 | PB10D | PB12A | I/O |
| 7 | PL3D | PL4D | I/O | 49 | DONE | DONE | DONE |
| 8 | PL3A | PL4A | I/O-A4 | 50 | VDD | VDD | VDD |
| 9 | PL4D | PL5D | I/O-A5 | 51 | RESET | RESET | RESET |
| 10 | PL4A | PL5A | I/O-A6 | 52 | PRGM | PRGM | PRGM |
| 11 | PL5D | PL6D | I/O | 53 | PR10A | PR12A | I/O-M0 |
| 12 | PL5A | PL6A | I/O-A7 | 54 | PR10D | PR11A | I/O |
| 13 | VDD | VDD | VDD | 55 | PR9A | PR10A | I/O-M1 |
| 14 | PL6A | PL7A | I/O-A8 | 56 | PR9D | PR10D | I/O |
| 15 | VSS | VSS | VSS | 57 | PR8A | PR9A | I/O-M2 |
| 16 | PL7D | PL8D | I/O-A9 | 58 | PR8D | PR9D | I/O |
| 17 | PL7A | PL8A | I/O-A10 | 59 | PR7A | PR8A | I/O-M3 |
| 18 | PL8A | PL9A | I/O-A11 | 60 | PR7D | PR8D | I/O |
| 19 | PL9D | PL10D | I/O-A12 | 61 | VSS | VSS | VSS |
| 20 | PL9C | PL10C | I/O | 62 | PR6A | PR7A | I/O |
| 21 | PL9A | PL10A | I/O-A13 | 63 | VDD | VDD | VDD |
| 22 | PL10D | PL11A | I/O-A14 | 64 | PR5A | PR6A | I/O |
| 23 | PL10A | PL12A | I/O-A15 | 65 | VSS | VSS | VSS |
| 24 | VSS | VSS | VSS | 66 | PR4A | PR5A | I/O |
| 25 | CCLK | CCLK | CCLK | 67 | PR4D | PR5D | I/O |
| 26 | VDD | VDD | VDD | 68 | PR3A | PR4A | I/O-CS1 |
| 27 | VSS | VSS | VSS | 69 | PR3D | PR4D | I/O |
| 28 | PB1A | PB1A | I/O-A16 | 70 | PR2A | PR3A | I/O-CS0 |
| 29 | PB1C | PB1D | I/O | 71 | PR2D | PR3D | I/O |
| 30 | PB1D | PB2A | I/O-A17 | 72 | PR1A | PR2A | I/O-RD |
| 31 | PB2A | PB3A | I/O | 73 | PR1C | PR2D | I/O |
| 32 | PB2D | PB3D | I/O | 74 | PR1D | PR1A | I/O-WF |
| 33 | PB3A | PB4A | I/O | 75 | RD_CFGN | RD_CFGN | RD_CFGN |
| 34 | PB4A | PB5A | I/O | 76 | VDD | VDD | VDD |
| 35 | PB4D | PB5D | I/O | 77 | VSS | VSS | VSS |
| 36 | PB5A | PB6A | I/O | 78 | PT10C | PT12A | I/O-RDY/RCLK |
| 37 | VSS | VSS | VSS | 79 | PT9D | PT11A | I/O-D7 |
| 38 | PB6A | PB7A | I/O | 80 | PT9C | PT10D | I/O |
| 39 | VSS | VSS | VSS | 81 | PT9A | PT10A | I/O-D6 |
| 40 | PB7A | PB8A | I/O | 82 | PT8D | PT9D | I/O |
| 41 | PB7D | PB8D | I/O | 83 | PT8A | PT9A | I/O-D5 |
| 42 | PB8A | PB9A | I/O-HDC | 84 | PT7D | PT8D | I/O |

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Pin Information (continued)**Table 17. ATT2C04 and ATT2C06 100-Pin TQFP Pinout** (continued)

| Pin | 2C04 Pad | 2C06 Pad | Function | Pin | 2C04 Pad | 2C06 Pad | Function |
|-----|----------|----------|------------|-----|-------------|-------------|-------------|
| 85 | PT7A | PT8A | I/O-D4 | 93 | PT3D | PT4D | I/O |
| 86 | PT6D | PT7D | I/O | 94 | PT3A | PT4A | I/O-DOUT |
| 87 | PT6A | PT7A | I/O-D3 | 95 | PT2D | PT3D | I/O |
| 88 | Vss | Vss | Vss | 96 | PT2A | PT3A | I/O-TDI |
| 89 | PT5A | PT6A | I/O-D2 | 97 | PT1D | PT2A | I/O-TMS |
| 90 | Vss | Vss | Vss | 98 | PT1C | PT1D | I/O |
| 91 | PT4D | PT5D | I/O-D1 | 99 | PT1A | PT1A | I/O-TCK |
| 92 | PT4A | PT5A | I/O-D0/DIN | 100 | RD_DATA/TDO | RD_DATA/TDO | RD_DATA/TDO |

Pin Information (continued)

Table 18. ATT2C04 and ATT2C06 144-Pin TQFP Pinout

| Pin | 2C04 Pad | 2C06 Pad | Function | Pin | 2C04 Pad | 2C06 Pad | Function |
|-----|----------|----------|----------|-----|----------|----------|----------|
| 1 | VDD | VDD | VDD | 43 | PB2B | PB3B | I/O |
| 2 | Vss | Vss | Vss | 44 | PB2D | PB3D | I/O |
| 3 | PL1C | PL1A | I/O-A0 | 45 | VDD | VDD | VDD |
| 4 | PL1B | PL2D | I/O | 46 | PB3A | PB4A | I/O |
| 5 | PL1A | PL2A | I/O-A1 | 47 | PB3D | PB4D | I/O |
| 6 | PL2D | PL3D | I/O-A2 | 48 | PB4A | PB5A | I/O |
| 7 | PL2A | PL3A | I/O-A3 | 49 | PB4C | PB5C | I/O |
| 8 | PL3D | PL4D | I/O | 50 | PB4D | PB5D | I/O |
| 9 | PL3C | PL4C | I/O | 51 | PB5A | PB6A | I/O |
| 10 | PL3A | PL4A | I/O-A4 | 52 | PB5C | PB6C | I/O |
| 11 | PL4D | PL5D | I/O-A5 | 53 | PB5D | PB6D | I/O |
| 12 | PB4C | PB5C | I/O | 54 | Vss | Vss | Vss |
| 13 | PL4A | PL5A | I/O-A6 | 55 | PB6A | PB7A | I/O |
| 14 | Vss | Vss | Vss | 56 | PB6C | PB7C | I/O |
| 15 | PL5D | PL6D | I/O | 57 | PB6D | PB7D | I/O |
| 16 | PL5C | PL6C | I/O | 58 | PB7A | PB8A | I/O |
| 17 | PL5A | PL6A | I/O-A7 | 59 | PB7D | PB8D | I/O |
| 18 | VDD | VDD | VDD | 60 | PB8A | PB9A | I/O-HDC |
| 19 | PL6D | PL7D | I/O | 61 | PB8C | PB9C | I/O |
| 20 | PL6C | PL7C | I/O | 62 | PB8D | PB9D | I/O |
| 21 | PL6A | PL7A | I/O-A8 | 63 | VDD | VDD | VDD |
| 22 | Vss | Vss | Vss | 64 | PB9A | PB10A | I/O-LDC |
| 23 | PL7D | PL8D | I/O-A9 | 65 | PB9C | PB10C | I/O |
| 24 | PL7A | PL8A | I/O-A10 | 66 | PB9D | PB10D | I/O |
| 25 | PL8D | PL9D | I/O | 67 | PB10A | PB11A | I/O-INIT |
| 26 | PL8C | PL9C | I/O | 68 | PB10C | PB11D | I/O |
| 27 | PL8A | PL9A | I/O-A11 | 69 | PB10D | PB12A | I/O |
| 28 | PL9D | PL10D | I/O-A12 | 70 | Vss | Vss | Vss |
| 29 | PB9C | PB10C | I/O | 71 | DONE | DONE | DONE |
| 30 | PL9A | PL10A | I/O-A13 | 72 | VDD | VDD | VDD |
| 31 | PL10D | PL11A | I/O-A14 | 73 | Vss | Vss | Vss |
| 32 | PL10C | PL12D | I/O | 74 | RESET | RESET | RESET |
| 33 | PL10B | PL12B | I/O | 75 | PRGM | PRGM | PRGM |
| 34 | PL10A | PL12A | I/O-A15 | 76 | PR10A | PR12A | I/O-M0 |
| 35 | Vss | Vss | Vss | 77 | PR10B | PR12D | I/O |
| 36 | CCLK | CCLK | CCLK | 78 | PR10D | PR11A | I/O |
| 37 | VDD | VDD | VDD | 79 | PR9A | PR10A | I/O-M1 |
| 38 | Vss | Vss | Vss | 80 | PR9C | PR10C | I/O |
| 39 | PB1A | PB1A | I/O-A16 | 81 | PR9D | PR10D | I/O |
| 40 | PB1C | PB1D | I/O | 82 | PR8A | PR9A | I/O-M2 |
| 41 | PB1D | PB2A | I/O-A17 | 83 | PR8B | PR9B | I/O |
| 42 | PB2A | PB3A | I/O | 84 | PR8D | PR9D | I/O |

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Pin Information (continued)

Table 18. ATT2C04 and ATT2C06 144-Pin TQFP Pinout (continued)

| Pin | 2C04 Pad | 2C06 Pad | Function | Pin | 2C04 Pad | 2C06 Pad | Function |
|-----|----------|----------|--------------|-----|-----------------|-----------------|-------------|
| 85 | PR7A | PR8A | I/O-M3 | 115 | PT9C | PT10D | I/O |
| 86 | PR7D | PR8D | I/O | 116 | PT9B | PT10C | I/O |
| 87 | Vss | Vss | Vss | 117 | PT9A | PT10A | I/O-D6 |
| 88 | PR6A | PR7A | I/O | 118 | Vdd | Vdd | Vdd |
| 89 | PR6C | PR7C | I/O | 119 | PT8D | PT9D | I/O |
| 90 | PR6D | PR7D | I/O | 120 | PT8A | PT9A | I/O-D5 |
| 91 | Vdd | Vdd | Vdd | 121 | PT7D | PT8D | I/O |
| 92 | PR5A | PR6A | I/O | 122 | PT7B | PT8B | I/O |
| 93 | PR5C | PR6C | I/O | 123 | PT7A | PT8A | I/O-D4 |
| 94 | PR5D | PR6D | I/O | 124 | PT6D | PT7D | I/O |
| 95 | Vss | Vss | Vss | 125 | PT6C | PT7C | I/O |
| 96 | PR4A | PR5A | I/O | 126 | PT6A | PT7A | I/O-D3 |
| 97 | PR4C | PR5C | I/O | 127 | Vss | Vss | Vss |
| 98 | PR4D | PR5D | I/O | 128 | PT5D | PT6D | I/O |
| 99 | PR3A | PR4A | I/O-CS1 | 129 | PT5C | PT6C | I/O |
| 100 | PR3D | PR4D | I/O | 130 | PT5A | PT6A | I/O-D2 |
| 101 | PR2A | PR3A | I/O-CS0 | 131 | PT4D | PT5D | I/O-D1 |
| 102 | PR2D | PR3D | I/O | 132 | PT4C | PT5C | I/O |
| 103 | PR1A | PR2A | I/O-RD | 133 | PT4A | PT5A | I/O-D0/DIN |
| 104 | PR1B | PR2B | I/O | 134 | PT3D | PT4D | I/O |
| 105 | PR1C | PR2D | I/O | 135 | PT3A | PT4A | I/O-DOUT |
| 106 | PR1D | PR1A | I/O-WR | 136 | Vdd | Vdd | Vdd |
| 107 | Vss | Vss | Vss | 137 | PT2D | PT3D | I/O |
| 108 | RD_CFGN | RD_CFGN | RD_CFGN | 138 | PT2C | PT3C | I/O |
| 109 | Vdd | Vdd | Vdd | 139 | PT2A | PT3A | I/O-TDI |
| 110 | Vss | Vss | Vss | 140 | PT1D | PT2A | I/O-TMS |
| 111 | PT10D | PT10D | I/O | 141 | PT1C | PT1D | I/O |
| 112 | PT10C | PT12A | I/O-RDY/RCLK | 142 | PT1A | PT1A | I/O-TCK |
| 113 | PT10B | PT11D | I/O | 143 | Vss | Vss | Vss |
| 114 | PT9D | PT11A | I/O-D7 | 144 | RD_DATA/ TDO | RD_DATA/ TDO | RD_DATA/TDO |

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Pin Information (continued)

Table 19. ATT2C04, ATT2C06, ATT2C08, and ATT2C10 160-Pin QFP Pinout

| Pin | 2C04 Pad | 2C06 Pad | 2C08 Pad | 2C10 Pad | Function |
|-----|----------|----------|----------|----------|----------|
| 1 | VDD | VDD | VDD | VDD | VDD |
| 2 | VSS | VSS | VSS | VSS | VSS |
| 3 | PL1D | PL1D | PL1D | PL1D | I/O |
| 4 | PL1C | PL1A | PL2D | PL2D | I/O-A0 |
| 5 | PL1B | PL2D | PL3D | PL3D | I/O |
| 6 | PL1A | PL2A | PL3A | PL3A | I/O-A1 |
| 7 | PL2D | PL3D | PL4D | PL4A | I/O-A2 |
| 8 | PL2C | PL3C | PL4C | PL5C | I/O |
| 9 | PL2A | PL3A | PL4A | PL5A | I/O-A3 |
| 10 | PL3D | PL4D | PL5D | PL6D | I/O |
| 11 | PL3C | PL4C | PL5C | PL6C | I/O |
| 12 | PL3A | PL4A | PL5A | PL6A | I/O-A4 |
| 13 | PL4D | PL5D | PL6D | PL7D | I/O-A5 |
| 14 | PL4C | PL5C | PL6C | PL7C | I/O |
| 15 | PL4A | PL5A | PL6A | PL7A | I/O-A6 |
| 16 | VSS | VSS | VSS | VSS | VSS |
| 17 | PL5D | PL6D | PL7D | PL8D | I/O |
| 18 | PL5C | PL6C | PL7C | PL8C | I/O |
| 19 | PL5A | PL6A | PL7A | PL8A | I/O-A7 |
| 20 | VDD | VDD | VDD | VDD | VDD |
| 21 | PL6D | PL7D | PL8D | PL9D | I/O |
| 22 | PL6C | PL7C | PL8C | PL9C | I/O |
| 23 | PL6A | PL7A | PL8A | PL9A | I/O-A8 |
| 24 | VSS | VSS | VSS | VSS | VSS |
| 25 | PL7D | PL8D | PL9D | PL10D | I/O-A9 |
| 26 | PL7B | PL8B | PL9B | PL10B | I/O |
| 27 | PL7A | PL8A | PL9A | PL10A | I/O-A10 |
| 28 | PL8D | PL9D | PL10D | PL11D | I/O |
| 29 | PL8C | PL9C | PL10C | PL11C | I/O |
| 30 | PL8A | PL9A | PL10A | PL11A | I/O-A11 |
| 31 | PL9D | PL10D | PL11D | PL12D | I/O-A12 |
| 32 | PL9C | PL10C | PL11C | PL12C | I/O |
| 33 | PL9B | PL10B | PL11B | PL12B | I/O |
| 34 | PL9A | PL10A | PL11A | PL13D | I/O-A13 |
| 35 | PL10D | PL11A | PL12A | PL14C | I/O-A14 |
| 36 | PL10C | PL12D | PL13D | PL15D | I/O |
| 37 | PL10B | PL12B | PL14D | PL16D | I/O |
| 38 | PL10A | PL12A | PL14A | PL16A | I/O-A15 |
| 39 | CCLK | CCLK | CCLK | CCLK | CCLK |
| 40 | VSS | VSS | VSS | VSS | VSS |
| 41 | VDD | VDD | VDD | VDD | VDD |
| 42 | VSS | VSS | VSS | VSS | VSS |
| 43 | PB1A | PB1A | PB1A | PB1A | I/O-A16 |

Pin Information (continued)

Table 19. ATT2C04, ATT2C06, ATT2C08, and ATT2C10 160-Pin QFP Pinout (continued)

| Pin | 2C04 Pad | 2C06 Pad | 2C08 Pad | 2C10 Pad | Function |
|-----|----------|----------|----------|----------|----------|
| 44 | PB1B | PB1C | PB2A | PB2A | I/O |
| 45 | PB1C | PB1D | PB2D | PB2D | I/O |
| 46 | PB1D | PB2A | PB3A | PB3B | I/O-A17 |
| 47 | PB2A | PB3A | PB3D | PB4D | I/O |
| 48 | PB2B | PB3B | PB4A | PB5A | I/O |
| 49 | PB2C | PB3C | PB4C | PB5C | I/O |
| 50 | PB2D | PB3D | PB4D | PB5D | I/O |
| 51 | VDD | VDD | VDD | VDD | VDD |
| 52 | PB3A | PB4A | PB5A | PB6A | I/O |
| 53 | PB3D | PB4D | PB5D | PB6D | I/O |
| 54 | PB4A | PB5A | PB6A | PB7A | I/O |
| 55 | PB4C | PB5C | PB6C | PB7C | I/O |
| 56 | PB4D | PB5D | PB6D | PB7D | I/O |
| 57 | PB5A | PB6A | PB7A | PB8A | I/O |
| 58 | PB5C | PB6C | PB7C | PB8C | I/O |
| 59 | PB5D | PB6D | PB7D | PB8D | I/O |
| 60 | VSS | VSS | VSS | VSS | VSS |
| 61 | PB6A | PB7A | PB8A | PB9A | I/O |
| 62 | PB6C | PB7C | PB8C | PB9C | I/O |
| 63 | PB6D | PB7D | PB8D | PB9D | I/O |
| 64 | PB7A | PB8A | PB9A | PB10A | I/O |
| 65 | PB7D | PB8D | PB9D | PB10D | I/O |
| 66 | PB8A | PB9A | PB10A | PB11A | I/O-HDC |
| 67 | PB8C | PB9C | PB10C | PB11C | I/O |
| 68 | PB8D | PB9D | PB10D | PB11D | I/O |
| 69 | VDD | VDD | VDD | VDD | VDD |
| 70 | PB9A | PB10A | PB11A | PB12A | I/O-LDC |
| 71 | PB9B | PB10B | PB11D | PB13A | I/O |
| 72 | PB9C | PB10C | PB12A | PB13B | I/O |
| 73 | PB9D | PB10D | PB12B | PB13C | I/O |
| 74 | PB10A | PB11A | PB12C | PB13D | I/O-INIT |
| 75 | PB10B | PB11C | PB12D | PB14A | I/O |
| 76 | PB10C | PB11D | PB13D | PB15D | I/O |
| 77 | PB10D | PB12A | PB14D | PB16D | I/O |
| 78 | VSS | VSS | VSS | VSS | VSS |
| 79 | DONE | DONE | DONE | DONE | DONE |
| 80 | VDD | VDD | VDD | VDD | VDD |
| 81 | VSS | VSS | VSS | VSS | VSS |
| 82 | RESET | RESET | RESET | RESET | RESET |
| 83 | PRGM | PRGM | PRGM | PRGM | PRGM |
| 84 | PR10A | PR12A | PR14A | PR16A | I/O-MO |
| 85 | PR10B | PR12D | PR13A | PR15A | I/O |

Pin Information (continued)

Table 19. ATT2C04, ATT2C06, ATT2C08, and ATT2C10 160-Pin QFP Pinout (continued)

| Pin | 2C04 Pad | 2C06 Pad | 2C08 Pad | 2C10 Pad | Function |
|-----|----------|----------|----------|----------|--------------|
| 86 | PR10C | PR11A | PR13D | PR15D | I/O |
| 87 | PR10D | PR11B | PR12A | PR14A | I/O |
| 88 | PR9A | PR10A | PR11A | PR13B | I/O-M1 |
| 89 | PR9B | PR10B | PR11B | PR13C | I/O |
| 90 | PR9C | PR10C | PR11C | PR12A | I/O |
| 91 | PR9D | PR10D | PR11D | PR12B | I/O |
| 92 | PR8A | PR9A | PR10A | PR11A | I/O-M2 |
| 93 | PR8B | PR9B | PR10B | PR11B | I/O |
| 94 | PR8D | PR9D | PR10D | PR11D | I/O |
| 95 | PR7A | PR8A | PR9A | PR10A | I/O-M3 |
| 96 | PR7D | PR8D | PR9D | PR10D | I/O |
| 97 | Vss | Vss | Vss | Vss | Vss |
| 98 | PR6A | PR7A | PR8A | PR9A | I/O |
| 99 | PR6C | PR7C | PR8C | PR9C | I/O |
| 100 | PR6D | PR7D | PR8D | PR9D | I/O |
| 101 | VDD | VDD | VDD | VDD | VDD |
| 102 | PR5A | PR6A | PR7A | PR8A | I/O |
| 103 | PR5C | PR6C | PR7C | PR8C | I/O |
| 104 | PR5D | PR6D | PR7D | PR8D | I/O |
| 105 | Vss | Vss | Vss | Vss | Vss |
| 106 | PR4A | PR5A | PR6A | PR7A | I/O |
| 107 | PR4C | PR5C | PR6C | PR7C | I/O |
| 108 | PR4D | PR5D | PR6D | PR7D | I/O |
| 109 | PR3A | PR4A | PR5A | PR6A | I/O-CS1 |
| 110 | PR3B | PR4B | PR5B | PR6B | I/O |
| 111 | PR3D | PR4D | PR5D | PR6D | I/O |
| 112 | PR2A | PR3A | PR4A | PR5A | I/O-CS0 |
| 113 | PR2C | PR3C | PR4B | PR4B | I/O |
| 114 | PR2D | PR3D | PR4D | PR4D | I/O |
| 115 | PR1A | PR2A | PR3A | PR3A | I/O-RD |
| 116 | PR1B | PR2C | PR3C | PR3C | I/O |
| 117 | PR1C | PR2D | PR3D | PR3D | I/O |
| 118 | PR1D | PR1A | PR2A | PR2A | I/O-WR |
| 119 | Vss | Vss | Vss | Vss | Vss |
| 120 | RD_CFGN | RD_CFGN | RD_CFGN | RD_CFGN | RD_CFGN |
| 121 | VDD | VDD | VDD | VDD | VDD |
| 122 | Vss | Vss | Vss | Vss | Vss |
| 123 | PT10D | PT12D | PT14D | PT16D | I/O |
| 124 | PT10C | PT12A | PT13D | PT15D | I/O-RDY/RCLK |
| 125 | PT10B | PT11D | PT13A | PT15A | I/O |
| 126 | PT10A | PT11C | PT12D | PT14D | I/O |
| 127 | PT9D | PT11A | PT12C | PT13D | I/O-D7 |

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Pin Information (continued)

Table 19. ATT2C04, ATT2C06, ATT2C08, and ATT2C10 160-Pin QFP Pinout (continued)

| Pin | 2C04 Pad | 2C06 Pad | 2C08 Pad | 2C10 Pad | Function |
|-----|-------------|-------------|-------------|-------------|-------------|
| 128 | PT9C | PT10D | PT12A | PT13B | I/O |
| 129 | PT9B | PT10C | PT11D | PT13A | I/O |
| 130 | PT9A | PT10A | PT11B | PT12B | I/O-D6 |
| 131 | VDD | VDD | VDD | VDD | VDD |
| 132 | PT8D | PT9D | PT10D | PT11D | I/O |
| 133 | PT8A | PT9A | PT10A | PT11A | I/O-D5 |
| 134 | PT7D | PT8D | PT9D | PT10D | I/O |
| 135 | PT7B | PT8B | PT9B | PT10B | I/O |
| 136 | PT7A | PT8A | PT9A | PT10A | I/O-D4 |
| 137 | PT6D | PT7D | PT8D | PT9D | I/O |
| 138 | PT6C | PT7C | PT8C | PT9C | I/O |
| 139 | PT6A | PT7A | PT8A | PT9A | I/O-D3 |
| 140 | VSS | VSS | VSS | VSS | VSS |
| 141 | PT5D | PT6D | PT7D | PT8D | I/O |
| 142 | PT5C | PT6C | PT7C | PT8C | I/O |
| 143 | PT5A | PT6A | PT7A | PT8A | I/O-D2 |
| 144 | PT4D | PT5D | PT6D | PT7D | I/O-D1 |
| 145 | PT4C | PT5C | PT6C | PT7C | I/O |
| 146 | PT4A | PT5A | PT6A | PT7A | I/O-D0/DIN |
| 147 | PT3D | PT4D | PT5D | PT6D | I/O |
| 148 | PT3C | PT4C | PT5C | PT6C | I/O |
| 149 | PT3A | PT4A | PT5A | PT6A | I/O-DOUT |
| 150 | VDD | VDD | VDD | VDD | VDD |
| 151 | PT2D | PT3D | PT4D | PT5D | I/O |
| 152 | PT2C | PT3C | PT4C | PT5A | I/O |
| 153 | PT2B | PT3B | PT4B | PT4D | I/O |
| 154 | PT2A | PT3A | PT4A | PT4A | I/O-TDI |
| 155 | PT1D | PT2A | PT3A | PT3A | I/O-TMS |
| 156 | PT1C | PT1D | PT2A | PT2A | I/O |
| 157 | PT1B | PT1C | PT1D | PT1D | I/O |
| 158 | PT1A | PT1A | PT1A | PT1A | I/O-TCK |
| 159 | VSS | VSS | VSS | VSS | VSS |
| 160 | RD_DATA/TDO | RD_DATA/TDO | RD_DATA/TDO | RD_DATA/TDO | RD_DATA/TDO |

Pin Information (continued)

Table 20. ATT2C04, ATT2C06, ATT2C08, ATT2C10, ATT2C12, ATT2C15, ATT2C26, and ATT2C40 208-Pin SQFP/SQFP-PQ2 Pinout

| Pin | 2C04 Pad | 2C06 Pad | 2C08 Pad | 2C10 Pad | 2C12 Pad | 2C15 Pad | 2C26 Pad | 2C40 Pad | Function |
|-----|----------|----------|----------|----------|----------|----------|----------|----------|----------|
| 1 | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS |
| 2 | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS |
| 3 | PL1D | PL1D | PL1D | PL1D | PL1D | PL1D | PL1D | PL1D | I/O |
| 4 | PL1C | PL1A | PL2D | PL2D | PL2D | PL2D | PL2D | PL3D | I/O-A0 |
| 5 | PL1B | PL2D | PL3D | PL3D | PL3D | PL4D | PL4D | PL5D | I/O |
| 6 | See Note | PL2C | PL3C | PL3C | PL3A | PL4A | PL4A | PL6D | I/O |
| 7 | PL1A | PL2A | PL3A | PL3A | PL4A | PL5A | PL5A | PL8D | I/O-A1 |
| 8 | PL2D | PL3D | PL4D | PL4A | PL5A | PL6A | PL6A | PL9A | I/O-A2 |
| 9 | PL2C | PL3C | PL4C | PL5C | PL6D | PL7D | PL7D | PL10D | I/O |
| 10 | PL2B | PL3B | PL4B | PL5B | PL6B | PL7B | PL7B | PL10B | I/O |
| 11 | PL2A | PL3A | PL4A | PL5A | PL6A | PL7A | PL7A | PL10A | I/O-A3 |
| 12 | VDD | VDD | VDD | VDD | VDD | VDD | VDD | VDD | VDD |
| 13 | PL3D | PL4D | PL5D | PL6D | PL7D | PL8D | PL8D | PL11D | I/O |
| 14 | PL3C | PL4C | PL5C | PL6C | PL7C | PL8C | PL8A | PL11A | I/O |
| 15 | PL3B | PL4B | PL5B | PL6B | PL7B | PL8B | PL9D | PL12D | I/O |
| 16 | PL3A | PL4A | PL5A | PL6A | PL7A | PL8A | PL9A | PL12A | I/O-A4 |
| 17 | PL4D | PL5D | PL6D | PL7D | PL8D | PL9D | PL10D | PL13D | I/O-A5 |
| 18 | PL4C | PL5C | PL6C | PL7C | PL8C | PL9C | PL10A | PL13A | I/O |
| 19 | PL4B | PL5B | PL6B | PL7B | PL8B | PL9B | PL11D | PL14D | I/O |
| 20 | PL4A | PL5A | PL6A | PL7A | PL8A | PL9A | PL11A | PL14A | I/O-A6 |
| 21 | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS |
| 22 | PL5D | PL6D | PL7D | PL8D | PL9D | PL10D | PL12D | PL15D | I/O |
| 23 | PL5C | PL6C | PL7C | PL8C | PL9C | PL10C | PL12C | PL15C | I/O |
| 24 | PL5B | PL6B | PL7B | PL8B | PL9B | PL10B | PL12B | PL15B | I/O |
| 25 | PL5A | PL6A | PL7A | PL8A | PL9A | PL10A | PL12A | PL15A | I/O-A7 |
| 26 | VDD | VDD | VDD | VDD | VDD | VDD | VDD | VDD | VDD |
| 27 | PL6D | PL7D | PL8D | PL9D | PL10D | PL11D | PL13D | PL16D | I/O |
| 28 | PL6C | PL7C | PL8C | PL9C | PL10C | PL11C | PL13C | PL16C | I/O |
| 29 | PL6B | PL7B | PL8B | PL9B | PL10B | PL11B | PL13B | PL16B | I/O |
| 30 | PL6A | PL7A | PL8A | PL9A | PL10A | PL11A | PL13A | PL16A | I/O-A8 |
| 31 | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS |
| 32 | PL7D | PL8D | PL9D | PL10D | PL11D | PL12D | PL14D | PL17D | I/O-A9 |
| 33 | PL7C | PL8C | PL9C | PL10C | PL11C | PL12C | PL14A | PL17A | I/O |
| 34 | PL7B | PL8B | PL9B | PL10B | PL11B | PL12B | PL15D | PL18D | I/O |
| 35 | PL7A | PL8A | PL9A | PL10A | PL11A | PL12A | PL15A | PL18A | I/O-A10 |
| 36 | PL8D | PL9D | PL10D | PL11D | PL12D | PL13D | PL16D | PL19D | I/O |
| 37 | PL8C | PL9C | PL10C | PL11C | PL12C | PL13C | PL16A | PL19A | I/O |
| 38 | PL8B | PL9B | PL10B | PL11B | PL12B | PL13B | PL17D | PL20D | I/O |

Note: The ATT2C04 does not have bond pads connected to 208-pin SQFP package pin numbers 6, 45, 47, 56, 60, 102, 153, 154, 166, 201, and 203.

Pin Information (continued)

Table 20. ATT2C04, ATT2C06, ATT2C08, ATT2C10, ATT2C12, ATT2C15, ATT2C26, and ATT2C40 208-Pin SQFP/SQFP-PQ2 Pinout (continued)

| Pin | 2C04 Pad | 2C06 Pad | 2C08 Pad | 2C10 Pad | 2C12 Pad | 2C15 Pad | 2C26 Pad | 2C40 Pad | Function |
|-----|----------|----------|----------|----------|----------|----------|----------|----------|----------|
| 39 | PL8A | PL9A | PL10A | PL11A | PL12A | PL13A | PL17A | PL20A | I/O-A11 |
| 40 | VDD | VDD | VDD | VDD | VDD | VDD | VDD | VDD | VDD |
| 41 | PL9D | PL10D | PL11D | PL12D | PL13D | PL14D | PL18D | PL21D | I/O-A12 |
| 42 | PL9C | PL10C | PL11C | PL12C | PL13B | PL14B | PL18B | PL21B | I/O |
| 43 | PL9B | PL10B | PL11B | PL12B | PL14D | PL15D | PL19D | PL22D | I/O |
| 44 | PL9A | PL10A | PL11A | PL13D | PL14B | PL15B | PL19B | PL22B | I/O-A13 |
| 45 | See Note | PL11D | PL12D | PL13B | PL15D | PL16D | PL20D | PL23D | I/O |
| 46 | PL10D | PL11A | PL12A | PL14C | PL16D | PL17D | PL21D | PL25A | I/O-A14 |
| 47 | See Note | PL12D | PL13D | PL15D | PL17D | PL18D | PL22D | PL27D | I/O |
| 48 | PL10C | PL12C | PL13A | PL15A | PL17A | PL19D | PL23D | PL28D | I/O |
| 49 | PL10B | PL12B | PL14D | PL16D | PL18C | PL19A | PL23A | PL28A | I/O |
| 50 | PL10A | PL12A | PL14A | PL16A | PL18A | PL20A | PL24A | PL30A | I/O-A15 |
| 51 | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS |
| 52 | CCLK | CCLK | CCLK | CCLK | CCLK | CCLK | CCLK | CCLK | CCLK |
| 53 | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS |
| 54 | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS |
| 55 | PB1A | PB1A | PB1A | PB1A | PB1A | PB1A | PB1A | PB1A | I/O-A16 |
| 56 | See Note | PB1B | PB1D | PB1D | PB1D | PB2A | PB2A | PB3A | I/O |
| 57 | PB1B | PB1C | PB2A | PB2A | PB2A | PB2D | PB2D | PB3D | I/O |
| 58 | PB1C | PB1D | PB2D | PB2D | PB2D | PB3D | PB3D | PB4D | I/O |
| 59 | PB1D | PB2A | PB3A | PB3B | PB3D | PB4D | PB4D | PB5D | I/O-A17 |
| 60 | See Note | PB2D | PB3D | PB4D | PB4D | PB5D | PB5D | PB6D | I/O |
| 61 | PB2A | PB3A | PB4A | PB5A | PB5B | PB6B | PB6B | PB7D | I/O |
| 62 | PB2B | PB3B | PB4B | PB5B | PB5D | PB6D | PB6D | PB8D | I/O |
| 63 | PB2C | PB3C | PB4C | PB5C | PB6B | PB7B | PB7B | PB9D | I/O |
| 64 | PB2D | PB3D | PB4D | PB5D | PB6D | PB7D | PB7D | PB10D | I/O |
| 65 | VDD | VDD | VDD | VDD | VDD | VDD | VDD | VDD | VDD |
| 66 | PB3A | PB4A | PB5A | PB6A | PB7A | PB8A | PB8A | PB11A | I/O |
| 67 | PB3B | PB4B | PB5B | PB6B | PB7B | PB8B | PB8D | PB11D | I/O |
| 68 | PB3C | PB4C | PB5C | PB6C | PB7C | PB8C | PB9A | PB12A | I/O |
| 69 | PB3D | PB4D | PB5D | PB6D | PB7D | PB8D | PB9D | PB12D | I/O |
| 70 | PB4A | PB5A | PB6A | PB7A | PB8A | PB9A | PB10A | PB13A | I/O |
| 71 | PB4B | PB5B | PB6B | PB7B | PB8B | PB9B | PB10D | PB13D | I/O |
| 72 | PB4C | PB5C | PB6C | PB7C | PB8C | PB9C | PB11A | PB14A | I/O |
| 73 | PB4D | PB5D | PB6D | PB7D | PB8D | PB9D | PB11D | PB14D | I/O |
| 74 | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS |

Note: The ATT2C04 does not have bond pads connected to 208-pin SQFP package pin numbers 6, 45, 47, 56, 60, 102, 153, 154, 166, 201, and 203.

Pin Information (continued)

Table 20. ATT2C04, ATT2C06, ATT2C08, ATT2C10, ATT2C12, ATT2C15, ATT2C26, and ATT2C40 208-Pin SQFP/SQFP-PQ2 Pinout (continued)

| Pin | 2C04 Pad | 2C06 Pad | 2C08 Pad | 2C10 Pad | 2C12 Pad | 2C15 Pad | 2C26 Pad | 2C40 Pad | Function |
|-----|----------|----------|----------|----------|----------|----------|----------|----------|----------|
| 75 | PB5A | PB6A | PB7A | PB8A | PB9A | PB10A | PB12A | PB15A | I/O |
| 76 | PB5B | PB6B | PB7B | PB8B | PB9B | PB10B | PB12B | PB15B | I/O |
| 77 | PB5C | PB6C | PB7C | PB8C | PB9C | PB10C | PB12C | PB15C | I/O |
| 78 | PB5D | PB6D | PB7D | PB8D | PB9D | PB10D | PB12D | PB15D | I/O |
| 79 | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS |
| 80 | PB6A | PB7A | PB8A | PB9A | PB10A | PB11A | PB13A | PB16A | I/O |
| 81 | PB6B | PB7B | PB8B | PB9B | PB10B | PB11B | PB13B | PB16B | I/O |
| 82 | PB6C | PB7C | PB8C | PB9C | PB10C | PB11C | PB13C | PB16C | I/O |
| 83 | PB6D | PB7D | PB8D | PB9D | PB10D | PB11D | PB13D | PB16D | I/O |
| 84 | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS |
| 85 | PB7A | PB8A | PB9A | PB10A | PB11A | PB12A | PB14A | PB17A | I/O |
| 86 | PB7B | PB8B | PB9B | PB10B | PB11B | PB12B | PB14D | PB17D | I/O |
| 87 | PB7C | PB8C | PB9C | PB10C | PB11C | PB12C | PB15A | PB18A | I/O |
| 88 | PB7D | PB8D | PB9D | PB10D | PB11D | PB12D | PB15D | PB18D | I/O |
| 89 | PB8A | PB9A | PB10A | PB11A | PB12A | PB13A | PB16A | PB19A | I/O-HDC |
| 90 | PB8B | PB9B | PB10B | PB11B | PB12B | PB13B | PB16D | PB19D | I/O |
| 91 | PB8C | PB9C | PB10C | PB11C | PB12C | PB13C | PB17A | PB20A | I/O |
| 92 | PB8D | PB9D | PB10D | PB11D | PB12D | PB13D | PB17D | PB20D | I/O |
| 93 | VDD | VDD | VDD | VDD | VDD | VDD | VDD | VDD | VDD |
| 94 | PB9A | PB10A | PB11A | PB12A | PB13A | PB14A | PB18A | PB21A | I/O-LDC |
| 95 | PB9B | PB10B | PB11D | PB13A | PB13D | PB14D | PB18D | PB22D | I/O |
| 96 | PB9C | PB10C | PB12A | PB13B | PB14A | PB15A | PB19A | PB23A | I/O |
| 97 | PB9D | PB10D | PB12B | PB13C | PB14D | PB15D | PB19D | PB24D | I/O |
| 98 | PB10A | PB11A | PB12C | PB13D | PB15A | PB16A | PB20A | PB25A | I/O-INIT |
| 99 | PB10B | PB11C | PB12D | PB14A | PB16A | PB17A | PB21A | PB26A | I/O |
| 100 | PB10C | PB11D | PB13A | PB15A | PB17A | PB18A | PB22A | PB1A | I/O |
| 101 | PB10D | PB12A | PB13D | PB15D | PB18A | PB19D | PB23D | PB28D | I/O |
| 102 | See Note | PB12D | PB14D | PB16D | PB18D | PB20D | PB24D | PB30D | I/O |
| 103 | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS |
| 104 | DONE | DONE | DONE | DONE | DONE | DONE | DONE | DONE | DONE |
| 105 | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS |
| 106 | RESET | RESET | RESET | RESET | RESET | RESET | RESET | RESET | RESET |
| 107 | PRGM | PRGM | PRGM | PRGM | PRGM | PRGM | PRGM | PRGM | PRGM |
| 108 | PR10A | PR12A | PR14A | PR16A | PR18A | PR20A | PR24A | PR30A | I/O-M0 |
| 109 | PR10B | PR12D | PR13A | PR15A | PR18D | PR19A | PR23A | PR28A | I/O |
| 110 | PR10C | PR11A | PR13D | PR15D | PR17B | PR18A | PR22A | PR27A | I/O |

Note: The ATT2C04 does not have bond pads connected to 208-pin SQFP package pin numbers 6, 45, 47, 56, 60, 102, 153, 154, 166, 201, and 203.

Pin Information (continued)

Table 20. ATT2C04, ATT2C06, ATT2C08, ATT2C10, ATT2C12, ATT2C15, ATT2C26, and ATT2C40 208-Pin SQFP/SQFP-PQ2 Pinout (continued)

| Pin | 2C04 Pad | 2C06 Pad | 2C08 Pad | 2C10 Pad | 2C12 Pad | 2C15 Pad | 2C26 Pad | 2C40 Pad | Function |
|-----|----------|----------|----------|----------|----------|----------|----------|----------|----------|
| 111 | PR10D | PR11B | PR12A | PR14A | PR16A | PR17A | PR21A | PR26A | I/O |
| 112 | PR9A | PR10A | PR11A | PR13B | PR15D | PR16D | PR20D | PR23D | I/O-M1 |
| 113 | PR9B | PR10B | PR11B | PR13C | PR14A | PR15A | PR19A | PR22A | I/O |
| 114 | PR9C | PR10C | PR11C | PR12A | PR14D | PR15D | PR19D | PR22D | I/O |
| 115 | PR9D | PR10D | PR11D | PR12B | PR13A | PR14A | PR18A | PR21A | I/O |
| 116 | VDD | VDD | VDD | VDD | VDD | VDD | VDD | VDD | VDD |
| 117 | PR8A | PR9A | PR10A | PR11A | PR12A | PR13A | PR17A | PR20A | I/O-M2 |
| 118 | PR8B | PR9B | PR10B | PR11B | PR12B | PR13B | PR17D | PR20D | I/O |
| 119 | PR8C | PR9C | PR10C | PR11C | PR12C | PR13C | PR16A | PR19A | I/O |
| 120 | PR8D | PR9D | PR10D | PR11D | PR12D | PR13D | PR16D | PR19D | I/O |
| 121 | PR7A | PR8A | PR9A | PR10A | PR11A | PR12A | PR15A | PR18A | I/O-M3 |
| 122 | PR7B | PR8B | PR9B | PR10B | PR11B | PR12B | PR15D | PR18D | I/O |
| 123 | PR7C | PR8C | PR9C | PR10C | PR11C | PR12C | PR14A | PR17A | I/O |
| 124 | PR7D | PR8D | PR9D | PR10D | PR11D | PR12D | PR14D | PR17D | I/O |
| 125 | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS |
| 126 | PR6A | PR7A | PR8A | PR9A | PR10A | PR11A | PR13A | PR16A | I/O |
| 127 | PR6B | PR7B | PR8B | PR9B | PR10B | PR11B | PR13B | PR16B | I/O |
| 128 | PR6C | PR7C | PR8C | PR9C | PR10C | PR11C | PR13C | PR16C | I/O |
| 129 | PR6D | PR7D | PR8D | PR9D | PR10D | PR11D | PR13D | PR16D | I/O |
| 130 | VDD | VDD | VDD | VDD | VDD | VDD | VDD | VDD | VDD |
| 131 | PR5A | PR6A | PR7A | PR8A | PR9A | PR10A | PR12A | PR15A | I/O |
| 132 | PR5B | PR6B | PR7B | PR8B | PR9B | PR10B | PR12B | PR15B | I/O |
| 133 | PR5C | PR6C | PR7C | PR8C | PR9C | PR10C | PR12C | PR15C | I/O |
| 134 | PR5D | PR6D | PR7D | PR8D | PR9D | PR10D | PR12D | PR15D | I/O |
| 135 | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS |
| 136 | PR4A | PR5A | PR6A | PR7A | PR8A | PR9A | PR11A | PR14A | I/O |
| 137 | PR4B | PR5B | PR6B | PR7B | PR8B | PR9B | PR11D | PR14D | I/O |
| 138 | PR4C | PR5C | PR6C | PR7C | PR8C | PR9C | PR10A | PR13A | I/O |
| 139 | PR4D | PR5D | PR6D | PR7D | PR8D | PR9D | PR10D | PR13D | I/O |
| 140 | PR3A | PR4A | PR5A | PR6A | PR7A | PR8A | PR9A | PR12A | I/O-CS1 |
| 141 | PR3B | PR4B | PR5B | PR6B | PR7B | PR8B | PR9D | PR12D | I/O |
| 142 | PR3C | PR4C | PR5C | PR6C | PR7C | PR8C | PR8A | PR11A | I/O |
| 143 | PR3D | PR4D | PR5D | PR6D | PR7D | PR8D | PR8D | PR11D | I/O |
| 144 | VDD | VDD | VDD | VDD | VDD | VDD | VDD | VDD | VDD |
| 145 | PR2A | PR3A | PR4A | PR5A | PR6A | PR7A | PR7A | PR10A | I/O-CS0 |
| 146 | PR2B | PR3B | PR4B | PR4B | PR6B | PR7B | PR7B | PR10B | I/O |

Note: The ATT2C04 does not have bond pads connected to 208-pin SQFP package pin numbers 6, 45, 47, 56, 60, 102, 153, 154, 166, 201, and 203.

Pin Information (continued)

Table 20. ATT2C04, ATT2C06, ATT2C08, ATT2C10, ATT2C12, ATT2C15, ATT2C26, and ATT2C40 208-Pin SQFP/SQFP-PQ2 Pinout (continued)

| Pin | 2C04 Pad | 2C06 Pad | 2C08 Pad | 2C10 Pad | 2C12 Pad | 2C15 Pad | 2C26 Pad | 2C40 Pad | Function |
|-----|----------|----------|----------|----------|----------|----------|----------|----------|--------------|
| 147 | PR2C | PR3C | PR4C | PR4C | PR5B | PR6B | PR6B | PR9B | I/O |
| 148 | PR2D | PR3D | PR4D | PR4D | PR5D | PR6D | PR6D | PR9D | I/O |
| 149 | PR1A | PR2A | PR3A | PR3A | PR4A | PR5A | PR5A | PR8A | I/O-RD |
| 150 | PR1B | PR2C | PR3C | PR3C | PR4D | PR5D | PR5D | PR6A | I/O |
| 151 | PR1C | PR2D | PR3D | PR3D | PR3A | PR4A | PR4A | PR5A | I/O |
| 152 | PR1D | PR1A | PR2A | PR2A | PR2A | PR3A | PR3A | PR4A | I/O-WR |
| 153 | See Note | PR1C | PR2D | PR2D | PR2C | PR2A | PR2A | PR3A | I/O |
| 154 | See Note | PR1D | PR1A | PR1A | PR1A | PR1A | PR1A | PR2A | I/O |
| 155 | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS |
| 156 | RD_CFGN | RD_CFGN | RD_CFGN | RD_CFGN | RD_CFGN | RD_CFGN | RD_CFGN | RD_CFGN | RD_CFGN |
| 157 | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS |
| 158 | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS |
| 159 | PT10D | PT12D | PT14D | PT16D | PT18D | PT20D | PT24D | PT30D | I/O |
| 160 | PT10C | PT12A | PT13D | PT15D | PT17D | PT19A | PT23A | PT28A | I/O-RDY/RCLK |
| 161 | PT10B | PT11D | PT13A | PT15A | PT16D | PT17D | PT21D | PT26D | I/O |
| 162 | PT10A | PT11C | PT12D | PT14D | PT16A | PT17A | PT21A | PT26A | I/O |
| 163 | PT9D | PT11A | PT12C | PT13D | PT15D | PT16D | PT20D | PT25D | I/O-D7 |
| 164 | PT9C | PT10D | PT12A | PT13B | PT14D | PT15D | PT19D | PT24D | I/O |
| 165 | PT9B | PT10C | PT11D | PT13A | PT14A | PT15A | PT19A | PT23D | I/O |
| 166 | See Note | PT10B | PT11C | PT12D | PT13D | PT14D | PT18D | PT22D | I/O |
| 167 | PT9A | PT10A | PT11B | PT12B | PT13B | PT14B | PT18B | PT21D | I/O-D6 |
| 168 | VDD | VDD | VDD | VDD | VDD | VDD | VDD | VDD | VDD |
| 169 | PT8D | PT9D | PT10D | PT11D | PT12D | PT13D | PT17D | PT20D | I/O |
| 170 | PT8C | PT9C | PT10C | PT11C | PT12C | PT13C | PT17A | PT20A | I/O |
| 171 | PT8B | PT9B | PT10B | PT11B | PT12B | PT13B | PT16D | PT19D | I/O |
| 172 | PT8A | PT9A | PT10A | PT11A | PT12A | PT13A | PT16A | PT19A | I/O-D5 |
| 173 | PT7D | PT8D | PT9D | PT10D | PT11D | PT12D | PT15D | PT18D | I/O |
| 174 | PT7C | PT8C | PT9C | PT10C | PT11C | PT12C | PT15A | PT18A | I/O |
| 175 | PT7B | PT8B | PT9B | PT10B | PT11B | PT12B | PT14D | PT17D | I/O |
| 176 | PT7A | PT8A | PT9A | PT10A | PT11A | PT12A | PT14A | PT17A | I/O-D4 |
| 177 | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS |
| 178 | PT6D | PT7D | PT8D | PT9D | PT10D | PT11D | PT13D | PT16D | I/O |
| 179 | PT6C | PT7C | PT8C | PT9C | PT10C | PT11C | PT13C | PT16C | I/O |
| 180 | PT6B | PT7B | PT8B | PT9B | PT10B | PT11B | PT13B | PT16B | I/O |
| 181 | PT6A | PT7A | PT8A | PT9A | PT10A | PT11A | PT13A | PT16A | I/O-D3 |
| 182 | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS |

Note: The ATT2C04 does not have bond pads connected to 208-pin SQFP package pin numbers 6, 45, 47, 56, 60, 102, 153, 154, 166, 201, and 203.

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Pin Information (continued)

Table 20. ATT2C04, ATT2C06, ATT2C08, ATT2C10, ATT2C12, ATT2C15, ATT2C26, and ATT2C40 208-Pin SQFP/SQFP-PQ2 Pinout (continued)

| Pin | 2C04 Pad | 2C06 Pad | 2C08 Pad | 2C10 Pad | 2C12 Pad | 2C15 Pad | 2C26 Pad | 2C40 Pad | Function |
|-----|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-------------|
| 183 | PT5D | PT6D | PT7D | PT8D | PT9D | PT10D | PT12D | PT15D | I/O |
| 184 | PT5C | PT6C | PT7C | PT8C | PT9C | PT10C | PT12C | PT15C | I/O |
| 185 | PT5B | PT6B | PT7B | PT8B | PT9B | PT10B | PT12B | PT15B | I/O |
| 186 | PT5A | PT6A | PT7A | PT8A | PT9A | PT10A | PT12A | PT15A | I/O-D2 |
| 187 | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS |
| 188 | PT4D | PT5D | PT6D | PT7D | PT8D | PT9D | PT11D | PT14D | I/O-D1 |
| 189 | PT4C | PT5C | PT6C | PT7C | PT8C | PT9C | PT11A | PT14A | I/O |
| 190 | PT4B | PT5B | PT6B | PT7B | PT8B | PT9B | PT10D | PT13D | I/O |
| 191 | PT4A | PT5A | PT6A | PT7A | PT8A | PT9A | PT10A | PT13A | I/O-D0/DIN |
| 192 | PT3D | PT4D | PT5D | PT6D | PT7D | PT8D | PT9D | PT12D | I/O |
| 193 | PT3C | PT4C | PT5C | PT6C | PT7C | PT8C | PT9A | PT12A | I/O |
| 194 | PT3B | PT4B | PT5B | PT6B | PT7B | PT8B | PT8D | PT11D | I/O |
| 195 | PT3A | PT4A | PT5A | PT6A | PT7A | PT8A | PT8A | PT11A | I/O-DOUT |
| 196 | VDD | VDD | VDD | VDD | VDD | VDD | VDD | VDD | VDD |
| 197 | PT2D | PT3D | PT4D | PT5D | PT6D | PT7D | PT7D | PT10D | I/O |
| 198 | PT2C | PT3C | PT4C | PT5A | PT6A | PT7A | PT7A | PT9A | I/O |
| 199 | PT2B | PT3B | PT4B | PT4D | PT5C | PT6C | PT6C | PT8A | I/O |
| 200 | PT2A | PT3A | PT4A | PT4A | PT5A | PT6A | PT6A | PT7A | I/O-TDI |
| 201 | See Note | PT2D | PT3D | PT3D | PT4A | PT5A | PT5A | PT6A | I/O |
| 202 | PT1D | PT2A | PT3A | PT3A | PT3A | PT4A | PT4A | PT5A | I/O-TMS |
| 203 | See Note | PT1D | PT2D | PT2D | PT2C | PT3A | PT3A | PT4A | I/O |
| 204 | PT1C | PT1C | PT2A | PT2A | PT2A | PT2A | PT2A | PT3A | I/O |
| 205 | PT1B | PT1B | PT1D | PT1D | PT1D | PT1D | PT1D | PT2D | I/O |
| 206 | PT1A | PT1A | PT1A | PT1A | PT1A | PT1A | PT1A | PT1A | I/O-TCK |
| 207 | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS |
| 208 | RD_DATA/ TDO | RD_DATA/ TDO | RD_DATA/ TDO | RD_DATA/ TDO | RD_DATA/ TDO | RD_DATA/ TDO | RD_DATA/ TDO | RD_DATA/ TDO | RD_DATA/TDO |

Note: The ATT2C04 does not have bond pads connected to 208-pin SQFP package pin numbers 6, 45, 47, 56, 60, 102, 153, 154, 166, 201, and 203.

Pin Information (continued)

Table 21. ATT2C06, ATT2C08, ATT2C10, ATT2C12, ATT2C15, ATT2C26, ATT2C40 and 240-Pin SQFP/SQFP-PQ2 Pinout

| Pin | 2C06 Pad | 2C08 Pad | 2C10 Pad | 2C12 Pad | 2C15 Pad | 2C26 Pad | 2C40 Pad | Function |
|-----|----------|----------|----------|----------|----------|----------|----------|----------|
| 1 | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS |
| 2 | VDD | VDD | VDD | VDD | VDD | VDD | VDD | VDD |
| 3 | PL1D | PL1D | PL1D | PL1D | PL1D | PL1D | PL1D | I/O |
| 4 | PL1C | PL1B | PL1B | PL1C | PL1C | PL1C | PL1A | I/O |
| 5 | PL1B | PL1A | PL1A | PL1B | PL1B | PL1B | PL2D | I/O |
| 6 | PL1A | PL2D | PL2D | PL2D | PL2D | PL2D | PL3D | I/O-A0 |
| 7 | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS |
| 8 | PL2D | PL3D | PL3D | PL3D | PL4D | PL4D | PL5D | I/O |
| 9 | PL2C | PL3C | PL3C | PL3A | PL4A | PL4A | PL6D | I/O |
| 10 | PL2B | PL3B | PL3B | PL4D | PL5D | PL5D | PL7D | I/O |
| 11 | PL2A | PL3A | PL3A | PL4A | PL5A | PL5A | PL8D | I/O-A1 |
| 12 | PL3D | PL4D | PL4A | PL5A | PL6A | PL6A | PL9A | I/O-A2 |
| 13 | PL3C | PL4C | PL5C | PL6D | PL7D | PL7D | PL10D | I/O |
| 14 | PL3B | PL4B | PL5B | PL6B | PL7B | PL7B | PL10B | I/O |
| 15 | PL3A | PL4A | PL5A | PL6A | PL7A | PL7A | PL10A | I/O-A3 |
| 16 | VDD | VDD | VDD | VDD | VDD | VDD | VDD | VDD |
| 17 | PL4D | PL5D | PL6D | PL7D | PL8D | PL8D | PL11D | I/O |
| 18 | PL4C | PL5C | PL6C | PL7C | PL8C | PL8A | PL11A | I/O |
| 19 | PL4B | PL5B | PL6B | PL7B | PL8B | PL9D | PL12D | I/O |
| 20 | PL4A | PL5A | PL6A | PL7A | PL8A | PL9A | PL12A | I/O-A4 |
| 21 | PL5D | PL6D | PL7D | PL8D | PL9D | PL10D | PL13D | I/O-A5 |
| 22 | PL5C | PL6C | PL7C | PL8C | PL9C | PL10A | PL13A | I/O |
| 23 | PL5B | PL6B | PL7B | PL8B | PL9B | PL11D | PL14D | I/O |
| 24 | PL5A | PL6A | PL7A | PL8A | PL9A | PL11A | PL14A | I/O-A6 |
| 25 | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS |
| 26 | PL6D | PL7D | PL8D | PL9D | PL10D | PL12D | PL15D | I/O |
| 27 | PL6C | PL7C | PL8C | PL9C | PL10C | PL12C | PL15C | I/O |
| 28 | PL6B | PL7B | PL8B | PL9B | PL10B | PL12B | PL15B | I/O |
| 29 | PL6A | PL7A | PL8A | PL9A | PL10A | PL12A | PL15A | I/O-A7 |
| 30 | VDD | VDD | VDD | VDD | VDD | VDD | VDD | VDD |
| 31 | PL7D | PL8D | PL9D | PL10D | PL11D | PL13D | PL16D | I/O |
| 32 | PL7C | PL8C | PL9C | PL10C | PL11C | PL13C | PL16C | I/O |
| 33 | PL7B | PL8B | PL9B | PL10B | PL11B | PL13B | PL16B | I/O |
| 34 | PL7A | PL8A | PL9A | PL10A | PL11A | PL13A | PL16A | I/O-A8 |
| 35 | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS |
| 36 | PL8D | PL9D | PL10D | PL11D | PL12D | PL14D | PL17D | I/O-A9 |
| 37 | PL8C | PL9C | PL10C | PL11C | PL12C | PL14A | PL17A | I/O |
| 38 | PL8B | PL9B | PL10B | PL11B | PL12B | PL15D | PL18D | I/O |
| 39 | PL8A | PL9A | PL10A | PL11A | PL12A | PL15A | PL18A | I/O-A10 |
| 40 | PL9D | PL10D | PL11D | PL12D | PL13D | PL16D | PL19D | I/O |
| 41 | PL9C | PL10C | PL11C | PL12C | PL13C | PL16A | PL19A | I/O |
| 42 | PL9B | PL10B | PL11B | PL12B | PL13B | PL17D | PL20D | I/O |
| 43 | PL9A | PL10A | PL11A | PL12A | PL13A | PL17A | PL20A | I/O-A11 |
| 44 | VDD | VDD | VDD | VDD | VDD | VDD | VDD | VDD |

Note: The ATT2C08 and ATT2C10 do not have bond pads connected to 240-pin SQFP package pin numbers 113 and 188.

Pin Information (continued)

Table 21. ATT2C06, ATT2C08, ATT2C10, ATT2C12, ATT2C15, ATT2C26, ATT2C40 and 240-Pin SQFP/SQFP-PQ2 Pinout (continued)

| Pin | 2C06 Pad | 2C08 Pad | 2C10 Pad | 2C12 Pad | 2C15 Pad | 2C26 Pad | 2C40 Pad | Function |
|-----|----------|----------|----------|----------|----------|----------|----------|----------|
| 45 | PL10D | PL11D | PL12D | PL13D | PL14D | PL18D | PL21D | I/O-A12 |
| 46 | PL10C | PL11C | PL12C | PL13B | PL14B | PL18B | PL21B | I/O |
| 47 | PL10B | PL11B | PL12B | PL14D | PL15D | PL19D | PL22D | I/O |
| 48 | PL10A | PL11A | PL13D | PL14B | PL15B | PL19B | PL22B | I/O-A13 |
| 49 | PL11D | PL12D | PL13B | PL14A | PL15A | PL19A | PL22A | I/O |
| 50 | PL11C | PL12C | PL13A | PL15D | PL16D | PL20D | PL23D | I/O |
| 51 | PL11B | PL12B | PL14D | PL15B | PL16B | PL20B | PL24D | I/O |
| 52 | PL11A | PL12A | PL14C | PL16D | PL17D | PL21D | PL25A | I/O-A14 |
| 53 | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS |
| 54 | PL12D | PL13D | PL15D | PL17D | PL18D | PL22D | PL27D | I/O |
| 55 | PL12C | PL13A | PL15A | PL17A | PL19D | PL23D | PL28D | I/O |
| 56 | PL12B | PL14D | PL16D | PL18C | PL19A | PL23A | PL28A | I/O |
| 57 | PL12A | PL14A | PL16A | PL18A | PL20A | PL24A | PL30A | I/O-A15 |
| 58 | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS |
| 59 | CCLK | CCLK | CCLK | CCLK | CCLK | CCLK | CCLK | CCLK |
| 60 | VDD | VDD | VDD | VDD | VDD | VDD | VDD | VDD |
| 61 | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS |
| 62 | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS |
| 63 | PB1A | PB1A | PB1A | PB1A | PB1A | PB1A | PB1A | I/O-A16 |
| 64 | PB1B | PB1D | PB1D | PB1D | PB2A | PB2A | PB3A | I/O |
| 65 | PB1C | PB2A | PB2A | PB2A | PB2D | PB2D | PB3D | I/O |
| 66 | PB1D | PB2D | PB2D | PB2D | PB3D | PB3D | PB4D | I/O |
| 67 | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS |
| 68 | PB2A | PB3A | PB3B | PB3D | PB4D | PB4D | PB5D | I/O-A17 |
| 69 | PB2B | PB3B | PB4B | PB4D | PB5D | PB5D | PB6D | I/O |
| 70 | PB2C | PB3C | PB4C | PB5A | PB6A | PB6A | PB7A | I/O |
| 71 | PB2D | PB3D | PB4D | PB5B | PB6B | PB6B | PB7D | I/O |
| 72 | PB3A | PB4A | PB5A | PB5D | PB6D | PB6D | PB8D | I/O |
| 73 | PB3B | PB4B | PB5B | PB6A | PB7A | PB7A | PB9A | I/O |
| 74 | PB3C | PB4C | PB5C | PB6B | PB7B | PB7B | PB9D | I/O |
| 75 | PB3D | PB4D | PB5D | PB6D | PB7D | PB7D | PB10D | I/O |
| 76 | VDD | VDD | VDD | VDD | VDD | VDD | VDD | VDD |
| 77 | PB4A | PB5A | PB6A | PB7A | PB8A | PB8A | PB11A | I/O |
| 78 | PB4B | PB5B | PB6B | PB7B | PB8B | PB8D | PB11D | I/O |
| 79 | PB4C | PB5C | PB6C | PB7C | PB8C | PB9A | PB12A | I/O |
| 80 | PB4D | PB5D | PB6D | PB7D | PB8D | PB9D | PB12D | I/O |
| 81 | PB5A | PB6A | PB7A | PB8A | PB9A | PB10A | PB13A | I/O |
| 82 | PB5B | PB6B | PB7B | PB8B | PB9B | PB10D | PB13D | I/O |
| 83 | PB5C | PB6C | PB7C | PB8C | PB9C | PB11A | PB14A | I/O |
| 84 | PB5D | PB6D | PB7D | PB8D | PB9D | PB11D | PB14D | I/O |
| 85 | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS |
| 86 | PB6A | PB7A | PB8A | PB9A | PB10A | PB12A | PB15A | I/O |
| 87 | PB6B | PB7B | PB8B | PB9B | PB10B | PB12B | PB15B | I/O |
| 88 | PB6C | PB7C | PB8C | PB9C | PB10C | PB12C | PB15C | I/O |

Note: The ATT2C08 and ATT2C10 do not have bond pads connected to 240-pin SQFP package pin numbers 113 and 188.

Pin Information (continued)

Table 21. ATT2C06, ATT2C08, ATT2C10, ATT2C12, ATT2C15, ATT2C26, ATT2C40 and 240-Pin SQFP/SQFP-PQ2 Pinout (continued)

| Pin | 2C06 Pad | 2C08 Pad | 2C10 Pad | 2C12 Pad | 2C15 Pad | 2C26 Pad | 2C40 Pad | Function |
|-----|----------|----------|----------|----------|----------|----------|----------|----------|
| 89 | PB6D | PB7D | PB8D | PB9D | PB10D | PB12D | PB15D | I/O |
| 90 | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS |
| 91 | PB7A | PB8A | PB9A | PB10A | PB11A | PB13A | PB16A | I/O |
| 92 | PB7B | PB8B | PB9B | PB10B | PB11B | PB13B | PB16B | I/O |
| 93 | PB7C | PB8C | PB9C | PB10C | PB11C | PB13C | PB16C | I/O |
| 94 | PB7D | PB8D | PB9D | PB10D | PB11D | PB13D | PB16D | I/O |
| 95 | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS |
| 96 | PB8A | PB9A | PB10A | PB11A | PB12A | PB14A | PB17A | I/O |
| 97 | PB8B | PB9B | PB10B | PB11B | PB12B | PB14D | PB17D | I/O |
| 98 | PB8C | PB9C | PB10C | PB11C | PB12C | PB15A | PB18A | I/O |
| 99 | PB8D | PB9D | PB10D | PB11D | PB12D | PB15D | PB18D | I/O |
| 100 | PB9A | PB10A | PB11A | PB12A | PB13A | PB16A | PB19A | I/O-HDC |
| 101 | PB9B | PB10B | PB11B | PB12B | PB13B | PB16D | PB19D | I/O |
| 102 | PB9C | PB10C | PB11C | PB12C | PB13C | PB17A | PB20A | I/O |
| 103 | PB9D | PB10D | PB11D | PB12D | PB13D | PB17D | PB20D | I/O |
| 104 | VDD | VDD | VDD | VDD | VDD | VDD | VDD | VDD |
| 105 | PB10A | PB11A | PB12A | PB13A | PB14A | PB18A | PB21A | I/O-LDC |
| 106 | PB10B | PB11D | PB13A | PB13D | PB14D | PB18D | PB22D | I/O |
| 107 | PB10C | PB12A | PB13B | PB14A | PB15A | PB19A | PB23A | I/O |
| 108 | PB10D | PB12B | PB13C | PB14D | PB15D | PB19D | PB24D | I/O |
| 109 | PB11A | PB12C | PB13D | PB15A | PB16A | PB20A | PB25A | I/O-INIT |
| 110 | PB11B | PB12D | PB14A | PB15D | PB16D | PB20D | PB25D | I/O |
| 111 | PB11C | PB13A | PB15A | PB16A | PB17A | PB21A | PB26A | I/O |
| 112 | PB11D | PB13B | PB15B | PB16D | PB17D | PB21D | PB26D | I/O |
| 113 | VSS | See Note | See Note | VSS | VSS | VSS | VSS | VSS |
| 114 | PB12A | PB13D | PB15D | PB17A | PB18A | PB22A | PB27A | I/O |
| 115 | PB12B | PB14A | PB16A | PB17D | PB19A | PB23A | PB28A | I/O |
| 116 | PB12C | PB14B | PB16B | PB18A | PB19D | PB23D | PB28D | I/O |
| 117 | PB12D | PB14D | PB16D | PB18D | PB20D | PB24D | PB30D | I/O |
| 118 | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS |
| 119 | DONE | DONE | DONE | DONE | DONE | DONE | DONE | DONE |
| 120 | VDD | VDD | VDD | VDD | VDD | VDD | VDD | VDD |
| 121 | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS |
| 122 | RESET | RESET | RESET | RESET | RESET | RESET | RESET | RESET |
| 123 | PRGM | PRGM | PRGM | PRGM | PRGM | PRGM | PRGM | PRGM |
| 124 | PR12A | PR14A | PR16A | PR18A | PR20A | PR24A | PR30A | I/O-M0 |
| 125 | PR12B | PR14D | PR16D | PR18C | PR20D | PR24D | PR29D | I/O |
| 126 | PR12C | PR13A | PR15A | PR18D | PR19A | PR23A | PR28A | I/O |
| 127 | PR12D | PR13D | PR15D | PR17B | PR18A | PR22A | PR27A | I/O |
| 128 | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS |
| 129 | PR11A | PR12A | PR14A | PR16A | PR17A | PR21A | PR26A | I/O |
| 130 | PR11B | PR12B | PR14C | PR16D | PR17D | PR21D | PR25A | I/O |
| 131 | PR11C | PR12C | PR14D | PR15A | PR16A | PR20A | PR24A | I/O |
| 132 | PR11D | PR12D | PR13A | PR15C | PR16C | PR20C | PR24D | I/O |

Note: The ATT2C08 and ATT2C10 do not have bond pads connected to 240-pin SQFP package pin numbers 113 and 188.

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Pin Information (continued)

Table 21. ATT2C06, ATT2C08, ATT2C10, ATT2C12, ATT2C15, ATT2C26, ATT2C40 and 240-Pin SQFP/SQFP-PQ2 Pinout (continued)

| Pin | 2C06 Pad | 2C08 Pad | 2C10 Pad | 2C12 Pad | 2C15 Pad | 2C26 Pad | 2C40 Pad | Function |
|-----|----------|----------|----------|----------|----------|----------|----------|----------|
| 133 | PR10A | PR11A | PR13B | PR15D | PR16D | PR20D | PR23D | I/O-M1 |
| 134 | PR10B | PR11B | PR13C | PR14A | PR15A | PR19A | PR22A | I/O |
| 135 | PR10C | PR11C | PR12A | PR14D | PR15D | PR19D | PR22D | I/O |
| 136 | PR10D | PR11D | PR12B | PR13A | PR14A | PR18A | PR21A | I/O |
| 137 | VDD | VDD | VDD | VDD | VDD | VDD | VDD | VDD |
| 138 | PR9A | PR10A | PR11A | PR12A | PR13A | PR17A | PR20A | I/O-M2 |
| 139 | PR9B | PR10B | PR11B | PR12B | PR13B | PR17D | PR20D | I/O |
| 140 | PR9C | PR10C | PR11C | PR12C | PR13C | PR16A | PR19A | I/O |
| 141 | PR9D | PR10D | PR11D | PR12D | PR13D | PR16D | PR19D | I/O |
| 142 | PR8A | PR9A | PR10A | PR11A | PR12A | PR15A | PR18A | I/O-M3 |
| 143 | PR8B | PR9B | PR10B | PR11B | PR12B | PR15D | PR18D | I/O |
| 144 | PR8C | PR9C | PR10C | PR11C | PR12C | PR14A | PR17A | I/O |
| 145 | PR8D | PR9D | PR10D | PR11D | PR12D | PR14D | PR17D | I/O |
| 146 | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS |
| 147 | PR7A | PR8A | PR9A | PR10A | PR11A | PR13A | PR16A | I/O |
| 148 | PR7B | PR8B | PR9B | PR10B | PR11B | PR13B | PR16B | I/O |
| 149 | PR7C | PR8C | PR9C | PR10C | PR11C | PR13C | PR16C | I/O |
| 150 | PR7D | PR8D | PR9D | PR10D | PR11D | PR13D | PR16D | I/O |
| 151 | VDD | VDD | VDD | VDD | VDD | VDD | VDD | VDD |
| 152 | PR6A | PR7A | PR8A | PR9A | PR10A | PR12A | PR15A | I/O |
| 153 | PR6B | PR7B | PR8B | PR9B | PR10B | PR12B | PR15B | I/O |
| 154 | PR6C | PR7C | PR8C | PR9C | PR10C | PR12C | PR15C | I/O |
| 155 | PR6D | PR7D | PR8D | PR9D | PR10D | PR12D | PR15D | I/O |
| 156 | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS |
| 157 | PR5A | PR6A | PR7A | PR8A | PR9A | PR11A | PR14A | I/O |
| 158 | PR5B | PR6B | PR7B | PR8B | PR9B | PR11D | PR14D | I/O |
| 159 | PR5C | PR6C | PR7C | PR8C | PR9C | PR10A | PR13A | I/O |
| 160 | PR5D | PR6D | PR7D | PR8D | PR9D | PR10D | PR13D | I/O |
| 161 | PR4A | PR5A | PR6A | PR7A | PR8A | PR9A | PR12A | I/O-CS1 |
| 162 | PR4B | PR5B | PR6B | PR7B | PR8B | PR9D | PR12D | I/O |
| 163 | PR4C | PR5C | PR6C | PR7C | PR8C | PR8A | PR11A | I/O |
| 164 | PR4D | PR5D | PR6D | PR7D | PR8D | PR8D | PR11D | I/O |
| 165 | VDD | VDD | VDD | VDD | VDD | VDD | VDD | VDD |
| 166 | PR3A | PR4A | PR5A | PR6A | PR7A | PR7A | PR10A | I/O-CS0 |
| 167 | PR3B | PR4B | PR4B | PR6B | PR7B | PR7B | PR10B | I/O |
| 168 | PR3C | PR4C | PR4C | PR5B | PR6B | PR6B | PR9B | I/O |
| 169 | PR3D | PR4D | PR4D | PR5D | PR6D | PR6D | PR9D | I/O |
| 170 | PR2A | PR3A | PR3A | PR4A | PR5A | PR5A | PR8A | I/O-RD |
| 171 | PR2B | PR3B | PR3B | PR4B | PR5B | PR5B | PR7A | I/O |
| 172 | PR2C | PR3C | PR3C | PR4D | PR5D | PR5D | PR6A | I/O |
| 173 | PR2D | PR3D | PR3D | PR3A | PR4A | PR4A | PR5A | I/O |
| 174 | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS |
| 175 | PR1A | PR2A | PR2A | PR2A | PR3A | PR3A | PR4A | I/O-WR |
| 176 | PR1B | PR2D | PR2D | PR2C | PR2A | PR2A | PR3A | I/O |

Note: The ATT2C08 and ATT2C10 do not have bond pads connected to 240-pin SQFP package pin numbers 113 and 188.

Pin Information (continued)

Table 21. ATT2C06, ATT2C08, ATT2C10, ATT2C12, ATT2C15, ATT2C26, ATT2C40 and 240-Pin SQFP/SQFP-PQ2 Pinout (continued)

| Pin | 2C06 Pad | 2C08 Pad | 2C10 Pad | 2C12 Pad | 2C15 Pad | 2C26 Pad | 2C40 Pad | Function |
|-----|----------|----------|----------|----------|----------|----------|----------|--------------|
| 177 | PR1C | PR1A | PR1A | PR1A | PR1A | PR1A | PR2A | I/O |
| 178 | PR1D | PR1D | PR1D | PR1D | PR1D | PR1D | PR1D | I/O |
| 179 | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS |
| 180 | RD_CFGN | RD_CFGN | RD_CFGN | RD_CFGN | RD_CFGN | RD_CFGN | RD_CFGN | RD_CFGN |
| 181 | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS |
| 182 | VDD | VDD | VDD | VDD | VDD | VDD | VDD | VDD |
| 183 | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS |
| 184 | PT12D | PT14D | PT16D | PT18D | PT20D | PT24D | PT30D | I/O |
| 185 | PT12C | PT14C | PT16C | PT18B | PT20A | PT24A | PT29A | I/O |
| 186 | PT12B | PT14A | PT16A | PT18A | PT19D | PT23D | PT28D | I/O |
| 187 | PT12A | PT13D | PT15D | PT17D | PT19A | PT23A | PT28A | I/O-RDY/RCLK |
| 188 | VSS | See Note | See Note | VSS | VSS | VSS | VSS | VSS |
| 189 | PT11D | PT13B | PT15B | PT16D | PT17D | PT21D | PT26D | I/O |
| 190 | PT11C | PT13A | PT15A | PT16C | PT17C | PT21C | PT26C | I/O |
| 191 | PT11B | PT12D | PT14D | PT16A | PT17A | PT21A | PT26A | I/O |
| 192 | PT11A | PT12C | PT13D | PT15D | PT16D | PT20D | PT25D | I/O-D7 |
| 193 | PT10D | PT12A | PT13B | PT14D | PT15D | PT19D | PT24D | I/O |
| 194 | PT10C | PT11D | PT13A | PT14A | PT15A | PT19A | PT23D | I/O |
| 195 | PT10B | PT11C | PT12D | PT13D | PT14D | PT18D | PT22D | I/O |
| 196 | PT10A | PT11B | PT12B | PT13B | PT14B | PT18B | PT21D | I/O-D6 |
| 197 | VDD | VDD | VDD | VDD | VDD | VDD | VDD | VDD |
| 198 | PT9D | PT10D | PT11D | PT12D | PT13D | PT17D | PT20D | I/O |
| 199 | PT9C | PT10C | PT11C | PT12C | PT13C | PT17A | PT20A | I/O |
| 200 | PT9B | PT10B | PT11B | PT12B | PT13B | PT16D | PT19D | I/O |
| 201 | PT9A | PT10A | PT11A | PT12A | PT13A | PT16A | PT19A | I/O-D5 |
| 202 | PT8D | PT9D | PT10D | PT11D | PT12D | PT15D | PT18D | I/O |
| 203 | PT8C | PT9C | PT10C | PT11C | PT12C | PT15A | PT18A | I/O |
| 204 | PT8B | PT9B | PT10B | PT11B | PT12B | PT14D | PT17D | I/O |
| 205 | PT8A | PT9A | PT10A | PT11A | PT12A | PT14A | PT17A | I/O-D4 |
| 206 | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS |
| 207 | PT7D | PT8D | PT9D | PT10D | PT11D | PT13D | PT16D | I/O |
| 208 | PT7C | PT8C | PT9C | PT10C | PT11C | PT13C | PT16C | I/O |
| 209 | PT7B | PT8B | PT9B | PT10B | PT11B | PT13B | PT16B | I/O |
| 210 | PT7A | PT8A | PT9A | PT10A | PT11A | PT13A | PT16A | I/O-D3 |
| 211 | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS |
| 212 | PT6D | PT7D | PT8D | PT9D | PT10D | PT12D | PT15D | I/O |
| 213 | PT6C | PT7C | PT8C | PT9C | PT10C | PT12C | PT15C | I/O |
| 214 | PT6B | PT7B | PT8B | PT9B | PT10B | PT12B | PT15B | I/O |
| 215 | PT6A | PT7A | PT8A | PT9A | PT10A | PT12A | PT15A | I/O-D2 |
| 216 | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS |
| 217 | PT5D | PT6D | PT7D | PT8D | PT9D | PT11D | PT14D | I/O-D1 |
| 218 | PT5C | PT6C | PT7C | PT8C | PT9C | PT11A | PT14A | I/O |
| 219 | PT5B | PT6B | PT7B | PT8B | PT9B | PT10D | PT13D | I/O |
| 220 | PT5A | PT6A | PT7A | PT8A | PT9A | PT10A | PT13A | I/O-D0/DIN |

Note: The ATT2C08 and ATT2C10 do not have bond pads connected to 240-pin SQFP package pin numbers 113 and 188.

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Pin Information (continued)

Table 21. ATT2C06, ATT2C08, ATT2C10, ATT2C12, ATT2C15, ATT2C26, ATT2C40 and 240-Pin SQFP/SQFP-PQ2 Pinout (continued)

| Pin | 2C06 Pad | 2C08 Pad | 2C10 Pad | 2C12 Pad | 2C15 Pad | 2C26 Pad | 2C40 Pad | Function |
|-----|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-------------|
| 221 | PT4D | PT5D | PT6D | PT7D | PT8D | PT9D | PT12D | I/O |
| 222 | PT4C | PT5C | PT6C | PT7C | PT8C | PT9A | PT12A | I/O |
| 223 | PT4B | PT5B | PT6B | PT7B | PT8B | PT8D | PT11D | I/O |
| 224 | PT4A | PT5A | PT6A | PT7A | PT8A | PT8A | PT11A | I/O-DOUT |
| 225 | VDD | VDD | VDD | VDD | VDD | VDD | VDD | VDD |
| 226 | PT3D | PT4D | PT5D | PT6D | PT7D | PT7D | PT10D | I/O |
| 227 | PT3C | PT4C | PT5A | PT6A | PT7A | PT7A | PT9A | I/O |
| 228 | PT3B | PT4B | PT4D | PT5C | PT6C | PT6C | PT8A | I/O |
| 229 | PT3A | PT4A | PT4A | PT5A | PT6A | PT6A | PT7A | I/O-TDI |
| 230 | PT2D | PT3D | PT3D | PT4D | PT5D | PT5D | PT6D | I/O |
| 231 | PT2C | PT3C | PT3C | PT4A | PT5A | PT5A | PT6A | I/O |
| 232 | PT2B | PT3B | PT3B | PT3D | PT4D | PT4D | PT5D | I/O |
| 233 | PT2A | PT3A | PT3A | PT3A | PT4A | PT4A | PT5A | I/O-TMS |
| 234 | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS |
| 235 | PT1D | PT2D | PT2D | PT2C | PT3A | PT3A | PT4A | I/O |
| 236 | PT1C | PT2A | PT2A | PT2A | PT2A | PT2A | PT3A | I/O |
| 237 | PT1B | PT1D | PT1D | PT1D | PT1D | PT1D | PT2D | I/O |
| 238 | PT1A | PT1A | PT1A | PT1A | PT1A | PT1A | PT1A | I/O-TCK |
| 239 | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS |
| 240 | RD_DATA/ TDO | RD_DATA/ TDO | RD_DATA/ TDO | RD_DATA/ TDO | RD_DATA/ TDO | RD_DATA/ TDO | RD_DATA/ TDO | RD_DATA/TDO |

Note: The ATT2C08 and ATT2C10 do not have bond pads connected to 240-pin SQFP package pin numbers 113 and 188.

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Pin Information (continued)

Table 22. ATT2C08, ATT2C10, and ATT2C12 256-Pin PBGA Pinout

| Pin | 2C08 Pad | 2C10 Pad | 2C12 Pad | Function |
|-----|----------|----------|----------|----------|
| A1 | Vss | Vss | Vss | Vss |
| B1 | Vdd | Vdd | Vdd | Vdd |
| C2 | PL1D | PL1D | PL1D | I/O |
| D2 | PL1B | PL1B | PL1C | I/O |
| D3 | PL1A | PL1A | PL1B | I/O |
| E4 | PL2D | PL2D | PL2D | I/O-A0 |
| C1 | PL2C | PL2C | PL2C | I/O |
| D1 | PL2B | PL2B | PL2B | I/O |
| E3 | PL2A | PL2A | PL2A | I/O |
| D4 | Vss | Vss | Vss | Vss |
| E2 | PL3D | PL3D | PL3D | I/O |
| E1 | PL3C | PL3C | PL3A | I/O |
| F3 | PL3B | PL3B | PL4D | I/O |
| G4 | PL3A | PL3A | PL4A | I/O-A1 |
| D8 | Vss | Vss | Vss | Vss |
| F2 | — | PL4D | PL5D | I/O |
| F1 | PL4D | PL4A | PL5A | I/O-A2 |
| G3 | PL4C | PL5C | PL6D | I/O |
| G2 | PL4B | PL5B | PL6B | I/O |
| G1 | PL4A | PL5A | PL6A | I/O-A3 |
| D6 | Vdd | Vdd | Vdd | Vdd |
| H3 | PL5D | PL6D | PL7D | I/O |
| H2 | PL5C | PL6C | PL7C | I/O |
| H1 | PL5B | PL6B | PL7B | I/O |
| J4 | PL5A | PL6A | PL7A | I/O-A4 |
| J3 | PL6D | PL7D | PL8D | I/O-A5 |
| J2 | PL6C | PL7C | PL8C | I/O |
| J1 | PL6B | PL7B | PL8B | I/O |
| K2 | PL6A | PL7A | PL8A | I/O-A6 |
| D13 | Vss | Vss | Vss | Vss |
| K3 | PL7D | PL8D | PL9D | I/O |
| K1 | PL7C | PL8C | PL9C | I/O |
| L1 | PL7B | PL8B | PL9B | I/O |
| L2 | PL7A | PL8A | PL9A | I/O-A7 |
| D11 | Vdd | Vdd | Vdd | Vdd |
| L3 | PL8D | PL9D | PL10D | I/O |
| L4 | PL8C | PL9C | PL10C | I/O |
| M1 | PL8B | PL9B | PL10B | I/O |
| M2 | PL8A | PL9A | PL10A | I/O-A8 |
| D17 | Vss | Vss | Vss | Vss |
| M3 | PL9D | PL10D | PL11D | I/O-A9 |
| M4 | PL9C | PL10C | PL11C | I/O |
| N1 | PL9B | PL10B | PL11B | I/O |

| Pin | 2C08 Pad | 2C10 Pad | 2C12 Pad | Function |
|-----|----------|----------|----------|------------|
| N2 | PL9A | PL10A | PL11A | I/O-A10 |
| N3 | PL10D | PL11D | PL12D | I/O |
| P1 | PL10C | PL11C | PL12C | I/O |
| P2 | PL10B | PL11B | PL12B | I/O |
| R1 | PL10A | PL11A | PL12A | I/O-A11 |
| D15 | Vdd | Vdd | Vdd | Vdd |
| P3 | PL11D | PL12D | PL13D | I/O-A12 |
| R2 | PL11C | PL12C | PL13B | I/O |
| T1 | PL11B | PL12B | PL14D | I/O |
| P4 | PL11A | PL13D | PL14B | I/O-A13 |
| R3 | PL12D | PL13B | PL14A | I/O |
| H4 | Vss | Vss | Vss | Vss |
| T2 | PL12C | PL13A | PL15D | I/O |
| W3 | — | — | — | No Connect |
| U1 | PL12B | PL14D | PL15B | I/O |
| T3 | PL12A | PL14C | PL16D | I/O-A14 |
| H17 | Vss | Vss | Vss | Vss |
| U2 | PL13D | PL15D | PL17D | I/O |
| V1 | PL13C | PL15C | PL17C | I/O |
| T4 | PL13B | PL15B | PL17B | I/O |
| U3 | PL13A | PL15A | PL17A | I/O |
| V2 | PL14D | PL16D | PL18D | I/O |
| W1 | PL14C | PL16C | PL18C | I/O |
| V3 | PL14B | PL16B | PL18B | I/O |
| W2 | PL14A | PL16A | PL18A | I/O-A15 |
| N4 | Vss | Vss | Vss | Vss |
| Y1 | CCLK | CCLK | CCLK | CCLK |
| F4 | Vdd | Vdd | Vdd | Vdd |
| N17 | Vss | Vss | Vss | Vss |
| F17 | Vdd | Vdd | Vdd | Vdd |
| Y2 | PB1A | PB1A | PB1A | I/O-A16 |
| W4 | PB1C | PB1C | PB1C | I/O |
| V4 | PB1D | PB1D | PB1D | I/O |
| U5 | PB2A | PB2A | PB2A | I/O |
| Y3 | PB2B | PB2B | PB2B | I/O |
| Y4 | PB2C | PB2C | PB2C | I/O |
| V5 | PB2D | PB2D | PB2D | I/O |
| U4 | Vss | Vss | Vss | Vss |
| W5 | PB3A | PB3B | PB3D | I/O-A17 |
| U8 | Vss | Vss | Vss | Vss |
| Y5 | PB3B | PB4B | PB4D | I/O |
| V6 | PB3C | PB4C | PB5A | I/O |
| U7 | PB3D | PB4D | PB5B | I/O |

Notes:

The W3 pin on the 256-pin PBGA package is unconnected for all devices listed in this table.

The ATT2C08 does not have bond pads connected to the 256-pin PBGA package pins F2 and Y17.

A 4 x 4 array of thermal balls is found at the center of the package. The balls can be attached to the ground plane of the board for enhanced thermal capability (see Table 26) or left unconnected.

Pin Information (continued)

Table 22. ATT2C08, ATT2C10, and ATT2C12 256-Pin PBGA Pinout (continued)

| Pin | 2C08 Pad | 2C10 Pad | 2C12 Pad | Function |
|-----|----------|----------|----------|----------|
| W6 | PB4A | PB5A | PB5D | I/O |
| Y6 | PB4B | PB5B | PB6A | I/O |
| V7 | PB4C | PB5C | PB6B | I/O |
| W7 | PB4D | PB5D | PB6D | I/O |
| K4 | VDD | VDD | VDD | VDD |
| Y7 | PB5A | PB6A | PB7A | I/O |
| V8 | PB5B | PB6B | PB7B | I/O |
| W8 | PB5C | PB6C | PB7C | I/O |
| Y8 | PB5D | PB6D | PB7D | I/O |
| U9 | PB6A | PB7A | PB8A | I/O |
| V9 | PB6B | PB7B | PB8B | I/O |
| W9 | PB6C | PB7C | PB8C | I/O |
| Y9 | PB6D | PB7D | PB8D | I/O |
| U13 | VSS | VSS | VSS | VSS |
| W10 | PB7A | PB8A | PB9A | I/O |
| V10 | PB7B | PB8B | PB9B | I/O |
| Y10 | PB7C | PB8C | PB9C | I/O |
| Y11 | PB7D | PB8D | PB9D | I/O |
| U17 | VSS | VSS | VSS | VSS |
| W11 | PB8A | PB9A | PB10A | I/O |
| V11 | PB8B | PB9B | PB10B | I/O |
| U11 | PB8C | PB9C | PB10C | I/O |
| Y12 | PB8D | PB9D | PB10D | I/O |
| W12 | PB9A | PB10A | PB11A | I/O |
| V12 | PB9B | PB10B | PB11B | I/O |
| U12 | PB9C | PB10C | PB11C | I/O |
| Y13 | PB9D | PB10D | PB11D | I/O |
| W13 | PB10A | PB11A | PB12A | I/O-HDC |
| V13 | PB10B | PB11B | PB12B | I/O |
| Y14 | PB10C | PB11C | PB12C | I/O |
| W14 | PB10D | PB11D | PB12D | I/O |
| L17 | VDD | VDD | VDD | VDD |
| Y15 | PB11A | PB12A | PB13A | I/O-LDC |
| V14 | PB11B | PB12C | PB13B | I/O |
| W15 | PB11C | PB12D | PB13C | I/O |
| Y16 | PB11D | PB13A | PB13D | I/O |
| U14 | PB12A | PB13B | PB14A | I/O |
| V15 | PB12B | PB13C | PB14D | I/O |
| W16 | PB12C | PB13D | PB15A | I/O-INIT |
| Y17 | — | PB14A | PB15D | I/O |
| V16 | PB12D | PB14B | PB16A | I/O |
| W17 | PB13A | PB15A | PB16D | I/O |
| Y18 | PB13B | PB15B | PB17A | I/O |

| Pin | 2C08 Pad | 2C10 Pad | 2C12 Pad | Function |
|-----|----------|----------|----------|----------|
| U16 | PB13C | PB15C | PB17C | I/O |
| V17 | PB13D | PB15D | PB17D | I/O |
| W18 | PB14A | PB16A | PB18A | I/O |
| Y19 | PB14B | PB16B | PB18B | I/O |
| V18 | PB14C | PB16C | PB18C | I/O |
| W19 | PB14D | PB16D | PB18D | I/O |
| Y20 | DONE | DONE | DONE | DONE |
| R4 | VDD | VDD | VDD | VDD |
| W20 | RESET | RESET | RESET | RESET |
| V19 | PRGM | PRGM | PRGM | PRGM |
| U19 | PR14A | PR16A | PR18A | I/O-M0 |
| U18 | PR14C | PR16C | PR18C | I/O |
| T17 | PR14D | PR16D | PR18D | I/O |
| V20 | PR13A | PR15A | PR17A | I/O |
| U20 | PR13B | PR15B | PR17B | I/O |
| T18 | PR13C | PR15C | PR17C | I/O |
| T19 | PR13D | PR15D | PR17D | I/O |
| T20 | PR12A | PR14A | PR16A | I/O |
| R18 | PR12B | PR14C | PR16D | I/O |
| P17 | PR12C | PR14D | PR15A | I/O |
| R19 | PR12D | PR13A | PR15C | I/O |
| R20 | PR11A | PR13B | PR15D | I/O-M1 |
| P18 | PR11B | PR13C | PR14A | I/O |
| P19 | PR11C | PR12A | PR14D | I/O |
| P20 | PR11D | PR12B | PR13A | I/O |
| R17 | VDD | VDD | VDD | VDD |
| N18 | PR10A | PR11A | PR12A | I/O-M2 |
| N19 | PR10B | PR11B | PR12B | I/O |
| N20 | PR10C | PR11C | PR12C | I/O |
| M17 | PR10D | PR11D | PR12D | I/O |
| M18 | PR9A | PR10A | PR11A | I/O-M3 |
| M19 | PR9B | PR10B | PR11B | I/O |
| M20 | PR9C | PR10C | PR11C | I/O |
| L19 | PR9D | PR10D | PR11D | I/O |
| L18 | PR8A | PR9A | PR10A | I/O |
| L20 | PR8B | PR9B | PR10B | I/O |
| K20 | PR8C | PR9C | PR10C | I/O |
| K19 | PR8D | PR9D | PR10D | I/O |
| U6 | VDD | VDD | VDD | VDD |
| K18 | PR7A | PR8A | PR9A | I/O |
| K17 | PR7B | PR8B | PR9B | I/O |
| J20 | PR7C | PR8C | PR9C | I/O |
| J19 | PR7D | PR8D | PR9D | I/O |

Notes:

The W3 pin on the 256-pin PBGA package is unconnected for all devices listed in this table.

The ATT2C08 does not have bond pads connected to the 256-pin PBGA package pins F2 and Y17.

A 4 x 4 array of thermal balls is found at the center of the package. The balls can be attached to the ground plane of the board for enhanced thermal capability (see Table 26) or left unconnected.

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Pin Information (continued)

Table 22. ATT2C08, ATT2C10, and ATT2C12 256-Pin PBGA Pinout (continued)

| Pin | 2C08 Pad | 2C10 Pad | 2C12 Pad | Function |
|-----|----------|----------|----------|------------------|
| J18 | PR6A | PR7A | PR8A | I/O |
| J17 | PR6B | PR7B | PR8B | I/O |
| H20 | PR6C | PR7C | PR8C | I/O |
| H19 | PR6D | PR7D | PR8D | I/O |
| H18 | PR5A | PR6A | PR7A | I/O-CS1 |
| G20 | PR5B | PR6B | PR7B | I/O |
| G19 | PR5C | PR6C | PR7C | I/O |
| F20 | PR5D | PR6D | PR7D | I/O |
| U10 | VDD | VDD | VDD | VDD |
| G18 | PR4A | PR5A | PR6A | I/O-CS0 |
| F19 | PR4B | PR4B | PR6B | I/O |
| E20 | PR4C | PR4C | PR5B | I/O |
| G17 | PR4D | PR4D | PR5D | I/O |
| F18 | PR3A | PR3A | PR4A | I/O-RD |
| E19 | PR3B | PR3B | PR4B | I/O |
| D20 | PR3C | PR3C | PR4D | I/O |
| E18 | PR3D | PR3D | PR3A | I/O |
| D19 | PR2A | PR2A | PR2A | I/O-WR |
| C20 | PR2B | PR2B | PR2B | I/O |
| E17 | PR2C | PR2C | PR2C | I/O |
| D18 | PR2D | PR2D | PR2D | I/O |
| C19 | PR1A | PR1A | PR1A | I/O |
| B20 | PR1B | PR1B | PR1B | I/O |
| C18 | PR1C | PR1C | PR1C | I/O |
| B19 | PR1D | PR1D | PR1D | I/O |
| A20 | RD_CFGN | RD_CFGN | RD_CFGN | RD_CFGN |
| U15 | VDD | VDD | VDD | VDD |
| A19 | PT14D | PT16D | PT18D | I/O |
| B18 | PT14C | PT16C | PT18C | I/O |
| B17 | PT14B | PT16B | PT18B | I/O |
| C17 | PT14A | PT16A | PT18A | I/O |
| D16 | PT13D | PT15D | PT17D | I/O-RDY/ RCLK |
| A18 | PT13C | PT15C | PT17A | I/O |
| A17 | PT13B | PT15B | PT16D | I/O |
| C16 | PT13A | PT15A | PT16C | I/O |
| B16 | PT12D | PT14D | PT16A | I/O |
| A16 | PT12C | PT13D | PT15D | I/O-D7 |
| C15 | PT12B | PT13C | PT15A | I/O |
| D14 | PT12A | PT13B | PT14D | I/O |
| B15 | PT11D | PT13A | PT14A | I/O |
| A15 | PT11C | PT12D | PT13D | I/O |
| C14 | PT11B | PT12B | PT13B | I/O-D6 |

| Pin | 2C08 Pad | 2C10 Pad | 2C12 Pad | Function |
|-----|-----------------|-----------------|-----------------|-----------------|
| B14 | PT11A | PT12A | PT13A | I/O |
| A14 | PT10D | PT11D | PT12D | I/O |
| C13 | PT10C | PT11C | PT12C | I/O |
| B13 | PT10B | PT11B | PT12B | I/O |
| A13 | PT10A | PT11A | PT12A | I/O-D5 |
| D12 | PT9D | PT10D | PT11D | I/O |
| C12 | PT9C | PT10C | PT11C | I/O |
| B12 | PT9B | PT10B | PT11B | I/O |
| A12 | PT9A | PT10A | PT11A | I/O-D4 |
| B11 | PT8D | PT9D | PT10D | I/O |
| C11 | PT8C | PT9C | PT10C | I/O |
| A11 | PT8B | PT9B | PT10B | I/O |
| A10 | PT8A | PT9A | PT10A | I/O-D3 |
| B10 | PT7D | PT8D | PT9D | I/O |
| C10 | PT7C | PT8C | PT9C | I/O |
| D10 | PT7B | PT8B | PT9B | I/O |
| A9 | PT7A | PT8A | PT9A | I/O-D2 |
| B9 | PT6D | PT7D | PT8D | I/O-D1 |
| C9 | PT6C | PT7C | PT8C | I/O |
| D9 | PT6B | PT7B | PT8B | I/O |
| A8 | PT6A | PT7A | PT8A | I/O-DO/DIN |
| B8 | PT5D | PT6D | PT7D | I/O |
| C8 | PT5C | PT6C | PT7C | I/O |
| A7 | PT5B | PT6B | PT7B | I/O |
| B7 | PT5A | PT6A | PT7A | I/O-DOUT |
| A6 | PT4D | PT5D | PT6D | I/O |
| C7 | PT4C | PT5A | PT6A | I/O |
| B6 | PT4B | PT4D | PT5C | I/O |
| A5 | PT4A | PT4A | PT5A | I/O-TDI |
| D7 | PT3D | PT3D | PT4D | I/O |
| C6 | PT3C | PT3C | PT4A | I/O |
| B5 | PT3B | PT3B | PT3D | I/O |
| A4 | PT3A | PT3A | PT3A | I/O-TMS |
| C5 | PT2D | PT2D | PT2D | I/O |
| B4 | PT2C | PT2C | PT2C | I/O |
| A3 | PT2B | PT2B | PT2B | I/O |
| D5 | PT2A | PT2A | PT2A | I/O |
| C4 | PT1D | PT1D | PT1D | I/O |
| B3 | PT1C | PT1C | PT1C | I/O |
| B2 | PT1B | PT1B | PT1B | I/O |
| A2 | PT1A | PT1A | PT1A | I/O-TCK |
| C3 | RD_DATA /TDO | RD_DATA /TDO | RD_DATA /TDO | RD_DATA/ TDO |

Notes:

The W3 pin on the 256-pin PBGA package is unconnected for all devices listed in this table.

The ATT2C08 does not have bond pads connected to the 256-pin PBGA package pins F2 and Y17.

A 4 x 4 array of thermal balls is found at the center of the package. The balls can be attached to the ground plane of the board for enhanced thermal capability (see Table 26) or left unconnected.

Pin Information (continued)

Table 23. ATT2C08, ATT2C10, ATT2C12, ATT2C15, ATT2C26, and ATT2C40
304-Pin SQFP/SQFP-PQ2 Pinout

| Pin | 2C08 Pad | 2C10 Pad | 2C12 Pad | 2C15 Pad | 2C26 Pad | 2C40 Pad | Function |
|-----|----------|----------|----------|----------|----------|----------|----------|
| 1 | Vss | Vss | Vss | Vss | Vss | Vss | Vss |
| 2 | VDD | VDD | VDD | VDD | VDD | VDD | VDD |
| 3 | Vss | Vss | Vss | Vss | Vss | Vss | Vss |
| 4 | PL1D | PL1D | PL1D | PL1D | PL1D | PL1D | I/O |
| 5 | PL1C | PL1C | PL1C | PL1C | PL1C | PL1A | I/O |
| 6 | PL1B | PL1B | PL1B | PL1B | PL1B | PL2D | I/O |
| 7 | PL1A | PL1A | PL1A | PL1A | PL1A | PL2A | I/O |
| 8 | PL2D | PL2D | PL2D | PL2D | PL2D | PL3D | I/O-A0 |
| 9 | PL2C | PL2C | PL2C | PL2A | PL2A | PL3A | I/O |
| 10 | PL2B | PL2B | PL2B | PL3D | PL3D | PL4D | I/O |
| 11 | PL2A | PL2A | PL2A | PL3A | PL3A | PL4A | I/O |
| 12 | Vss | Vss | Vss | Vss | Vss | Vss | Vss |
| 13 | PL3D | PL3D | PL3D | PL4D | PL4D | PL5D | I/O |
| 14 | PL3C | PL3C | PL3A | PL4A | PL4A | PL6D | I/O |
| 15 | PL3B | PL3B | PL4D | PL5D | PL5D | PL7D | I/O |
| 16 | PL3A | PL3A | PL4A | PL5A | PL5A | PL8D | I/O-A1 |
| 17 | See Note | PL4D | PL5D | PL6D | PL6D | PL9D | I/O |
| 18 | See Note | PL4C | PL5C | PL6C | PL6C | PL9C | I/O |
| 19 | See Note | PL4B | PL5B | PL6B | PL6B | PL9B | I/O |
| 20 | PL4D | PL4A | PL5A | PL6A | PL6A | PL9A | I/O-A2 |
| 21 | See Note | PL5D | PL6D | PL7D | PL7D | PL10D | I/O |
| 22 | PL4C | PL5C | PL6C | PL7C | PL7C | PL10C | I/O |
| 23 | PL4B | PL5B | PL6B | PL7B | PL7B | PL10B | I/O |
| 24 | PL4A | PL5A | PL6A | PL7A | PL7A | PL10A | I/O-A3 |
| 25 | VDD | VDD | VDD | VDD | VDD | VDD | VDD |
| 26 | PL5D | PL6D | PL7D | PL8D | PL8D | PL11D | I/O |
| 27 | PL5C | PL6C | PL7C | PL8C | PL8A | PL11A | I/O |
| 28 | PL5B | PL6B | PL7B | PL8B | PL9D | PL12D | I/O |
| 29 | PL5A | PL6A | PL7A | PL8A | PL9A | PL12A | I/O-A4 |
| 30 | PL6D | PL7D | PL8D | PL9D | PL10D | PL13D | I/O-A5 |
| 31 | PL6C | PL7C | PL8C | PL9C | PL10A | PL13A | I/O |
| 32 | PL6B | PL7B | PL8B | PL9B | PL11D | PL14D | I/O |
| 33 | PL6A | PL7A | PL8A | PL9A | PL11A | PL14A | I/O-A6 |
| 34 | Vss | Vss | Vss | Vss | Vss | Vss | Vss |
| 35 | PL7D | PL8D | PL9D | PL10D | PL12D | PL15D | I/O |
| 36 | PL7C | PL8C | PL9C | PL10C | PL12C | PL15C | I/O |
| 37 | PL7B | PL8B | PL9B | PL10B | PL12B | PL15B | I/O |
| 38 | PL7A | PL8A | PL9A | PL10A | PL12A | PL15A | I/O-A7 |
| 39 | VDD | VDD | VDD | VDD | VDD | VDD | VDD |
| 40 | PL8D | PL9D | PL10D | PL11D | PL13D | PL16D | I/O |
| 41 | PL8C | PL9C | PL10C | PL11C | PL13C | PL16C | I/O |

Note: The ATT2C08 does not have bond pads connected to 304-pin SQFP package pin numbers 17, 18, 19, 21, 57, 59, 64, 89, 91—93, 131, 138, 140, 171, 174, 175, 206—209, 242, 243, 249, 282, 283, 286, and 287.

Pin Information (continued)

Table 23. ATT2C08, ATT2C10, ATT2C12, ATT2C15, ATT2C26, and ATT2C40
304-Pin SQFP/SQFP-PQ2 Pinout (continued)

| Pin | 2C08 Pad | 2C10 Pad | 2C12 Pad | 2C15 Pad | 2C26 Pad | 2C40 Pad | Function |
|-----|----------|----------|----------|----------|----------|----------|----------|
| 42 | PL8B | PL9B | PL10B | PL11B | PL13B | PL16B | I/O |
| 43 | PL8A | PL9A | PL10A | PL11A | PL13A | PL16A | I/O-A8 |
| 44 | Vss | Vss | Vss | Vss | Vss | Vss | Vss |
| 45 | PL9D | PL10D | PL11D | PL12D | PL14D | PL17D | I/O-A9 |
| 46 | PL9C | PL10C | PL11C | PL12C | PL14A | PL17A | I/O |
| 47 | PL9B | PL10B | PL11B | PL12B | PL15D | PL18D | I/O |
| 48 | PL9A | PL10A | PL11A | PL12A | PL15A | PL18A | I/O-A10 |
| 49 | PL10D | PL11D | PL12D | PL13D | PL16D | PL19D | I/O |
| 50 | PL10C | PL11C | PL12C | PL13C | PL16A | PL19A | I/O |
| 51 | PL10B | PL11B | PL12B | PL13B | PL17D | PL20D | I/O |
| 52 | PL10A | PL11A | PL12A | PL13A | PL17A | PL20A | I/O-A11 |
| 53 | Vdd | Vdd | Vdd | Vdd | Vdd | Vdd | Vdd |
| 54 | PL11D | PL12D | PL13D | PL14D | PL18D | PL21D | I/O-A12 |
| 55 | PL11C | PL12C | PL13B | PL14B | PL18B | PL21B | I/O |
| 56 | PL11B | PL12B | PL13A | PL14A | PL18A | PL21A | I/O |
| 57 | See Note | PL12A | PL14D | PL15D | PL19D | PL22D | I/O |
| 58 | PL11A | PL13D | PL14B | PL15B | PL19B | PL22B | I/O-A13 |
| 59 | See Note | PL13C | PL14A | PL15A | PL19A | PL22A | I/O |
| 60 | PL12D | PL13B | PL15D | PL16D | PL20D | PL23D | I/O |
| 61 | PL12C | PL13A | PL15B | PL16B | PL20B | PL24D | I/O |
| 62 | PL12B | PL14D | PL15A | PL16A | PL20A | PL25D | I/O |
| 63 | PL12A | PL14C | PL16D | PL17D | PL21D | PL25A | I/O-A14 |
| 64 | See Note | PL14A | PL16A | PL17A | PL21A | PL26A | I/O |
| 65 | Vss | Vss | Vss | Vss | Vss | Vss | Vss |
| 66 | PL13D | PL15D | PL17D | PL18D | PL22D | PL27D | I/O |
| 67 | PL13C | PL15C | PL17C | PL18C | PL22C | PL27C | I/O |
| 68 | PL13B | PL15B | PL17B | PL18A | PL22A | PL27A | I/O |
| 69 | PL13A | PL15A | PL17A | PL19D | PL23D | PL28D | I/O |
| 70 | PL14D | PL16D | PL18D | PL19C | PL23C | PL28C | I/O |
| 71 | PL14C | PL16C | PL18C | PL19A | PL23A | PL28A | I/O |
| 72 | PL14B | PL16B | PL18B | PL20D | PL24D | PL29A | I/O |
| 73 | PL14A | PL16A | PL18A | PL20A | PL24A | PL30A | I/O-A15 |
| 74 | Vss | Vss | Vss | Vss | Vss | Vss | Vss |
| 75 | CCLK | CCLK | CCLK | CCLK | CCLK | CCLK | CCLK |
| 76 | Vdd | Vdd | Vdd | Vdd | Vdd | Vdd | Vdd |
| 77 | Vss | Vss | Vss | Vss | Vss | Vss | Vss |
| 78 | Vdd | Vdd | Vdd | Vdd | Vdd | Vdd | Vdd |
| 79 | Vss | Vss | Vss | Vss | Vss | Vss | Vss |
| 80 | PB1A | PB1A | PB1A | PB1A | PB1A | PB1A | I/O-A16 |
| 81 | PB1B | PB1B | PB1B | PB1C | PB1C | PB2A | I/O |
| 82 | PB1C | PB1C | PB1C | PB1D | PB1D | PB2D | I/O |

Note: The ATT2C08 does not have bond pads connected to 304-pin SQFP package pin numbers 17, 18, 19, 21, 57, 59, 64, 89, 91–93, 131, 138, 140, 171, 174, 175, 206–209, 242, 243, 249, 282, 283, 286, and 287.

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Pin Information (continued)

**Table 23. ATT2C08, ATT2C10, ATT2C12, ATT2C15, ATT2C26, and ATT2C40
304-Pin SQFP/SQFP-PQ2 Pinout (continued)**

| Pin | 2C08 Pad | 2C10 Pad | 2C12 Pad | 2C15 Pad | 2C26 Pad | 2C40 Pad | Function |
|-----|----------|----------|----------|----------|----------|----------|----------|
| 83 | PB1D | PB1D | PB1D | PB2A | PB2A | PB3A | I/O |
| 84 | PB2A | PB2A | PB2A | PB2D | PB2D | PB3D | I/O |
| 85 | PB2B | PB2B | PB2B | PB3A | PB3A | PB4A | I/O |
| 86 | PB2C | PB2C | PB2C | PB3C | PB3C | PB4C | I/O |
| 87 | PB2D | PB2D | PB2D | PB3D | PB3D | PB4D | I/O |
| 88 | Vss | Vss | Vss | Vss | Vss | Vss | Vss |
| 89 | See Note | PB3A | PB3A | PB4A | PB4A | PB5A | I/O |
| 90 | PB3A | PB3B | PB3D | PB4D | PB4D | PB5D | I/O-A17 |
| 91 | See Note | PB3C | PB4A | PB5A | PB5A | PB6A | I/O |
| 92 | See Note | PB3D | PB4D | PB5D | PB5D | PB6D | I/O |
| 93 | See Note | PB4A | PB5A | PB6A | PB6A | PB7A | I/O |
| 94 | PB3B | PB4B | PB5B | PB6B | PB6B | PB7D | I/O |
| 95 | PB3C | PB4C | PB5C | PB6C | PB6C | PB8A | I/O |
| 96 | PB3D | PB4D | PB5D | PB6D | PB6D | PB8D | I/O |
| 97 | PB4A | PB5A | PB6A | PB7A | PB7A | PB9A | I/O |
| 98 | PB4B | PB5B | PB6B | PB7B | PB7B | PB9D | I/O |
| 99 | PB4C | PB5C | PB6C | PB7C | PB7C | PB10A | I/O |
| 100 | PB4D | PB5D | PB6D | PB7D | PB7D | PB10D | I/O |
| 101 | VDD | VDD | VDD | VDD | VDD | VDD | VDD |
| 102 | PB5A | PB6A | PB7A | PB8A | PB8A | PB11A | I/O |
| 103 | PB5B | PB6B | PB7B | PB8B | PB8D | PB11D | I/O |
| 104 | PB5C | PB6C | PB7C | PB8C | PB9A | PB12A | I/O |
| 105 | PB5D | PB6D | PB7D | PB8D | PB9D | PB12D | I/O |
| 106 | PB6A | PB7A | PB8A | PB9A | PB10A | PB13A | I/O |
| 107 | PB6B | PB7B | PB8B | PB9B | PB10D | PB13D | I/O |
| 108 | PB6C | PB7C | PB8C | PB9C | PB11A | PB14A | I/O |
| 109 | PB6D | PB7D | PB8D | PB9D | PB11D | PB14D | I/O |
| 110 | Vss | Vss | Vss | Vss | Vss | Vss | Vss |
| 111 | PB7A | PB8A | PB9A | PB10A | PB12A | PB15A | I/O |
| 112 | PB7B | PB8B | PB9B | PB10B | PB12B | PB15B | I/O |
| 113 | PB7C | PB8C | PB9C | PB10C | PB12C | PB15C | I/O |
| 114 | PB7D | PB8D | PB9D | PB10D | PB12D | PB15D | I/O |
| 115 | Vss | Vss | Vss | Vss | Vss | Vss | Vss |
| 116 | PB8A | PB9A | PB10A | PB11A | PB13A | PB16A | I/O |
| 117 | PB8B | PB9B | PB10B | PB11B | PB13B | PB16B | I/O |
| 118 | PB8C | PB9C | PB10C | PB11C | PB13C | PB16C | I/O |
| 119 | PB8D | PB9D | PB10D | PB11D | PB13D | PB16D | I/O |
| 120 | Vss | Vss | Vss | Vss | Vss | Vss | Vss |
| 121 | PB9A | PB10A | PB11A | PB12A | PB14A | PB17A | I/O |
| 122 | PB9B | PB10B | PB11B | PB12B | PB14D | PB17D | I/O |
| 123 | PB9C | PB10C | PB11C | PB12C | PB15A | PB18A | I/O |

Note: The ATT2C08 does not have bond pads connected to 304-pin SQFP package pin numbers 17, 18, 19, 21, 57, 59, 64, 89, 91—93, 131, 138, 140, 171, 174, 175, 206—209, 242, 243, 249, 282, 283, 286, and 287.

Pin Information (continued)

Table 23. ATT2C08, ATT2C10, ATT2C12, ATT2C15, ATT2C26, and ATT2C40
304-Pin SQFP/SQFP-PQ2 Pinout (continued)

| Pin | 2C08 Pad | 2C10 Pad | 2C12 Pad | 2C15 Pad | 2C26 Pad | 2C40 Pad | Function |
|-----|----------|----------|----------|----------|----------|----------|----------|
| 124 | PB9D | PB10D | PB11D | PB12D | PB15D | PB18D | I/O |
| 125 | PB10A | PB11A | PB12A | PB13A | PB16A | PB19A | I/O-HDC |
| 126 | PB10B | PB11B | PB12B | PB13B | PB16D | PB19D | I/O |
| 127 | PB10C | PB11C | PB12C | PB13C | PB17A | PB20A | I/O |
| 128 | PB10D | PB11D | PB12D | PB13D | PB17D | PB20D | I/O |
| 129 | VDD | VDD | VDD | VDD | VDD | VDD | VDD |
| 130 | PB11A | PB12A | PB13A | PB14A | PB18A | PB21A | I/O-LDC |
| 131 | See Note | PB12B | PB13B | PB14B | PB18B | PB21D | I/O |
| 132 | PB11B | PB12C | PB13C | PB14C | PB18C | PB22A | I/O |
| 133 | PB11C | PB12D | PB13D | PB14D | PB18D | PB22D | I/O |
| 134 | PB11D | PB13A | PB14A | PB15A | PB19A | PB23A | I/O |
| 135 | PB12A | PB13B | PB14B | PB15B | PB19B | PB24A | I/O |
| 136 | PB12B | PB13C | PB14D | PB15D | PB19D | PB24D | I/O |
| 137 | PB12C | PB13D | PB15A | PB16A | PB20A | PB25A | I/O-INIT |
| 138 | See Note | PB14A | PB15D | PB16D | PB20D | PB25D | I/O |
| 139 | PB12D | PB14B | PB16A | PB17A | PB21A | PB26A | I/O |
| 140 | See Note | PB14D | PB16D | PB17D | PB21D | PB26D | I/O |
| 141 | VSS | VSS | VSS | VSS | VSS | VSS | VSS |
| 142 | PB13A | PB15A | PB17A | PB18A | PB22A | PB27A | I/O |
| 143 | PB13B | PB15B | PB17B | PB18B | PB22B | PB27B | I/O |
| 144 | PB13C | PB15C | PB17C | PB18D | PB22D | PB27D | I/O |
| 145 | PB13D | PB15D | PB17D | PB19A | PB23A | PB28A | I/O |
| 146 | PB14A | PB16A | PB18A | PB19D | PB23D | PB28D | I/O |
| 147 | PB14B | PB16B | PB18B | PB20A | PB24A | PB29A | I/O |
| 148 | PB14C | PB16C | PB18C | PB20B | PB24B | PB29D | I/O |
| 149 | PB14D | PB16D | PB18D | PB20D | PB24D | PB30D | I/O |
| 150 | VSS | VSS | VSS | VSS | VSS | VSS | VSS |
| 151 | DONE | DONE | DONE | DONE | DONE | DONE | DONE |
| 152 | VDD | VDD | VDD | VDD | VDD | VDD | VDD |
| 153 | VSS | VSS | VSS | VSS | VSS | VSS | VSS |
| 154 | RESET | RESET | RESET | RESET | RESET | RESET | RESET |
| 155 | PRGM | PRGM | PRGM | PRGM | PRGM | PRGM | PRGM |
| 156 | PR14A | PR16A | PR18A | PR20A | PR24A | PR30A | I/O-M0 |
| 157 | PR14B | PR16B | PR18B | PR20C | PR24C | PR29A | I/O |
| 158 | PR14C | PR16C | PR18C | PR20D | PR24D | PR29D | I/O |
| 159 | PR14D | PR16D | PR18D | PR19A | PR23A | PR28A | I/O |
| 160 | PR13A | PR15A | PR17A | PR19D | PR23D | PR28D | I/O |
| 161 | PR13B | PR15B | PR17B | PR18A | PR22A | PR27A | I/O |
| 162 | PR13C | PR15C | PR17C | PR18B | PR22B | PR27B | I/O |
| 163 | PR13D | PR15D | PR17D | PR18D | PR22D | PR27D | I/O |
| 164 | VSS | VSS | VSS | VSS | VSS | VSS | VSS |

Note: The ATT2C08 does not have bond pads connected to 304-pin SQFP package pin numbers 17, 18, 19, 21, 57, 59, 64, 89, 91–93, 131, 138, 140, 171, 174, 175, 206–209, 242, 243, 249, 282, 283, 286, and 287.

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Pin Information (continued)

Table 23. ATT2C08, ATT2C10, ATT2C12, ATT2C15, ATT2C26, and ATT2C40
304-Pin SQFP/SQFP-PQ2 Pinout (continued)

| Pin | 2C08 Pad | 2C10 Pad | 2C12 Pad | 2C15 Pad | 2C26 Pad | 2C40 Pad | Function |
|-----|----------|----------|----------|----------|----------|----------|----------|
| 165 | PR12A | PR14A | PR16A | PR17A | PR21A | PR26A | I/O |
| 166 | PR12B | PR14C | PR16D | PR17D | PR21D | PR25A | I/O |
| 167 | PR12C | PR14D | PR15A | PR16A | PR20A | PR24A | I/O |
| 168 | PR12D | PR13A | PR15C | PR16C | PR20C | PR24D | I/O |
| 169 | PR11A | PR13B | PR15D | PR16D | PR20D | PR23D | I/O-M1 |
| 170 | PR11B | PR13C | PR14A | PR15A | PR19A | PR22A | I/O |
| 171 | See Note | PR13D | PR14C | PR15C | PR19C | PR22C | I/O |
| 172 | PR11C | PR12A | PR14D | PR15D | PR19D | PR22D | I/O |
| 173 | PR11D | PR12B | PR13A | PR14A | PR18A | PR21A | I/O |
| 174 | See Note | PR12C | PR13C | PR14C | PR18C | PR21C | I/O |
| 175 | See Note | PR12D | PR13D | PR14D | PR18D | PR21D | I/O |
| 176 | VDD | VDD | VDD | VDD | VDD | VDD | VDD |
| 177 | PR10A | PR11A | PR12A | PR13A | PR17A | PR20A | I/O-M2 |
| 178 | PR10B | PR11B | PR12B | PR13B | PR17D | PR20D | I/O |
| 179 | PR10C | PR11C | PR12C | PR13C | PR16A | PR19A | I/O |
| 180 | PR10D | PR11D | PR12D | PR13D | PR16D | PR19D | I/O |
| 181 | PR9A | PR10A | PR11A | PR12A | PR15A | PR18A | I/O-M3 |
| 182 | PR9B | PR10B | PR11B | PR12B | PR15D | PR18D | I/O |
| 183 | PR9C | PR10C | PR11C | PR12C | PR14A | PR17A | I/O |
| 184 | PR9D | PR10D | PR11D | PR12D | PR14D | PR17D | I/O |
| 185 | VSS | VSS | VSS | VSS | VSS | VSS | VSS |
| 186 | PR8A | PR9A | PR10A | PR11A | PR13A | PR16A | I/O |
| 187 | PR8B | PR9B | PR10B | PR11B | PR13B | PR16B | I/O |
| 188 | PR8C | PR9C | PR10C | PR11C | PR13C | PR16C | I/O |
| 189 | PR8D | PR9D | PR10D | PR11D | PR13D | PR16D | I/O |
| 190 | VDD | VDD | VDD | VDD | VDD | VDD | VDD |
| 191 | PR7A | PR8A | PR9A | PR10A | PR12A | PR15A | I/O |
| 192 | PR7B | PR8B | PR9B | PR10B | PR12B | PR15B | I/O |
| 193 | PR7C | PR8C | PR9C | PR10C | PR12C | PR15C | I/O |
| 194 | PR7D | PR8D | PR9D | PR10D | PR12D | PR15D | I/O |
| 195 | VSS | VSS | VSS | VSS | VSS | VSS | VSS |
| 196 | PR6A | PR7A | PR8A | PR9A | PR11A | PR14A | I/O |
| 197 | PR6B | PR7B | PR8B | PR9B | PR11D | PR14D | I/O |
| 198 | PR6C | PR7C | PR8C | PR9C | PR10A | PR13A | I/O |
| 199 | PR6D | PR7D | PR8D | PR9D | PR10D | PR13D | I/O |
| 200 | PR5A | PR6A | PR7A | PR8A | PR9A | PR12A | I/O-CS1 |
| 201 | PR5B | PR6B | PR7B | PR8B | PR9D | PR12D | I/O |
| 202 | PR5C | PR6C | PR7C | PR8C | PR8A | PR11A | I/O |
| 203 | PR5D | PR6D | PR7D | PR8D | PR8D | PR11D | I/O |
| 204 | VDD | VDD | VDD | VDD | VDD | VDD | VDD |
| 205 | PR4A | PR5A | PR6A | PR7A | PR7A | PR10A | I/O-CS0 |

Note: The ATT2C08 does not have bond pads connected to 304-pin SQFP package pin numbers 17, 18, 19, 21, 57, 59, 64, 89, 91—93, 131, 138, 140, 171, 174, 175, 206—209, 242, 243, 249, 282, 283, 286, and 287.

Pin Information (continued)

Table 23. ATT2C08, ATT2C10, ATT2C12, ATT2C15, ATT2C26, and ATT2C40
304-Pin SQFP/SQFP-PQ2 Pinout (continued)

| Pin | 2C08 Pad | 2C10 Pad | 2C12 Pad | 2C15 Pad | 2C26 Pad | 2C40 Pad | Function |
|-----|----------|----------|----------|----------|----------|----------|--------------|
| 206 | See Note | PR5B | PR6B | PR7B | PR7B | PR10B | I/O |
| 207 | See Note | PR5C | PR6C | PR7C | PR7C | PR10C | I/O |
| 208 | See Note | PR5D | PR6D | PR7D | PR7D | PR10D | I/O |
| 209 | See Note | PR4A | PR5A | PR6A | PR6A | PR9A | I/O |
| 210 | PR4B | PR4B | PR5B | PR6B | PR6B | PR9B | I/O |
| 211 | PR4C | PR4C | PR5C | PR6C | PR6C | PR9C | I/O |
| 212 | PR4D | PR4D | PR5D | PR6D | PR6D | PR9D | I/O |
| 213 | PR3A | PR3A | PR4A | PR5A | PR5A | PR8A | I/O-RD |
| 214 | PR3B | PR3B | PR4B | PR5B | PR5B | PR7A | I/O |
| 215 | PR3C | PR3C | PR4D | PR5D | PR5D | PR6A | I/O |
| 216 | PR3D | PR3D | PR3A | PR4A | PR4A | PR5A | I/O |
| 217 | Vss | Vss | Vss | Vss | Vss | Vss | Vss |
| 218 | PR2A | PR2A | PR2A | PR3A | PR3A | PR4A | I/O-WR |
| 219 | PR2B | PR2B | PR2B | PR3B | PR3B | PR4B | I/O |
| 220 | PR2C | PR2C | PR2C | PR2A | PR2A | PR3A | I/O |
| 221 | PR2D | PR2D | PR2D | PR2D | PR2D | PR3D | I/O |
| 222 | PR1A | PR1A | PR1A | PR1A | PR1A | PR2A | I/O |
| 223 | PR1B | PR1B | PR1B | PR1B | PR1B | PR2D | I/O |
| 224 | PR1C | PR1C | PR1C | PR1C | PR1C | PR1A | I/O |
| 225 | PR1D | PR1D | PR1D | PR1D | PR1D | PR1D | I/O |
| 226 | Vss | Vss | Vss | Vss | Vss | Vss | Vss |
| 227 | RD_CFGN | RD_CFGN | RD_CFGN | RD_CFGN | RD_CFGN | RD_CFGN | RD_CFGN |
| 228 | VDD | VDD | VDD | VDD | VDD | VDD | VDD |
| 229 | Vss | Vss | Vss | Vss | Vss | Vss | Vss |
| 230 | VDD | VDD | VDD | VDD | VDD | VDD | VDD |
| 231 | Vss | Vss | Vss | Vss | Vss | Vss | Vss |
| 232 | PT14D | PT16D | PT18D | PT20D | PT24D | PT30D | I/O |
| 233 | PT14C | PT16C | PT18C | PT20C | PT24C | PT30A | I/O |
| 234 | PT14B | PT16B | PT18B | PT20A | PT24A | PT29A | I/O |
| 235 | PT14A | PT16A | PT18A | PT19D | PT23D | PT28D | I/O |
| 236 | PT13D | PT15D | PT17D | PT19A | PT23A | PT28A | I/O-RDY/RCLK |
| 237 | PT13C | PT15C | PT17C | PT18D | PT22D | PT27D | I/O |
| 238 | PT13B | PT15B | PT17B | PT18C | PT22C | PT27C | I/O |
| 239 | PT13A | PT15A | PT17A | PT18A | PT22A | PT27A | I/O |
| 240 | Vss | Vss | Vss | Vss | Vss | Vss | Vss |
| 241 | PT12D | PT14D | PT16D | PT17D | PT21D | PT26D | I/O |
| 242 | See Note | PT14B | PT16C | PT17C | PT21C | PT26C | I/O |
| 243 | See Note | PT14A | PT16A | PT17A | PT21A | PT26A | I/O |
| 244 | PT12C | PT13D | PT15D | PT16D | PT20D | PT25D | I/O-D7 |
| 245 | PT12B | PT13C | PT15A | PT16A | PT20A | PT25A | I/O |
| 246 | PT12A | PT13B | PT14D | PT15D | PT19D | PT24D | I/O |

Note: The ATT2C08 does not have bond pads connected to 304-pin SQFP package pin numbers 17, 18, 19, 21, 57, 59, 64, 89, 91–93, 131, 138, 140, 171, 174, 175, 206–209, 242, 243, 249, 282, 283, 286, and 287.

Pin Information (continued)

Table 23. ATT2C08, ATT2C10, ATT2C12, ATT2C15, ATT2C26, and ATT2C40
304-Pin SQFP/SQFP-PQ2 Pinout (continued)

| Pin | 2C08 Pad | 2C10 Pad | 2C12 Pad | 2C15 Pad | 2C26 Pad | 2C40 Pad | Function |
|-----|----------|----------|----------|----------|----------|----------|------------|
| 247 | PT11D | PT13A | PT14A | PT15A | PT19A | PT23D | I/O |
| 248 | PT11C | PT12D | PT13D | PT14D | PT18D | PT22D | I/O |
| 249 | See Note | PT12C | PT13C | PT14C | PT18C | PT22A | I/O |
| 250 | PT11B | PT12B | PT13B | PT14B | PT18B | PT21D | I/O-D6 |
| 251 | PT11A | PT12A | PT13A | PT14A | PT18A | PT21A | I/O |
| 252 | VDD | VDD | VDD | VDD | VDD | VDD | VDD |
| 253 | PT10D | PT11D | PT12D | PT13D | PT17D | PT20D | I/O |
| 254 | PT10C | PT11C | PT12C | PT13C | PT17A | PT20A | I/O |
| 255 | PT10B | PT11B | PT12B | PT13B | PT16D | PT19D | I/O |
| 256 | PT10A | PT11A | PT12A | PT13A | PT16A | PT19A | I/O-D5 |
| 257 | PT9D | PT10D | PT11D | PT12D | PT15D | PT18D | I/O |
| 258 | PT9C | PT10C | PT11C | PT12C | PT15A | PT18A | I/O |
| 259 | PT9B | PT10B | PT11B | PT12B | PT14D | PT17D | I/O |
| 260 | PT9A | PT10A | PT11A | PT12A | PT14A | PT17A | I/O-D4 |
| 261 | VSS | VSS | VSS | VSS | VSS | VSS | VSS |
| 262 | PT8D | PT9D | PT10D | PT11D | PT13D | PT16D | I/O |
| 263 | PT8C | PT9C | PT10C | PT11C | PT13C | PT16C | I/O |
| 264 | PT8B | PT9B | PT10B | PT11B | PT13B | PT16B | I/O |
| 265 | PT8A | PT9A | PT10A | PT11A | PT13A | PT16A | I/O-D3 |
| 266 | VSS | VSS | VSS | VSS | VSS | VSS | VSS |
| 267 | PT7D | PT8D | PT9D | PT10D | PT12D | PT15D | I/O |
| 268 | PT7C | PT8C | PT9C | PT10C | PT12C | PT15C | I/O |
| 269 | PT7B | PT8B | PT9B | PT10B | PT12B | PT15B | I/O |
| 270 | PT7A | PT8A | PT9A | PT10A | PT12A | PT15A | I/O-D2 |
| 271 | VSS | VSS | VSS | VSS | VSS | VSS | VSS |
| 272 | PT6D | PT7D | PT8D | PT9D | PT11D | PT14D | I/O-D1 |
| 273 | PT6C | PT7C | PT8C | PT9C | PT11A | PT14A | I/O |
| 274 | PT6B | PT7B | PT8B | PT9B | PT10D | PT13D | I/O |
| 275 | PT6A | PT7A | PT8A | PT9A | PT10A | PT13A | I/O-D0/DIN |
| 276 | PT5D | PT6D | PT7D | PT8D | PT9D | PT12D | I/O |
| 277 | PT5C | PT6C | PT7C | PT8C | PT9A | PT12A | I/O |
| 278 | PT5B | PT6B | PT7B | PT8B | PT8D | PT11D | I/O |
| 279 | PT5A | PT6A | PT7A | PT8A | PT8A | PT11A | I/O-DOUT |
| 280 | VDD | VDD | VDD | VDD | VDD | VDD | VDD |
| 281 | PT4D | PT5D | PT6D | PT7D | PT7D | PT10D | I/O |
| 282 | See Note | PT5C | PT6C | PT7C | PT7C | PT10A | I/O |
| 283 | See Note | PT5B | PT6B | PT7B | PT7B | PT9D | I/O |
| 284 | PT4C | PT5A | PT6A | PT7A | PT7A | PT9A | I/O |
| 285 | PT4B | PT4D | PT5D | PT6D | PT6D | PT8D | I/O |
| 286 | See Note | PT4C | PT5C | PT6C | PT6C | PT8A | I/O |
| 287 | See Note | PT4B | PT5B | PT6B | PT6B | PT7D | I/O |

Note: The ATT2C08 does not have bond pads connected to 304-pin SQFP package pin numbers 17, 18, 19, 21, 57, 59, 64, 89, 91–93, 131, 138, 140, 171, 174, 175, 206–209, 242, 243, 249, 282, 283, 286, and 287.

Pin Information (continued)

Table 23. ATT2C08, ATT2C10, ATT2C12, ATT2C15, ATT2C26, and ATT2C40
304-Pin SQFP/SQFP-PQ2 Pinout (continued)

| Pin | 2C08 Pad | 2C10 Pad | 2C12 Pad | 2C15 Pad | 2C26 Pad | 2C40 Pad | Function |
|-----|-----------------|-----------------|-------------|-------------|-------------|-------------|-------------|
| 288 | PT4A | PT4A | PT5A | PT6A | PT6A | PT7A | I/O-TDI |
| 289 | PT3D | PT3D | PT4D | PT5D | PT5D | PT6D | I/O |
| 290 | PT3C | PT3C | PT4A | PT5A | PT5A | PT6A | I/O |
| 291 | PT3B | PT3B | PT3D | PT4D | PT4D | PT5D | I/O |
| 292 | PT3A | PT3A | PT3A | PT4A | PT4A | PT5A | I/O-TMS |
| 293 | Vss | Vss | Vss | Vss | Vss | Vss | Vss |
| 294 | PT2D | PT2D | PT2D | PT3D | PT3D | PT4D | I/O |
| 295 | PT2C | PT2C | PT2C | PT3A | PT3A | PT4A | I/O |
| 296 | PT2B | PT2B | PT2B | PT2D | PT2D | PT3D | I/O |
| 297 | PT2A | PT2A | PT2A | PT2A | PT2A | PT3A | I/O |
| 298 | PT1D | PT1D | PT1D | PT1D | PT1D | PT2D | I/O |
| 299 | PT1C | PT1C | PT1C | PT1C | PT1C | PT1C | I/O |
| 300 | PT1B | PT1B | PT1B | PT1B | PT1B | PT1D | I/O |
| 301 | PT1A | PT1A | PT1A | PT1A | PT1A | PT1A | I/O-TCK |
| 302 | Vss | Vss | Vss | Vss | Vss | Vss | Vss |
| 303 | RD_DATA/ TDO | RD_DATA/ TDO | RD_DATA/TDO | RD_DATA/TDO | RD_DATA/TDO | RD_DATA/TDO | RD_DATA/TDO |
| 304 | VDD | VDD | VDD | VDD | VDD | VDD | VDD |

Note: The ATT2C08 does not have bond pads connected to 304-pin SQFP package pin numbers 17, 18, 19, 21, 57, 59, 64, 89, 91—93, 131, 138, 140, 171, 174, 175, 206—209, 242, 243, 249, 282, 283, 286, and 287.

Pin Information (continued)

Table 24. ATT2C12 and ATT2C15 364-Pin CPGA Pinout

| Pin | 2C12 Pad | 2C15 Pad | Function | Pin | 2C12 Pad | 2C15 Pad | Function |
|-----|----------|----------|----------|-----|----------|----------|----------|
| G25 | Vss | Vss | Vss | A19 | PL9D | PL10D | I/O |
| J27 | Vdd | Vdd | Vdd | D18 | PL9C | PL10C | I/O |
| G23 | Vss | Vss | Vss | B18 | PL9B | PL10B | I/O |
| E29 | PL1D | PL1D | I/O | C17 | PL9A | PL10A | I/O-A7 |
| B32 | PL1C | PL1C | I/O | G7 | Vdd | Vdd | Vdd |
| D28 | PL1B | PL1B | I/O | E17 | PL10D | PL11D | I/O |
| A33 | PL1A | PL1A | I/O | A17 | PL10C | PL11C | I/O |
| C29 | PL2D | PL2D | I/O-A0 | D16 | PL10B | PL11B | I/O |
| E27 | See Note | PL2C | I/O | B16 | PL10A | PL11A | I/O-A8 |
| B30 | See Note | PL2B | I/O | G15 | Vss | Vss | Vss |
| F26 | PL2C | PL2A | I/O | A15 | PL11D | PL12D | I/O-A9 |
| A31 | PL2B | PL3D | I/O | F16 | PL11C | PL12C | I/O |
| D26 | See Note | PL3C | I/O | B14 | PL11B | PL12B | I/O |
| C27 | See Note | PL3B | I/O | C15 | PL11A | PL12A | I/O-A10 |
| E25 | PL2A | PL3A | I/O | A13 | PL12D | PL13D | I/O |
| G21 | Vss | Vss | Vss | E15 | PL12C | PL13C | I/O |
| B28 | PL3D | PL4D | I/O | A11 | PL12B | PL13B | I/O |
| F24 | PL3C | PL4C | I/O | D14 | PL12A | PL13A | I/O-A11 |
| A29 | PL3B | PL4B | I/O | C13 | PL13D | PL14D | I/O-A12 |
| D24 | PL3A | PL4A | I/O | B12 | PL13C | PL14C | I/O |
| C25 | PL4D | PL5D | I/O | F14 | PL13B | PL14B | I/O |
| E23 | PL4C | PL5C | I/O | A9 | PL13A | PL14A | I/O |
| B26 | PL4B | PL5B | I/O | E13 | PL14D | PL15D | I/O |
| F22 | PL4A | PL5A | I/O-A1 | B10 | PL14C | PL15C | I/O |
| G19 | Vss | Vss | Vss | D12 | PL14B | PL15B | I/O-A13 |
| D22 | PL5D | PL6D | I/O | C11 | PL14A | PL15A | I/O |
| A27 | PL5C | PL6C | I/O | G13 | Vss | Vss | Vss |
| E21 | PL5B | PL6B | I/O | F12 | PL15D | PL16D | I/O |
| C23 | PL5A | PL6A | I/O-A2 | A7 | PL15C | PL16C | I/O |
| F20 | PL6D | PL7D | I/O | E11 | PL15B | PL16B | I/O |
| B24 | PL6C | PL7C | I/O | B8 | PL15A | PL16A | I/O |
| C21 | PL6B | PL7B | I/O | D10 | PL16D | PL17D | I/O-A14 |
| A25 | PL6A | PL7A | I/O-A3 | C9 | PL16C | PL17C | I/O |
| G27 | Vdd | Vdd | Vdd | F10 | PL16B | PL17B | I/O |
| B22 | PL7D | PL8D | I/O | A5 | PL16A | PL17A | I/O |
| D20 | PL7C | PL8C | I/O | G11 | Vss | Vss | Vss |
| A23 | PL7B | PL8B | I/O | E9 | PL17D | PL18D | I/O |
| E19 | PL7A | PL8A | I/O-A4 | B6 | PL17C | PL18C | I/O |
| A21 | PL8D | PL9D | I/O-A5 | D8 | See Note | PL18B | I/O |
| C19 | PL8C | PL9C | I/O | C7 | PL17B | PL18A | I/O |
| B20 | PL8B | PL9B | I/O | F8 | PL17A | PL19D | I/O |
| F18 | PL8A | PL9A | I/O-A6 | A3 | PL18D | PL19C | I/O |
| G17 | Vss | Vss | Vss | E7 | See Note | PL19B | I/O |

Notes: The ATT2C12 does not have bond pads connected to 364-pin CPGA package pin numbers E27, B30, D26, C27, D8, E7, D6, C3, B2, G5, D2, H4, AF4, AL1, AG5, AL3, AK6, AM4, AH8, AJ9, AN31, AK26, AH26, AL29, AH30, AG29, AK32, AG31, F32, H30, C33, and G29. The J9 pin is used for package orientation only. The ceramic PGA contains single large Vdd and Vss planes to which all Vdd and Vss bond pads are connected.

Pin Information (continued)

Table 24. ATT2C12 and ATT2C15 364-Pin CPGA Pinout (continued)

| Pin | 2C12 Pad | 2C15 Pad | Function | Pin | 2C12 Pad | 2C15 Pad | Function |
|-----|----------|----------|----------|-----|----------|----------|------------------|
| B4 | PL18C | PL19A | I/O | L1 | PB7C | PB8C | I/O |
| C5 | PL18B | PL20D | I/O | R5 | PB7D | PB8D | I/O |
| D6 | See Note | PL20C | I/O | N1 | PB8A | PB9A | I/O |
| C3 | See Note | PL20B | I/O | R3 | PB8B | PB9B | I/O |
| F6 | PL18A | PL20A | I/O-A15 | P2 | PB8C | PB9C | I/O |
| G9 | Vss | Vss | Vss | T6 | PB8D | PB9D | I/O |
| D4 | CCLK | CCLK | CCLK | R1 | PB9A | PB10A | I/O |
| J7 | Vdd | Vdd | Vdd | T4 | PB9B | PB10B | I/O |
| L7 | Vdd | Vdd | Vdd | T2 | PB9C | PB10C | I/O |
| R7 | Vss | Vss | Vss | U3 | PB9D | PB10D | I/O |
| E5 | PB1A | PB1A | I/O-A16 | U7 | Vss | Vss | Vss |
| B2 | See Note | PB1B | I/O | U5 | PB10A | PB11A | I/O |
| F4 | PB1B | PB1C | I/O | U1 | PB10B | PB11B | I/O |
| A1 | PB1C | PB1D | I/O | V4 | PB10C | PB11C | I/O |
| E3 | PB1D | PB2A | I/O | V2 | PB10D | PB11D | I/O |
| G5 | See Note | PB2B | I/O | W1 | PB11A | PB12A | I/O |
| D2 | See Note | PB2C | I/O | V6 | PB11B | PB12B | I/O |
| H6 | PB2A | PB2D | I/O | Y2 | PB11C | PB12C | I/O |
| C1 | PB2B | PB3A | I/O | W3 | PB11D | PB12D | I/O |
| H4 | See Note | PB3B | I/O | AA1 | PB12A | PB13A | I/O-HDC |
| G3 | PB2C | PB3C | I/O | W5 | PB12B | PB13B | I/O |
| J5 | PB2D | PB3D | I/O | AC1 | PB12C | PB13C | I/O |
| F2 | PB3A | PB4A | I/O | Y4 | PB12D | PB13D | I/O |
| K6 | PB3B | PB4B | I/O | AA7 | Vdd | Vdd | Vdd |
| E1 | PB3C | PB4C | I/O | AA3 | PB13A | PB14A | I/O-LD \bar{C} |
| K4 | PB3D | PB4D | I/O-A17 | AB2 | PB13B | PB14B | I/O |
| J3 | PB4A | PB5A | I/O | Y6 | PB13C | PB14C | I/O |
| L5 | PB4B | PB5B | I/O | AE1 | PB13D | PB14D | I/O |
| H2 | PB4C | PB5C | I/O | AA5 | PB14A | PB15A | I/O |
| M6 | PB4D | PB5D | I/O | AD2 | PB14B | PB15B | I/O |
| M4 | PB5A | PB6A | I/O | AB4 | PB14C | PB15C | I/O |
| G1 | PB5B | PB6B | I/O | AC3 | PB14D | PB15D | I/O |
| N5 | PB5C | PB6C | I/O | AB6 | PB15A | PB16A | I/O-INIT |
| L3 | PB5D | PB6D | I/O | AG1 | PB15B | PB16B | I/O |
| P6 | PB6A | PB7A | I/O | AC5 | PB15C | PB16C | I/O |
| K2 | PB6B | PB7B | I/O | AF2 | PB15D | PB16D | I/O |
| N3 | PB6C | PB7C | I/O | AD4 | PB16A | PB17A | I/O |
| J1 | PB6D | PB7D | I/O | AE3 | PB16B | PB17B | I/O |
| N7 | Vdd | Vdd | Vdd | AD6 | PB16C | PB17C | I/O |
| M2 | PB7A | PB8A | I/O | AJ1 | PB16D | PB17D | I/O |
| P4 | PB7B | PB8B | I/O | AE5 | PB17A | PB18A | I/O |

Notes: The ATT2C12 does not have bond pads connected to 364-pin CPGA package pin numbers E27, B30, D26, C27, D8, E7, D6, C3, B2, G5, D2, H4, AF4, AL1, AG5, AL3, AK6, AM4, AH8, AJ9, AN31, AK26, AH26, AL29, AH30, AG29, AK32, AG31, F32, H30, C33, and G29. The J9 pin is used for package orientation only. The ceramic PGA contains single large Vdd and Vss planes to which all Vdd and Vss bond pads are connected.

Pin Information (continued)

Table 24. ATT2C12 and ATT2C15 364-Pin CPGA Pinout (continued)

| Pin | 2C12 Pad | 2C15 Pad | Function | Pin | 2C12 Pad | 2C15 Pad | Function |
|------|----------|----------|----------|------|----------|----------|----------|
| AH2 | PB17B | PB18B | I/O | AM12 | PR13C | PR14C | I/O |
| AF4 | See Note | PB18C | I/O | AL13 | PR13D | PR14D | I/O |
| AG3 | PB17C | PB18D | I/O | AE7 | VDD | VDD | VDD |
| AF6 | PB17D | PB19A | I/O | AK14 | PR12A | PR13A | I/O-M2 |
| AL1 | See Note | PB19B | I/O | AN11 | PR12B | PR13B | I/O |
| AG5 | See Note | PB19C | I/O | AJ15 | PR12C | PR13C | I/O |
| AK2 | PB18A | PB19D | I/O | AN13 | PR12D | PR13D | I/O |
| AJ3 | PB18B | PB20A | I/O | AL15 | PR11A | PR12A | I/O-M3 |
| AH4 | PB18C | PB20B | I/O | AM14 | PR11B | PR12B | I/O |
| AL3 | See Note | PB20C | I/O | AH16 | PR11C | PR12C | I/O |
| AH6 | PB18D | PB20D | I/O | AN15 | PR11D | PR12D | I/O |
| W7 | VSS | VSS | VSS | AG15 | VSS | VSS | VSS |
| AK4 | DONE | DONE | DONE | AK16 | PR10A | PR11A | I/O |
| AC7 | VDD | VDD | VDD | AM16 | PR10B | PR11B | I/O |
| AG11 | VSS | VSS | VSS | AJ17 | PR10C | PR11C | I/O |
| AM2 | RESET | RESET | RESET | AN17 | PR10D | PR11D | I/O |
| AJ5 | PRGM | PRGM | PRGM | AG7 | VDD | VDD | VDD |
| AN1 | PR18A | PR20A | I/O-M0 | AL17 | PR9A | PR10A | I/O |
| AK6 | See Note | PR20B | I/O | AK18 | PR9B | PR10B | I/O |
| AL5 | PR18B | PR20C | I/O | AM18 | PR9C | PR10C | I/O |
| AJ7 | PR18C | PR20D | I/O | AN19 | PR9D | PR10D | I/O |
| AG9 | PR18D | PR19A | I/O | AG17 | VSS | VSS | VSS |
| AM4 | See Note | PR19B | I/O | AH18 | PR8A | PR9A | I/O |
| AH8 | See Note | PR19C | I/O | AM20 | PR8B | PR9B | I/O |
| AN3 | PR17A | PR19D | I/O | AL19 | PR8C | PR9C | I/O |
| AK8 | PR17B | PR18A | I/O | AN21 | PR8D | PR9D | I/O |
| AL7 | PR17C | PR18B | I/O | AJ19 | PR7A | PR8A | I/O-CS1 |
| AJ9 | See Note | PR18C | I/O | AN23 | PR7B | PR8B | I/O |
| AM6 | PR17D | PR18D | I/O | AK20 | PR7C | PR8C | I/O |
| AG13 | VSS | VSS | VSS | AM22 | PR7D | PR8D | I/O |
| AH10 | PR16A | PR17A | I/O | AG27 | VDD | VDD | VDD |
| AN5 | PR16B | PR17B | I/O | AN25 | PR6A | PR7A | I/O-CS0 |
| AK10 | PR16C | PR17C | I/O | AL21 | PR6B | PR7B | I/O |
| AL9 | PR16D | PR17D | I/O | AM24 | PR6C | PR7C | I/O |
| AJ11 | PR15A | PR16A | I/O | AH20 | PR6D | PR7D | I/O |
| AM8 | PR15B | PR16B | I/O | AL23 | PR5A | PR6A | I/O |
| AH12 | PR15C | PR16C | I/O | AJ21 | PR5B | PR6B | I/O |
| AN7 | PR15D | PR16D | I/O-M1 | AN27 | PR5C | PR6C | I/O |
| AL11 | PR14A | PR15A | I/O | AK22 | PR5D | PR6D | I/O |
| AK12 | PR14B | PR15B | I/O | AG19 | VSS | VSS | VSS |
| AM10 | PR14C | PR15C | I/O | AM26 | PR4A | PR5A | I/O-RD |
| AJ13 | PR14D | PR15D | I/O | AH22 | PR4B | PR5B | I/O |
| AN9 | PR13A | PR14A | I/O | AL25 | PR4C | PR5C | I/O |
| AH14 | PR13B | PR14B | I/O | AJ23 | PR4D | PR5D | I/O |

Notes: The ATT2C12 does not have bond pads connected to 364-pin CPGA package pin numbers E27, B30, D26, C27, D8, E7, D6, C3, B2, G5, D2, H4, AF4, AL1, AG5, AL3, AK6, AM4, AH8, AJ9, AN31, AK26, AH26, AL29, AH30, AG29, AK32, AG31, F32, H30, C33, and G29. The J9 pin is used for package orientation only. The ceramic PGA contains single large VDD and VSS planes to which all VDD and VSS bond pads are connected.

Pin Information (continued)

Table 24. ATT2C12 and ATT2C15 364-Pin CPGA Pinout (continued)

| Pin | 2C12 Pad | 2C15 Pad | Function | Pin | 2C12 Pad | 2C15 Pad | Function |
|------|----------|----------|--------------|------|----------|----------|------------|
| AN29 | PR3A | PR4A | I/O | AA29 | PT14B | PT15B | I/O |
| AK24 | PR3B | PR4B | I/O | AC31 | PT14A | PT15A | I/O |
| AM28 | PR3C | PR4C | I/O | Y28 | PT13D | PT14D | I/O |
| AH24 | PR3D | PR4D | I/O | AD32 | PT13C | PT14C | I/O |
| AG21 | Vss | Vss | Vss | AA31 | PT13B | PT14B | I/O-D6 |
| AL27 | PR2A | PR3A | I/O-WR | AE33 | PT13A | PT14A | I/O |
| AJ25 | PR2B | PR3B | I/O | AA27 | Vdd | Vdd | Vdd |
| AN31 | See Note | PR3C | I/O | AB32 | PT12D | PT13D | I/O |
| AK26 | See Note | PR3D | I/O | Y30 | PT12C | PT13C | I/O |
| AM30 | PR2C | PR2A | I/O | AC33 | PT12B | PT13B | I/O |
| AH26 | See Note | PR2B | I/O | W29 | PT12A | PT13A | I/O-D5 |
| AL29 | See Note | PR2C | I/O | AA33 | PT11D | PT12D | I/O |
| AG25 | PR2D | PR2D | I/O | W31 | PT11C | PT12C | I/O |
| AJ27 | PR1A | PR1A | I/O | Y32 | PT11B | PT12B | I/O |
| AL31 | PR1B | PR1B | I/O | V28 | PT11A | PT12A | I/O-D4 |
| AK28 | PR1C | PR1C | I/O | W33 | PT10D | PT11D | I/O |
| AK30 | PR1D | PR1D | I/O | V30 | PT10C | PT11C | I/O |
| AG23 | Vss | Vss | Vss | V32 | PT10B | PT11B | I/O |
| AH28 | RD_CFGN | RD_CFGN | RD_CFGN | U31 | PT10A | PT11A | I/O-D3 |
| AE27 | Vdd | Vdd | Vdd | U27 | Vss | Vss | Vss |
| AC27 | Vdd | Vdd | Vdd | U29 | PT9D | PT10D | I/O |
| W27 | Vss | Vss | Vss | U33 | PT9C | PT10C | I/O |
| AJ29 | PT18D | PT20D | I/O | T30 | PT9B | PT10B | I/O |
| AM32 | PT18C | PT20C | I/O | T32 | PT9A | PT10A | I/O-D2 |
| AH30 | See Note | PT20B | I/O | R33 | PT8D | PT9D | I/O-D1 |
| AN33 | PT18B | PT20A | I/O | T28 | PT8C | PT9C | I/O |
| AJ31 | PT18A | PT19D | I/O | P32 | PT8B | PT9B | I/O |
| AG29 | See Note | PT19C | I/O | R31 | PT8A | PT9A | I/O-D0/DIN |
| AK32 | See Note | PT19B | I/O | N33 | PT7D | PT8D | I/O |
| AF28 | PT17D | PT19A | I/O-RDY/RCLK | R29 | PT7C | PT8C | I/O |
| AL33 | PT17C | PT18D | I/O | L33 | PT7B | PT8B | I/O |
| AF30 | PT17B | PT18C | I/O | P30 | PT7A | PT8A | I/O-DOUT |
| AG31 | See Note | PT18B | I/O | N27 | Vdd | Vdd | Vdd |
| AE29 | PT17A | PT18A | I/O | N31 | PT6D | PT7D | I/O |
| AH32 | PT16D | PT17D | I/O | M32 | PT6C | PT7C | I/O |
| AD28 | PT16C | PT17C | I/O | P28 | PT6B | PT7B | I/O |
| AJ33 | PT16B | PT17B | I/O | J33 | PT6A | PT7A | I/O |
| AD30 | PT16A | PT17A | I/O | N29 | PT5D | PT6D | I/O |
| AE31 | PT15D | PT16D | I/O-D7 | K32 | PT5C | PT6C | I/O |
| AC29 | PT15C | PT16C | I/O | M30 | PT5B | PT6B | I/O |
| AF32 | PT15B | PT16B | I/O | L31 | PT5A | PT6A | I/O-TDI |
| AB28 | PT15A | PT16A | I/O | M28 | PT4D | PT5D | I/O |
| AB30 | PT14D | PT15D | I/O | G33 | PT4C | PT5C | I/O |

Notes: The ATT2C12 does not have bond pads connected to 364-pin CPGA package pin numbers E27, B30, D26, C27, D8, E7, D6, C3, B2, G5, D2, H4, AF4, AL1, AG5, AL3, AK6, AM4, AH8, AJ9, AN31, AK26, AH26, AL29, AH30, AG29, AK32, AG31, F32, H30, C33, and G29. The J9 pin is used for package orientation only. The ceramic PGA contains single large Vdd and Vss planes to which all Vdd and Vss bond pads are connected.

Pin Information (continued)

Table 24. ATT2C12 and ATT2C15 364-Pin CPGA Pinout (continued)

| Pin | 2C12 Pad | 2C15 Pad | Function | Pin | 2C12 Pad | 2C15 Pad | Function |
|------|----------|----------|----------|-----|-------------|-------------|-------------|
| AG33 | PT14C | PT15C | I/O | L29 | PT4B | PT5B | I/O |
| H32 | PT4A | PT5A | I/O | C33 | See Note | PT2C | I/O |
| K30 | PT3D | PT4D | I/O | G29 | See Note | PT2B | I/O |
| J31 | PT3C | PT4C | I/O | D32 | PT2A | PT2A | I/O |
| K28 | PT3B | PT4B | I/O | E31 | PT1D | PT1D | I/O |
| E33 | PT3A | PT4A | I/O-TMS | F30 | PT1C | PT1C | I/O |
| J29 | PT2D | PT3D | I/O | C31 | PT1B | PT1B | I/O |
| F32 | See Note | PT3C | I/O | F28 | PT1A | PT1A | I/O-TCK |
| H30 | See Note | PT3B | I/O | R27 | Vss | Vss | Vss |
| G31 | PT2C | PT3A | I/O | D30 | RD_DATA/TDO | RD_DATA/TDO | RD_DATA/TDO |
| H28 | PT2B | PT2D | I/O | L27 | VDD | VDD | VDD |

Notes: The ATT2C12 does not have bond pads connected to 364-pin CPGA package pin numbers E27, B30, D26, C27, D8, E7, D6, C3, B2, G5, D2, H4, AF4, AL1, AG5, AL3, AK6, AM4, AH8, AJ9, AN31, AK26, AH26, AL29, AH30, AG29, AK32, AG31, F32, H30, C33, and G29. The J9 pin is used for package orientation only. The ceramic PGA contains single large VDD and VSS planes to which all VDD and VSS bond pads are connected.

Pin Information (continued)

Table 25. ATT2C26 and ATT2C40 428-Pin CPGA Pinout

| Pin | 2C26 Pad | 2C40 Pad | Function | Pin | 2C26 Pad | 2C40 Pad | Function |
|------|----------|----------|----------|-----|----------|----------|----------|
| D34 | Vss | Vss | Vss | B22 | PL10B | PL13B | I/O |
| AL33 | Vdd | Vdd | Vdd | F20 | PL10A | PL13A | I/O |
| E33 | Vss | Vss | Vss | C21 | PL11D | PL14D | I/O |
| C33 | PL1D | PL1D | I/O | D20 | PL11C | PL14C | I/O |
| D32 | PL1C | PL1A | I/O | A21 | PL11B | PL14B | I/O |
| B32 | PL1B | PL2D | I/O | G19 | PL11A | PL14A | I/O-A6 |
| E29 | PL1A | PL2A | I/O | F32 | Vss | Vss | Vss |
| F28 | PL2D | PL3D | I/O-A0 | B20 | PL12D | PL15D | I/O |
| C31 | PL2C | PL3C | I/O | F18 | PL12C | PL15C | I/O |
| G27 | PL2B | PL3B | I/O | C19 | PL12B | PL15B | I/O |
| A31 | PL2A | PL3A | I/O | E19 | PL12A | PL15A | I/O-A7 |
| H26 | PL3D | PL4D | I/O | H18 | Vdd | Vdd | Vdd |
| D30 | PL3C | PL4C | I/O | E17 | PL13D | PL16D | I/O |
| D28 | PL3B | PL4B | I/O | A19 | PL13C | PL16C | I/O |
| B30 | PL3A | PL4A | I/O | D18 | PL13B | PL16B | I/O |
| F26 | PL4D | PL5D | I/O | B18 | PL13A | PL16A | I/O-A8 |
| C29 | PL4C | PL5C | I/O | G31 | Vss | Vss | Vss |
| G25 | PL4B | PL5B | I/O | D14 | PL14D | PL17D | I/O-A9 |
| A29 | PL4A | PL6D | I/O | A17 | PL14C | PL17C | I/O |
| E27 | PL5D | PL7D | I/O | G17 | PL14B | PL17B | I/O |
| B28 | PL5C | PL7C | I/O | C17 | PL14A | PL17A | I/O |
| H24 | PL5B | PL7B | I/O | F16 | PL15D | PL18D | I/O |
| C27 | PL5A | PL8D | I/O-A1 | B16 | PL15C | PL18C | I/O |
| E25 | PL6D | PL9D | I/O | E15 | PL15B | PL18B | I/O |
| A27 | PL6C | PL9C | I/O | D16 | PL15A | PL18A | I/O-A10 |
| G23 | PL6B | PL9B | I/O | E13 | PL16D | PL19D | I/O |
| D26 | PL6A | PL9A | I/O-A2 | A15 | PL16C | PL19C | I/O |
| F24 | PL7D | PL10D | I/O | F14 | PL16B | PL19B | I/O |
| B26 | PL7C | PL10C | I/O | C15 | PL16A | PL19A | I/O |
| D24 | PL7B | PL10B | I/O | H16 | PL17D | PL20D | I/O |
| C25 | PL7A | PL10A | I/O-A3 | B14 | PL17C | PL20C | I/O |
| H22 | Vdd | Vdd | Vdd | G15 | PL17B | PL20B | I/O |
| A25 | PL8D | PL11D | I/O | A13 | PL17A | PL20A | I/O-A11 |
| E23 | PL8C | PL11C | I/O | H14 | Vdd | Vdd | Vdd |
| B24 | PL8B | PL11B | I/O | C13 | PL18D | PL21D | I/O-A12 |
| F22 | PL8A | PL11A | I/O | D10 | PL18C | PL21C | I/O |
| C23 | PL9D | PL12D | I/O | B12 | PL18B | PL21B | I/O |
| G21 | PL9C | PL12C | I/O | E11 | PL18A | PL21A | I/O |
| A23 | PL9B | PL12B | I/O | D12 | PL19D | PL22D | I/O |
| H20 | PL9A | PL12A | I/O-A4 | F12 | PL19C | PL22C | I/O |
| D22 | PL10D | PL13D | I/O-A5 | A11 | PL19B | PL22B | I/O-A13 |
| E21 | PL10C | PL13C | I/O | G13 | PL19A | PL22A | I/O |

Note: The ceramic PGA contains single large Vdd and Vss planes to which all Vdd and Vss bond pads are connected.

Pin Information (continued)

Table 25. ATT2C26 and ATT2C40 428-Pin CPGA Pinout (continued)

| Pin | 2C26 Pad | 2C40 Pad | Function | Pin | 2C26 Pad | 2C40 Pad | Function |
|------|----------|----------|----------|-----|----------|----------|----------|
| C11 | PL20D | PL23D | I/O | L3 | PB5C | PB6C | I/O |
| E9 | PL20C | PL23C | I/O | M6 | PB5D | PB6D | I/O |
| B10 | PL20B | PL24D | I/O | L1 | PB6A | PB7A | I/O |
| H12 | PL20A | PL25D | I/O | N7 | PB6B | PB7D | I/O |
| A9 | PL21D | PL25A | I/O-A14 | M4 | PB6C | PB8A | I/O |
| F10 | PL21C | PL26C | I/O | N5 | PB6D | PB8D | I/O |
| C9 | PL21B | PL26B | I/O | M2 | PB7A | PB9A | I/O |
| G11 | PL21A | PL26A | I/O | P6 | PB7B | PB9D | I/O |
| B8 | PL22D | PL27D | I/O | N3 | PB7C | PB10A | I/O |
| E7 | PL22C | PL27C | I/O | P4 | PB7D | PB10D | I/O |
| D8 | PL22B | PL27B | I/O | P8 | VDD | VDD | VDD |
| F8 | PL22A | PL27A | I/O | R7 | PB8A | PB11A | I/O |
| A7 | PL23D | PL28D | I/O | N1 | PB8B | PB11B | I/O |
| G9 | PL23C | PL28C | I/O | T8 | PB8C | PB11C | I/O |
| C7 | PL23B | PL28B | I/O | P2 | PB8D | PB11D | I/O |
| H10 | PL23A | PL28A | I/O | R5 | PB9A | PB12A | I/O |
| D6 | PL24D | PL29A | I/O | R3 | PB9B | PB12B | I/O |
| B6 | PL24C | PL30C | I/O | T6 | PB9C | PB12C | I/O |
| F4 | PL24B | PL30B | I/O | R1 | PB9D | PB12D | I/O |
| C5 | PL24A | PL30A | I/O-A15 | T4 | PB10A | PB13A | I/O |
| H30 | VSS | VSS | VSS | U7 | PB10B | PB13B | I/O |
| G5 | CCLK | CCLK | CCLK | T2 | PB10C | PB13C | I/O |
| AM34 | VDD | VDD | VDD | U5 | PB10D | PB13D | I/O |
| AN35 | VDD | VDD | VDD | U3 | PB11A | PB14A | I/O |
| D4 | VSS | VSS | VSS | V4 | PB11B | PB14B | I/O |
| H6 | PB1A | PB1A | I/O-A16 | U1 | PB11C | PB14C | I/O |
| E3 | PB1B | PB1B | I/O | V6 | PB11D | PB14D | I/O |
| J7 | PB1C | PB2A | I/O | E5 | VSS | VSS | VSS |
| F2 | PB1D | PB2D | I/O | V2 | PB12A | PB15A | I/O |
| G3 | PB2A | PB3A | I/O | W5 | PB12B | PB15B | I/O |
| J5 | PB2B | PB3B | I/O | W3 | PB12C | PB15C | I/O |
| G1 | PB2C | PB3C | I/O | W7 | PB12D | PB15D | I/O |
| K8 | PB2D | PB3D | I/O | F6 | VSS | VSS | VSS |
| H4 | PB3A | PB4A | I/O | W1 | PB13A | PB16A | I/O |
| K6 | PB3B | PB4B | I/O | Y4 | PB13B | PB16B | I/O |
| H2 | PB3C | PB4C | I/O | Y2 | PB13C | PB16C | I/O |
| K4 | PB3D | PB4D | I/O | Y6 | PB13D | PB16D | I/O |
| J3 | PB4A | PB5A | I/O | G7 | VSS | VSS | VSS |
| L7 | PB4B | PB5B | I/O | AA1 | PB14A | PB17A | I/O |
| J1 | PB4C | PB5C | I/O | Y8 | PB14B | PB17B | I/O |
| M8 | PB4D | PB5D | I/O-A17 | AA3 | PB14C | PB17C | I/O |
| K2 | PB5A | PB6A | I/O | AA5 | PB14D | PB17D | I/O |
| L5 | PB5B | PB6B | I/O | AB2 | PB15A | PB18A | I/O |

Note: The ceramic PGA contains single large VDD and VSS planes to which all VDD and VSS bond pads are connected.

Pin Information (continued)

Table 25. ATT2C26 and ATT2C40 428-Pin CPGA Pinout (continued)

| Pin | 2C26 Pad | 2C40 Pad | Function | Pin | 2C26 Pad | 2C40 Pad | Function |
|-----|----------|----------|----------|------|----------|----------|----------|
| AA7 | PB15B | PB18B | I/O | AR5 | RESET | RESET | RESET |
| AB4 | PB15C | PB18C | I/O | AP6 | PRGM | PRGM | PRGM |
| AB6 | PB15D | PB18D | I/O | AT6 | PR24A | PR30A | I/O-M0 |
| AC5 | PB16A | PB19A | I/O-HDC | AN7 | PR24B | PR30B | I/O |
| AC1 | PB16B | PB19B | I/O | AR7 | PR24C | PR29A | I/O |
| AD4 | PB16C | PB19C | I/O | AM8 | PR24D | PR29D | I/O |
| AC3 | PB16D | PB19D | I/O | AK32 | VDD | VDD | VDD |
| AD6 | PB17A | PB20A | I/O | AK10 | PR23A | PR28A | I/O |
| AD2 | PB17B | PB20B | I/O | AU7 | PR23B | PR28B | I/O |
| AC7 | PB17C | PB20C | I/O | AL9 | PR23C | PR28C | I/O |
| AE1 | PB17D | PB20D | I/O | AP8 | PR23D | PR28D | I/O |
| V8 | VDD | VDD | VDD | AN9 | PR22A | PR27A | I/O |
| AE3 | PB18A | PB21A | I/O-LDC | AT8 | PR22B | PR27B | I/O |
| AE5 | PB18B | PB21D | I/O | AL11 | PR22C | PR27C | I/O |
| AF2 | PB18C | PB22A | I/O | AR9 | PR22D | PR27D | I/O |
| AG5 | PB18D | PB22D | I/O | AP4 | VSS | VSS | VSS |
| AF4 | PB19A | PB23A | I/O | AK12 | PR21A | PR26A | I/O |
| AF6 | PB19B | PB24A | I/O | AU9 | PR21B | PR26B | I/O |
| AG1 | PB19C | PB24C | I/O | AM10 | PR21C | PR26C | I/O |
| AD8 | PB19D | PB24D | I/O | AT10 | PR21D | PR25A | I/O |
| AG3 | PB20A | PB25A | I/O-INIT | AP10 | PR20A | PR24A | I/O |
| AE7 | PB20B | PB25B | I/O | AR11 | PR20B | PR24B | I/O |
| AH2 | PB20C | PB25C | I/O | AL13 | PR20C | PR24D | I/O |
| AH4 | PB20D | PB25D | I/O | AU11 | PR20D | PR23D | I/O-M1 |
| AJ1 | PB21A | PB26A | I/O | AK14 | PR19A | PR22A | I/O |
| AH6 | PB21B | PB26B | I/O | AP12 | PR19B | PR22B | I/O |
| AJ3 | PB21C | PB26C | I/O | AM12 | PR19C | PR22C | I/O |
| AF8 | PB21D | PB26D | I/O | AT12 | PR19D | PR22D | I/O |
| AK2 | PB22A | PB27A | I/O | AN11 | PR18A | PR21A | I/O |
| AG7 | PB22B | PB27B | I/O | AR13 | PR18B | PR21B | I/O |
| AK4 | PB22C | PB27C | I/O | AN13 | PR18C | PR21C | I/O |
| AJ5 | PB22D | PB27D | I/O | AU13 | PR18D | PR21D | I/O |
| AL1 | PB23A | PB28A | I/O | AK16 | VDD | VDD | VDD |
| AJ7 | PB23B | PB28B | I/O | AT14 | PR17A | PR20A | I/O-M2 |
| AL3 | PB23C | PB28C | I/O | AL15 | PR17B | PR20B | I/O |
| AH8 | PB23D | PB28D | I/O | AR15 | PR17C | PR20C | I/O |
| AK6 | PB24A | PB29A | I/O | AM14 | PR17D | PR20D | I/O |
| AM2 | PB24B | PB29D | I/O | AU15 | PR16A | PR19A | I/O |
| AL5 | PB24C | PB30C | I/O | AP14 | PR16B | PR19B | I/O |
| AN3 | PB24D | PB30D | I/O | AP16 | PR16C | PR19C | I/O |
| H8 | VSS | VSS | VSS | AN15 | PR16D | PR19D | I/O |
| AM4 | DONE | DONE | DONE | AT16 | PR15A | PR18A | I/O-M3 |
| AB8 | VDD | VDD | VDD | AM16 | PR15B | PR18B | I/O |

Note: The ceramic PGA contains single large VDD and VSS planes to which all VDD and VSS bond pads are connected.

Pin Information (continued)

Table 25. ATT2C26 and ATT2C40 428-Pin CPGA Pinout (continued)

| Pin | 2C26 Pad | 2C40 Pad | Function | Pin | 2C26 Pad | 2C40 Pad | Function |
|------|----------|----------|----------|------|----------|----------|--------------|
| AR17 | PR15C | PR18C | I/O | AR27 | PR5A | PR8A | I/O-RD |
| AL17 | PR15D | PR18D | I/O | AL25 | PR5B | PR7A | I/O |
| AU17 | PR14A | PR17A | I/O | AT28 | PR5C | PR7C | I/O |
| AN17 | PR14B | PR17B | I/O | AP28 | PR5D | PR6A | I/O |
| AT18 | PR14C | PR17C | I/O | AU29 | PR4A | PR5A | I/O |
| AK18 | PR14D | PR17D | I/O | AM28 | PR4B | PR5B | I/O |
| AN5 | Vss | Vss | Vss | AR29 | PR4C | PR5C | I/O |
| AR19 | PR13A | PR16A | I/O | AK26 | PR4D | PR5D | I/O |
| AM18 | PR13B | PR16B | I/O | AL7 | Vss | Vss | Vss |
| AN19 | PR13C | PR16C | I/O | AT30 | PR3A | PR4A | I/O-WR |
| AP18 | PR13D | PR16D | I/O | AL27 | PR3B | PR4B | I/O |
| AK20 | VDD | VDD | VDD | AP30 | PR3C | PR4C | I/O |
| AL19 | PR12A | PR15A | I/O | AN29 | PR3D | PR4D | I/O |
| AU19 | PR12B | PR15B | I/O | AU31 | PR2A | PR3A | I/O |
| AP20 | PR12C | PR15C | I/O | AL29 | PR2B | PR3B | I/O |
| AT20 | PR12D | PR15D | I/O | AR31 | PR2C | PR3C | I/O |
| AM6 | Vss | Vss | Vss | AK28 | PR2D | PR3D | I/O |
| AM20 | PR11A | PR14A | I/O | AM30 | PR1A | PR2A | I/O |
| AU21 | PR11B | PR14B | I/O | AT32 | PR1B | PR2D | I/O |
| AN21 | PR11C | PR14C | I/O | AN31 | PR1C | PR1A | I/O |
| AR21 | PR11D | PR14D | I/O | AR33 | PR1D | PR1D | I/O |
| AL21 | PR10A | PR13A | I/O | AK8 | Vss | Vss | Vss |
| AT22 | PR10B | PR13B | I/O | AP32 | RD_CFGN | RD_CFGN | RD_CFGN |
| AM22 | PR10C | PR13C | I/O | AJ31 | VDD | VDD | VDD |
| AP22 | PR10D | PR13D | I/O | AH30 | VDD | VDD | VDD |
| AN23 | PR9A | PR12A | I/O-CS1 | AP34 | Vss | Vss | Vss |
| AU23 | PR9B | PR12B | I/O | AJ33 | PT24D | PT30D | I/O |
| AP24 | PR9C | PR12C | I/O | AM36 | PT24C | PT30A | I/O |
| AR23 | PR9D | PR12D | I/O | AH32 | PT24B | PT29B | I/O |
| AK22 | PR8A | PR11A | I/O | AL35 | PT24A | PT29A | I/O |
| AT24 | PR8B | PR11B | I/O | AL37 | PT23D | PT28D | I/O |
| AL23 | PR8C | PR11C | I/O | AH34 | PT23C | PT28C | I/O |
| AU25 | PR8D | PR11D | I/O | AK34 | PT23B | PT28B | I/O |
| AK24 | VDD | VDD | VDD | AG31 | PT23A | PT28A | I/O-RDY/RCLK |
| AR25 | PR7A | PR10A | I/O-CS0 | AK36 | PT22D | PT27D | I/O |
| AM24 | PR7B | PR10B | I/O | AF30 | PT22C | PT27C | I/O |
| AT26 | PR7C | PR10C | I/O | AJ35 | PT22B | PT27B | I/O |
| AN25 | PR7D | PR10D | I/O | AG33 | PT22A | PT27A | I/O |
| AP26 | PR6A | PR9A | I/O | AJ37 | PT21D | PT26D | I/O |
| AN27 | PR6B | PR9B | I/O | AF32 | PT21C | PT26C | I/O |
| AU27 | PR6C | PR9C | I/O | AH36 | PT21B | PT26B | I/O |
| AM26 | PR6D | PR9D | I/O | AE31 | PT21A | PT26A | I/O |

Note: The ceramic PGA contains single large VDD and VSS planes to which all VDD and VSS bond pads are connected.

Pin Information (continued)

Table 25. ATT2C26 and ATT2C40 428-Pin CPGA Pinout (continued)

| Pin | 2C26 Pad | 2C40 Pad | Function | Pin | 2C26 Pad | 2C40 Pad | Function |
|------|-----------------|-----------------|-----------------|------|-----------------|-----------------|-----------------|
| AG35 | PT20D | PT25D | I/O-D7 | T32 | PT10C | PT13C | I/O |
| AE33 | PT20C | PT25C | I/O | T34 | PT10B | PT13B | I/O |
| AG37 | PT20B | PT25B | I/O | N33 | PT10A | PT13A | I/O-D0/DIN |
| AD32 | PT20A | PT25A | I/O | P32 | PT9D | PT12D | I/O |
| AF34 | PT19D | PT24D | I/O | R35 | PT9C | PT12C | I/O |
| AD34 | PT19C | PT24C | I/O | R31 | PT9B | PT12B | I/O |
| AF36 | PT19B | PT24B | I/O | P36 | PT9A | PT12A | I/O |
| AC33 | PT19A | PT23D | I/O | M32 | PT8D | PT11D | I/O |
| AE35 | PT18D | PT22D | I/O | N37 | PT8C | PT11C | I/O |
| AC31 | PT18C | PT22A | I/O | N31 | PT8B | PT11B | I/O |
| AE37 | PT18B | PT21D | I/O-D6 | M36 | PT8A | PT11A | I/O-DOUT |
| AB32 | PT18A | PT21A | I/O | Y30 | V _{DD} | V _{DD} | V _{DD} |
| AD30 | V _{DD} | V _{DD} | V _{DD} | N35 | PT7D | PT10D | I/O |
| AB30 | PT17D | PT20D | I/O | P30 | PT7C | PT10A | I/O |
| AD36 | PT17C | PT20C | I/O | L37 | PT7B | PT9D | I/O |
| Y34 | PT17B | PT20B | I/O | L33 | PT7A | PT9A | I/O |
| AC35 | PT17A | PT20A | I/O | M34 | PT6D | PT8D | I/O |
| AA33 | PT16D | PT19D | I/O | K34 | PT6C | PT8A | I/O |
| AC37 | PT16C | PT19C | I/O | L35 | PT6B | PT7D | I/O |
| AA31 | PT16B | PT19B | I/O | M30 | PT6A | PT7A | I/O-TDI |
| AB34 | PT16A | PT19A | I/O-D5 | J37 | PT5D | PT6D | I/O |
| AB36 | PT15D | PT18D | I/O | L31 | PT5C | PT6C | I/O |
| V34 | PT15C | PT18C | I/O | K36 | PT5B | PT6B | I/O |
| AA35 | PT15B | PT18B | I/O | K32 | PT5A | PT6A | I/O |
| Y32 | PT15A | PT18A | I/O | H36 | PT4D | PT5D | I/O |
| AA37 | PT14D | PT17D | I/O | J33 | PT4C | PT5C | I/O |
| W33 | PT14C | PT17C | I/O | J35 | PT4B | PT5B | I/O |
| Y36 | PT14B | PT17B | I/O | J31 | PT4A | PT5A | I/O-TMS |
| U33 | PT14A | PT17A | I/O-D4 | AL31 | V _{SS} | V _{SS} | V _{SS} |
| W35 | PT13D | PT16D | I/O | G37 | PT3D | PT4D | I/O |
| W31 | PT13C | PT16C | I/O | K30 | PT3C | PT4C | I/O |
| W37 | PT13B | PT16B | I/O | H34 | PT3B | PT4B | I/O |
| V32 | PT13A | PT16A | I/O-D3 | H32 | PT3A | PT4A | I/O |
| AN33 | V _{SS} | V _{SS} | V _{SS} | G35 | PT2D | PT3D | I/O |
| V36 | PT12D | PT15D | I/O | G33 | PT2C | PT3C | I/O |
| P34 | PT12C | PT15C | I/O | F36 | PT2B | PT3B | I/O |
| U37 | PT12B | PT15B | I/O | E31 | PT2A | PT3A | I/O |
| V30 | PT12A | PT15A | I/O-D2 | F30 | PT1D | PT2D | I/O |
| AM32 | V _{SS} | V _{SS} | V _{SS} | F34 | PT1C | PT2A | I/O |
| T36 | PT11D | PT14D | I/O-D1 | G29 | PT1B | PT1D | I/O |
| R33 | PT11C | PT14C | I/O | E35 | PT1A | PT1A | I/O-TCK |
| U35 | PT11B | PT14B | I/O | AK30 | V _{SS} | V _{SS} | V _{SS} |
| U31 | PT11A | PT14A | I/O | H28 | RD DATA/TDO | RD DATA/TDO | RD_DATA/TDO |
| R37 | PT10D | PT13D | I/O | T30 | V _{DD} | V _{DD} | V _{DD} |

Note: The ceramic PGA contains single large V_{DD} and V_{SS} planes to which all V_{DD} and V_{SS} bond pads are connected.

Package Thermal Characteristics

When silicon die junction temperature is below the recommended junction temperature of 125 °C, the temperature-activated failure mechanisms are minimized. There are four major factors that affect the thermal resistance value: silicon device size/paddle size, board mounting configuration (board density, multilayer nature of board), package type and size, and system airflow over the package. The values in the table below reflect the capability of the various package types to dissipate heat at given airflow rates. The numbers represent the delta °C/W between the ambient temperature and the device junction temperature.

To test package thermal characteristics, a single package containing a 0.269 in. sq. test IC of each configuration is mounted at the center of a printed-circuit board (PCB) measuring 8 in. x 13 in. x 0.062 in. The assembled PCB is mounted vertically in the center of the rectangular test section of a wind tunnel. The walls of the wind tunnel simulate adjacent boards in the electronic rack and can be adjusted to study the effects of PCB spacing. Forced air at room temperature is supplied by a pair of push-pull blowers which can be regulated to supply the desired air velocities. The air velocity is measured with a hot-wire anemometer at the center of the channel, 3 in. upstream from the package.

A typical test consists of regulating the wind tunnel blowers to obtain the desired air velocity and applying power to the test IC. The power to the IC is adjusted until the maximum junction temperature (as measured by its diodes) reaches 115 °C to 120 °C. The thermal resistance Θ_{JA} (°C/W) is computed by using the power supplied to the IC, junction temperature, ambient temperature, and air velocity:

$$\Theta_{JA} = \frac{T_J - T_A}{Q_C}$$

where:

T_J = peak temperature on the active surface of the IC

T_A = ambient air temperature

Q_C = IC power

The tests are repeated at several velocities from 0 fpm (feet per minute) to 1000 fpm.

The definition of the junction-to-case thermal resistance Θ_{JC} is:

$$\Theta_{JC} = \frac{T_J - T_C}{Q_C}$$

where:

T_C = temperature measured to the thermocouple at the top dead center of the package

The actual Θ_{JC} measurement performed at Lucent, Θ_{J-TDC} , uses a different package mounting arrangement than the one defined for Θ_{JC} in MIL-STD-883D and SEMI standards. Please contact Lucent for a diagram.

The maximum power dissipation for a package is calculated from the maximum allowed junction temperature (T_{Jmax} , 125 °C), the maximum ambient temperature (T_{Amax}), and the junction-to-ambient thermal characteristic for the given package (Θ_{JA}). The maximum power for the package is calculated as follows:

$$\text{Max. Power (Watts)} = (125\text{ °C} - T_{Amax}) \times (1/\Theta_{JA})$$

In Table 26 and Table 26, a maximum power dissipation for each package is shown with $T_{Amax} = 70\text{ °C}$ for the commercial temperature range and the Θ_{JA} used is for 0 feet per minute of air flowing over the package. If your application does not correspond to these parameters, the maximum power dissipation should be recalculated using the formula above.

Once the power dissipated by the FPGA has been determined (see the Estimating Power Dissipation section), the maximum junction temperature of the FPGA can be found. This is needed to determine if speed derating of the device from the 85 °C junction temperature used in all of the delay tables is needed. Using the maximum ambient temperature, T_{Amax} , and the power dissipated by the device, P , the maximum junction temperature is given by:

$$T_{Jmax} = T_{Amax} + (P \cdot \Theta_{JA})\text{ °C}$$

Table 26 and Table 26 list the thermal characteristics for all packages used with the ORCA 2C Series of FPGAs.

Package Thermal Characteristics (continued)

Table 26. ORCA Plastic Package Thermal Characteristics

| Package | Θ_{JA} ($^{\circ}\text{C/W}$) | | | Θ_{JC} ($^{\circ}\text{C/W}$) | Max Power (W) (70 $^{\circ}\text{C}$ —0 fpm) |
|---------------------------|--|-----------|-----------|---|---|
| | 0 fpm | 200 fpm | 400 fpm | | |
| 84-Pin PLCC | 40 | 35 | 32 | 9 | 1.38 |
| 100-Pin TQFP | 61 | 49 | 46 | 6 | 0.9 |
| 144-Pin TQFP | 52 | 39 | 36 | 4 | 1.05 |
| 160-Pin QFP | 40 | 36 | 32 | 8 | 1.38 |
| 208-Pin SQFP | 37 | 33 | 29 | 8 | 1.49 |
| 208-Pin SQFP-PQ2 | 16 | 14 | 12 | 1.3 | 3.43 |
| 240-Pin SQFP | 35 | 31 | 28 | 7 | 1.57 |
| 240-Pin SQFP-PQ2 | 15 | 12 | 10 | 1.3 | 3.66 |
| 256-Pin PBGA ¹ | 21 | 17 (est.) | 14 (est.) | TBD | 2.62 |
| 256-Pin PBGA ² | 28 | 24 (est.) | 22 (est.) | TBD | 1.97 |
| 304-Pin SQFP | 33 | 30 | 27 | 6 | 1.67 |
| 304-Pin SQFP-PQ2 | 12 | 10 | 8 | 1.3 | 4.58 |

Notes:

1. With thermal balls connected to board ground plane.

2. Without thermal balls connected to board ground plane.

Table 27. ORCA Ceramic Package Thermal Characteristics

| Package | Θ_{JA} ($^{\circ}\text{C/W}$) | | | Θ_{JC} ($^{\circ}\text{C/W}$) | Max Power (W) (70 $^{\circ}\text{C}$ —0 fpm) |
|--------------|--|---------|---------|---|---|
| | 0 fpm | 200 fpm | 400 fpm | | |
| 364-Pin CPGA | 18 | 16 | 14 | 2.3 | 3.05 |
| 428-Pin CPGA | 18 | 16 | 14 | 2.3 | 3.05 |

Package Coplanarity

The coplanarity of Lucent Technologies' postmolded packages is 4 mils. The coplanarity of selected packages is scheduled to be reduced to 3.1 mils. All Lucent ORCA Series FPGA ceramic packages are through-hole mount.

Package Parasitics

The electrical performance of an IC package, such as signal quality and noise sensitivity, is directly affected by the package parasitics. Table 28 lists eight parasitics associated with the ORCA packages. These parasitics represent the contributions of all components of a package, which include the bond wires, all internal package routing, and the external leads.

Four inductances in nH are listed: L_w and L_L , the self-inductance of the lead; and L_{mw} and L_{mL} , the mutual inductance to the nearest neighbor lead. These parameters are important in determining ground bounce

noise and inductive crosstalk noise. Three capacitances in pF are listed: C_M , the mutual capacitance of the lead to the nearest neighbor lead; and C_1 and C_2 , the total capacitance of the lead to all other leads (all other leads are assumed to be grounded). These parameters are important in determining capacitive crosstalk and the capacitive loading effect of the lead.

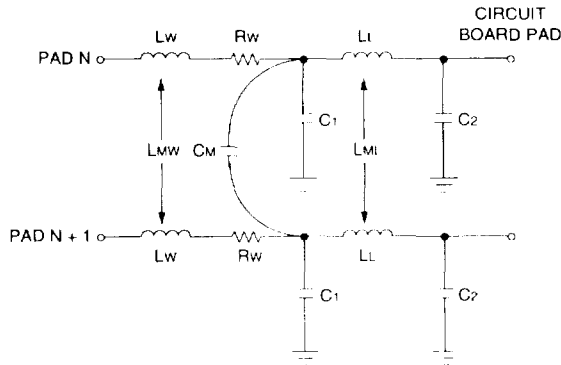
The parasitic values in Table 28 are for the circuit model of bond wire and package lead parasitics. If the mutual capacitance value is not used in the designer's model, then the value listed as mutual capacitance should be added to each of the C_1 and C_2 capacitors. The PGAs contain power and ground planes that will make the inductance value for power and ground leads the minimum value listed. The PGAs also have a significant range of parasitic values. This is due to the large variation in internal trace lengths and is also due to two signal metal layers that are separated from the ground plane by different distances. The upper signal layer is more inductive but less capacitive than the closer, lower signal layer.

Package Parasitics (continued)

Table 28. ORCA 2C Package Parasitics

| Package Type | Lw | Mw | Rw | C1 | C2 | CM | LL | ML |
|------------------|-----|-----|------|-----|-----|---------|-------|-------|
| 84-Pin PLCC | 3 | 1 | 160 | 1 | 1 | 0.5 | 7—11 | 3—6 |
| 100-Pin TQFP | 3 | 1 | 160 | 0.7 | 0.7 | 0.94 | 3—4 | 1.5—2 |
| 144-Pin TQFP | 3.5 | 1.5 | 175 | 1 | 1 | 0.6 | 4—6 | 2—2.5 |
| 160-Pin QFP | 4 | 2 | 200 | 1 | 1 | 1 | 13—17 | 8—11 |
| 208-Pin SQFP | 4 | 2 | 200 | 1 | 1 | 1 | 7—10 | 4—6 |
| 208-Pin SQFP-PQ2 | 4 | 2 | 200 | 1 | 1 | 1 | 6—9 | 4—6 |
| 240-Pin SQFP | 4 | 2 | 200 | 1 | 1 | 1 | 8—12 | 5—8 |
| 240-Pin SQFP-PQ2 | 4 | 2 | 200 | 1 | 1 | 1 | 7—11 | 4—7 |
| 256-Pin PBGA | 5 | 2 | 220 | 1 | 1 | 1 | 5—13 | 2—6 |
| 304-Pin SQFP | 5 | 2 | 220 | 1 | 1 | 1 | 12—18 | 7—12 |
| 304-Pin SQFP-PQ2 | 5 | 2 | 220 | 1 | 1 | 1 | 11—17 | 7—12 |
| 364-Pin CPGA | 2 | 1 | 1000 | 1—2 | 1—2 | 0.5—1 | 2—11* | 1—4 |
| 428-Pin CPGA | 2 | 1 | 1000 | 1—2 | 1—2 | 0.6—1.2 | 2—11* | 1—4 |

* Leads designated as ground (power) can be connected to the ground plane, reducing the trace inductance to the minimum value listed.



5-3862(C)

Figure 48. Package Parasitics

Absolute Maximum Ratings

Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operations sections of this data sheet. Exposure to Absolute Maximum Ratings for extended periods can adversely affect device reliability.

The Lucent ORCA Series FPGAs include circuitry designed to protect the chips from damaging substrate injection currents and prevent accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use to avoid exposure to excessive electrical stress.

2

| Parameter | Symbol | Min | Max | Unit |
|---|------------------|------|-----------------------|------|
| Storage Temperature | T _{stg} | -65 | 150 | °C |
| Supply Voltage with Respect to Ground | V _{DD} | -0.5 | 7.0 | V |
| Input Signal with Respect to Ground | — | -0.5 | V _{DD} + 0.3 | V |
| Signal Applied to High-impedance Output | — | -0.5 | V _{DD} + 0.3 | V |
| Maximum Soldering Temperature | — | — | 260 | °C |

Recommended Operating Conditions

| Mode | Temperature Range (Ambient) | Supply Voltage |
|------------|-----------------------------|----------------|
| Commercial | 0 °C to 70 °C | 5 V ± 5% |
| Industrial | -40 °C to +85 °C | 5 V ± 10% |

Note: The maximum recommended junction temperature, T_J, during operation is 125 °C.

Electrical Characteristics

Table 29. Electrical Characteristics

 Commercial: $V_{DD} = 5.0\text{ V} \pm 5\%$, $0\text{ }^{\circ}\text{C} \leq T_A \leq 70\text{ }^{\circ}\text{C}$; Industrial: $V_{DD} = 5.0\text{ V} \pm 10\%$, $-40\text{ }^{\circ}\text{C} \leq T_A \leq +85\text{ }^{\circ}\text{C}$.

| Parameter | Symbol | Test Conditions | Min | Max | Unit |
|---|-------------------|---|--------------|----------------|---------------|
| Input Voltage: | | Input configured as CMOS | | | |
| High | V_{IH} | | 70% V_{DD} | $V_{DD} + 0.3$ | V |
| Low | V_{IL} | | GND - 0.5 | 20% V_{DD} | V |
| Input Voltage: | | Input configured as TTL | | | |
| High | V_{IH} | | 2.0 | $V_{DD} + 0.3$ | V |
| Low | V_{IL} | | -0.5 | 0.8 | V |
| Output Voltage: | | | | | |
| High | V_{OH} | $V_{DD} = \text{Min}$, $I_{OH} = 6\text{ mA}$ or 3 mA | 2.4 | — | V |
| Low | V_{OL} | $V_{DD} = \text{Min}$, $I_{OL} = 12\text{ mA}$ or 6 mA | — | 0.4 | V |
| Input Leakage Current | IL | $V_{DD} = \text{Max}$, $V_{IN} = V_{SS}$ or V_{DD} | -10 | 10 | μA |
| Standby Current: | I_{DDSB} | $T_A = 25\text{ }^{\circ}\text{C}$, $V_{DD} = 5.0\text{ V}$, internal oscillator running, no output loads, inputs at V_{DD} or GND | — | 6.5 | mA |
| ATT2C04 | | | — | 7.0 | mA |
| ATT2C06 | | | — | 7.7 | mA |
| ATT2C08 | | | — | 8.4 | mA |
| ATT2C10 | | | — | 9.2 | mA |
| ATT2C12 | | | — | 10.0 | mA |
| ATT2C15 | | | — | 12.2 | mA |
| ATT2C26 | | | — | 16.3 | mA |
| ATT2C40 | | | — | | |
| Standby Current: | I_{DDSB} | $T_A = 25\text{ }^{\circ}\text{C}$, $V_{DD} = 5.0\text{ V}$, internal oscillator stopped, no output loads, inputs at V_{DD} or GND | — | 1.5 | mA |
| ATT2C04 | | | — | 2.0 | mA |
| ATT2C06 | | | — | 2.7 | mA |
| ATT2C08 | | | — | 3.4 | mA |
| ATT2C10 | | | — | 4.2 | mA |
| ATT2C12 | | | — | 5.0 | mA |
| ATT2C15 | | | — | 7.2 | mA |
| ATT2C26 | | | — | 11.3 | mA |
| ATT2C40 | | | — | | |
| Data Retention Voltage | VDR | $T_A = 25\text{ }^{\circ}\text{C}$ | 2.3 | — | V |
| Input Capacitance | C_{IN} | $T_A = 25\text{ }^{\circ}\text{C}$, $V_{DD} = 5.0\text{ V}$ Test frequency = 1 MHz | — | 10 | pF |
| Output Capacitance | C_{OUT} | $T_A = 25\text{ }^{\circ}\text{C}$, $V_{DD} = 5.0\text{ V}$ Test frequency = 1 MHz | — | 10 | pF |
| DONE Pull-up Resistor | R _{DONE} | — | 100K | — | Ω |
| M3, M2, M1, and M0 Pull-up Resistors | R _M | — | 100K | — | Ω |
| I/O Pad Static Pull-up Current | I _{PU} | $V_{DD} = 5.25\text{ V}$, $V_{IN} = V_{SS}$, $T_A = 0\text{ }^{\circ}\text{C}$ | 14.4 | 50.9 | μA |
| I/O Pad Static Pull-down Current | I _{PD} | $V_{DD} = 5.25\text{ V}$, $V_{IN} = V_{DD}$, $T_A = 0\text{ }^{\circ}\text{C}$ | 26 | 103 | μA |
| I/O Pad Pull-up Resistor | R _{PU} | $V_{DD} = 5.25\text{ V}$, $V_{IN} = V_{SS}$, $T_A = 0\text{ }^{\circ}\text{C}$ | 100K | — | Ω |
| I/O Pad Pull-down Resistor | R _{PD} | $V_{DD} = 5.25\text{ V}$, $V_{IN} = V_{DD}$, $T_A = 0\text{ }^{\circ}\text{C}$ | 50K | — | Ω |

Timing Characteristics

Table 30. PFU Timing Characteristics

Commercial: VDD = 5.0 V ± 5%, 0 °C ≤ TA ≤ 70 °C; Industrial: VDD = 5.0 V ± 10%, -40 °C ≤ TA ≤ +85 °C.

| Parameter | Symbol | Speed | | | | | | Unit |
|--|------------|-------|-----|-----|-----|-----|-----|------|
| | | -2 | | -3 | | | | |
| | | Min | Max | Min | Max | Min | Max | |
| Input Requirements | | | | | | | | |
| Clock Low Time | TCL | 3.2 | — | 2.5 | — | | | ns |
| Clock High Time | TCH | 3.2 | — | 2.5 | — | | | ns |
| Global S/R Pulse Width (gsrn) | TRW | 2.8 | — | 2.5 | — | | | ns |
| Local S/R Pulse Width | TPW | 3.0 | — | 2.5 | — | | | ns |
| Combinatorial Setup Times (TJ = +85 °C, VDD = Min): | | | | | | | | |
| Four Input Variables to Clock (a[4:0], b[4:0] to ck) | F4* SET | 2.4 | — | 1.7 | — | | | ns |
| Five Input Variables to Clock (a[4:0], b[4:0] to ck) | F5* SET | 2.5 | — | 1.9 | — | | | ns |
| PFUMUX to Clock (a[4:0], b[4:0] to ck) | MUX_SET | 3.9 | — | 2.9 | — | | | ns |
| PFUMUX to Clock (c0 to ck) | COMUX_SET | 1.5 | — | 1.2 | — | | | ns |
| PFUNAND to Clock (a[4:0], b[4:0] to ck) | ND SET | 3.9 | — | 2.9 | — | | | ns |
| PFUNAND to Clock (c0 to ck) | C0ND SET | 1.7 | — | 1.2 | — | | | ns |
| PFUXOR to Clock (a[4:0], b[4:0] to ck) | XOR SET | 4.8 | — | 3.6 | — | | | ns |
| PFUXOR to Clock (c0 to ck) | C0XOR SET | 1.6 | — | 1.2 | — | | | ns |
| Data In to Clock (wd[3:0] to ck) | D* SET | 0.5 | — | 0.1 | — | | | ns |
| Clock Enable to Clock (ce to ck) | CKEN_SET | 1.6 | — | 1.2 | — | | | ns |
| Local Set/Reset (synchronous) (lsr to ck) | LSR_SET | 1.7 | — | 1.4 | — | | | ns |
| Data Select to Clock (sel to ck) | SELECT_SET | 1.9 | — | 1.5 | — | | | ns |
| Pad Direct In | PDIN_SET | 0.0 | — | 0.0 | — | | | ns |
| Combinatorial Hold Times (TJ = All, VDD = All): | | | | | | | | |
| Data In (wd[3:0] from ck) | D* HLD | 0.6 | — | 0.4 | — | | | ns |
| Clock Enable (ce from ck) | CKEN_HLD | 0.6 | — | 0.4 | — | | | ns |
| Local Set/Reset (synchronous) (lsr from ck) | LSR_HLD | 0.0 | — | 0.0 | — | | | ns |
| Data Select (sel from ck) | SELECT_HLD | 0.0 | — | 0.0 | — | | | ns |
| Pad Direct In Hold (dia[3:0], dib[3:0] to ck) | PDIN_HLD | 1.5 | — | 1.4 | — | | | ns |
| All Others | — | 0 | — | 0 | — | | | ns |
| Output Characteristics | | | | | | | | |
| Combinatorial Delays (TJ = +85 °C, VDD = Min): | | | | | | | | |
| Four Input Variables (a[4:0], b[4:0] to o[4:0]) | F4* DEL | — | 5.1 | — | 3.6 | | | ns |
| Five Input Variables (a[4:0], b[4:0] to o[4:0]) | F5* DEL | — | 5.2 | — | 3.7 | | | ns |
| PFUMUX (a[4:0], b[4:0] to o[4:0]) | MUX_DEL | — | 5.8 | — | 4.6 | | | ns |
| PFUMUX (c0 to o[4:0]) | COMUX_DEL | — | 4.1 | — | 3.0 | | | ns |
| PFUNAND (a[4:0], b[4:0] to o[4:0]) | ND DEL | — | 5.8 | — | 4.8 | | | ns |
| PFUNAND (c0 to o[4:0]) | C0ND_DEL | — | 3.8 | — | 3.0 | | | ns |
| PFUXOR (a[4:0], b[4:0] to o[4:0]) | XOR_DEL | — | 6.7 | — | 5.3 | | | ns |
| PFUXOR (c0 to o[4:0]) | C0XOR_DEL | — | 4.2 | — | 3.0 | | | ns |
| Sequential Delays (TJ = +85 °C, VDD = Min): | | | | | | | | |
| Local S/R (async) to PFU Out (lsr to o[4:0]) | LSR_DEL | — | 5.6 | — | 4.2 | | | ns |
| Global S/R to PFU Out (gsrn to o[4:0]) | GSR_DEL | — | 4.0 | — | 3.1 | | | ns |
| Clock to PFU Out (ck to o[4:0]) — Register | REG_DEL | — | 3.9 | — | 2.8 | | | ns |
| Clock to PFU Out (ck to o[4:0]) — Latch | LTCH_DEL | — | 4.0 | — | 2.8 | | | ns |
| Transparent Latch (wd[3:0] to o[4:0]) | LTCH_DDEL | — | 5.0 | — | 3.5 | | | ns |

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Timing Characteristics (continued)

Table 30. PFU Timing Characteristics (continued)

Commercial: VDD = 5.0 V ± 5%, 0 °C ≤ TA ≤ 70 °C; Industrial: VDD = 5.0 V ± 10%, -40 °C ≤ TA ≤ +85 °C.

| Parameter | Symbol | Speed | | | | | | Unit |
|--|-------------|-------|------|-----|-----|-----|-----|------|
| | | -2 | | -3 | | | | |
| | | Min | Max | Min | Max | Min | Max | |
| Ripple Mode Characteristics | | | | | | | | |
| Ripple Setup Times (TJ = +85 °C, VDD = Min): | | | | | | | | |
| Operands to Clock (a[3:0], b[3:0] to ck) | RIP_SET | 6.7 | — | 5.0 | — | | ns | |
| Carry-In to Clock (cin to ck) | CIN_SET | 4.0 | — | 3.2 | — | | ns | |
| Add/Subtract to Clock (a4 to ck) | AS_SET | 8.2 | — | 5.6 | — | | ns | |
| Ripple Hold Times (TJ = All, VDD = All): All | TH | 0 | — | 0 | — | | ns | |
| Ripple Delays (TJ = +85 °C, VDD = Min): | | | | | | | | |
| Operands to Carry-Out (a[3:0], b[3:0] to cout) | RIP_CODEL | — | 5.4 | — | 3.8 | | ns | |
| Operands to Carry-Out (o4) (a[3:0], b[3:0] to o4) | RIP_O4DEL | — | 6.9 | — | 4.8 | | ns | |
| Operands to PFU Out (a[3:0], b[3:0] to o[4:0]) | RIP_DEL | — | 9.3 | — | 6.8 | | ns | |
| Carry-In to Carry-Out (cin to cout) | CIN_CODEL | — | 1.9 | — | 1.6 | | ns | |
| Carry-In to Carry-Out (o4) (cin to o4) | CIN_O4DEL | — | 3.5 | — | 2.6 | | ns | |
| Carry-In to PFU Out (cin to o[4:0]) | CIN_DEL | — | 6.7 | — | 5.0 | | ns | |
| Add/Subtract to Carry-Out (a4 to cout) | AS_CODEL | — | 6.1 | — | 4.5 | | ns | |
| Add/Subtract to Carry-Out (o4) (a4 to o4) | AS_O4DEL | — | 7.6 | — | 5.6 | | ns | |
| Add/Subtract to PFU Out (a4 to o[4:0]) | AS_DEL | — | 10.8 | — | 7.6 | | ns | |
| Read/Write Memory Characteristics | | | | | | | | |
| Read Operation (TJ = +85 °C, VDD = Min): | | | | | | | | |
| Read Cycle Time | TRC | 5.1 | — | 3.6 | — | | ns | |
| Data Valid after Address (a[3:0], b[3:0] to o[4:0]) | MEM*_ADEL | — | 5.1 | — | 3.6 | | ns | |
| Read Operation, Clocking Data into Latch/Flip-Flop (TJ = +85 °C, VDD = Min): | | | | | | | | |
| Address to Clock Setup Time (a[3:0], b[3:0] to ck) | MEM*_ASET | 2.4 | — | 1.8 | — | | ns | |
| Clock to PFU Out (ck to o[4:0]) — Register | REG_DEL | — | 3.9 | — | 2.8 | | ns | |
| Write Operation (TJ = +85 °C, VDD = Min): | | | | | | | | |
| Write Cycle Time | TWC | 5.5 | — | 4.5 | — | | ns | |
| Write Enable Pulse Width (a4/b4) | TPW | 3.0 | — | 2.5 | — | | ns | |
| Setup Time (TJ = +85 °C, VDD = Min): | | | | | | | | |
| Address to wren (a[3:0]/b[3:0] to a4/b4) | MEM*_AWRSET | 0.1 | — | 0.1 | — | | ns | |
| Data to wren (wd[3:0] to a4/b4) | MEM*_DWRSET | 0.0 | — | 0.0 | — | | ns | |
| Hold Time (TJ = All, VDD = All): | | | | | | | | |
| Address from wren (a[3:0]/b[3:0] from a4/b4) | MEM*_WRAHLD | 2.4 | — | 1.7 | — | | ns | |
| Data from wren (wd[3:0] from a4/b4) | MEM*_WRDHLd | 2.4 | — | 2.0 | — | | ns | |

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Timing Characteristics (continued)

Table 30. PFU Timing Characteristics (continued)

Commercial: VDD = 5.0 V ± 5%, 0 °C ≤ TA ≤ 70 °C; Industrial: VDD = 5.0 V ± 10%, -40 °C ≤ TA ≤ +85 °C.

| Parameter | Symbol | Speed | | | | | | Unit |
|--|------------|-------|-----|-----|-----|-----|-----|------|
| | | -2 | | -3 | | | | |
| | | Min | Max | Min | Max | Min | Max | |
| Read During Write Operation (TJ = +85 °C, VDD = Min) | | | | | | | | |
| Write Enable to PFU Output Delay (a4/b4 to o[4:0]) | MEM*_WRDEL | — | 8.1 | — | 5.7 | | | ns |
| Data to PFU Output Delay (wd[3:0] to o[4:0]) | MEM*_DDEL | — | 6.1 | — | 4.4 | | | ns |
| Read During Write, Clocking Data into Latch/Flip-Flop | | | | | | | | |
| Setup Time (TJ = +85 °C, VDD = Min): | | | | | | | | |
| Write Enable to Clock (a4/b4 to ck) | MEM*_WRSET | 5.4 | — | 4.4 | — | | | ns |
| Data (wd[3:0] to ck) | MEM*_DSET | 3.5 | — | 2.6 | — | | | ns |
| Hold Time (TJ = All, VDD = All): All | TH | 0 | — | 0 | — | | | ns |
| Clock to PFU Out (ck to o[4:0]) — Register | REG_DEL | — | 3.9 | — | 2.8 | | | ns |

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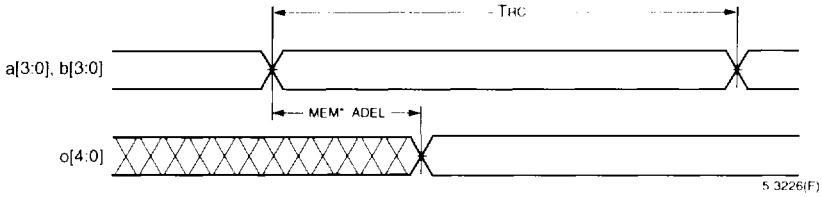


Figure 49. Read Operation—Flip-Flop Bypass

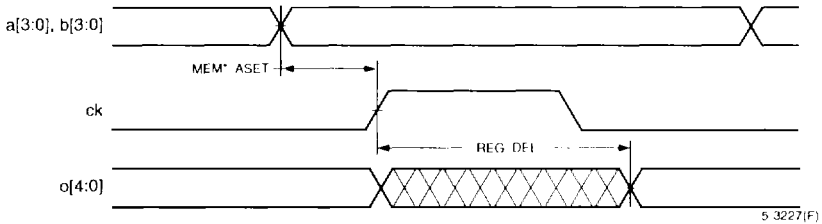


Figure 50. Read Operation—LUT Memory Loading Flip-Flops

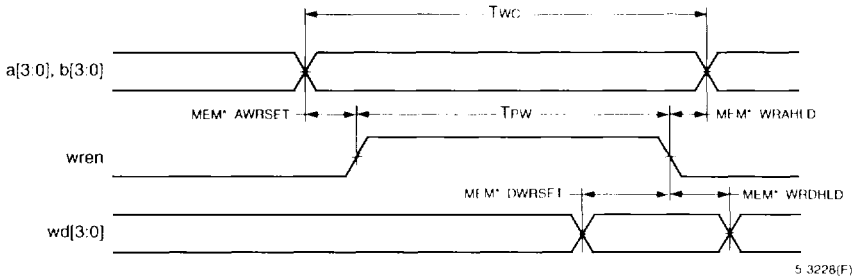


Figure 51. Write Operation

Timing Characteristics (continued)

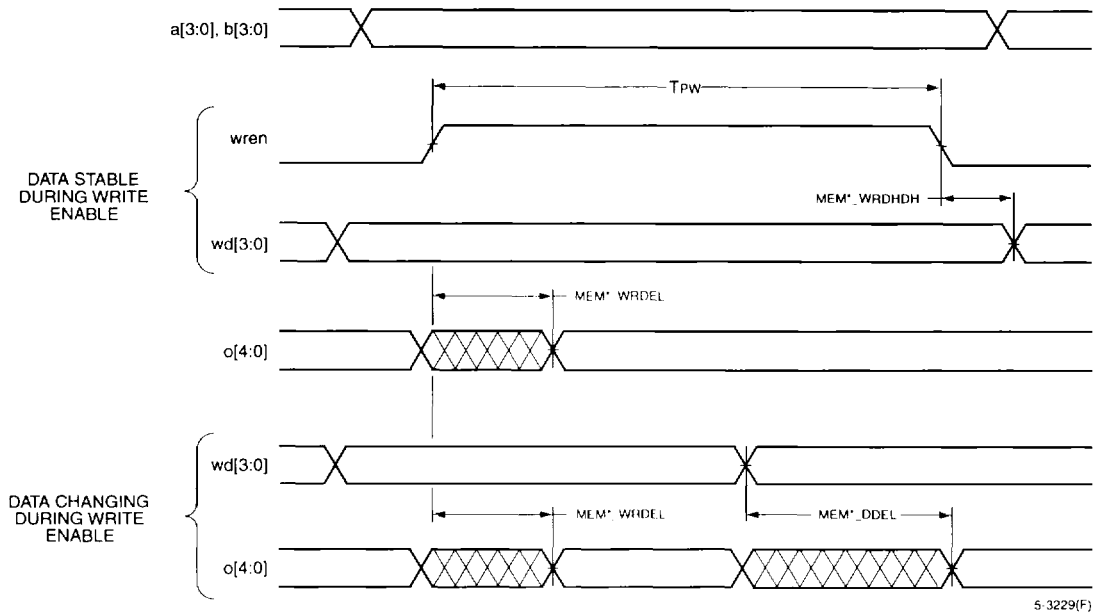


Figure 52. Read During Write

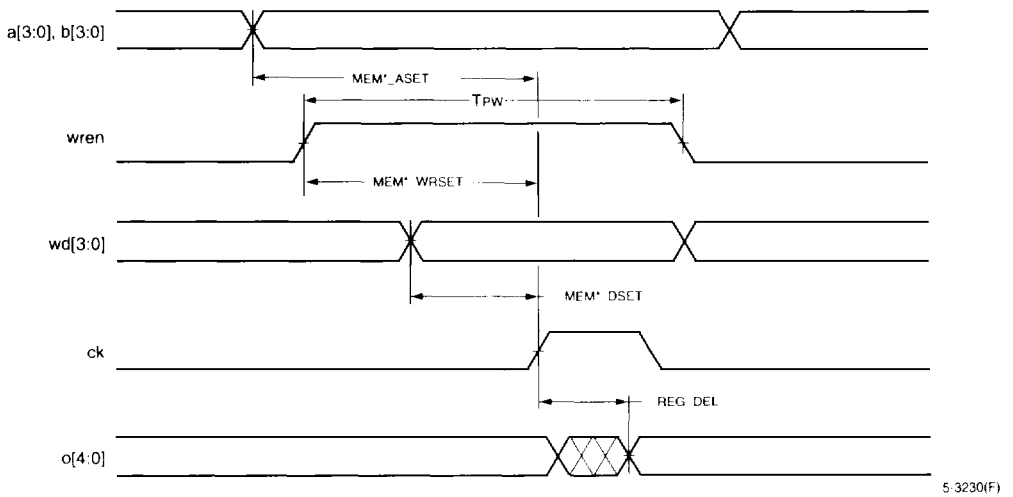


Figure 53. Read During Write—Clocking Data into Flip-Flop

Timing Characteristics (continued)

Table 31. PLC BIDI and Direct Routing Timing Characteristics

Commercial: VDD = 5.0 V ± 5%, 0 °C ≤ TA ≤ 70 °C; Industrial: VDD = 5.0 V ± 10%, -40 °C ≤ TA ≤ +85 °C.

| Parameter | Symbol | Speed | | | | | | Unit |
|---|------------|-------|-----|-----|-----|-----|-----|------|
| | | -2 | | -3 | | | | |
| | | Min | Max | Min | Max | Min | Max | |
| PLC 3-Statable BIDs (TJ = +85 °C, VDD = Min) | | | | | | | | |
| BIDI Propagation Delay | TRI_DEL | — | 1.2 | — | 1.0 | | | ns |
| BIDI 3-State Enable/Disable Delay | TRIE_N_DEL | — | 1.7 | — | 1.3 | | | ns |
| Direct Routing (TJ = +85 °C, VDD = Min) | | | | | | | | |
| PFU to PFU Delay (xSW) | DIR_DEL | — | 1.4 | — | 1.1 | | | ns |
| PFU Feedback (xSW) | FDBK_DEL | — | 1.0 | — | 0.8 | | | ns |

Table 32. Clock Delay

Commercial: VDD = 5.0 V ± 5%, 0 °C ≤ TA ≤ 70 °C; Industrial: VDD = 5.0 V ± 10%, -40 °C ≤ TA ≤ +85 °C.

| Device (TJ = +85 °C, VDD = Min) | Symbol | Speed | | | | | | Unit |
|------------------------------------|---------|-------|-----|-----|-----|-----|-----|------|
| | | -2 | | -3 | | | | |
| | | Min | Max | Min | Max | Min | Max | |
| ATT2C04 | CLK_DEL | — | 5.5 | — | 4.4 | | | |
| ATT2C06 | CLK_DEL | — | 5.6 | — | 4.5 | | | ns |
| ATT2C08 | CLK_DEL | — | 5.8 | — | 4.6 | | | ns |
| ATT2C10 | CLK_DEL | — | 5.9 | — | 4.7 | | | ns |
| ATT2C12 | CLK_DEL | — | 6.1 | — | 4.9 | | | ns |
| ATT2C15 | CLK_DEL | — | 6.2 | — | 5.0 | | | ns |
| ATT2C26 | CLK_DEL | — | 6.4 | — | 5.2 | | | ns |
| ATT2C40 | CLK_DEL | — | 6.9 | — | 5.8 | | | ns |

Note: This clock delay is for a fully routed clock tree that uses the primary clock network. It includes both the input buffer delay and the clock routing to the PFU CLK input. The delay will be reduced if any of the clock branches are not used.

Timing Characteristics (continued)

Table 33. Programmable I/O Cell Timing Characteristics

Commercial: VDD = 5.0 V ± 5%, 0 °C ≤ TA ≤ 70 °C; Industrial: VDD = 5.0 V ± 10%, -40 °C ≤ TA ≤ +85 °C; CL = 50 pF.

| Parameter | Symbol | Speed | | | | | | Unit |
|---|---|-------------|--------------------|-------------|-------------------|-----|-----|----------------|
| | | -2 | | -3 | | | | |
| | | Min | Max | Min | Max | Min | Max | |
| Inputs (TJ = +85 °C, VDD = Min) | | | | | | | | |
| Input Rise Time | TR | — | 500 | — | 500 | | | ns |
| Input Fall Time | TF | — | 500 | — | 500 | | | ns |
| Pad to In Delay | FASTIN_G_DEL | — | 3.1 | — | 2.3 | | | ns |
| Pad to TRIDI Delay | FASTIN_L_DEL | — | 2.7 | — | 1.9 | | | ns |
| Pad to In Delay (delay mode) | DLYIN_G_DEL | — | 7.8 | — | 6.2 | | | ns |
| Pad to TRIDI Delay (delay mode) | DLYIN_L_DEL | — | 2.5 | — | 1.9 | | | ns |
| Pad to Nearest PFU Latch Output | CHIP_LATCH | — | 6.8 | — | 5.1 | | | ns |
| Setup Time: Pad to Nearest PFU ck Pad to Nearest PFU ck (delay mode)* | CHIP_SET DLY_CHIP_SET | 2.8 8.7 | — — | 2.1 6.8 | — — | | | ns ns |
| Outputs (TJ = +85 °C, VDD = Min) | | | | | | | | |
| PFU ck to Pad Delay (dout[3:0] to pad): Fast Slewlim Sinklim | DOUT_DEL(F) DOUT_DEL(SL) DOUT_DEL(SI) | — — — | 7.6 9.3 12.4 | — — — | 5.7 6.9 8.9 | | | ns ns ns |
| Output to Pad Delay (out[3:0] to pad): Fast Slewlim Sinklim | OUT_DEL(F) OUT_DEL(SL) OUT_DEL(SI) | — — — | 5.0 6.7 9.8 | — — — | 4.0 5.2 7.2 | | | ns ns ns |
| 3-state Enable Delay (ts[3:0] to pad): Fast Slewlim Sinklim | TS_DEL(F) TS_DEL(SL) TS_DEL(SI) | — — — | 5.8 7.5 10.6 | — — — | 4.7 5.9 7.9 | | | ns ns ns |

* If the input buffer is placed in delay mode, the chip hold time to the nearest PFU latch is guaranteed to be 0 if the clock is routed using the primary clock network; (TJ = All, VDD = All). For the ATT2C40, this is only valid for input buffers on the same half of the device as the clock pin.

Note: The delays for all input buffers assume an input rise/fall time of ≤1 V/ns.

2

Timing Characteristics (continued)

Table 34. General Configuration Mode Timing Characteristics

Commercial: VDD = 5.0 V ± 5%, 0 °C ≤ TA ≤ 70 °C; Industrial: VDD = 5.0 V ± 10%, -40 °C ≤ TA ≤ +85 °C; CL = 50 pF.

| Parameter | Symbol | Min | Max | Unit |
|--|--------|--------|---------|------|
| All Configuration Modes | | | | |
| M[3:0] Setup Time to INIT High | TSMODE | 50.0 | — | ns |
| M[3:0] Hold Time from INIT High | THMODE | 600.0 | — | ns |
| RESET Pulse Width Low | TRW | 50.0 | — | ns |
| PRGM Pulse Width Low | TPGW | 50.0 | — | ns |
| Master and Asynchronous Peripheral Modes | | | | |
| Power-on Reset Delay | TPO | 16.24 | 43.80 | ms |
| CCLK Period (M3 = 0) | TCCLK | 62.00 | 167.00 | ns |
| (M3 = 1) | | 496.00 | 1336.00 | ns |
| Configuration Latency (noncompressed) | TCL | | | |
| ATT2C04 (M3 = 0) | | 4.05 | 10.90* | ms |
| (M3 = 1) | | 32.38 | 87.21* | ms |
| ATT2C06 (M3 = 0) | | 5.63 | 15.18* | ms |
| (M3 = 1) | | 45.08 | 121.42* | ms |
| ATT2C08 (M3 = 0) | | 7.16 | 19.28* | ms |
| (M3 = 1) | | 57.27 | 154.25* | ms |
| ATT2C10 (M3 = 0) | | 9.23 | 24.85* | ms |
| (M3 = 1) | | 73.80 | 198.80* | ms |
| ATT2C12 (M3 = 0) | | 11.14 | 30.01* | ms |
| (M3 = 1) | | 89.14 | 240.10* | ms |
| ATT2C15 (M3 = 0) | | 13.69 | 36.87* | ms |
| (M3 = 1) | | 109.52 | 294.99* | ms |
| ATT2C26 (M3 = 0) | | 19.03 | 51.25* | ms |
| (M3 = 1) | | 152.28 | 409.99* | ms |
| ATT2C40 (M3 = 0) | | 29.39 | 79.16* | ms |
| (M3 = 1) | | 235.12 | 633.31* | ms |
| Slave Serial and Synchronous Peripheral Modes | | | | |
| Power-on Reset Delay | TPO | 4.06 | 10.95 | ms |
| CCLK Period | TCCLK | 100.00 | — | ns |
| Configuration Latency (noncompressed): | TCL | | | |
| ATT2C04 | | 6.53 | — | ms |
| ATT2C06 | | 9.09 | — | ms |
| ATT2C08 | | 11.55 | — | ms |
| ATT2C10 | | 14.88 | — | ms |
| ATT2C12 | | 17.97 | — | ms |
| ATT2C15 | | 22.08 | — | ms |
| ATT2C26 | | 30.69 | — | ms |
| ATT2C40 | | 47.40 | — | ms |

* Not applicable to asynchronous peripheral mode.

Timing Characteristics (continued)

Table 34. General Configuration Mode Timing Characteristics (continued)

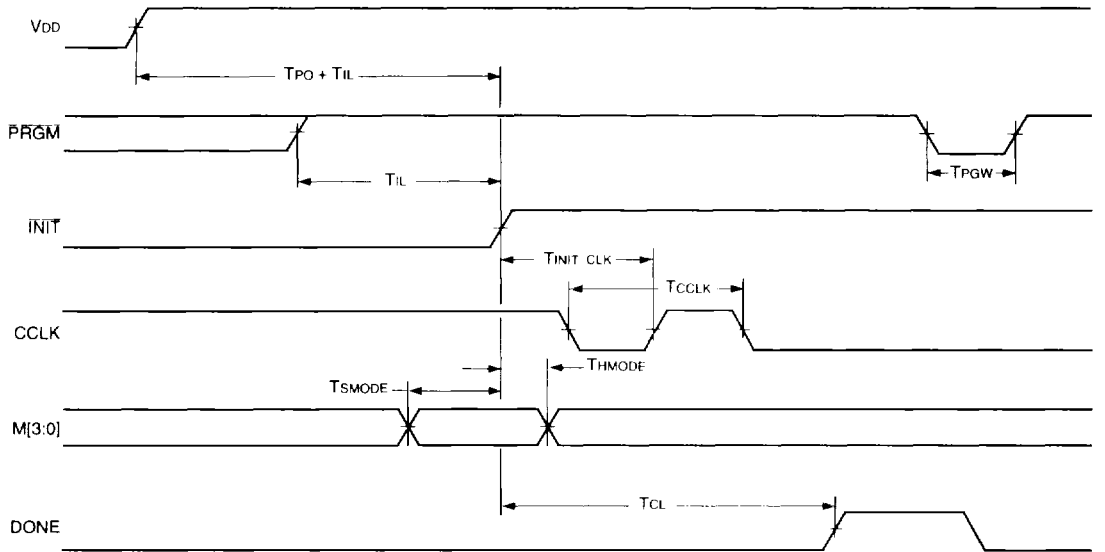
Commercial: VDD = 5.0 V ± 5%, 0 °C ≤ TA ≤ 70 °C; Industrial: VDD = 5.0 V ± 10%, -40 °C ≤ TA ≤ +85 °C; CL = 50 pF.

| Parameter | Symbol | Min | Max | Unit |
|---|------------|--------|--------|------|
| Slave Parallel Mode | | | | |
| Power-on Reset Delay | TPO | 4.06 | 10.95 | ms |
| CCLK Period | TCCLK | 100.00 | — | ns |
| Configuration Latency (noncompressed): | TCL | | | |
| ATT2C04 | | 0.82 | — | ms |
| ATT2C06 | | 1.14 | — | ms |
| ATT2C08 | | 1.44 | — | ms |
| ATT2C10 | | 1.86 | — | ms |
| ATT2C12 | | 2.25 | — | ms |
| ATT2C15 | | 2.76 | — | ms |
| ATT2C26 | | 3.84 | — | ms |
| ATT2C40 | | 5.93 | — | ms |
| INIT Timing | | | | |
| INIT High to CCLK Delay | TINIT CCLK | | | |
| Slave Parallel | | 1.00 | — | μs |
| Slave Serial | | 1.00 | — | μs |
| Synchronous Peripheral | | 1.00 | — | μs |
| Master Serial | | | | |
| M3 = 1 | | 1.00 | 2.90 | μs |
| M3 = 0 | | 0.50 | 0.70 | μs |
| Master Parallel | | | | |
| M3 = 1 | | 4.90 | 13.60 | μs |
| M3 = 0 | | 1.00 | 2.90 | μs |
| Initialization Latency (PRGM high to INIT high) | TIL | | | |
| ATT2C04 | | 59.51 | 162.33 | μs |
| ATT2C06 | | 70.43 | 191.72 | μs |
| ATT2C08 | | 81.34 | 221.11 | μs |
| ATT2C10 | | 92.25 | 250.51 | μs |
| ATT2C12 | | 103.16 | 279.90 | μs |
| ATT2C15 | | 114.07 | 309.29 | μs |
| ATT2C26 | | 135.90 | 368.07 | μs |
| ATT2C40 | | 170.87 | 462.26 | μs |
| INIT High to WR, Asynchronous Peripheral | TINIT WR | 1.50 | — | μs |

Note: TPO is triggered when VDD reaches between 3.0 V to 4.0 V.

Timing Characteristics (continued)

2



5-4531(F)

Figure 54. General Configuration Mode Timing Diagram

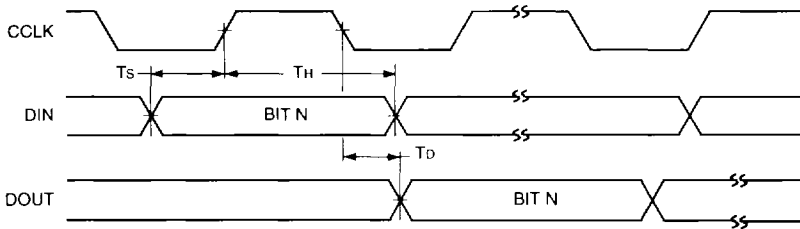
Timing Characteristics (continued)

Table 35. Master Serial Configuration Mode Timing Characteristics

Commercial: $V_{DD} = 5.0\text{ V} \pm 5\%$, $0\text{ }^{\circ}\text{C} \leq T_A \leq 70\text{ }^{\circ}\text{C}$; Industrial: $V_{DD} = 5.0\text{ V} \pm 10\%$, $-40\text{ }^{\circ}\text{C} \leq T_A \leq +85\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$.

| Parameter | Symbol | Min | Nom | Max | Unit |
|-------------------------|----------------|------|------|------|------|
| DIN Setup Time | T _S | 60.0 | — | — | ns |
| DIN Hold Time | T _H | 0 | — | — | ns |
| CCLK Frequency (M3 = 0) | F _C | 6.0 | 10.0 | 16.0 | MHz |
| CCLK Frequency (M3 = 1) | F _C | 0.75 | 1.25 | 2.0 | MHz |
| CCLK to DOUT Delay | T _D | — | — | 30 | ns |

Note: Serial configuration data is transmitted out on DOUT on the falling edge of CCLK after it is input DIN.



5-4532(F)

Figure 55. Master Serial Configuration Mode Timing Diagram

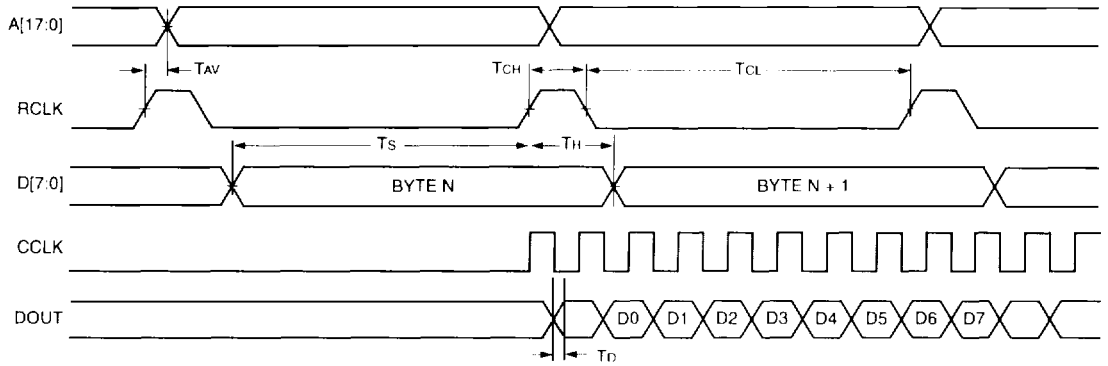
Timing Characteristics (continued)

Table 36. Master Parallel Configuration Mode Timing Characteristics

Commercial: VDD = 5.0 V ± 5%, 0 °C ≤ TA ≤ 70 °C; Industrial: VDD = 5.0 V ± 10%, -40 °C ≤ TA ≤ +85 °C; CL = 50 pF.

| Parameter | Symbol | Min | Max | Unit |
|--------------------------------|--------|------|------|------|
| RCLK to Address Valid | TAV | 0 | 200 | ns |
| D[7:0] Setup Time to RCLK High | TS | 60 | — | ns |
| D[7:0] Hold Time to RCLK High | TH | 0 | — | ns |
| RCLK Low Time (M3 = 0) | TCL | 434 | 1169 | ns |
| RCLK High Time (M3 = 0) | TCH | 62 | 167 | ns |
| RCLK Low Time (M3 = 1) | TCL | 3472 | 9352 | ns |
| RCLK High Time (M3 = 1) | TCH | 496 | 1336 | ns |
| CCLK to DOUT | TD | — | 30 | ns |

Notes: The RCLK period consists of seven CCLKs for RCLK low and one CCLK for RCLK high.
Serial data is transmitted out on DOUT 1.5 CCLK cycles after the byte is input D[7:0].



144(F)

Figure 56. Master Parallel Configuration Mode Timing Diagram

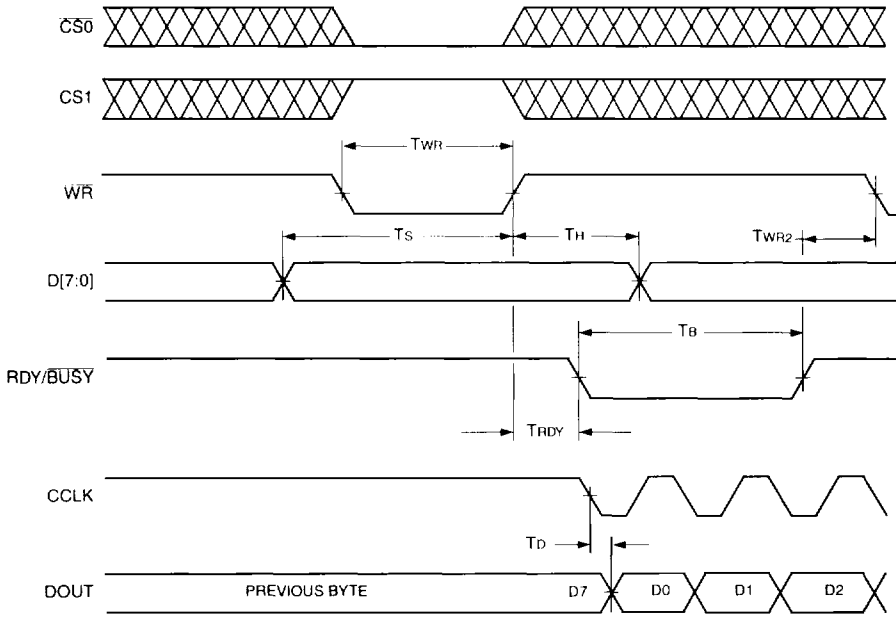
Timing Characteristics (continued)

Table 37. Asynchronous Peripheral Configuration Mode Timing Characteristics

Commercial: $V_{DD} = 5.0\text{ V} \pm 5\%$, $0\text{ }^{\circ}\text{C} \leq T_A \leq 70\text{ }^{\circ}\text{C}$; Industrial: $V_{DD} = 5.0\text{ V} \pm 10\%$, $-40\text{ }^{\circ}\text{C} \leq T_A \leq +85\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$.

| Parameter | Symbol | Min | Max | Unit |
|-------------------------------|--------|-----|-----|--------------|
| WR, CS0, and CS1 Pulse Width | TWR | 100 | — | ns |
| D[7:0] Setup Time | Ts | 20 | — | ns |
| D[7:0] Hold Time | TH | 0 | — | ns |
| RDY/BUSY Delay | TRDY | — | 60 | ns |
| RDY/BUSY Low | TB | 2 | 9 | CCLK Periods |
| Earliest WR After End of BUSY | TWR2 | 0 | — | ns |
| CCLK to DOUT | Td | — | 30 | ns |

Note: Serial data is transmitted out on DOUT on the falling edge of CCLK after the byte is input D[7:0].



5-4533(F)

Figure 57. Asynchronous Peripheral Configuration Mode Timing Diagram

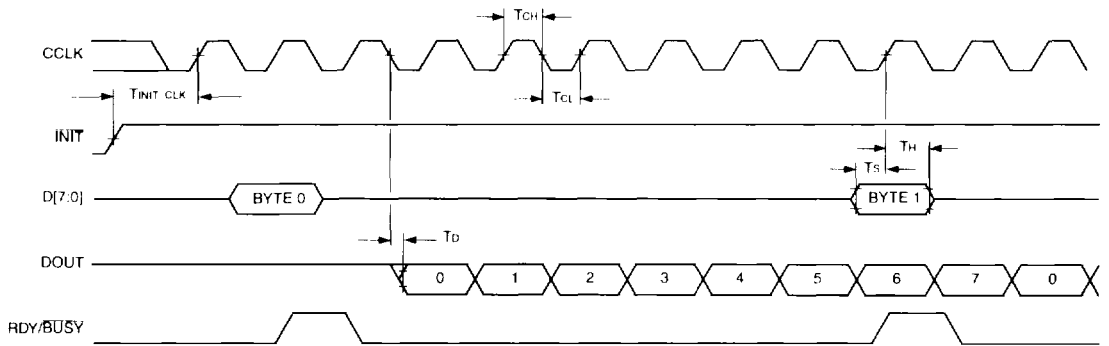
Timing Characteristics (continued)

Table 38. Synchronous Peripheral Configuration Mode Timing Characteristics

Commercial: $V_{DD} = 5.0\text{ V} \pm 5\%$, $0\text{ }^{\circ}\text{C} \leq T_A \leq 70\text{ }^{\circ}\text{C}$; Industrial: $V_{DD} = 5.0\text{ V} \pm 10\%$, $-40\text{ }^{\circ}\text{C} \leq T_A \leq +85\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$.

| Parameter | Symbol | Min | Max | Unit |
|-------------------|----------|-----|-----|------|
| D[7:0] Setup Time | T_S | 20 | — | ns |
| D[7:0] Hold Time | T_H | 0 | — | ns |
| CCLK High Time | T_{CH} | 50 | — | ns |
| CCLK Low Time | T_{CL} | 50 | — | ns |
| CCLK Frequency | F_C | — | 10 | MHz |
| CCLK to DOUT | T_D | — | 30 | ns |

Note: Serial data is transmitted out on DOUT 1.5 clock cycles after the byte is input D[7:0].



5-4534(F)

Figure 58. Synchronous Peripheral Configuration Mode Timing Diagram

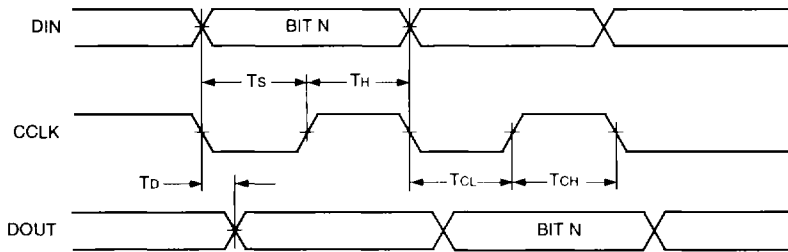
Timing Characteristics (continued)

Table 39. Slave Serial Configuration Mode Timing Characteristics

Commercial: $V_{DD} = 5.0 \pm 5\%$, $0\text{ }^{\circ}\text{C} \leq T_A \leq 70\text{ }^{\circ}\text{C}$; Industrial: $V_{DD} = 5.0\text{ V} \pm 10\%$, $-40\text{ }^{\circ}\text{C} \leq T_A \leq +85\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$.

| Parameter | Symbol | Min | Max | Unit |
|----------------|----------|-----|-----|------|
| DIN Setup Time | T_S | 20 | — | ns |
| DIN Hold Time | T_H | 0 | — | ns |
| CCLK High Time | T_{CH} | 50 | — | ns |
| CCLK Low Time | T_{CL} | 50 | — | ns |
| CCLK Frequency | F_C | — | 10 | MHz |
| CCLK to DOUT | T_D | — | 30 | ns |

Note: Serial configuration data is transmitted out on DOUT on the falling edge of CCLK after it is input on DIN.



5-4535(F)

Figure 59. Slave Serial Configuration Mode Timing Diagram

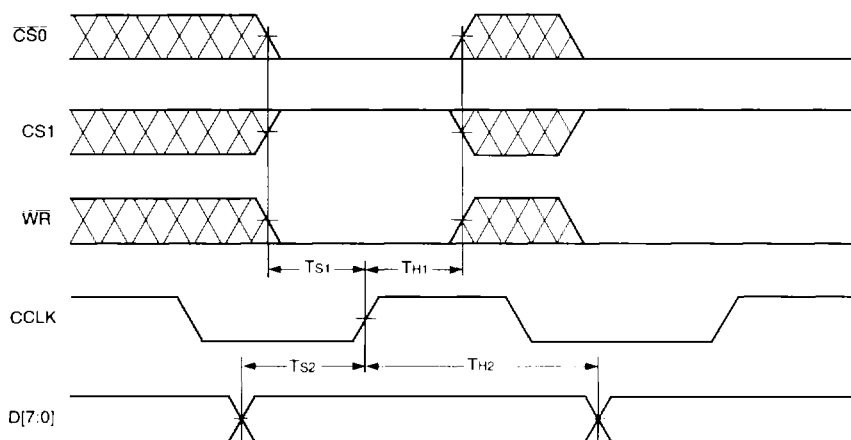
Timing Characteristics (continued)

Table 40. Slave Parallel Configuration Mode Timing Characteristics

Commercial: $V_{DD} = 5.0\text{ V} \pm 5\%$, $0\text{ }^{\circ}\text{C} \leq T_A \leq 70\text{ }^{\circ}\text{C}$; Industrial: $V_{DD} = 5.0\text{ V} \pm 10\%$, $-40\text{ }^{\circ}\text{C} \leq T_A \leq +85\text{ }^{\circ}\text{C}$.

| Parameter | Symbol | Min | Max | Unit |
|-------------------------|--------|-----|-----|------|
| CS0, CS1, WR Setup Time | TS1 | 60 | — | ns |
| CS0, CS1, WR Hold Time | TH1 | 20 | — | ns |
| D[7:0] Setup Time | TS2 | 20 | — | ns |
| D[7:0] Hold Time | TH2 | 0 | — | ns |
| CCLK High Time | TCH | 50 | — | ns |
| CCLK Low Time | TCL | 50 | — | ns |
| CCLK Frequency | Fc | — | 10 | MHz |

Note: Daisy chaining of FPGAs is not supported in this mode.



5 2848(F)

Figure 60. Slave Parallel Configuration Mode Timing Diagram

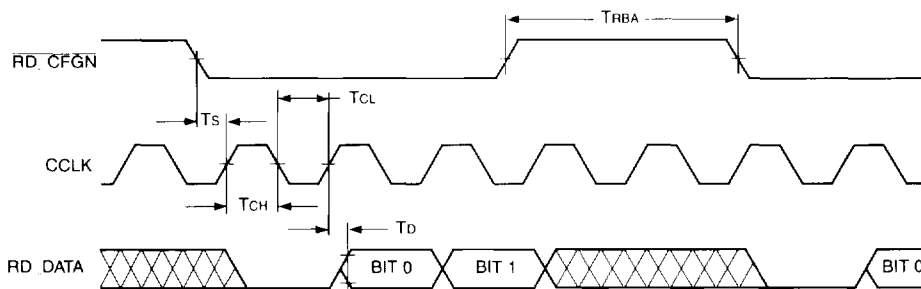
Timing Characteristics (continued)

Table 41. Readback Timing Characteristics

Commercial: $V_{DD} = 5.0\text{ V} \pm 5\%$, $0\text{ }^{\circ}\text{C} \leq T_A \leq 70\text{ }^{\circ}\text{C}$; Industrial: $V_{DD} = 5.0\text{ V} \pm 10\%$, $-40\text{ }^{\circ}\text{C} \leq T_A \leq +85\text{ }^{\circ}\text{C}$; $CL = 50\text{ pF}$.

| Parameter | Symbol | Min | Max | Unit |
|--------------------------------------|-----------|-----|-----|------|
| RD_CFGN to CCLK Setup Time | T_s | 50 | — | ns |
| RD_CFGN High Width to Abort Readback | T_{RBA} | 2 | — | CCLK |
| CCLK Low Time | T_{CL} | 50 | — | ns |
| CCLK High Time | T_{CH} | 50 | — | ns |
| CCLK Frequency | F_C | — | 10* | MHz |
| CCLK to RD_DATA Delay | T_D | — | 50 | ns |

* The maximum readback CCLK frequency for the ATT2C40 is 8 MHz.



5 4536(F)

Figure 61. Readback Timing Diagram

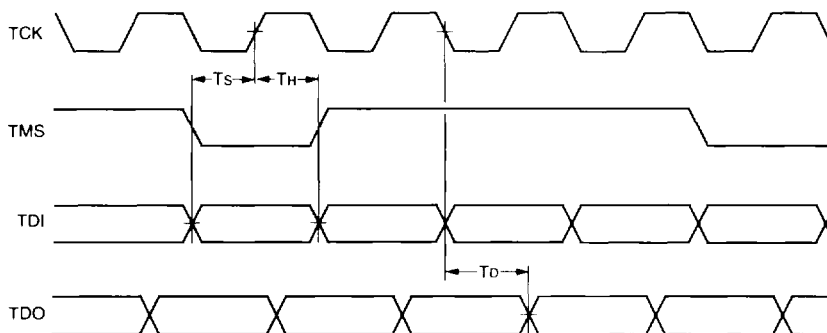
Timing Characteristics (continued)

Table 42. Boundary-Scan Timing Characteristics

Commercial: $V_{DD} = 5.0\text{ V} \pm 5\%$, $0\text{ }^{\circ}\text{C} \leq T_A \leq 70\text{ }^{\circ}\text{C}$; Industrial: $V_{DD} = 5.0\text{ V} \pm 10\%$, $-40\text{ }^{\circ}\text{C} \leq T_A \leq +85\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$.

| Parameter | Symbol | Min | Max | Unit |
|----------------------------|-----------|-----|-----|------|
| TDI/TMS to TCK Setup Time | T_s | 25 | — | ns |
| TDI/TMS Hold Time from TCK | T_H | 0 | — | ns |
| TCK Low Time | T_{CL} | 50 | — | ns |
| TCK High Time | T_{CH} | 50 | — | ns |
| TCK to TDO Delay | T_D | — | 20 | ns |
| TCK Frequency | T_{TCK} | — | 10 | MHz |

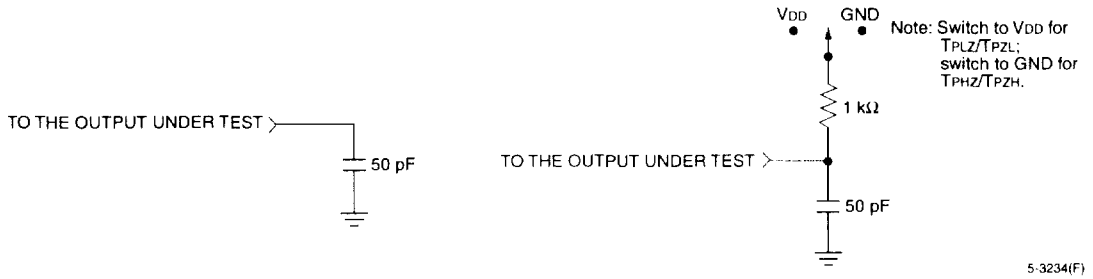
2



BSTD(C)

Figure 62. Boundary-Scan Timing Diagram

Measurement Conditions



2

A. Load Used to Measure Propagation Delay

B. Load Used to Measure Rising/Falling Edges

Figure 63. ac Test Loads

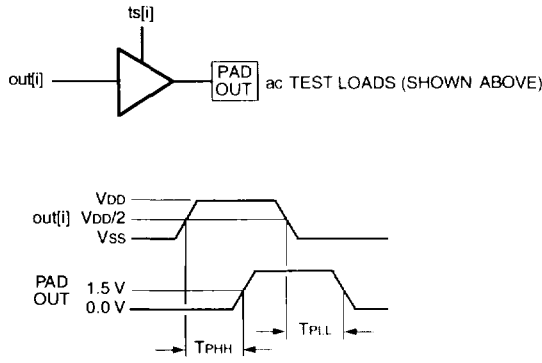


Figure 64. Output Buffer Delays

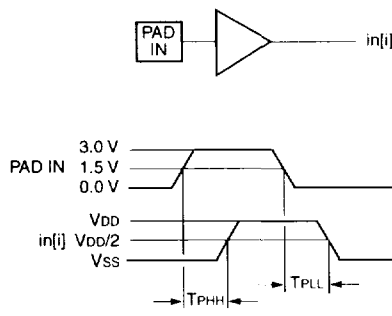
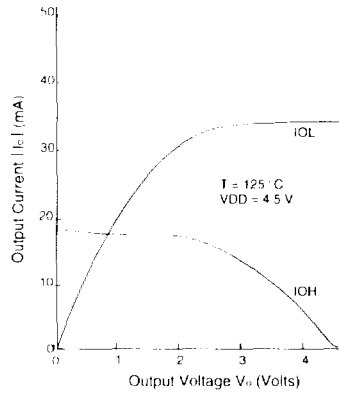
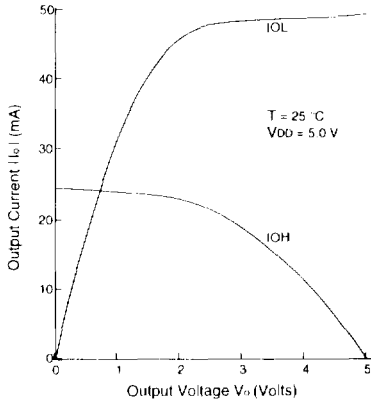


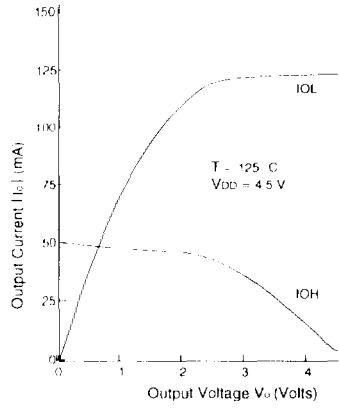
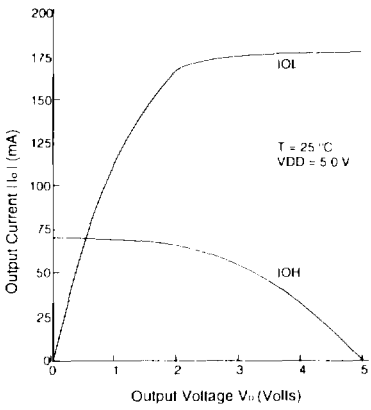
Figure 65. Input Buffer Delays

Output Buffer Characteristics

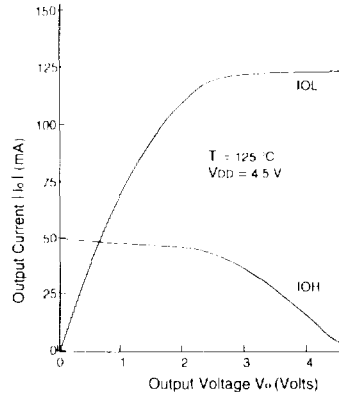
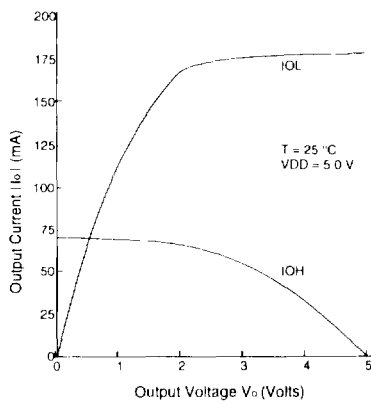
2



Sinklim



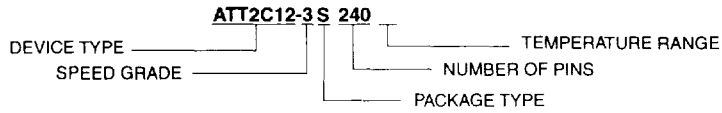
Slewlim



Fast

Ordering Information

Example:



ATT2C12, -3 Speed Grade, 240-pin Shrink Quad Flat Pack, Commercial Temperature.

Table 43. FPGA Temperature Options

| Symbol | Description | Temperature |
|---------|-------------|------------------|
| (Blank) | Commercial | 0 °C to 70 °C |
| I | Industrial | -40 °C to +85 °C |

Table 44. FPGA Package Options

| Symbol | Description |
|--------|---|
| B | Plastic Ball Grid Array (PBGA) |
| J | Quad Flat Package (QFP) |
| M | Plastic Leaded Chip Carrier (PLCC) |
| PS | Power Quad Shrink Flat Package (SQFP-PQ2) |
| R | Ceramic Pin Grid Array (CPGA) |
| S | Shrink Quad Flat Package (SQFP) |
| T | Thin Quad Flat Package (TQFP) |

Table 45. ORCA 2C Series Package Matrix

| Packages | 84-Pin PLCC | 100-Pin TQFP | 144-Pin TQFP | 160-Pin QFP | 208-Pin EIAJ SQFP/ SQFP-PQ2 | 240-Pin EIAJ SQFP/ SQFP-PQ2 | 256-Pin PBGA | 304-Pin EIAJ SQFP/ SQFP-PQ2 | 364-Pin CPGA | 428-Pin CPGA |
|----------|----------------|-----------------|-----------------|----------------|--------------------------------------|--------------------------------------|-----------------|--------------------------------------|-----------------|-----------------|
| | M84 | T100 | T144 | J160 | S208/ PS208 | S240/ PS240 | B256 | S304/ PS304 | R364 | R428 |
| ATT2C04 | CI | CI | CI | CI | CI | — | — | — | — | — |
| ATT2C06 | CI | CI | CI | CI | CI | CI | — | — | — | — |
| ATT2C08 | CI | — | — | CI | CI | CI | CI | CI | — | — |
| ATT2C10 | CI | — | — | CI | CI | CI | CI | CI | — | — |
| ATT2C12 | — | — | — | — | CI | CI | CI | CI | CI | — |
| ATT2C15 | — | — | — | — | CI | CI | — | CI | CI | — |
| ATT2C26 | — | — | — | — | CI | CI | — | CI | — | CI |
| ATT2C40 | — | — | — | — | CI | CI | — | CI | — | CI |

Key: C = commercial, I = industrial.

Note: The package options with the SQFP/SQFP-PQ2 designation in the table above use the SQFP package for all densities up to and including the ATT2C15, while the ATT2C26 uses the SQFP-PQ2 package (chip-up orientation), and the ATT2C40 uses the SQFP-PQ2 package (chip-down orientation).