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July 2012

FXMHD103 — HDMI Voltage Translator

Features

- CEC, DDC, and HPD Level Shifting without a Direction Pin
- Host Port Voltage Supply (V_{CCA}): 1.6V – 3.6V
- HDMI Port Voltage Supply (V_{CCC}): 4.8V – 5.3V
- Long HDMI Cable Support with Integrated DDC (I^2C) Edge Rate Accelerators
- Supports DDC (I^2C) Clock Stretching
- Pin Out Tailored for PCB Trace Routing to HDMI Type D Connectors
- Back Drive Protection
- Non-Preferential Power-Up/Down Sequencing between VCCA and VCCC
- Operating Temperature Range: -40°C to 85°C
- ESD Protection:
  - 8kV HBM (per JESD22-A114)
  - 2kV CDM (per JESD22-C101)

Applications

- Smart Phones
- Multimedia Phones
- Digital Camcorders
- Digital Still Cameras
- Portable Game Consoles
- Notebooks
- MP3 Players
- PC and Consumer Electronics

Description

The FXMHD103 is a reduced-pin-count, low-power, High-Definition Multimedia Interface (HDMI), voltage translator for the Data Display Channel (DDC), Consumer Electronic Control (CEC), and Hot Plug Detect (HPD) control lines.

There are three non-inverting bi-directional voltage translation circuits for the DDC serial data (SDA)/clock (SCL) lines and CEC lines. Each line has a common power rail (V_{CCA}) on the host side from 1.6V to 3.6V. On the HDMI connector side, the SCL_C and SDA_C pins each have an internal 1.75KΩ pull-up connected to the HDMI 5V rail, V_{CCC}. The SCL and SDA pins exceed the HDMI specification for driving up to 800pF loads. The CEC_C pin has an internal 27KΩ pull-up to an internal 3.3V supply (V_{REG}).

The HPD_C path is uni-directional. The direction is from the HDMI connector port to the host port. HPD_H references V_{CCA}, and HPD_C references V_{CCC}. HPD_C offers hysteresis to avoid false detection due to bouncing while inserting the HDMI plug.

The FXMHD103 device can be powered down if the OE pin is LOW. If OE is HIGH, the HPD path is enabled. If an HDMI sink asserts the HPD_C pin HIGH, the DDC and CEC paths are enabled. OE references V_{CCA}.

Back drive protection is provided on pins facing the HDMI connector.

Ordering Information

Part Number	Top Mark	Operating Temperature Range	Package	Packing Method
FXMHD103UMX	BZ	-40°C to 85°C	12-Terminal, Quad µMLP, 1.8mm x 1.8mm Package	5000 Units on Tape and Reel

Block Diagrams

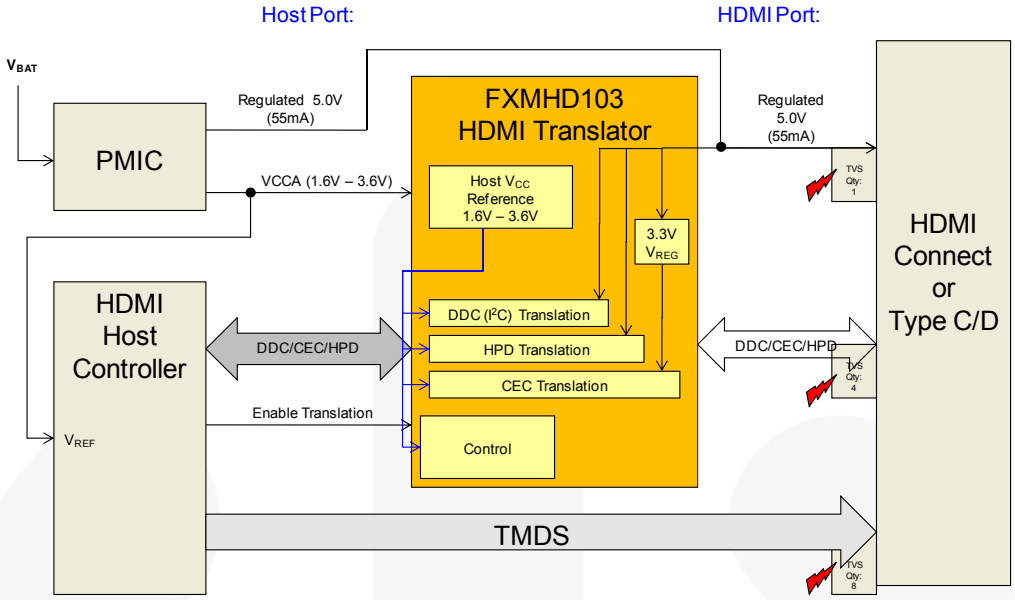

Figure 1. System Block Diagram

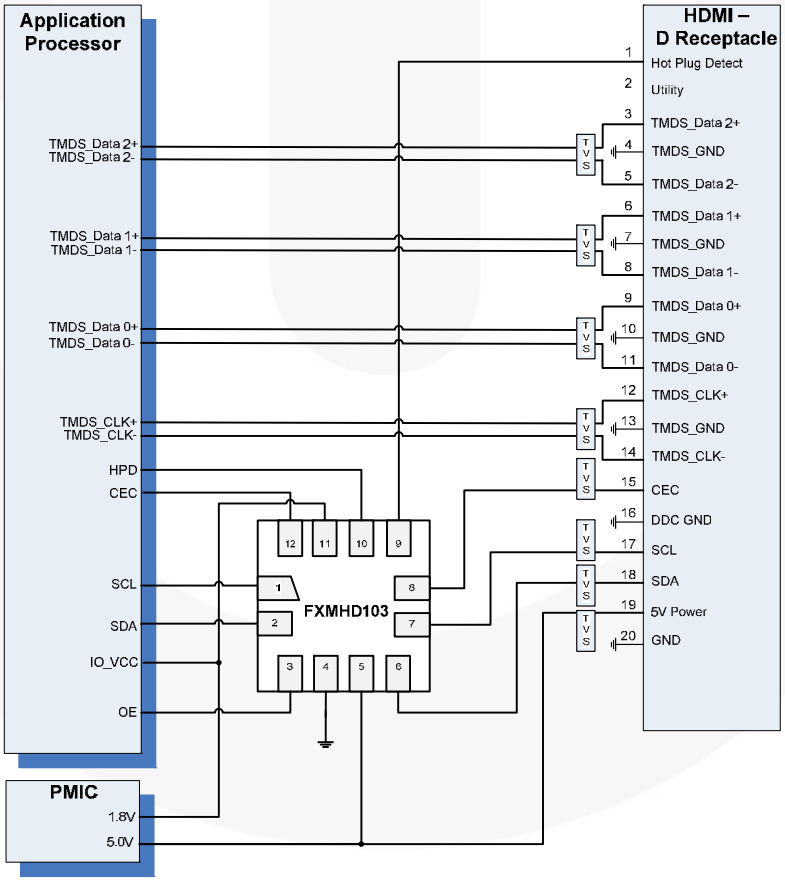

Figure 2. Application Drawing

Note:

1. The external TVS devices depicted in the Application Drawing (Figure 2) provide system-level IEC61000-4-2, Level 4 ESD protection to the mobile device system at the HDMI connector. The FXMHD103 provides device-level ESD protection defined in the ESD section of the Absolute Maximum Ratings table.

Block Diagrams (Continued)

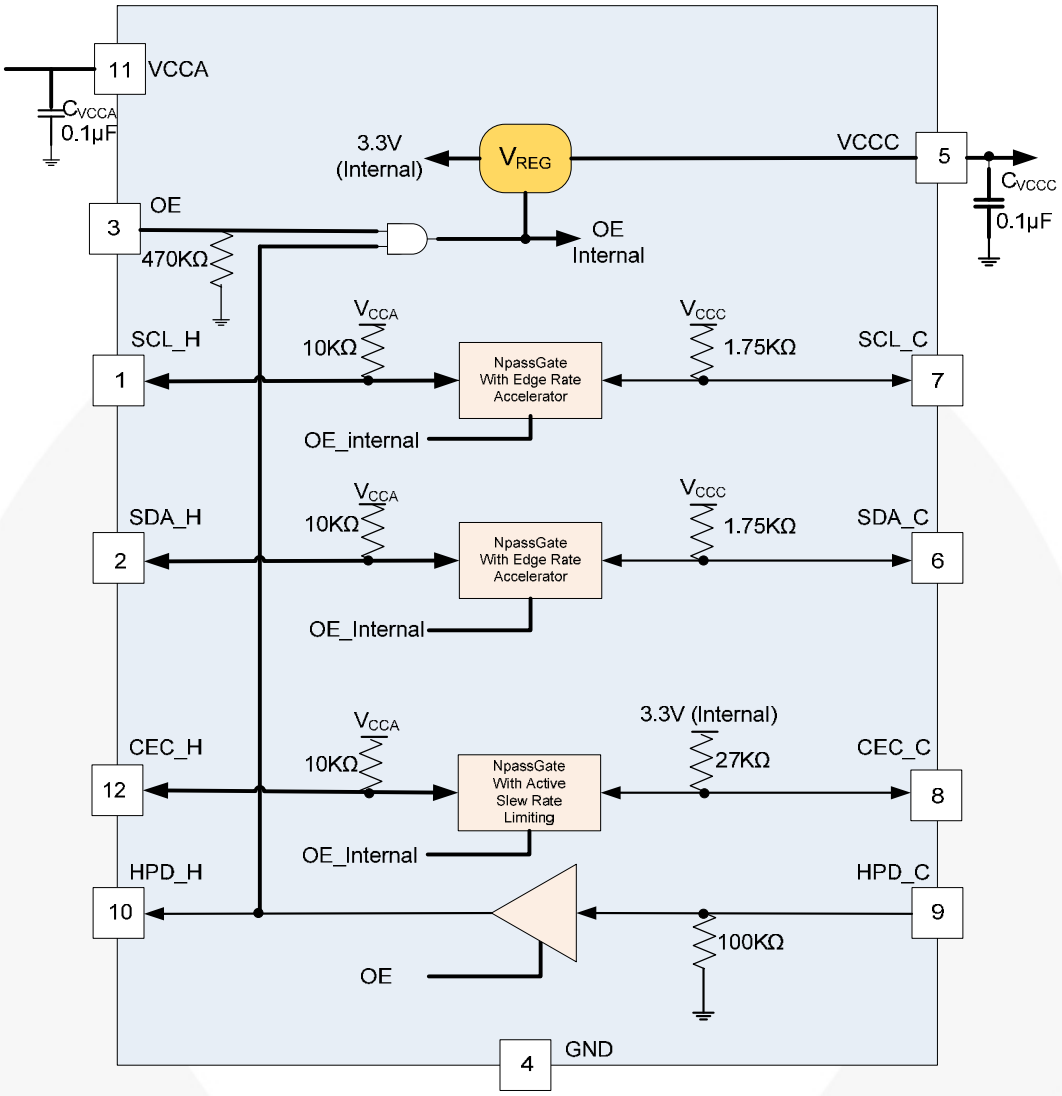

Figure 3. Circuit Block Diagram

Table 1. Truth Table (V_{CCA} & V_{CCC} Valid)

OE	HPD_C	OE Internal	VREG	HPD_H	SCL_C	SDA_C	CEC_C
LOW	Don't Care	LOW	Disabled	3-State	3-State	3-State	3-State
HIGH	LOW	LOW	Disabled	Enabled	3-State(2)	3-State(2)	3-State(2)
HIGH	HIGH	HIGH	Enabled	Enabled	Enabled	Enabled	Enabled

Note:

2. SCL_C and SDA_C internally pulled up to V_{CCC}. CEC_C is 0V because V_{REG} is disabled. This is required for HDMI compliance testing. The $VOUT_{DIS}$ parameter captures this requirement.

Pin Configuration

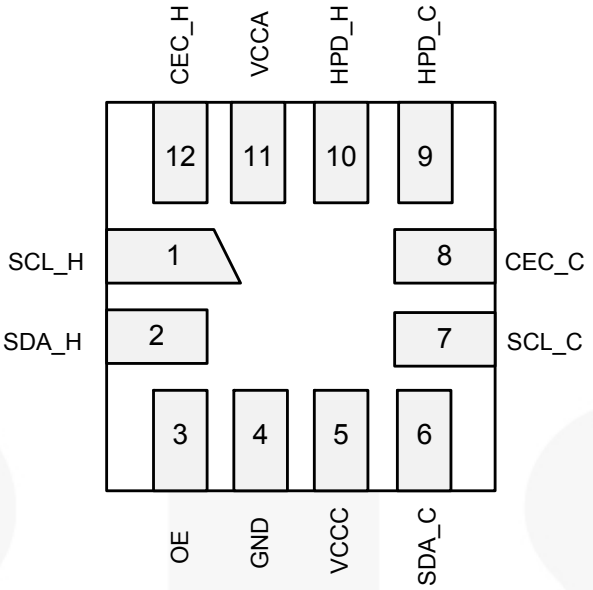

Figure 4. Pin Assignments (Top View)

Pin Definitions

Pin #	Signal Name	Description
1	SCL_H	Host-side (DDC) SCL bi-directional I^2C pin; referenced to VCCA.
2	SDA_H	Host-side (DDC) SDA bi-directional I^2C pin; referenced to VCCA.
3	OE	Output enable: LOW=DDC, CEC, & HPD paths disabled; HIGH=DDC, CEC, & HPD paths enabled.
4	GND	Device GND
5	VCCC	HDMI port supply: 5V V_{CC} reference for HPD_C, SCL_C, SDA_C, and V_{REG} input.
6	SDA_C	Connector-side (DDC) SDA bi-directional I^2C pin; referenced to VCCC.
7	SCL_C	Connector-side (DDC) SCL bi-directional I^2C pin; referenced to VCCC.
8	CEC_C	Connector-side (CEC) bi-directional pin; referenced to internal 3.3V voltage regulator (V_{REG}). RPU decoupled from “3.3V Internal” if OE=LOW.
9	HPD_C	Connector-side HPD, input for the “hot plug” detect.
10	HPD_H	Host-side HPD; output for the hot plug detect. This pin references VCCA and indicates to the HDMI controller (HDMI source) when there is an HDMI sink connected to the FXMHD103.
11	VCCA	Host-side power supply, 1.6V – 3.6V.
12	CEC_H	Host-side CEC, bi-directional pin; referenced to VCCA. RPU decoupled from VCCA if OE=LOW.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Condition		Min.	Max.	Unit
V_{CC}	Supply Voltage Range	VCCA, VCCC		-0.5	6.5	V
V_{IN}[3]	Input Voltage Range	SCL_H, SDA_H, CEC_H, OE		-0.5	6.5	V
		SCL_C, SDA_C, CEC_C, HPD_C		-0.5	6.5	
V_O[3]	Output Voltage	SCL_H, SDA_H, CEC_H, HPD_H		-0.5	6.5	V
		SCL_C, SDA_C, CEC_C		-0.5	6.5	
I_{IK}	Input Clamp Current	V_{IN} < 0V			-50	mA
I_{OK}	Output Clamp Current	V_O < 0V			-50	mA
T_J	Junction Temperature			-40	+150	°C
T_{STG}	Storage Temperature Range			-65	+150	°C
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114-B	All Pins		8	kV
		Charged Device Model, JESD22-C101	All Pins		2	
		IEC 61000-4-2	Air Gap		16	
			Contact		9	

Note:

3. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings. Unless otherwise noted, values are across the recommended operating free-air temperature range.

Symbol	Parameter	Condition		Min.	Max.	Unit
V_{CCA}	Supply Voltage	VCCA		1.6	3.6	V
V_{CCC}	Supply Voltage	VCCC		4.8	5.3	V
V_{IN}	Input Voltages	Host Port	SCL_H, SDA_H, CEC_H	0	V_{CCA}	V
			OE	0	V_{CCA}	
		Connector Port	SCL_C, SDA_C	0	V_{CCC}	
			CEC_C	0	3.3V (Internal)	
			HPD_C	0	V_{CCC}	
T_A	Ambient Temperature			-40	+85	°C
T_J	Junction Temperature			-40	+125	°C

Thermal Properties

Junction-to-ambient thermal resistance is a function of application and board layout. This data is measured with four-layer 2s2p boards in accordance to JEDEC standard JESD51. Special attention must be paid not to exceed junction temperature T_J (maximum) at a given ambient temperature.

Symbol	Parameter	Typ.	Unit
Θ_{JA}	Junction-to-Ambient Thermal Resistance	320	°C/W

DC Electrical Characteristics (I_{CC})

Unless otherwise specified, T_A=-40 to 85°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I_{CCPD1}	Power Down 1	V_{CCA}=0V, or V_{CCC}=0V, All Other Pins=Don't Care			1	µA
I_{CCPD2}	Power Down 2	OE=LOW, V_{CCA} and V_{CCC} Valid, All Other Pins=Don't Care			1	µA
I_{CCHPD}	Active HPD Only	OE=HIGH, V_{CCA} and V_{CCC} Valid, SCL_H, SDA_H and CEC_H=HIGH, HPD_C=0V			1.5	µA
I_{CCA}	Active HDMI Link	V_{CCA} and V_{CCC} Valid, SCL_H, SDA_H and CEC_H=HIGH, HPD_C=V_{CCC}, OE=HIGH			5	µA
I_{CCC}		V_{CCA} and V_{CCC} Valid, SCL_H, SDA_H and CEC_H=HIGH, HPD_C=V_{CCC}, OE=HIGH			5	µA

Back Drive Current

Unless otherwise specified, T_A=-40 to 85°C.

Symbol	Parameter	Condition	V_{CCA}	V_{CCC}	Typ.	Max.	Unit
$Iback_{CEC}$	Current Through CEC_C	CEC_C=0V - 5V	0V	0V	0.1	1.8	µA
$Iback_{DDC}$	Current Through SDA_C and SCL_C	SDA_C and SCL_C=0V – 5V	0V	0V	0.1	5.0	µA
$Iback_{VCCC}$	Current Through VCCC	V_{CCC}=0V – 5V	0V	NA	0.1	5.0	µA
$Iback_{HPD}$	Current Through HPD_C	HPD_C=0V – 5V	0V	0V	0.1	5.0	µA

Voltage Level Shifter: SCL, SDA Lines (Host/Connector Ports)

Unless otherwise specified, T_A=-40 to 85°C.

Symbol	Parameter	Condition	V_{CCA}	Min.	Typ.	Max.	Unit
V_{IH}	High Level input Voltage	Host Side	1.6V to 3.6V	V_{CCA} - 0.4			V
		Connector Side	1.6V to 3.6V	V_{CCC} - 0.4			
V_{IL}	Low Level Input Voltage	Host Side	<2V			0.2 x V_{CCA}	V
		Host Side	>2V			0.4	
		Connector Side	1.6V to 3.6V			0.4	
V_{OH}	High Level Output Voltage	Host Side: I_{OH}=-10µA	1.6V to 3.6V	V_{CCA} x 0.8			V
		Connector Side: I_{OH}=-10µA	1.6V to 3.6V	V_{CCC} - 0.3			
V_{OL1}	Low Level Output Voltage	I_{OL}=3mA, V_{IL}=0V; Both Directions	1.6V to 3.6V			0.05	V
V_{OL2}		I_{OL}=3mA, V_{IL}=0.25V; Both Directions	1.6V to 3.6V			0.30	V
V_{OL3}		I_{OL}=3mA, V_{IL}=0.3V; Both Directions	1.6V to 3.6V			0.35	V
V_{OL4}		I_{OL}=3mA, V_{IL}=0.4V; Both Directions	1.6V to 3.6V			0.45	V
V_{OL5}		I_{OL}=3mA, V_{IL}=0.6V C→ H Direction Only	1.6V to 3.6V			0.65	V
RPU	Internal Pull-up	SCL_H, Internal Pull-up Connected to SDA_H, VCCA Rail			10.00		kΩ
		SCL_C, Internal Pull-up Connected to SDA_C, VCCC			1.75		
$I_{PULLUPAC}$	Transient Boosted Pull-up Current (Edge Rate Accelerator)	SCL_C, Internal Pull-up Connected to SDA_C, VCCC			15		mA
I_{OFF}	Host Port	V_{CCA}=0V, V_I or V_O=0 to 3.6V	0V			±5	µA
	Connector Port	V_{CCC}=0V, V_I or V_O=0 to 5.3V	0V to 3.6V			±5	
I_{OZ}	Connector Port	V_O=VCCO or GND	1.6V to 3.6V			±5	µA
	Host Port	V_I=VCCI or GND	1.6V to 3.6V			±5	

Voltage Level Shifter: CEC Lines (Host/Connector Ports)

Unless otherwise specified, T_A=-40 to 85°C.

Symbol	Parameter	Condition	V_{CCA}	Min.	Typ.	Max.	Unit
V_{IH}	High Level input Voltage	Host Side	1.6V to 3.6V	V_{CCA} - 0.4		V_{CCA}	V
V_{IL}	Low Level Input Voltage	Host Side	<2V			0.2 x V_{CCA}	V
		Host Side	>2V			0.4	
		Connector Side	1.6V to 3.6V			0.6	
V_{OH}	High Level Output Voltage	Host Side, I_{OH}=-10µA	1.6V – 3.6V	V_{CCA} x 0.8			V
V_{OH}	High Level Output Voltage	Connector Side, I_{OH}=-10µA	1.6V – 3.6V	2.75	3.10		V
V_{OL1}	Low Level Output Voltage Host & Connector Sides	I_{OL}=3mA, V_{IL}=0V	1.6V to 3.6V			0.05	V
V_{OL2}		I_{OL}=3mA, V_{IL}=0.25V	1.6V to 3.6V			0.30	V
V_{OL3}		I_{OL}=3mA, V_{IL}=0.3V	1.6V to 3.6V			0.35	V
V_{OL4}		I_{OL}=3mA, V_{IL}=0.4V	1.6V to 3.6V			0.45	V
V_{OL5}		I_{OL}=3mA, V_{IL}=0.6V	1.6V to 3.6V			0.65	V
$VOUT_{DIS}$	Output Voltage when Disabled	CEC_C: HPD_C=LOW, OE=HIGH, V_{CCC}=4.8V – 5.3V	1.6V to 3.6V			0.3	V
R_{PU}	Internal Pull-up	CEC_H, Internal Pull-up Connected to VCCA Rail			10		kΩ
		CEC_C, Internal Pull-up Connected to Internal 3.3V Rail			27		
I_{OFF}	H Port	V_{CCA}=0V, V_I or V_O=0 to 3.6V	0V			±5.0	µA
	C Port	V_{CCC}=0V, V_I or V_O=0 to 5.3V	0V to 3.6V			±1.8	
I_{OZ}	C Port	V_O=VCCO or GND	1.6V to 3.6V			±5.0	µA
	H Port	V_I=VCCI or GND	1.6V to 3.6V			±5.0	

Voltage Level Shifter: HPD Lines (Host/Connector Ports)

T_A=-40 to 85°C unless otherwise specified.

Symbol	Parameter	Condition	V_{CCA}	Min.	Typ.	Max.	Unit
V_{IH}	High Level Input Voltage		1.6V to 3.6V	2			V
V_{IL}	Low Level Input Voltage		1.6V to 3.6V			0.8	V
V_{OH}	High Level Output Voltage	I_{OH}=-3mA	1.6V to 3.6V	0.7 x V_{CCA}			V
V_{OL}	Low Level Output Voltage	I_{OL}=3mA	1.6V to 3.6V			0.3	V
V_{HYS}	HPD_C (V_{T+} - V_{T-})		1.6V to 3.6V		200		mV
R_{PD}	Internal Pull-Down	HPD_C, Internal Pull-down Connected to Ground, VCCA and VCCC Powered up			100		KΩ
I_{OFF}	Host Port	V_O=V_{CCO} or GND	0V			±5	µA
I_{OZ}	Host Port	V_I=V_{CCI} or GND	3.6V			±5	µA

AC Electrical Characteristics[4]

Unless otherwise specified, T_A=-40 to 85°C. Typical values T_A= 25°C.

Voltage Level Shifter: SCL, SDA Lines (Host and Connector Ports); V_{CCA}=1.8V

Symbol	Parameter	Pins	Condition	Min.	Typ.	Max.	Unit
t_{PHL}	Propagation Delay	H to C	DDC Channels Enabled		100		ns
		C to H			5		
t_{PLH}		H to C			25		
		C to H			5		
t_f	H Port Fall Time	H Port	DDC Channels Enabled 70% -30%		2		ns
	C Port Fall time	C Port			80		
t_r	H Port Rise Time	H Port	DDC Channels Enabled 30% -70%		2		ns
	C Port Rise Time	C Port			50		
f_{MAX}	Maximum Switching Frequency		DDC Channels Enabled	400			kHZ

Voltage Level Shifter: CEC Line (Host and Connector Ports); V_{CCA}=1.8V

Symbol	Parameter	Pins	Condition	Min.	Typ.	Max.	Unit
t_{PHL}	Propagation Delay	H to C	CEC Channels Enabled		100		ns
		C to H			5		
t_{PLH}		H to C			25		ns
		C to H			5		
t_f	H Port Fall Time	H Port	CEC Channels Enabled 90% - 10%		10	50000	ns
	C Port Fall time	C Port			200	50000	
t_r	H Port Rise Time	H Port	CEC Channels Enabled 10% - 90%		5	400	ns
	C Port Rise Time	C Port			0.2	250	µs

Voltage Level Shifter: HPD Line (Host and Connector Ports); V_{CCA}=1.8V

Symbol	Parameter	Pins	Condition	Min.	Typ.	Max.	Unit
t_{PHL}	Propagation Delay	C to H	HPD Channel Enabled		10		ns
t_{PLH}		C to H			5		
t_f	H Port Fall Time	H Port	HPD Channel Enabled 90% - 10%		1		ns
t_r	H Port Rise Time	H Port	HPD Channel Enabled 10% - 90%		3		ns

I/O Capacitance

T_A= 25°C unless otherwise specified.

Symbol	Parameter	Condition	V_{CCA} & V_{CCC}	Min.	Typ.	Max.	Unit
C_I	Control Inputs		0V		2		pF
C_{IO}	DDC & CEC on Host Port		0V		5		pF
	DDC on Connector Port	LCR: V_{bias}=2.5V; AC Input=3.5V_{pp}; f=100kHZ	0V		10	16.5	pF
	CEC on Connector Port	LCR: V_{bias}=1.65V; AC Input=2.5V_{pp}; f=100kHZ	0V		10	16.5	pF

Note:

4. AC Characteristics are guaranteed by Design and Characterization, not production tested.

AC Parameter Measurement Information(5,6,7,8,9)

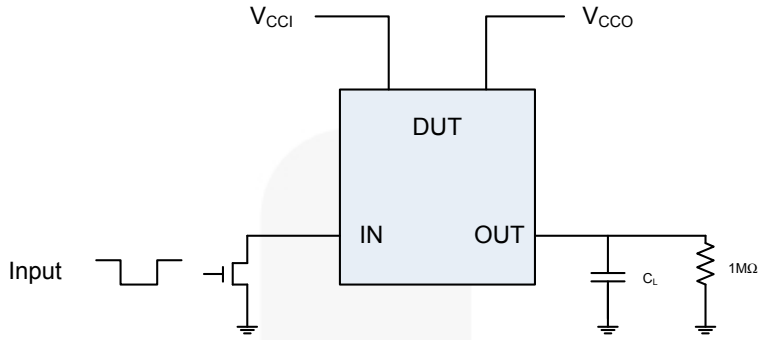

Figure 5. Device Under Test Setup

Table 2. AC Load

Symbol	Parameter	Condition	V_{CCA}	Min.	Typ.	Max.	Unit
C_L	Bus Load Capacitance (Connector-Side)	CEC	1.6V to 3.6V			1300	pF
	Bus Load Capacitance (Connector-Side)	DDC & HPD	1.6V to 3.6V			800	
	Bus Load Capacitance (Host-Side)	All Pins	1.6V to 3.6V			15	

Notes:

5. R_T termination resistance should be equal to Z_{OUT} of the pulse generator.
6. C_L includes probe and jig capacitance.
7. All input pulses supplied by generators have the following characteristics: PRR $\leq$ 10MHz, Z_O=50Ω, slew rate $\geq$ 1V/ns.
8. The outputs are measured one at a time, with one transition per measurement.
9. t_{PLH} and t_{PHL} are the same as t_{PD}.

Timing Diagrams(10,11,12,13,14)

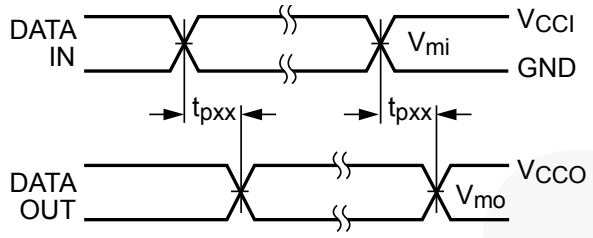

Figure 6. Waveform for Inverting and Non-Inverting Functions

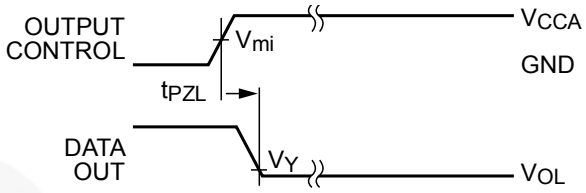

Figure 7. 3-STATE Output Low Enable Time

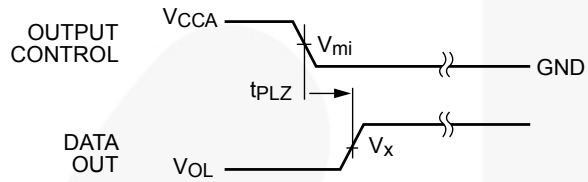

Figure 8. 3-STATE Output High Enable Time

Symbol	V_{CC}
V_{mi}	V_{CCI} / 2
V_{mo}	V_{CCO} / 2
V_X	0.5 x V_{CCO}
V_Y	0.1 x V_{CCO}

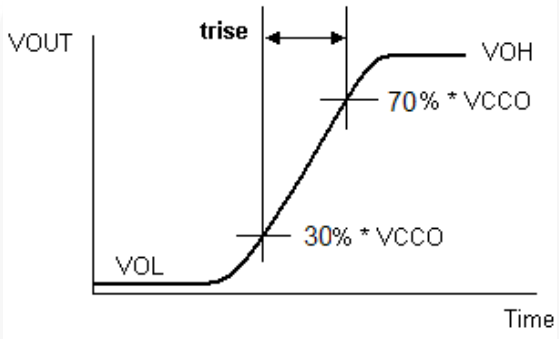

Figure 9. Active Output Rise Time

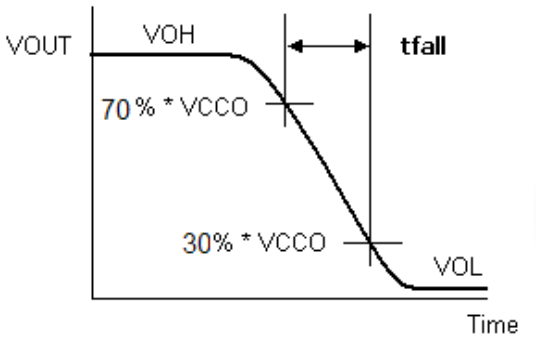

Figure 10. Active Output Fall Time

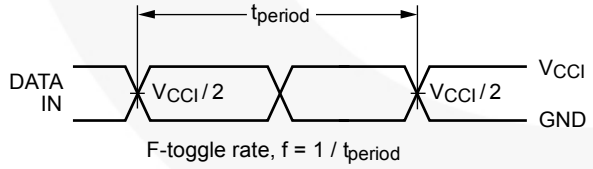

Figure 11. F-Toggle Rate

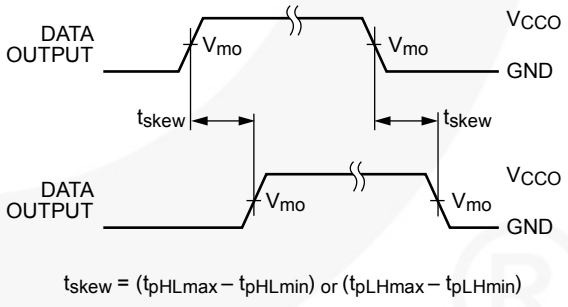

Figure 12. Output Skew Time

Notes:

10. Input t_R=t_F=2.0ns, 10% to 90% at V_{IN}=1.65V to 1.95V;
    Input t_R=t_F=2.0ns, 10% to 90% at V_{IN}=2.3 to 2.7V;
    Input t_R=t_F=2.5ns, 10% to 90%, at V_{IN}=3.0V to 3.6V only;
    Input t_R=t_F=2.5ns, 10% to 90%, at V_{IN}=4.5V to 5.5 only.
11. V_{CCI}=V_{CCA} for control pin OE or V_{mi}=(V_{CCA} / 2).
12. DDC Rise Times 30% - 70%, CEC & HPD Rise Times 10% - 90%
13. DDC Fall Times 30% - 70%, CEC & HPD Fall Times 10% - 90%
14. V_{CCI} is the V_{CC} associated with the input side. V_{CCO} is the V_{CC} associated with the output side.

Application Information

Power Down

The FXMHD103 can be powered down if either V_{CCA} or V_{CCC} equals 0V, or if OE is LOW.

"Hot Plug" Detect Operation

After VCCA and VCCC have powered up to valid levels, and OE enabled (HIGH) the HPD path is enabled. The internal 3.3V voltage regulator and the CEC & DDC blocks are disabled due to the internal weak pull-down resistor (100kΩ to GND) on HPD_C. When the HDMI sink recognizes a valid 5V signal on the HDMI connector, to inform the HDMI source there is a valid HDMI sink connected to the HDMI connector; the sink typically ties the HPD_C signal to the HDMI 5V supply through a 1KΩ resistor. A HIGH on HPD_C, in turn, enables the internal voltage regulator, as well as the DDC & CEC paths. The HDMI link is active between the HDMI source and the HDMI sink.

When HPD_C is LOW, the respective resistor pull-ups (RPUs) on the host and connector sides of the DDC paths remain coupled to their respective voltage references. Likewise, when HPD_C is LOW, the RPUs on the host and connector sides of the CEC path remain coupled to their respective voltage references. Since HPD_C disables V_{REG} and V_{REG} is the CEC_C voltage reference, CEC_C is held to 0V by a weak (50nA) current source when HPD_C is LOW. This is captured by the $VOUT_{DIS}$ parameter.

Backdrive Protection

Backdrive-current protection is available on all FXMHD103 signals interfacing with the HDMI connector, including VCCC, SCL_C, SDA_C, CEC_C, and HPD_C. If the FXMHD103 is powered down, V_{CCA}=0V or V_{CCC}=0V and the HDMI sink forces 0V – 5V onto any of the HDMI connector-facing pins (VCCC, SCL_C, SDA_C, CEC_C & HPD_C). The maximum current flow from the FXMHD103 is only 5µA, with the exception of 1.8µA (maximum) on CEC_C.

DDC Channel Description

The HDMI specification implements the Video Electronics Standards Association (VESA) Display Data Channel (DDC) for communication between a single HDMI source and a single HDMI sink. The DDC is used by the HDMI source to read the HDMI sink's Enhanced Extended Display Identification Data (E-EDID) to discover the sink's configuration or capabilities. DDC must meet the I^2C specification, version 2.1, for Standard Mode devices. Because the HDMI application is meant for high-definition Transition-Minimized Differential Signaling (TMDS) video transport across a cable, the HDMI specification requires the DDC signals (SCL & SDA) be able to drive a minimum capacitance of 800pF (source 50pF + cable assembly 700pF + sink 50pF). The I^2C specification requires a minimum of 400pF capacitance.

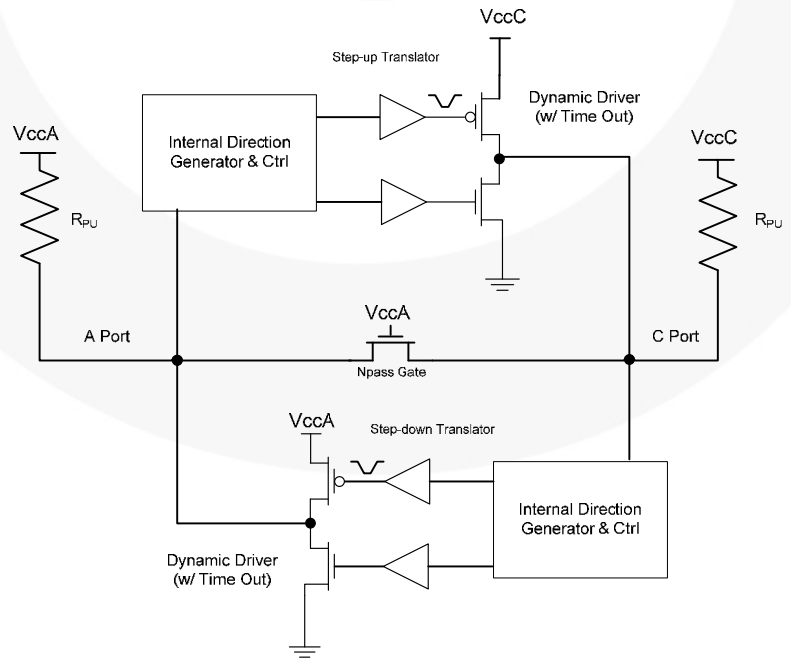

Figure 13. DDC Channel Block Diagram, 1 of 2 Channels (SDA & SCL)

Edge Rate Accelerators

The FXMHD103 DDC channel is designed for high-performance I^2C level shifting. Figure 13 shows that each bi-directional channel contains an Npassgate and two dynamic drivers. This hybrid architecture is highly beneficial in an I^2C application with large capacitive loads and where auto-direction is necessary.

For example, during the following I^2C protocol events the bus direction needs to change from “Source-to-Sink” to “Sink-to-Source” without the occurrence of an edge:

- Clock Stretching
- Slave’s ACK Bit (9th bit=0) following a Master’s Write Bit (8th bit=0)
- Clock Synchronization and Multi Master Arbitration

If there is an I^2C translator between the source and sink in these examples, the I^2C translator must change direction when both A and C ports are LOW. The Npassgate can accomplish this efficiently because, when both A and C ports are LOW, the Npassgate acts as a low resistive short between the (A and C) ports.

Due to the I^2C open-drain topology, I^2C drivers are not push/pull devices. Logic LOWs are “pulled down” (I_{sink}), while logic HIGHs are “let go” (3-state). For example, when the source lets go of SCL (SCL always comes from the source), the rise time of SCL is largely determined by the RC time constant, where R=RPU and C=the bus capacitance. If the FXMHD103 is attached to the source [on the A port] and there is a source on the C port, the Npassgate acts as a low-resistive short between both ports until either of the port’s $V_{CC/2}$ thresholds is reached. After the RC time constant has reached the $V_{CC/2}$ threshold of either port, the port’s edge detector triggers both dynamic drivers to drive their respective ports in the LOW-to-HIGH (LH) direction, accelerating the rising edge. The resulting rise time resembles the scope shot in Figure 14. Effectively, two distinct slew rates appear in rise time. The first slew rate (slower) is the RC time constant of the bus. The second slew rate (much faster) is the dynamic driver accelerating the edge.

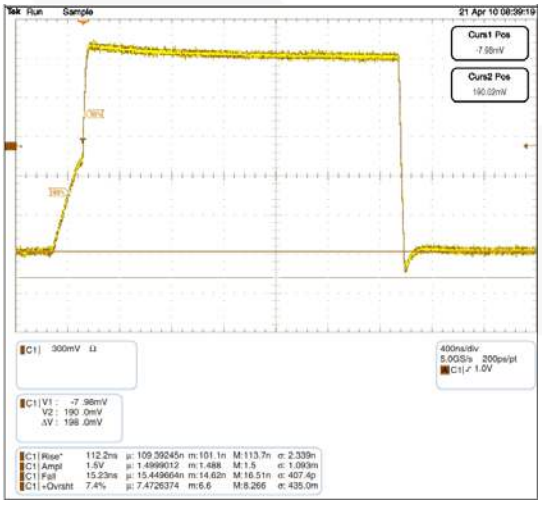

Figure 14. Rise Time Driving 600pF Load

If both the A and C ports of the translator are HIGH, a high-impedance path exists between the A and C ports because both the Npassgates are turned off. If a source or sink device decides to pull SCL or SDA LOW, that device’s driver pulls down (I_{sink}) SCL or SDA until the edge reaches the A or C port $V_{CC}/2$ threshold. When either the A or C port threshold is reached, the port’s edge detector triggers both dynamic drivers to drive their respective ports in the HIGH-to-LOW (HL) direction, accelerating the falling edge.

Driving a Capacitive Load

The FXMHD103 dynamic drivers have enough current sourcing capability to drive an 800pF capacitive bus. The Figure 14 scope shot is of an FXMHD103 driving a lumped load of 600pF. Notice the (30% - 70%) rise time is only 112ns (R_{PU}=5KΩ). This is well below the maximum rise time of 1000ns in Standard Mode (100KHz) or 300ns in Fast Mode (400KHz).

V_{OL} vs. V_{IL} & I_{OL}

The I^2C specification mandates a maximum V_{IL} (I_{OL} of 3mA) of V_{CC} x 0.3 for an I^2C receiver and a maximum V_{OL} of 0.4V for an I^2C transmitter. If there is an HDMI source on the A port of an I^2C translator with a V_{CC} of 1.8V and an HDMI sink on the I^2C translator C port with a V_{CC} of 5.0V, the maximum V_{IL} of the source is (1.6V x 0.3) 480mV. Meanwhile, the sink could transmit a valid logic LOW of 0.4V to the source. 80mV is not very much margin between the maximum transmitted V_{OL} of 400mV (HDMI sink) to the maximum received V_{IL} of 480mV (HDMI source). This appears to be an oversight in the I^2C specification, but there is an explanation. The I^2C specification assumes transmitters and receivers share the same V_{CC}. The I^2C specification does call out separate V_{OL} requirements vs. V_{CC} conditions where V_{OL1}=0.4V when V_{CC} is > 2.0V and V_{OL3}=0.2 x V_{CC}, when V_{CC} is < 2.0V. When there is V_{CC} alignment between I^2C transmitters and receivers, the I^2C specification provides adequate V_{IL} vs. V_{OL} margins. However, when you have a transmitter operating at 5V and a receiver operating at 1.6V through a translator or level shifter, the V_{OL} vs. V_{IL} margin gets very tight, as in the above example. Therefore, the voltage drop across the I^2C translator must be as low as possible.

In general, if the I^2C translator’s channel resistance is too high, the voltage drop across the translator could present a V_{IL} to a receiver greater than the receiver’s maximum V_{IL}. To complicate matters, the I^2C specification states that 6mA of I_{OL} is recommended for bus capacitances approaching 400pF in Fast Mode. More I_{OL} increases the voltage drop across the I^2C translator. The I^2C application benefits when I^2C translators exhibit low V_{OL} performance. Table 3 depicts the FXMHD103 targeted V_{OL} performance vs. V_{IL}/I_{OL} when the direction is from C side to A side, V_{CCC}=5.0V and V_{CCA}=1.6V.

Table 3. DDC Voltage Drop (V_{OL} vs. V_{IL}/I_{OL}): Port C → Port A Direction, V_{CCA}=1.6V

V_{IL} (mV)	I_{OL} (mA)	V_{OL} Max. (mV)	Voltage Drop Max. (mV)	Calculated Max. R_{ON} (Ω)
0	6	50	50	8.33
250	6	300	50	8.33
300	6	350	50	8.33
400	6	450	50	8.33
600	6	650	50	8.33

PCB Layout Recommendation

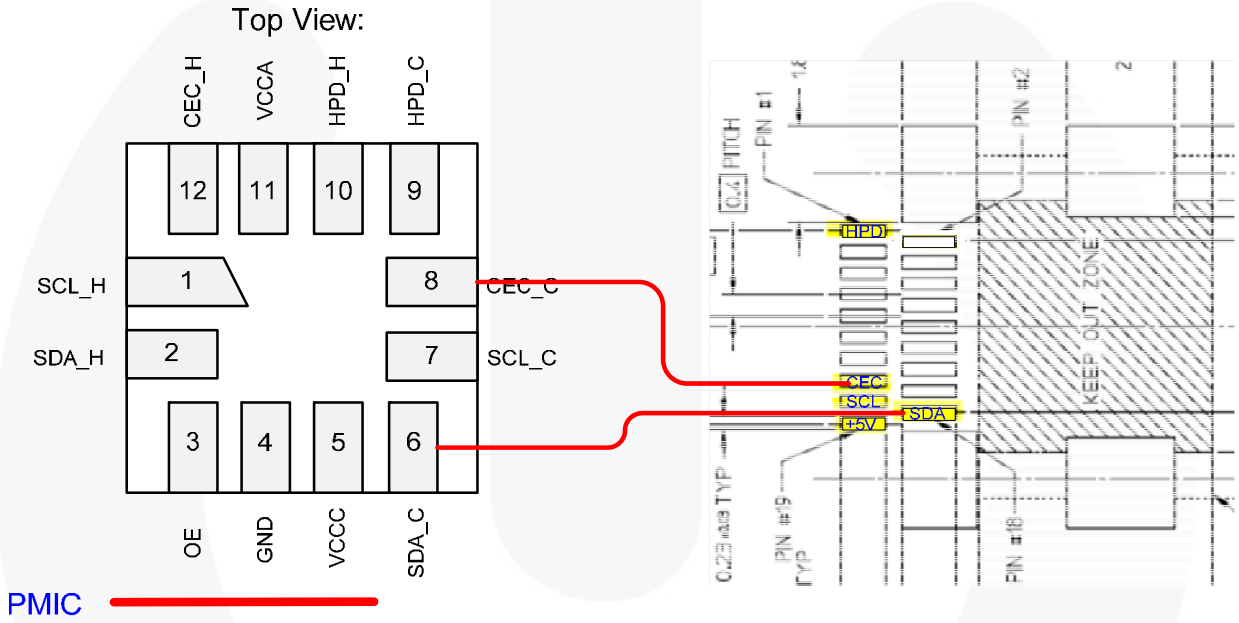

Figure 15. PCB Routing Example (Molex HDMI Type-D Connector)

Physical Dimensions

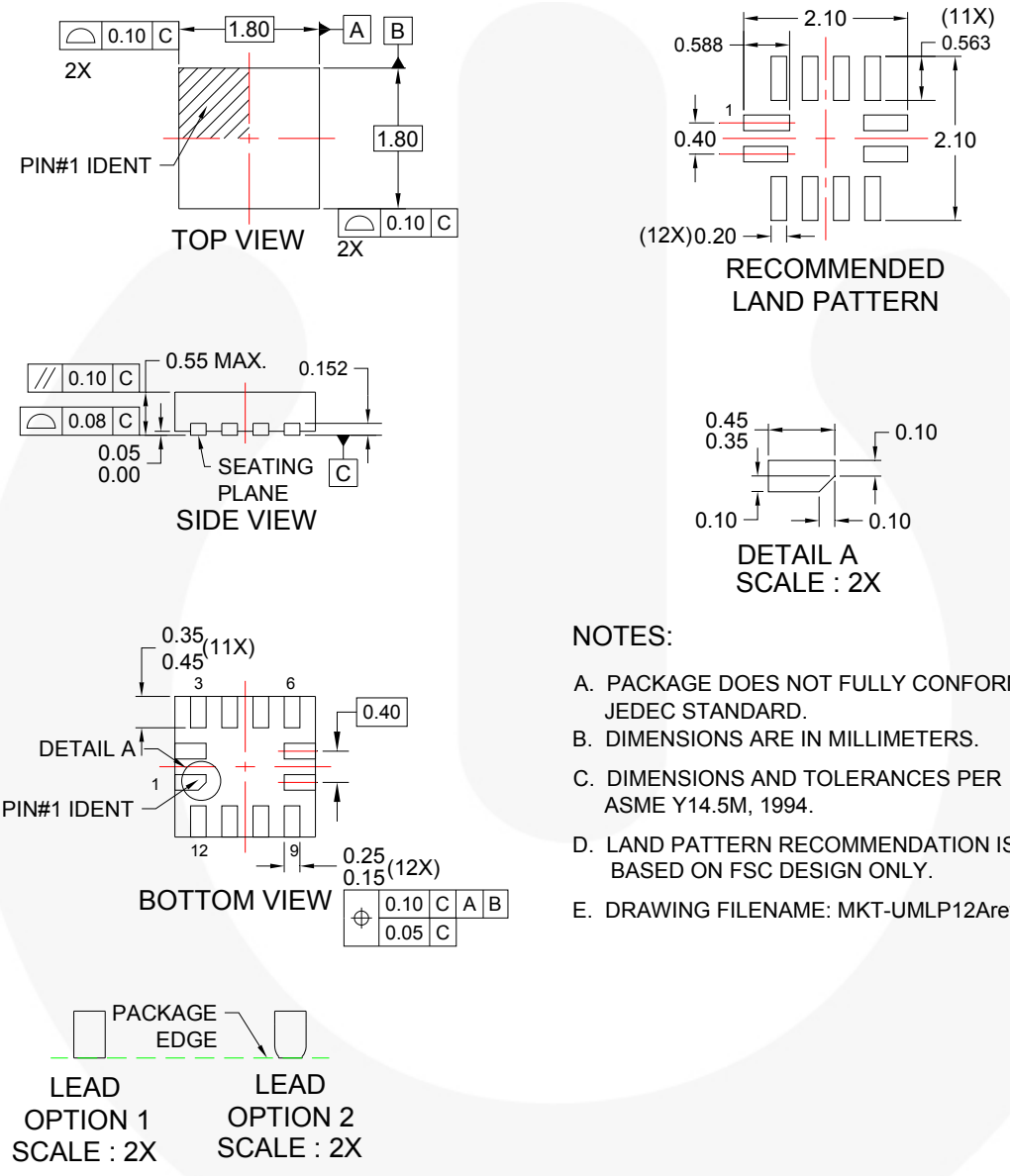

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Figure 16. 12-Lead, UMLP, Quad JEDEC MO-252, 1.8mm x 1.8mm, 0.4mm Pitch

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