

# SN54ALS564B, SN74ALS564B OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

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- 3-State Buffer-Type Inverting Outputs Drive Bus Lines Directly
- Bus-Structured Pinout
- Buffered Control Inputs
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), Standard Plastic (N) and Ceramic (J) 300-mil DIPs, and Ceramic Flat (W) Packages

## description

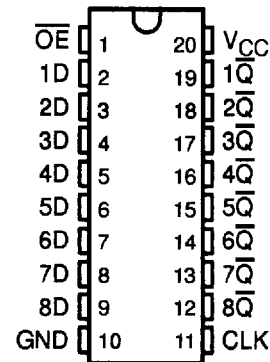
These octal D-type edge-triggered flip-flops feature inverting 3-state outputs designed specifically for bus driving. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops enter data on the low-to-high transition of the clock (CLK) input.

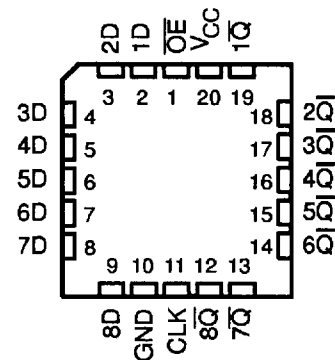
The output-enable ( $\overline{OE}$ ) input does not affect internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54ALS564B is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74ALS564B is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

SN54ALS564B ... J OR W PACKAGE  
SN74ALS564B ... DW OR N PACKAGE  
(TOP VIEW)



SN54ALS564B ... FK PACKAGE  
(TOP VIEW)



FUNCTION TABLE  
(each flip-flop)

INPUTS			OUTPUT
OE	CLK	D	$\overline{Q}$
L	$\uparrow$	H	L
L	$\uparrow$	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

PRODUCTION DATA Information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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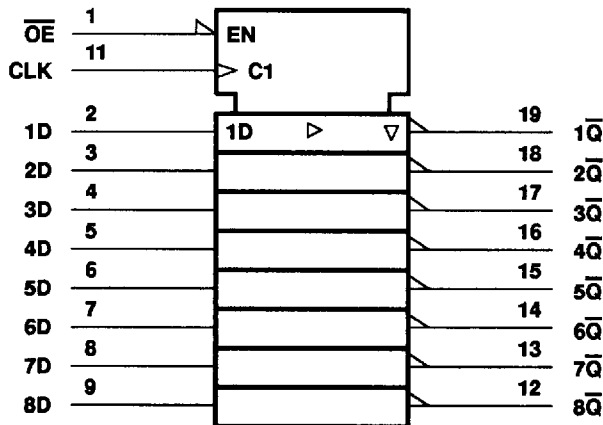
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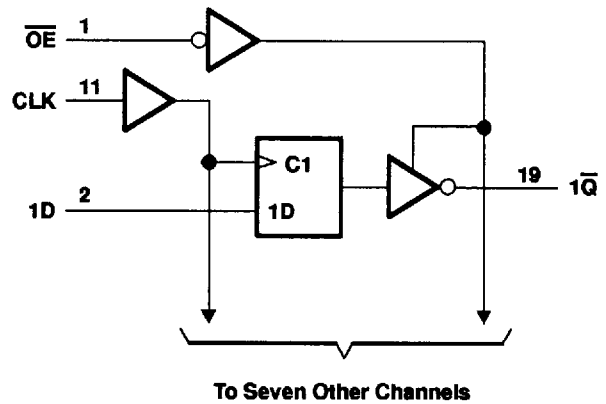
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## logic symbol†



## logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, $V_{CC}$	7 V
Input voltage, $V_I$	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, $T_A$ : SN54ALS564B	-55°C to 125°C
SN74ALS564B	0°C to 70°C
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## recommended operating conditions

	SN54ALS564B			SN74ALS564B			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$ Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$ High-level input voltage	2			2			V
$V_{IL}$ Low-level input voltage			0.7			0.8	V
$I_{OH}$ High-level output current			-1			-2.6	mA
$I_{OL}$ Low-level output current			12			24	mA
$f_{clock}$ Clock frequency	0		22	0		30	MHz
$t_w$ Pulse duration, CLK high or low	25			14			ns
$t_{su}$ Setup time, data before CLK↑	15			15			ns
$t_h$ Hold time, data after CLK↑	4			0			ns
$T_A$ Operating free-air temperature	-55		125	0		70	°C



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# SN54ALS564B, SN74ALS564B OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS564B		SN74ALS564B		UNIT	
			MIN	TYP†	MAX	MIN		TYP†
$V_{IK}$	$V_{CC} = 4.5 V$ ,	$I_I = -18 mA$			-1.2		-1.2	V
$V_{OH}$	$V_{CC} = 4.5 V$ to $5.5 V$ , $I_{OH} = -0.4 mA$		$V_{CC} - 2$		$V_{CC} - 2$		V	
	$V_{CC} = 4.5 V$	$I_{OH} = -1 mA$	2.4	3.3				
$V_{OL}$	$V_{CC} = 4.5 V$	$I_{OL} = 12 mA$	0.25	0.4	0.25	0.4	V	
		$I_{OL} = 24 mA$			0.35	0.5		
$I_{OZH}$	$V_{CC} = 5.5 V$ ,	$V_O = 2.7 V$			20		20	$\mu A$
$I_{OZL}$	$V_{CC} = 5.5 V$ ,	$V_O = 0.4 V$			-20		-20	$\mu A$
$I_I$	$V_{CC} = 5.5 V$ ,	$V_I = 7 V$			0.1		0.1	mA
$I_{IH}$	$V_{CC} = 5.5 V$ ,	$V_I = 2.7 V$			20		20	$\mu A$
$I_{IL}$	$V_{CC} = 5.5 V$ ,	$V_I = 0.4 V$			-0.2		-0.2	mA
$I_{O}^{\ddagger}$	$V_{CC} = 5.5 V$ ,	$V_O = 2.25 V$	-20		-112	-30	-112	mA
$I_{CC}$	$V_{CC} = 5.5 V$	Outputs high	10	18	10	18	mA	
		Outputs low	15	24	15	24		
		Outputs disabled	16	30	16	30		

† All typical values are at  $V_{CC} = 5 V$ ,  $T_A = 25^\circ C$ .

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .

### switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 V$ to $5.5 V$ , $C_L = 50 pF$ , $R_1 = 500 \Omega$ , $R_2 = 500 \Omega$ , $T_A = MIN$ to $MAX^{\S}$				UNIT
			SN54ALS564B		SN74ALS564B		
			MIN	MAX	MIN	MAX	
$f_{max}$			22		30	MHz	
$t_{PLH}$	CLK	Any $\bar{Q}$	4	24	3	14	ns
$t_{PHL}$			4	20	4	14	
$t_{PZH}$	$\overline{OE}$	Any $\bar{Q}$	4	24	3	18	ns
$t_{PZL}$			3	23	4	18	
$t_{PHZ}$	$\overline{OE}$	Any $\bar{Q}$	2	14	1	10	ns
$t_{PLZ}$			3	29	2	15	

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



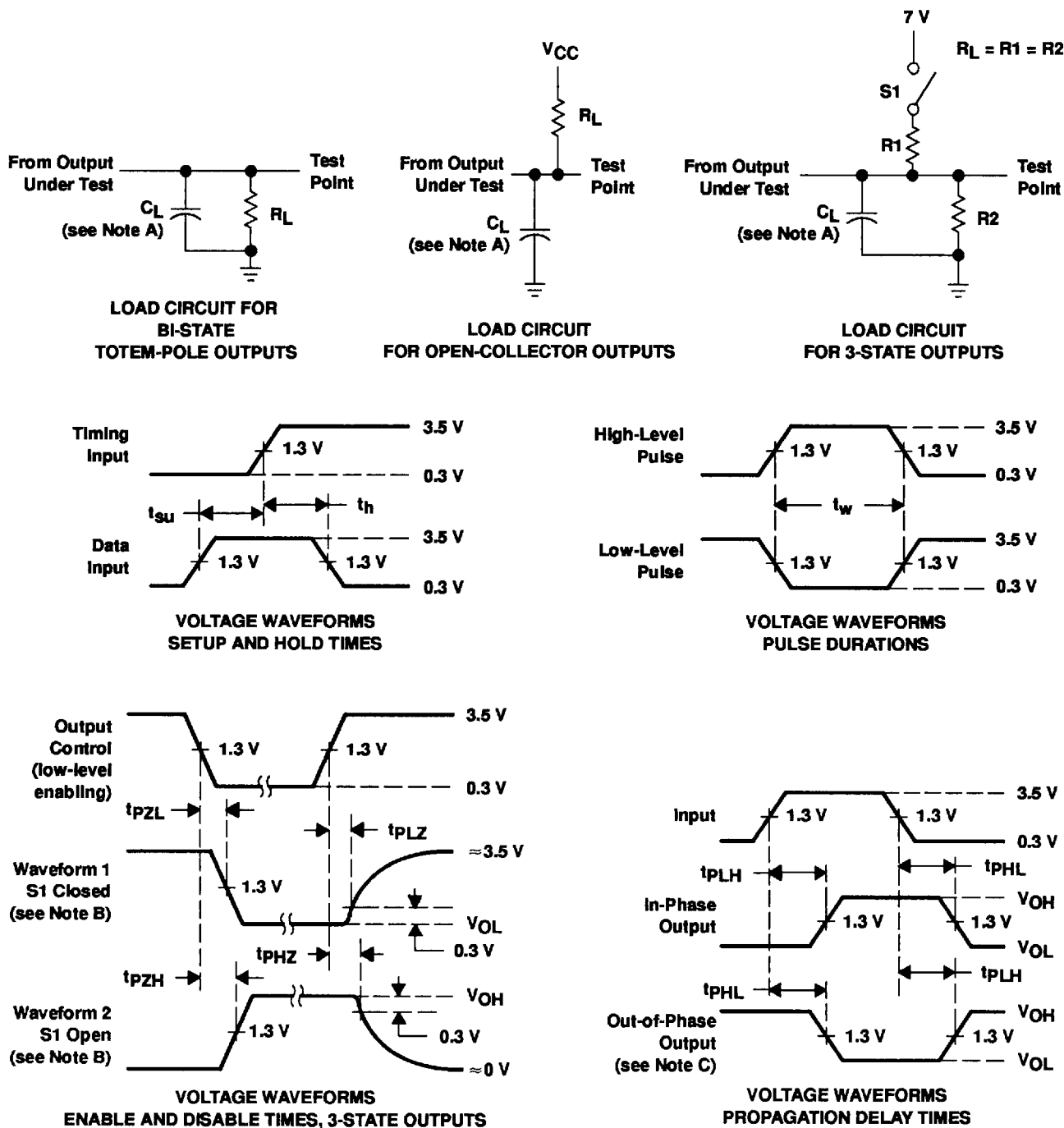
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## PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



NOTES: A.  $C_L$  includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. When measuring propagation delay items of 3-state outputs, switch S1 is open.

D. All input pulses have the following characteristics:  $PRR \leq 1$  MHz,  $t_r = t_f = 2$  ns, duty cycle = 50%.

E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

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