

Vishay Siliconix

N-Channel 20-V (D-S) 175 °C MOSFET

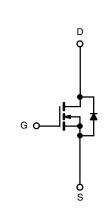
PRODUCT SUMMARY			
V _{(BR)DSS} (V)	$\mathbf{R}_{DSS}(V)$ $\mathbf{r}_{DS(on)}(\Omega)$		
20	0.0045 at V _{GS} = 10 V	60	
	0.0065 at V _{GS} = 4.5 V	60	

FEATURES

- TrenchFET[®] Power MOSFET
- 175 °C Junction Temperature
- 100 % R_g Tested
- 100 % UIS Tested

APPLICATIONS

• OR-ing



N-Channel MOSFET

GDS

TO-220AB

Ο

DRAIN connected to TAB

Top View

Ordering Information: SUP60N02-4m5P-E3 (Lead (Pb)-free)

ABSOLUTE MAXIMUM RATINGS $T_A = 25 \text{ °C}$, unless otherwise noted					
Parameter		Symbol	Limit	Unit	
Drain-Source Voltage		V _{DS}	20	V	
Gate-Source Voltage		V _{GS}	± 20		
Continuous Drain Current (T _J = 175 °C)	T _C = 25 °C	1-	60 ^a	A	
	T _C = 100 °C	I _D	60 ^a		
Pulsed Drain Current		I _{DM}	120		
Single Pulse Avalanche Current	L = 0.1 mH	I _{AS}	50		
Single Pulse Avalanche Energy		E _{AS}	125	mJ	
Maximum Power Dissipation ^b	T _C = 25 °C	– P _D	120 ^c	w	
	T _A = 25 °C ^d	۲D	3.75		
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 175	°C	

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Limit	Unit
Junction-to-Ambient (PCB Mount) ^d	R _{thJA}	40	°C/W
Junction-to-Case	R _{thJC}	1.25	0/11

Notes:

a. Package limited.

a. Fuddage immediate 1%.
b. Duty cycle ≤ 1%.
c. See SOA curve for voltage derating.
d. When mounted on 1" square PCB (FR-4 material).



SUP60N02-4m5P

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Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	$V_{DS} = 0 V, I_{D} = 250 \mu A$	20			V
Gate-Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \ \mu A$	1.0		3	
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 20 V$			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = 20 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$			1	μΑ
		V_{DS} = 20 V, V_{GS} = 0 V, T_{J} = 125 °C			50	
		$V_{DS} = 20$ V, $V_{GS} = 0$ V, $T_{J} = 175$ °C			250	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, \text{ V}_{GS} = 10 \text{ V}$	100			А
Drain-Source On-State Resistance ^a		$V_{GS} = 10 \text{ V}, \text{ I}_{D} = 20 \text{ A}$		0.0036	0.0045	- Ω
		V_{GS} = 10 V, I_{D} = 20 A, T_{J} = 125 °C			0.0068	
	r _{DS(on)}	V_{GS} = 10 V, I_{D} = 20 A, T_{J} = 175 °C			0.008	
		$V_{GS} = 4.5 \text{ V}, \text{ I}_{D} = 20 \text{ A}$		0.0052	0.0065	
Forward Transconductance ^a	9 _{fs}	V _{DS} = 10 V, I _D = 20 A		95		S
Dynamic ^b				4	·	
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 10 V, f = 1 MHz		5950		pF
Output Capacitance	C _{oss}			985		
Reverse Transfer Capacitance	C _{rss}			365		
Total Gate Charge ^b	Qg			33	50	nC
Gate-Source Charge ^b	Q _{gs}	$V_{DS} = 10 \text{ V}, V_{GS} = 4.5 \text{ V}, I_{D} = 50 \text{ A}$		18		
Gate-Drain Charge ^b	Q _{gd}			7		
Gate Resistance	R _g		0.75	1.5	2.3	Ω
Turn-On Delay Time ^b	t _{d(on)}			15	25	
Rise Time ^b	t _r	V_{DD} = 10 V, R _L = 0.2 Ω I _D \cong 50 A, V _{GEN} = 10 V, R _g = 1.0 Ω		7	11	- ns
Turn-Off Delay Time ^b	t _{d(off)}			35	55	
Fall Time ^b	t _f			8	12	
Source-Drain Diode Ratings and Cha	racteristics T	[−] _C = 25 °C ^c	<u> </u>		<u> </u>	
Continuous Current	ا _S				60	
Pulsed Current	I _{SM}				100	A
Forward Voltage ^a	V _{SD}	I _F = 20 A, V _{GS} = 0 V		0.85	1.5	V
Reverse Recovery Time	t _{rr}			45	90	ns
Peak Reverse Recovery Current	I _{RM}	I _F = 20 A, di/dt = 100 A/μs		1.7	3.4	Α
Reverse Recovery Charge	Q _{rr}			0.039	0.155	μC

Notes:

a. Pulse test; pulse width \leq 300 $\mu s,$ duty cycle \leq 2 %

b. Independent of operating temperature.

c. Guaranteed by design, not subject to production testing.

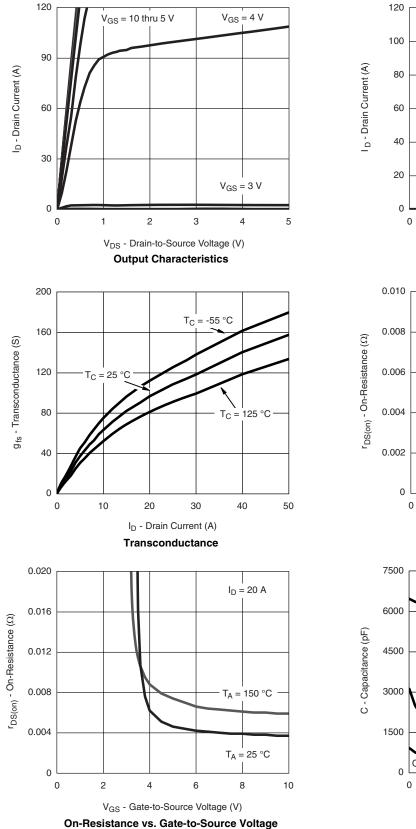
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

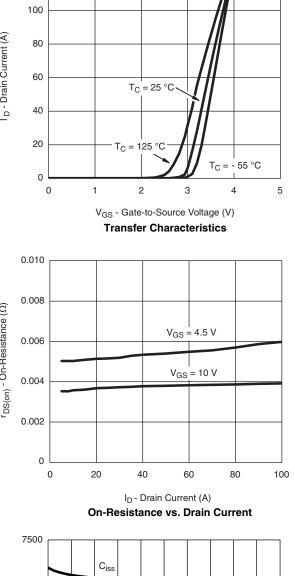


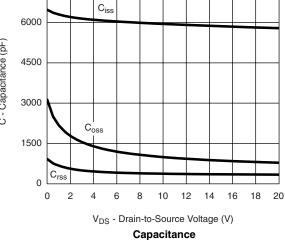
SUP60N02-4m5P

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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

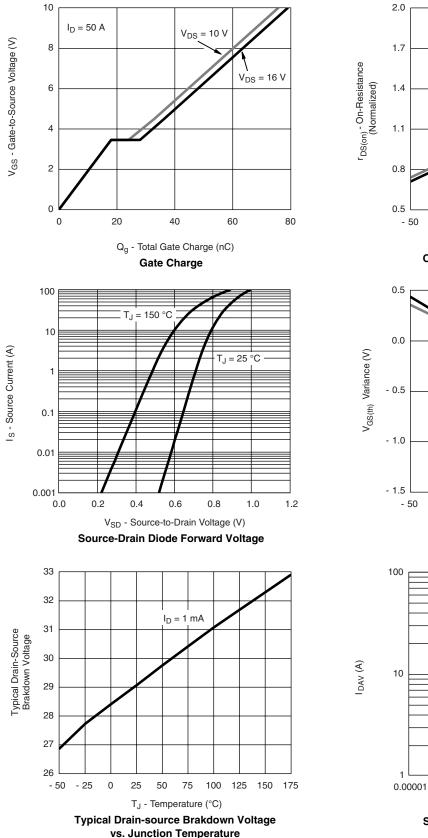


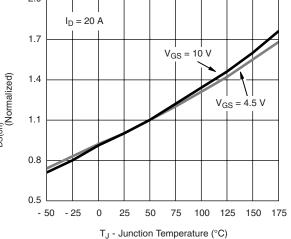




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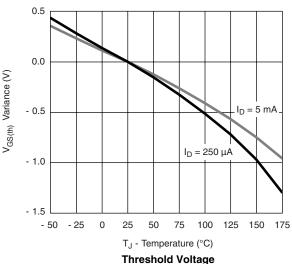
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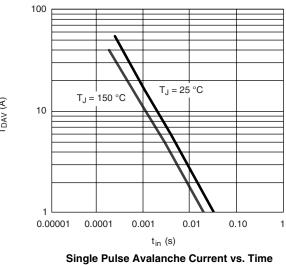


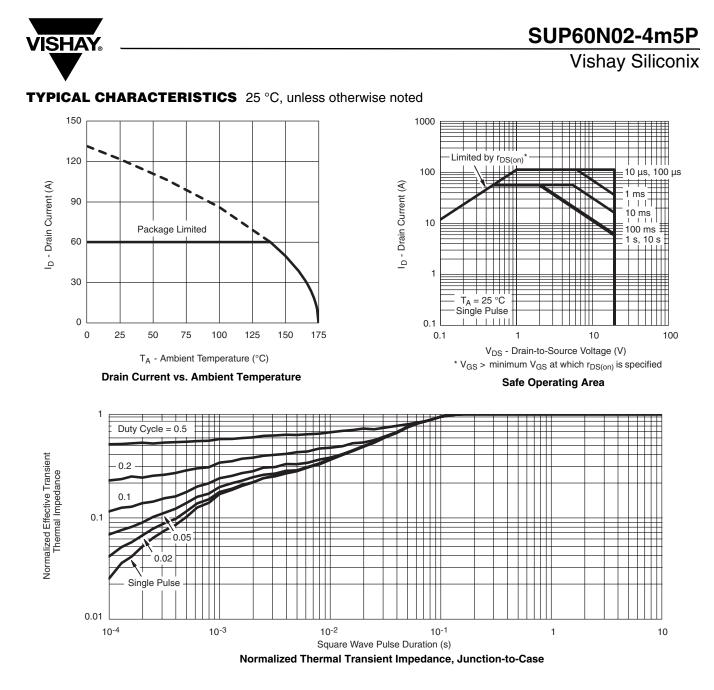


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On-Resistance vs. Junction Temperature







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