HARRIS SEMICONDUCTOR

HGTA32N60E2

April 1995

32A, 600V N-Channel IGBT

Features

- 32A, 600V
- Latch Free Operation
- Typical Fall Time 620ns
- High Input Impedance
- Low Conduction Loss

Description

The IGBT is a MOS gated high voltage switching device combining the best features of MOSFETs and bipolar transistors. The device has the high input impedance of a MOSFET and the low on-state conduction loss of a bipolar transistor. The much lower on-state voltage drop varies only moderately between +25°C and +150°C.

IGBTs are ideal for many high voltage switching applications operating at frequencies where low conduction losses are essential, such as: AC and DC motor controls, power supplies and drivers for solenoids, relays and contactors.

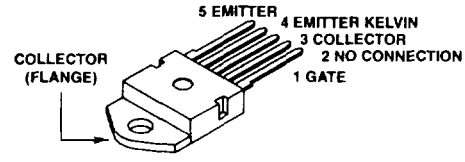
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
HGTA32N60E2	TO-218	GA32N60E2

NOTE: When ordering, use the entire part number.

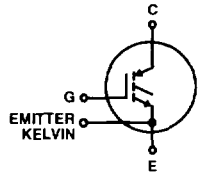
Package

JEDEC MO-093AA (5 LEAD TO-218)



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		HGTA32N60E2	UNITS
Collector-Emitter Voltage	BV_{CES}	600	V
Collector-Gate Voltage R_{GE} = 1MΩ	V_{CGR}	600	V
Collector Current Continuous at T_C = +25°C	I_{C25}	50	A
at V_{GE} = 15V at T_C = +90°C	I_{C90}	32	A
Collector Current Pulsed (Note 1)	I_{CM}	200	A
Gate-Emitter Voltage Continuous	V_{GES}	±20	V
Gate-Emitter Voltage Pulsed	V_{GEM}	±30	V
Switching Sage Operating Area T_J = +150°C	SSOA	200A at 0.8 BV_{CES}	-
Power Dissipation Total at T_C = +25°C	P_D	208	W
Power Dissipation Derating T_C > +25°C		1.67	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	°C
Maximum Lead Temperature for Soldering	T_L	260	°C
Short Circuit Withstand Time (Note 2) at V_{GE} = 15V	t_{SC}	3	µs
at V_{GE} = 10V	t_{SC}	15	µs

NOTES:

1. Repetitive Rating: Pulse width limited by maximum junctions temperature.
2. $V_{CE(PEAK)}$ = 360V, T_C = +125°C, R_{GE} = 25Ω.

HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951
4,969,027							

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

File Number **2833.3**

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Collector-Emitter Breakdown Voltage	BV_{CES}	I_C = 250μA, V_{GE} = 0V		600	-	-	V
Collector-Emitter Leakage Current	I_{CES}	V_{CE} = BV_{CES}	T_C = +25°C	-	-	250	μA
		V_{CE} = 0.8 BV_{CES}	T_C = +125°C	-	-	4.0	mA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = I_{C90}, V_{GE} = 15V	T_C = +25°C	-	2.4	2.9	V
			T_C = +125°C	-	2.4	3.0	V
Gate-Emitter Threshold Voltage	$V_{GE(TH)}$	I_C = 1.0mA, V_{CE} = V_{GE}	T_C = +25°C	3.0	4.5	6.0	V
Gate-Emitter Leakage Current	I_{GES}	V_{GE} = ±20V		-	-	±500	nA
Gate-Emitter Plateau Voltage	V_{GEP}	I_C = I_{C90}, V_{CE} = 0.5 BV_{CES}		-	6.5	-	V
On-State Gate Charge	$Q_{G(ON)}$	I_C = I_{C90}, V_{CE} = 0.5 BV_{CES}	V_{GE} = 15V	-	200	260	nC
			V_{GE} = 20V	-	265	345	nC
Current Turn-On Delay Time	$t_{D(ON)I}$	L = 500μH, I_C = I_{C90}, R_G = 25Ω, V_{GE} = 15V, T_J = +125°C, V_{CE} = 0.8 BV_{CES}		-	100	-	ns
Current Rise Time	t_{RI}			-	150	-	ns
Current Turn-Off Delay Time	$t_{D(OFF)I}$			-	630	820	ns
Current Fall Time	t_{FI}			-	620	800	ns
Turn-Off Energy (Note 1)	W_{OFF}			-	3.5	-	mJ
Thermal Resistance	$R_{\theta JC}$			-	0.5	0.6	°C/W

NOTE:

1. Turn-off Energy Loss (W_{OFF}) is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero (I_{CE} = 0A) The HGTA32N60E2 was tested per JEDEC standard No. 24-1 Method for Measurement of Power Device Turn-off Switching Loss. This test method produces the true total Turn-off Energy Loss.

Typical Performance Curves

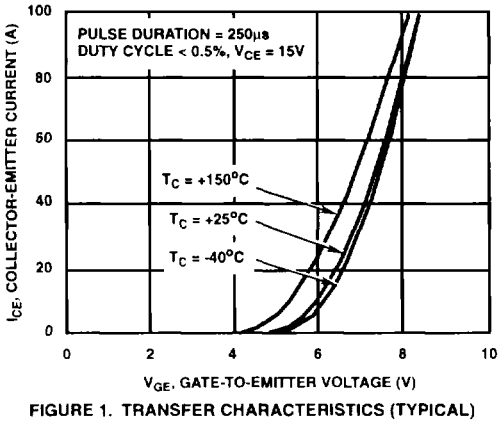


FIGURE 1. TRANSFER CHARACTERISTICS (TYPICAL)

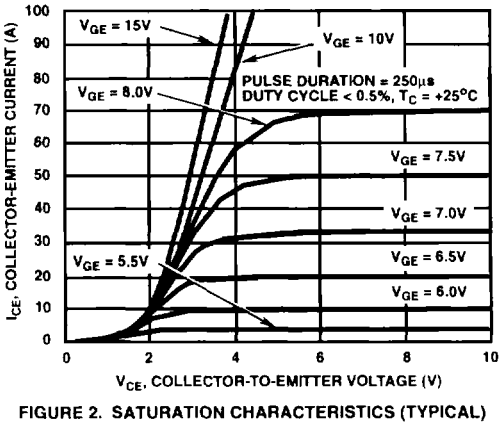


FIGURE 2. SATURATION CHARACTERISTICS (TYPICAL)

Typical Performance Curves (Continued)

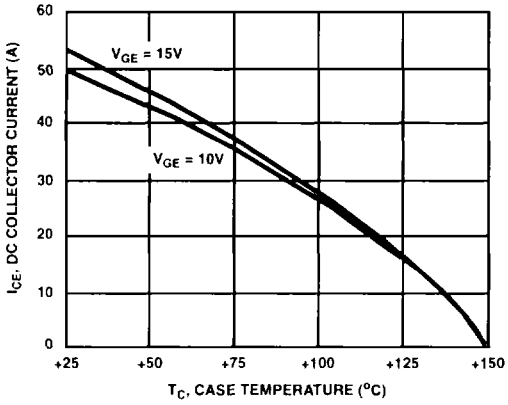


FIGURE 3. MAXIMUM DC COLLECTOR CURRENT vs CASE TEMPERATURE

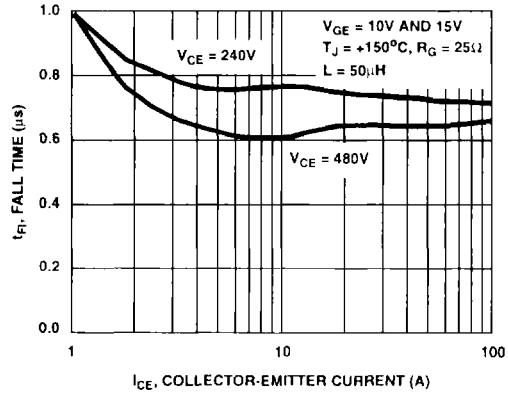


FIGURE 4. FALL TIME vs COLLECTOR-EMITTER CURRENT

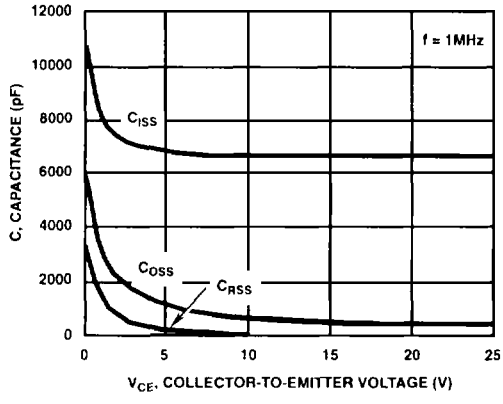


FIGURE 5. CAPACITANCE vs COLLECTOR-EMITTER VOLTAGE

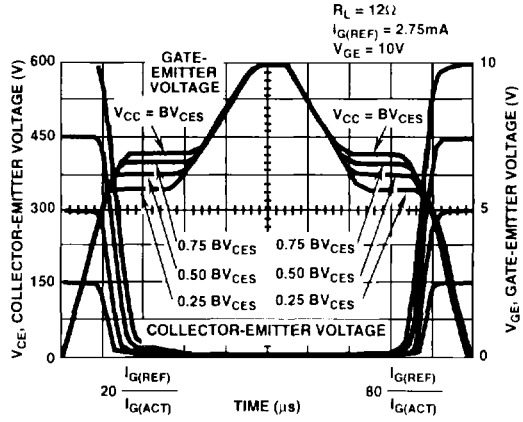


FIGURE 6. NORMALIZED SWITCHING WAVEFORMS AT CONSTANT GATE CURRENT (REFER TO APPLICATION NOTES AN7254 AND AN7260)

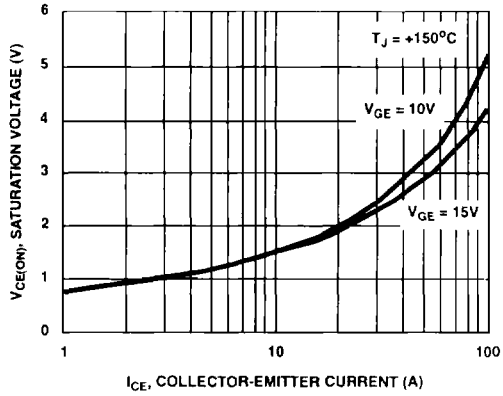


FIGURE 7. SATURATION VOLTAGE vs COLLECTOR-EMITTER CURRENT

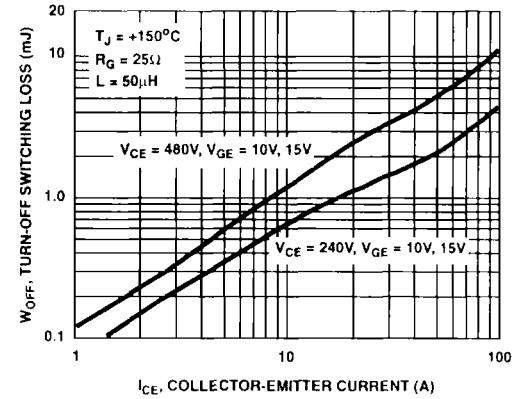


FIGURE 8. TURN-OFF SWITCHING LOSS vs COLLECTOR-EMITTER CURRENT

Typical Performance Curves (Continued)

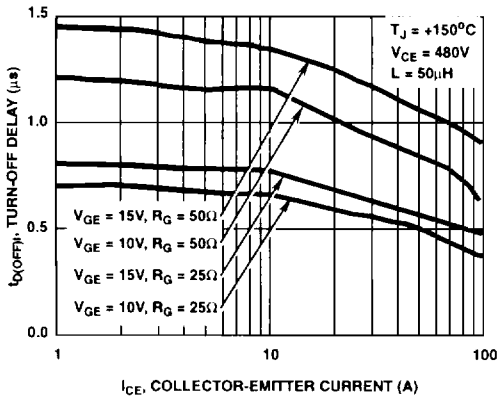
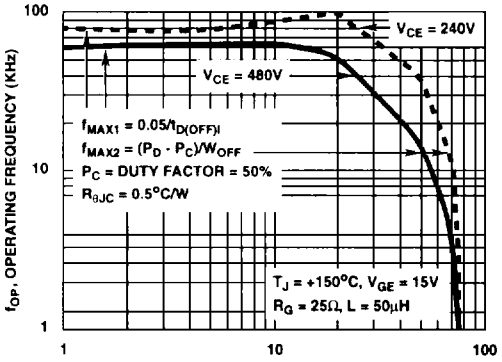


FIGURE 9. TURN-OFF DELAY vs COLLECTOR-EMITTER CURRENT



NOTE: P_D = ALLOWABLE DISSIPATION P_C = CONDUCTION DISSIPATION

FIGURE 10. OPERATING FREQUENCY vs COLLECTOR-EMITTER CURRENT AND VOLTAGE

Operating Frequency Information

Operating frequency information for a typical device (Figure 10) is presented as a guide for estimating device performance for a specific application. Other typical frequency vs collector current (I_{CE}) plots are possible using the information shown for a typical unit in Figures 7, 8 and 9. The operating frequency plot (Figure 10) of a typical device shows f_{MAX1} or f_{MAX2} whichever is smaller at each point. The information is based on measurements of a typical device and is bounded by the maximum rated junction temperature.

f_{MAX1} is defined by $f_{MAX1} = 0.05/t_{D(OFF)I}$. $t_{D(OFF)I}$ deadtime (the denominator) has been arbitrarily held to 10% of the on-state time for a 50% duty factor. Other definitions are possible. $t_{D(OFF)I}$ is defined as the time between the 90% point of the trailing edge of the input pulse and the point where the collector current falls to 90% of its maximum value. Device turn-off delay can establish an additional frequency limiting condition for an application other than T_{JMAX}. $t_{D(OFF)I}$ is important when controlling output ripple under a lightly loaded condition.

f_{MAX2} is defined by $f_{MAX2} = (P_D - P_C)/W_{OFF}$. The allowable dissipation (P_D) is defined by $P_D = (T_{JMAX} - T_C)/R_{\theta JC}$. The sum of device switching and conduction losses must not exceed P_D. A 50% duty factor was used (Figure 10) so that the conduction losses (P_C) can be approximated by $P_C = (V_{CE} \times I_{CE})/2$. W_{OFF} is defined as the sum of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero (I_{CE} - 0A).

The switching power loss (Figure 10) is defined as $f_{MAX1} \times W_{OFF}$. Turn on switching losses are not included because they can be greatly influenced by external circuit conditions and components.