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FAIRCHILD SEMICONDUCTOR®

December 2009

µSerDes™ FIN210AC

10-Bit Serializer / Deserializer Supporting Cameras and Small Displays up to 48MHz

Features

Data & Control Bits	10-bit
Frequency	48MHz
Capability	Camera or LCD
Interface	Microcontroller, RGB, YUV
µController Usage	m68 & i86
Selectable Edge Rates	Yes
Standby Current	<10µA
Core Voltage ($V_{DDA/S}$)	2.8 to 3.6V
I/O Voltage (V_{DDP})	1.65 to 3.6V
ESD (I/O to GND)	15kV
Package	32-Terminal MLP 42-Ball USS-BGA
Ordering Information	FIN210ACMLX FIN210ACGFX

Description

The FIN210AC µSerDes™ is a low-power serializer / deserializer optimized for use in cell phone displays and camera paths. The device reduces a 10-bit data path to four wires. For camera applications, an additional master clock can be passed in the opposite direction of data flow. The device utilizes Fairchild's proprietary ultra-low power, low-EMI technology.

Applications

- Slider, Folder, & Clamshell Mobile Handsets
- Printers
- Security Cameras

Related Resources

- For samples and questions, please contact: Interface@fairchildsemi.com.

Typical Application

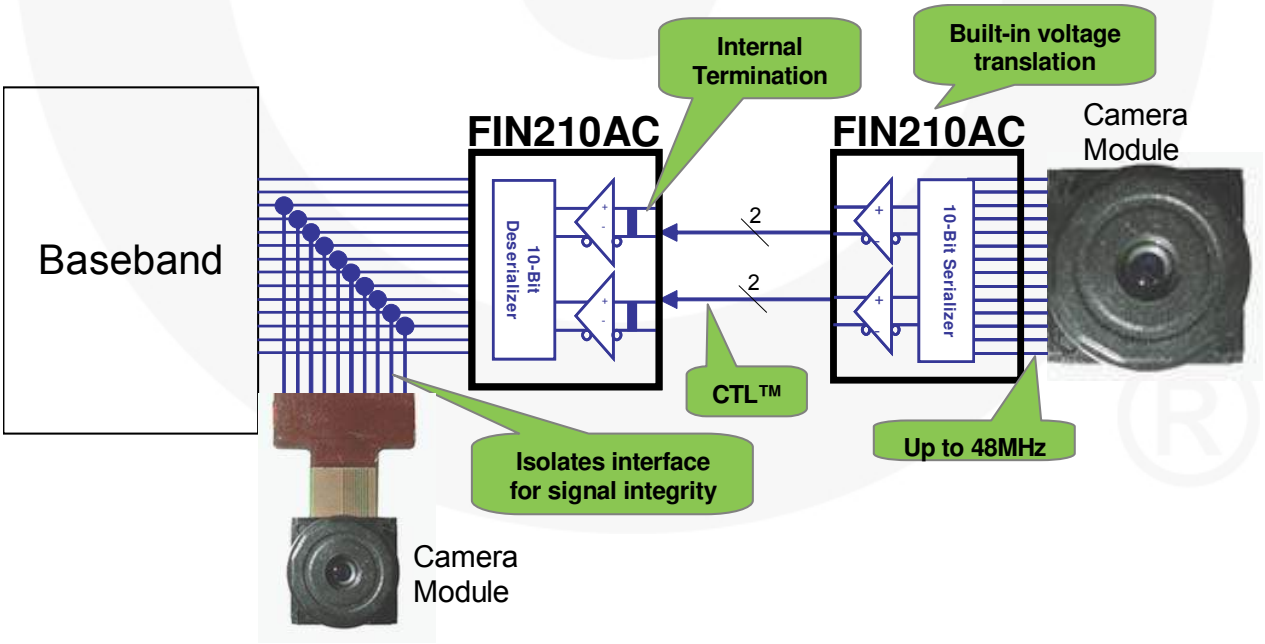


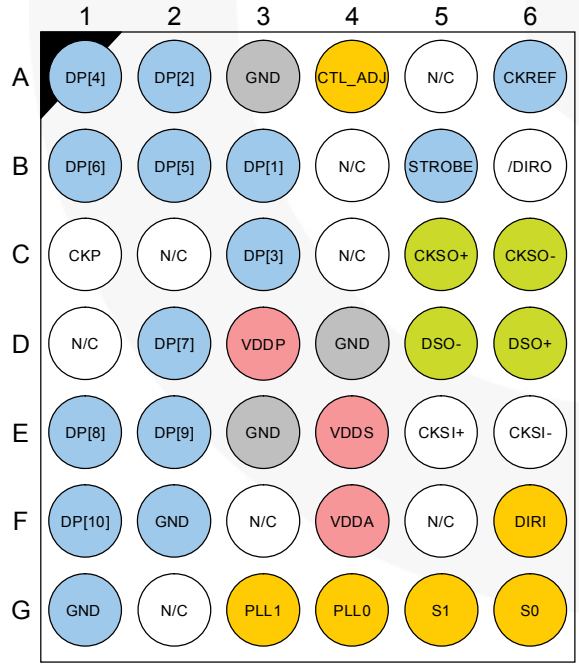
Figure 1. Mobile Phone Example

FIN210AC (Serializer DIRI=1) Pin Descriptions

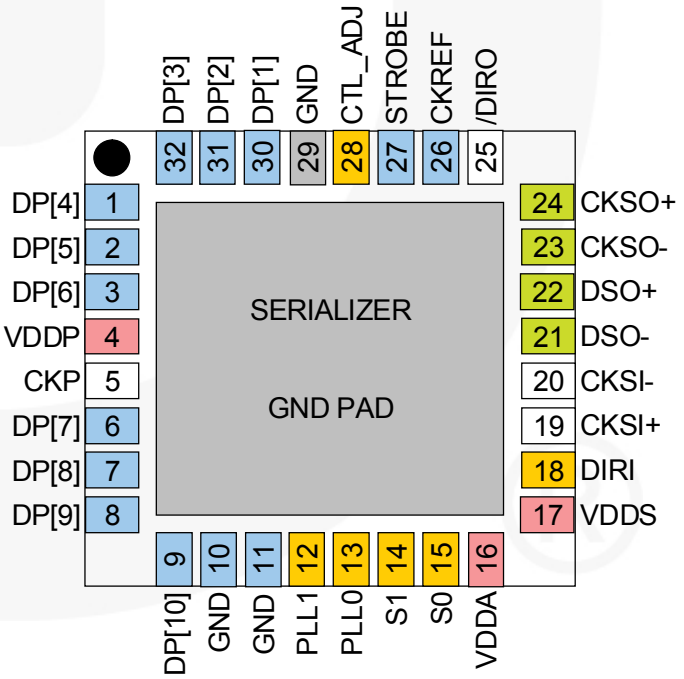
Pin Name	Description		
DIRI	Control to determine serializer or deserializer configuration.	0	Deserializer
		1	Serializer
CTL_ADJ	Adjusts CTL drive to compensate for environmental conditions and length.	0	Low drive (low power)
		1	High drive (high power)
S0	Configure frequency range for the PLL.	See Table 1 Serializer (DIRI=1) Control Pin.	
S1	Configure frequency range for the PLL.	See Table 1 Serializer (DIRI=1) Control Pin.	
PLL0	Divide or adjust the serial frequency.	See Table 1 Serializer (DIRI=1) Control Pin.	
PLL1	Divide or adjust the serial frequency.	See Table 1 Serializer (DIRI=1) Control Pin.	
CKREF	LV-CMOS clock input and PLL reference.		
STROBE	LV-CMOS strobe input for latching data (DP [1:12]) into the serializer on the rising edge.		
DP[1:10]	LV-CMOS parallel data input. (GND input if not used)		
CKSO+ / CKSO-	CTL Differential serializer output bit clock. CKSO+: Positive signal; CKSO-: Negative signal.		
DSO+ / DSO-	CTL Differential serial output data signals. DSO+: Positive signal; DSO-: Negative signal.		
CKSI+ / CKSI-	CTL Differential deserializer input bit clock. CKSI+: Positive signal; CKSI-: Negative signal.	No connect unless in “clock pass-through” mode.	
CKP	LV-CMOS word clock output or Pixel clock output.	No connect unless in “clock pass-through” mode.	
/DIRO	LV-CMOS output, Inversion of DIRI in normal operation. Can be used to drive the DIRI signal of the deserializer where the interface needs to be turned around.	No connect if not used.	
VDDP	Power supply for parallel I/O. (All VDDP pins must be connected to VDDP)		
VDDS	Power supply for serial I/O.		
VDDA	Power supply for core.		
GND	All GND pins must be connected to ground. BGA: all GND pads. MLP: Pins 10, 11, 29, and GND PAD must be grounded.		
N/C	No connect. (Do not connect to GND or VDD)		

Note:
1. 0=GND; 1=VDDP

FIN210AC (Serializer DIRI=1) Pin Configurations



42-Ball BGA, 3.5 x 4.5mm, .5mm pitch (Top View)



32-pin MLP, 5 x 5mm, .5mm pitch (Top View)
(Center pad must be grounded)

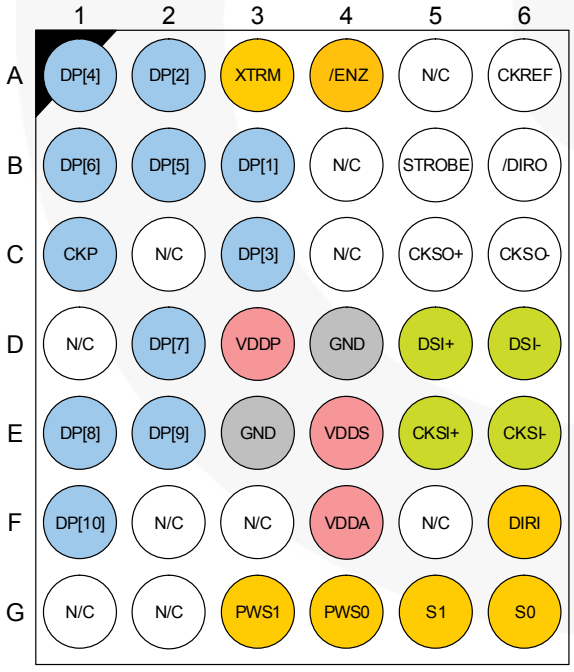
Figure 2. FIN210AC (Serializer DIRI=1) Pin Assignments (Top View)

FIN210AC (Deserializer DIRI=0) Pin Descriptions

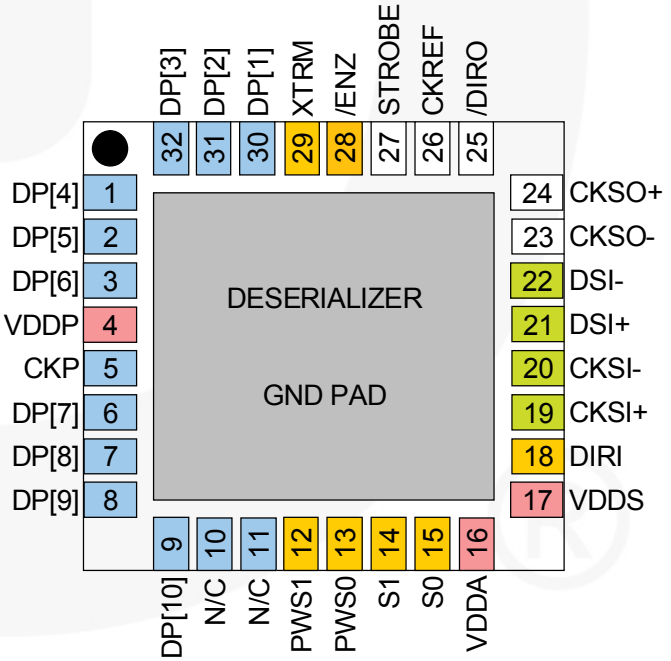
Pin Name	Description		
DIRI	Control to determine serializer or deserializer configuration.	0	Deserializer
		1	Serializer
XTERM	Control to determine if using internal or external termination	0	Internal termination used
		1	External termination required on CKSI & DSI
S0	Signals used to define the edge rate of parallel I/O.	See Table 2 Deserializer (DIRI=0) Control Pin.	
S1	Signals used to define the edge rate of parallel I/O.	See Table 2 Deserializer (DIRI=0) Control Pin.	
PWS0	Configure CKP pulse width.	See Table 2 Deserializer (DIRI=0) Control Pin.	
PWS1	Configure CKP pulse width.	See Table 2 Deserializer (DIRI=0) Control Pin.	
/ENZ	High-Z or known state outputs during power down	See Table 5 Deserializer (DIRI=0) Control Pin.	
DP[1:10]	LV-CMOS parallel data output. (N/C if not used)		
CKP	LV-CMOS word clock output or Pixel clock output.		
DSI+ / DSI-	CTL Differential serial input data signals. DSI+: Positive signal; DSI-: Negative signal.		
CKSI+ / CKSI-	CTL Differential deserializer input bit clock. CKSI+: Positive signal; CKSI-: Negative signal.		
CKSO+ / CKSO-	CTL Differential serializer output bit clock. CKSO+: Positive signal; CKSO-: Negative signal.	No connect unless in “clock pass-through” mode.	
CKREF	LV-CMOS clock input and PLL reference.	No connect unless in “clock pass-through” mode.	
STROBE	LV-CMOS strobe input for latching data into the serializer.	No connect unless in “clock pass-through” mode.	
/DIRO	LV-CMOS Output. Inversion of DIRI in normal operation.	No connect if not used.	
VDDP	Power supply for parallel I/O. (All VDDP pins must be connected to VDDP)		
VDDS	Power supply for serial I/O.		
VDDA	Power supply for core.		
GND	All GND pins must be connected to ground. BGA: all GND pads. MLP: GND PAD must be grounded.		
N/C	No connect. BGA: G1, F2; MLP: 10, 11; (Do not connect to GND or VDD)		

Note:
2. 0=GND; 1=VDDP

FIN210AC (Deserializer DIRI=0) Pin Configurations



42-Ball BGA, 3.5 x 4.5mm, .5mm pitch (Top View)



32-pin MLP, 5mm x 5mm, .5mm pitch (Top View)
(Center pad must be grounded)

Figure 3. FIN210AC (Deserializer DIRI=0) Pin Assignments (Top View)

System Control Pin

Table 1. Serializer (DIRI=1) Control Pin

Conditions	Function			Control Pin			
	CKREF	STROBE	PLL Multiplier	PLL0	PLL1	S0	S1
Slow Frequencies							
Normal operation	5MHz to 15MHz	≤ CKREF (Up to 15MHz)	1	1	0	0	1
Supports spread spectrum on CKREF	5MHz to 14.2MHz	≤ CKREF (Up to 14.2MHz)	0.947	0	0	0	1
With a fixed CKREF input; STROBE can be 1/2 the speed	5MHz to 15MHz	≤ CKREF / 2 (Up to 7.5MHz)	2	0	1	0	1
With a fixed CKREF input; STROBE can be 1/3 the speed	5MHz to 15MHz	≤ CKREF / 3 (Up to 5MHz)	3	1	1	0	1
Medium Frequencies							
Normal operation	10MHz to 30MHz	≤ CKREF (Up to 30MHz)	1	1	0	1	1
Supports spread spectrum on CKREF	10MHz to 28.4MHz	≤ CKREF (Up to 28.4MHz)	0.947	0	0	1	1
With a fixed CKREF input; STROBE can be 1/2 the speed	10MHz to 30MHz	≤ CKREF / 2 (Up to 15MHz)	2	0	1	1	1
With a fixed CKREF input; STROBE can be 1/3 the speed	10MHz to 30MHz	≤ CKREF / 3 (Up to 10MHz)	3	1	1	1	1
Fast Frequencies							
Normal operation	18MHz to 48MHz	≤ CKREF (Up to 48MHz)	1	1	0	1	0
Supports spread spectrum on CKREF	18MHz to 45.4MHz	≤ CKREF (Up to 45.4MHz)	0.947	0	0	1	0
With a fixed CKREF input; STROBE can be 1/2 the speed	18MHz to 48MHz	≤ CKREF / 2 (Up to 24MHz)	2	0	1	1	0
With a fixed CKREF input; STROBE can be 1/3 the speed	18MHz to 48MHz	≤ CKREF / 3 (Up to 16MHz)	3	1	1	1	0
Power-Down				X	X	0	0

Table 2. Deserializer (DIRI=0) PWS Control Pins (Pulse Width Examples)

CKP to STROBE	CKP Pulse Width Low Time			Reference		Control Pin	
	CKREF=19.2 MHz	CKREF=26 MHz	CKREF=48 MHz	PLL Multiplier (Serializer)	Pwidth Multiplier	PWS0	PWS1
Serializer PLL Multiplier = 3							
Non-Inverted	78.1ns	57.7ns	31.2ns	3	6	0	0
Inverted	78.1ns	57.7ns	31.2ns	3	6	1	0
Non-Inverted	156.3ns	115.4ns	62.5ns	3	12	0	1
Non-Inverted	208.3ns	153.8ns	83.3ns	3	16	1	1
Serializer PLL Multiplier = 2							
Non-Inverted	52.1ns	38.5ns	20.8ns	2	6	0	0
Inverted	52.1ns	38.5ns	20.8ns	2	6	1	0
Non-Inverted	104.2ns	76.9ns	41.7ns	2	12	0	1
Non-Inverted	138.9ns	102.6ns	55.6ns	2	16	1	1
Serializer PLL Multiplier = 1							
Non-Inverted	26ns	19.2ns	10.4ns	1	6	0	0
Inverted	26ns	19.2ns	10.4ns	1	6	1	0
Non-Inverted	52.1ns	38.5ns	20.8ns	1	12	0	1
Non-Inverted	69.4ns	51.3ns	27.8ns	1	16	1	1
Power-Down				X	X	0	0

Table 3. Deserializer S0 & S1 Control Pins (Note: All edge rates are typical values.)

LVCMOS Output Edge Rates		S0	S1
Slow Edge Rates	~7 - 8ns (C_L = 8pF)	0	1
Medium Edge Rates	~4 - 5ns (C_L = 8pF)	1	1
Fast Edge Rates	~2 - 3ns (C_L = 8pF)	1	0
Power Down		0	0

Pulse Width Calculations

CKP Pulse Width Low Time=(PLL Multiplier • Pwidth Multiplier) / (CKREF•12) (1)

Example: CKREF=26MHz; PLL Multiplier=1; Pwidth Multiplier=6

CKP Pulse width=(1 • 6) / (26MHz • 12)=19.2ns (2)

CKREF = Strobe 50% Duty Cycle

If CKREF = Strobe the below control states will provide a ~ 50% duty cycle pulse width output on CKP

Table 4. CKREF = Strobe 50% Duty Cycle

Serializer		Deserializer	
PLL0	PLL1	PWS0	PWS1
1	0	0	0

Power-Down States

When both S1 and S0 signals are 0, regardless of the state of the DIRI signal, the FIN210AC resets and powers down. The power-down mode shuts down all internal analog circuitry, disables the serial input and output of the device, and resets all internal digital logic. Table 5 indicates the state of the input states and output buffers in Power-Down mode.

Table 5. Power-Down

Signal Pins	DIRI=1 (Serializer)	DIRI=0 (Deserializer) /ENZ = 0	DIRI=0 (Deserializer) /ENZ = 1
DP[1:10]	Inputs Disabled	Outputs High-Z	Outputs Low
CKP	HIGH	High-Z	High
STROBE	Input Disabled	Input Disabled	Input Disabled
CKREF	Input Disabled	Input Disabled	Input Disabled
/DIRO	0	1	1

Clock Pass-Through Mode

Clock pass-through mode allows a harmonic rich clock source to be sent to the serializer in a CTL format to reduce the overall harmonic content of the phone, and can reduce the need for EMI filters. The Master Clock Pass through mode performs a translation to the clock in the CTL link, and does not serialize this signal. The following describes how to enable this functionality for an image sensor *(See Figure 6)*.

Deserializer Configuration (DIRI=0)

1. Connect CKREF(BGA pin A6) to GROUND
2. Connect master clock to STROBE (BGA pin B5)

Serializer Configuration (DIRI=1)

1. CKSI passes master clock to CKP output (BGA pin C1)

CKREF and STROBE Signals

Please note that there is a setup and hold time between STROBE and data that must be met as seen on the electrical characteristics section. The relationship between CKREF and STROBE can be synchronous or asynchronous depending on what is available in the system. It is suggested that if the signals are synchronous and in normal operation that CKREF is tied to STROBE as close to the chip as possible. If you are running an asynchronous or spread spectrum setup, please be aware this may result on cycle jitter on the CKP signal. They cycle jitter does not effect the output data and clock relationship, the display or end application should continue to work as normal.

PLL Note

Please note that the PLL ranges can overlap, power consumption can be reduced by selecting the operation in the lower end of the higher speed PLL range.

Application Diagrams

The following application diagrams illustrate the most typical applications for the FIN210 device. Specific configurations of the control pins may vary based on the needs of a given system. The following recommendations are valid for all of the applications shown.

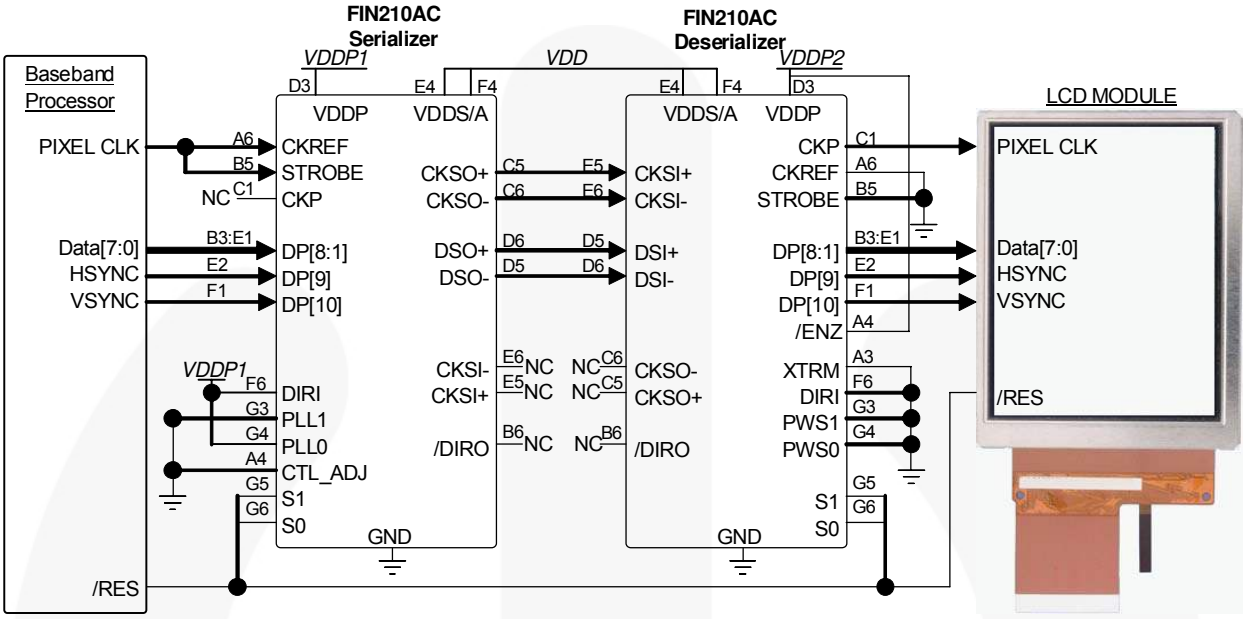


Figure 4. 8-Bit RGB Application (Example Shows BGA 42-Pin Package)

Serializer Configuration:

10MHz to 30MHz Frequency Range (S1=S0=1)

Normal Mode (PLL1=0; PLL0=1)

Deserializer Configuration:

~4 – 5ns output edge rates (S1=S0=1)

~50% CKP PW,(PWS1=PWS0=0)

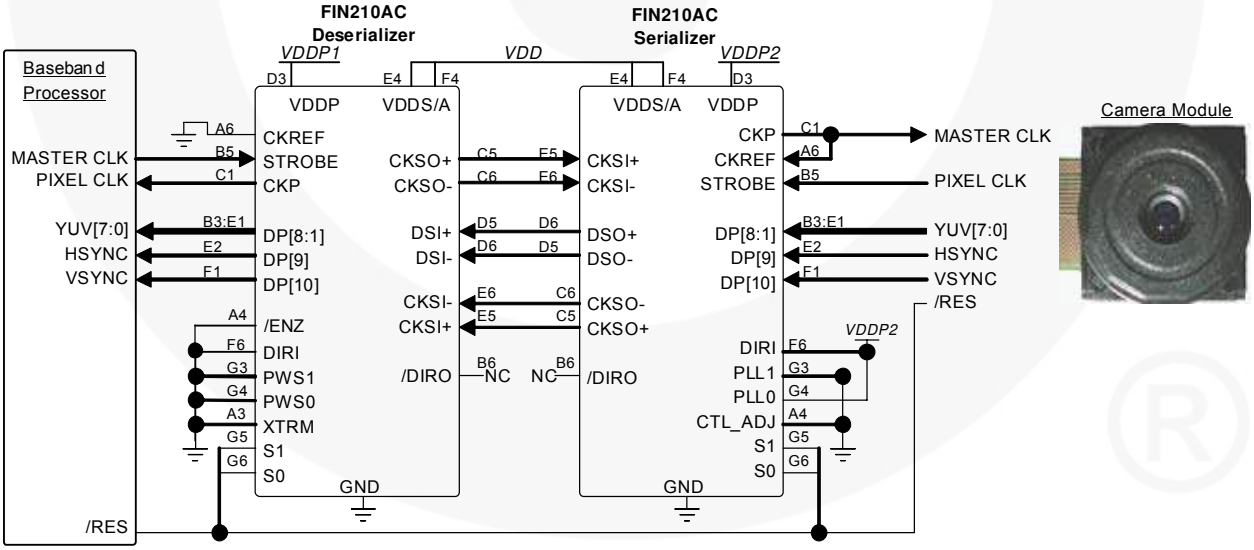


Figure 5. 8-Bit YUV 1.3MPixel CMOS Imager (Example Shows BGA 42-Pin Package)

Deserializer Configuration:

~2 – 3ns output edge rates (S1=0, S0=1)

~50% CKP PW,(PWS1=PWS0=0)

Serializer Configuration:

18MHz to 48MHz Frequency Range (S1=0, S0=1)

Normal Mode (PLL1=0, PLL0=1)

Application Diagrams (Continued)

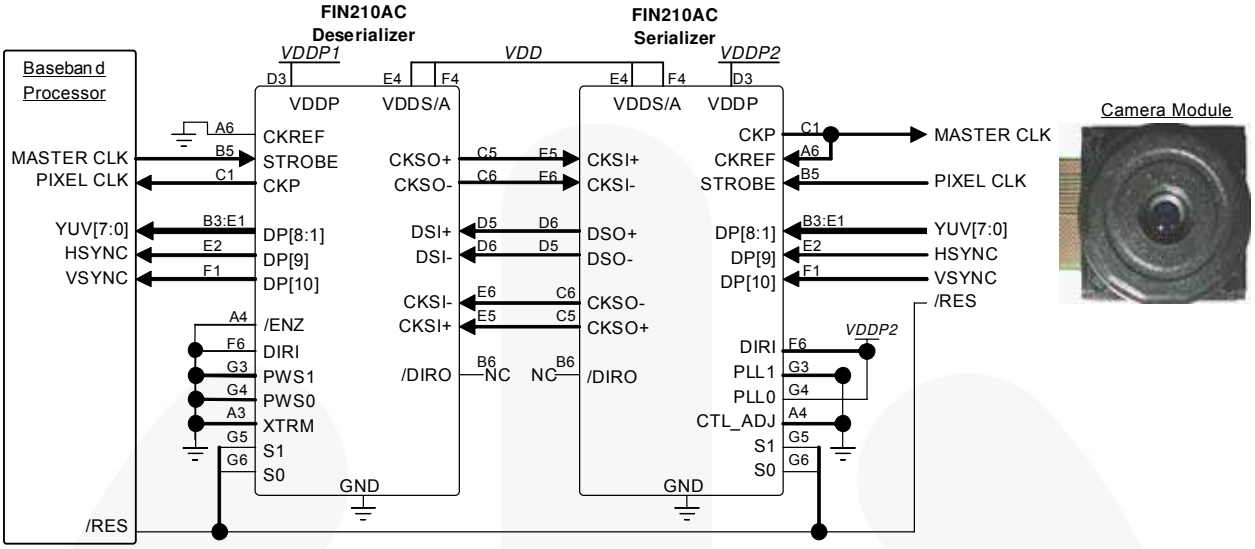


Figure 6. 8-Bit YUV 1.3MPixel CMOS Imager In Clock Pass-Through Mode

Serializer Configuration:

18MHz to 48MHz Frequency Range (S1=0, S0=1)

Normal Mode (PLL1=0; PLL0=1)

Master clock bypass mode.

Deserializer Configuration:

~2 – 3ns output edge rates (S1=0, S0=1)

~50% CKP PW,(PWS1=PWS0=0)

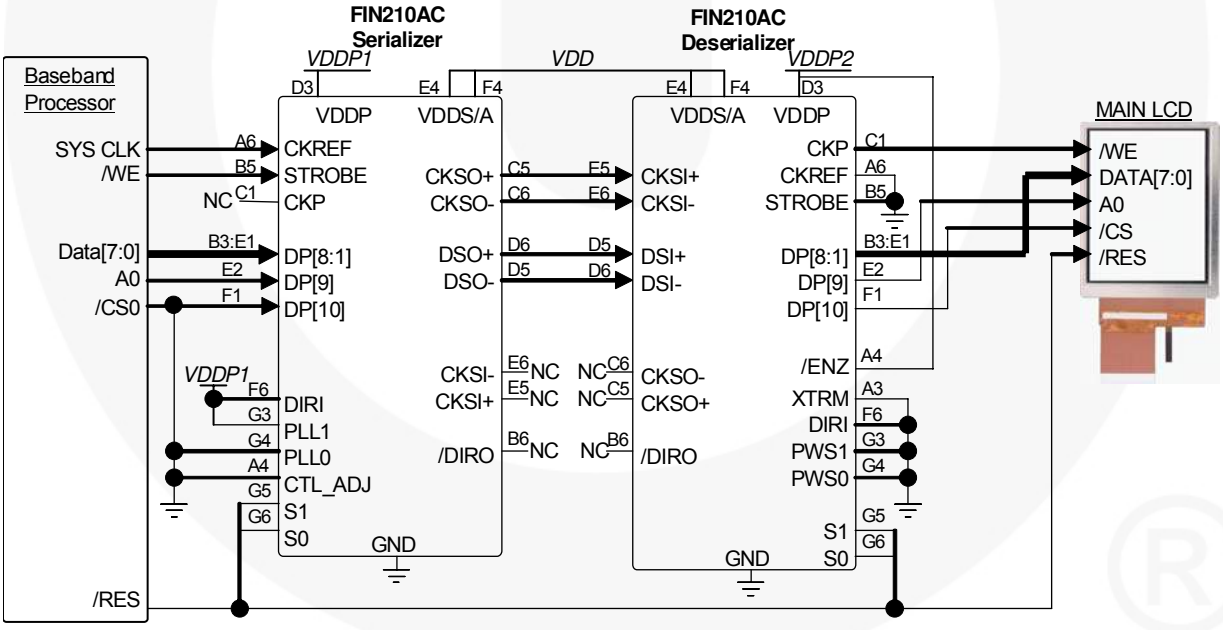


Figure 7. 8-Bit WRITE-Only Microcontroller Interface (Example Shows BGA 42-Pin Package)

Serializer Configuration:

18MHz to 48MHz Frequency Range (S1=0, S0=1)

CKREF is twice as fast STROBE (PLL1=1; PLL0=0)

CKREF=26MHz & STROBE Frequency=10 MHz

Deserializer Configuration:

~7 – 8ns output edge rates (S1=1, S0=0)

~50% CKP PW,(PWS1=PWS0=0)

Additional Application Information

Flex Cabling: The serial I/O information is transmitted at a high serial rate. Care must be taken implementing this serial I/O flex cable. The following best practices should be used when developing the flex cabling or Flex PCB.

- Keep all four differential Serial Wires the same length.
- Do not allow noisy signals over or near differential serial wires.
  Example: No LVCMOS traces over differential serial wires.
- Use only one ground plane or wire over the differential serial wires. Do not run ground over top and bottom.
- Design goal of 100Ω differential characteristic impedance.
- Do not place test points on differential serial wires.
- Use differential serial wires a minimum of 2cm away from the antenna.
- For additional applications notes or flex guidelines see your sales representative or contact Fairchild directly.
- For samples and questions, please contact: Interface@fairchildsemi.com.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{DD}	Supply Voltage		-0.5V	+4.6	V
	All Input/Output Voltage		-0.5	V_{DD}+0.5	V
	CTL Output Short-Circuit Duration		Continuous		
T_{STG}	Storage Temperature Range		-65	+150	°C
T_J	Maximum Junction Temperature		+150		°C
T_L	Lead Temperature (Soldering, four seconds)		+260		°C
ESD	Human Body Model JESD22-A114	Serial I/O Pins to GND		12	kV
		All Pins		8	
	Charged Device Model, JESD22-C101			2	
	IEC61000-4-2			15	

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
V_{DDA}, V_{DDS}	Supply Voltage	2.8	3.6	V
V_{DDP}	Supply Voltage	1.65	3.60	V
T_A	Operating Temperature	-30	+70	ºC
V_{DDA-PP}	Supply Noise Voltage	100		mV_{PP}

DC Electrical Characteristics

Values are provided for over-supply voltage and operating temperature ranges, unless otherwise specified.

Symbol	Parameter		Test Conditions	Min.	Typ.[3]	Max.	Unit
LVCMOS I/O							
V_{IH}	Input High Voltage			0.65xV_{DDP}		V_{DDP}	
V_{IL}	Input Low Voltage			GND		0.35xV_{DDP}	V
V_{OH}	Output High Voltage		I_{OH}=-2.0mA, S1=0,S0=1	0.75xV_{DDP}		V_{DDP}	V
			I_{OH}=-0.4mA, S1=1,S0=0				
			I_{OH}=-1.0mA, S1=1,S0=1				
V_{OL}	Output Low Voltage		I_{OL}=2.0mA, S1=0,S0=1	0		0.25xV_{DDP}	V
			I_{OL}=0.4mA, S1=1,S0=0				
			I_{OL}=1.0mA, S1=1,S0=1				
I_{IN}	Input Current		V_{IN}= 0V to 3.6V	-5.0		5.0	µA
DIFFERENTIAL I/O							
I_{ODH}	Output HIGH Source Current	V_{OS}=1.0V	CTL_ADJ=0		-4.1		mA
			CTL_ADJ=1		-5.3		
I_{ODL}	Output LOW Sink Current	V_{OS}=1.0V	CTL_ADJ=0		2.1		mA
			CTL_ADJ=1		3.1		
V_{GO}	Input Voltage Ground Offset[4]				0		V
R_{TRM}	CKS Internal Receiver Termination Resistor		V_{ID}=50mV, V_{IC}=925mV	80	100	120	Ω
			DIRI=0				
	DS Internal Receiver Termination Resistor		V_{ID}=50mV, V_{IC}=925mV	80	100	120	Ω
			DIRI=0				

Notes:

3. Typical values are given for V_{DD}=2.775V and T_A=25°C. Positive current values refer to the current flowing into the device and negative values refer to the current flowing out of pins. Voltages are referenced to GROUND unless otherwise specified (except ΔV_{OD} and V_{OD}).
4. V_{GO} is the difference in device ground levels between the CTL driver and the CTL receiver.

Power Supply Currents

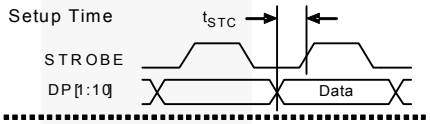
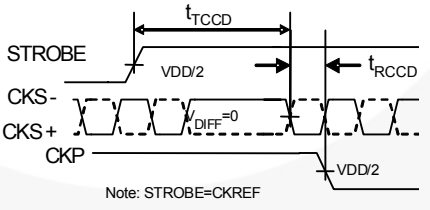
Symbol	Parameter	Test Conditions			Min.	Typ.	Max.	Unit
I_{DD_PD}	V_{DD} Power-Down Supply Current	S1=S0=0, All Inputs at GND or VDD				0.1		µA
I_{DD_SER1}	Dynamic Serializer Power Supply Current	f_{CKREF}=f_{STRB}, PLL1=0,PLL0=1; CTL_ADJ=0; C_L=0pF; CKSI+/CKSI- Not Connected	S1=L S0=H	20MHz		9.5		mA
				48MHz		15.5		mA
			S1=H S0=L	5MHz		7.5		mA
				14MHz		12.5		mA
			S1=H S0=H	8MHz		7.5		mA
				28MHz		14.0		mA
I_{DD_DES1}	Dynamic Deserializer Power Supply Current	f_{CKREF}=f_{STRB}, PWS1=0, PWS0=1; CTL_ADJ=0; C_L=0pF; CKSI+/CKSI- Not Connected	S1=L S0=H	20MHz		7.5		mA
				48MHz		10.0		mA
			S1=H S0=L	5MHz		6.0		mA
				14MHz		7.0		mA
			S1=H S0=H	8MHz		6.5		mA
				28MHz		8.0		mA

Pin Capacitance Tables

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
C_{IN}, C_{IO}, $C_{IO-DIFF}$	Capacitance of Input Only Signals; Parallel Port Pins DP[1:10]; Differential I/O	DIRI=1, S1=0, S0=0, V_{DD}=2.5V		2		pF

AC Electrical Characteristics

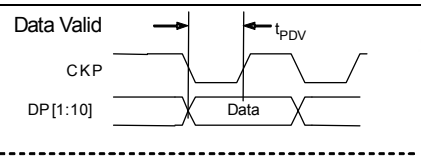
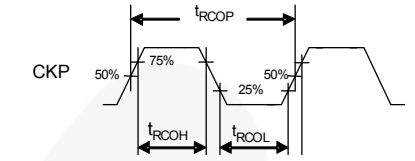
Values are provided for over-supply voltage and operating temperature ranges, unless otherwise specified.

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
Serializer Input Operating Conditions							
f_{CKREF}	CKREF Clock Frequency (5MHz - ≤ 48MHz);	$f_{CKREF}=f_{STRB}$	S1=0, S0=1	18		48	MHz
			S1=1, S0=0	5		15	
			S1=1, S0=1	10		30	
f_{STRB}	Strobe Frequency Relative to CKREF Frequency	$f_{CKREF} \neq f_{STRB}$	PLL1=0, PLL0=0			94.7	% of f_{CKREF}
			PLL1=0, PLL0=1			100	
			PLL1=1, PLL0=0			50	
			PLL1=1, PLL0=1			$33^1/_3$	
t_{CPWH}	CKREF DC	$T=1/f_{CKREF}$		0.2	0.5	0.8	T
t_{CPWL}	CKREF DC	$T=1/f_{CKREF}$		0.2	0.5	0.8	T
t_{CLKT}	LVCMOS Input Transition Time(5)	10-90%				20	ns
$t_{SPWH/L}$	STROBE Pulse Width HIGH/LOW	$T=1/f_{CKREF}$		$T \times {}^4/_{12}$		$T \times {}^8/_{12}$	ns
t_{STC}	$DP_{(n)}$ Setup to STROBE (DIRI=1, f=5MHz)			2.5			ns
t_{HTC}	$DP_{(n)}$ Hold to STROBE (DIRI=1, f=5MHz)			2.0			ns
Serializer AC Electrical Characteristics							
t_{TCCD}	Transmitter Clock Input to Clock Output Delay(6)	 DIRI=1, $f_{CKREF}=f_{STRB}$		19a+1.5		21a+6.5	ns
Phase Lock Loop (PLL) AC Electrical Characteristics							
t_{TPLLS0}	Serializer PLL Stabilization Time	CKREF Toggling and Stable		200		600	µs
t_{TPLLD0}	PLL Disable Time Loss of Clock					30.0	µs
t_{TPLLD1}	PLL Power-Down Time					20.0	ns

Continued on the following page…

AC Electrical Characteristics (Continued)

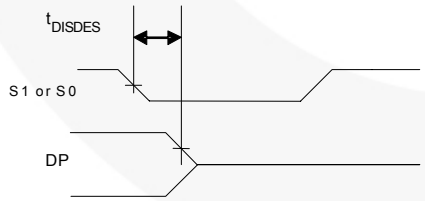
Values are provided for over-supply voltage and operating temperature ranges, unless otherwise specified.

Symbol	Parameter	Test Conditions			Min.	Typ.	Max.	Unit
Deserializer AC Electrical Characteristics								
t_{RCOL}			PWS1	PWS0				ns
		$f_{STRB}=f_{CKREF}$	0	0	6a-3		6a+3	
		$f_{STRB}=f_{CKREF}$	0	1	6a-3		6a+3	
		$f_{STRB}=.5x\ f_{CKREF}$	1	0	12a-3		12a+3	
		$f_{STRB}=.5x\ f_{CKREF}$	1	1	16a-3		16a+3	
t_{PDV}	 Setup: DIRI= 0, CKSI and DS are valid signals.	Data Valid to CKP HIGH (Rising Edge STROBE), C_L=5pF			8a-3		8a+3	ns
t_{RFD}	Output Rise/Fall Time Data (20% to 80%)	C_L=8pF	S1=0,S0=1			3		ns
			S1=1,S0=0			8		
			S1=1,S0=1			5		
t_{RFC}	Output Rise/Fall Time CKP (20% to 80%)	C_L=8pF	S1=0,S0=1			2		ns
			S1=1,S0=0			7		
			S1=1,S0=1			4		

Notes:

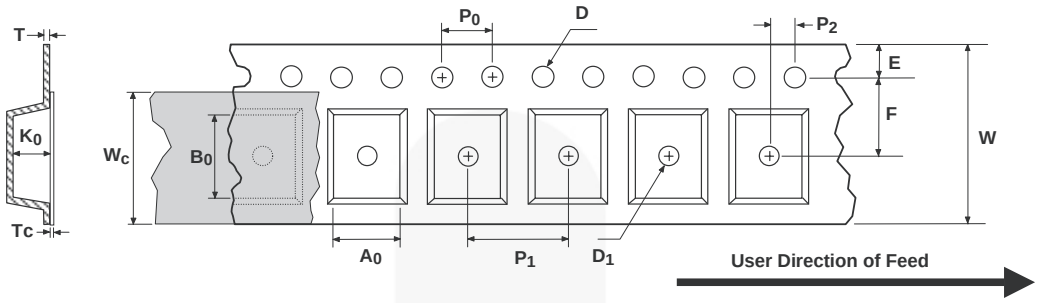
5. Parameter is characterized, but not production tested.
6. The average bit time “a” is a function of the serializer CKREF frequency; a=(1/f)/12.

Logic Timing Controls

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{PHL_DIR}, t_{PLH_DIR}	Propagation Delay DIRI to /DIRO	DIRI L->H or H->L			17	ns
t_{PLZ}, t_{PHZ}	Propagation Delay DIRI to DP	DIRI L->H or H->L			25	ns
t_{DISDES}	Deserializer Disable Time: S0 or S1 LOW to DPTri-State; DIRI=0,  Note: If S0(2) is transitioning, S1(1) must =0 for test to be valid.				25	ns
t_{DISSER}	Serializer Disable Time: S0 or S1 LOW to CKP HIGH	DIRI=1; S1(0) and S0(1)=H->L			25	ns

Tape and Reel Specifications

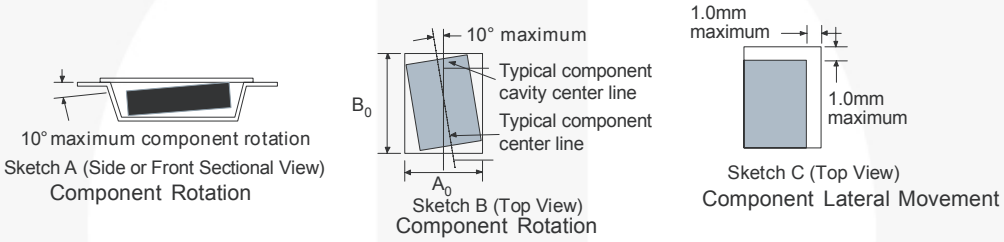
MLP Embossed Tape Dimensions

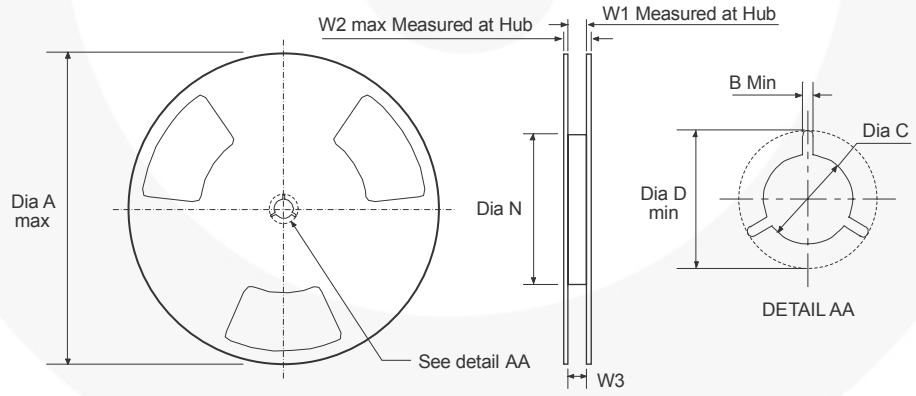


Package	A_0 ±0.1	B_0 ±0.1	D ±0.5	D_1 Min.	E ±0.1	F ±0.1	K_0 ±0.1	P_1 Typ.	P_0 Typ.	P_2 ±0.5	T Typ.	T_C ±0/05	W ±0.3	W_C Typ.
5 x 5	5.35	5.35	1.55	1.50	1.75	5.50	1.40	8.00	4.00	2.00	0.30	0.07	12.00	9.30
6 x 6	5.35	5.35	1.55	1.50	1.75	5.50	1.40	8.00	4.00	2.00	0.30	0.07	12.00	9.30

Notes:
A_0, B_0, and K_0 dimensions are determined with respect to the EIA/JEDEC RS-481 rotational and lateral movement requirements (see sketches A, B, and C).

MLP Shipping Reel Dimensions

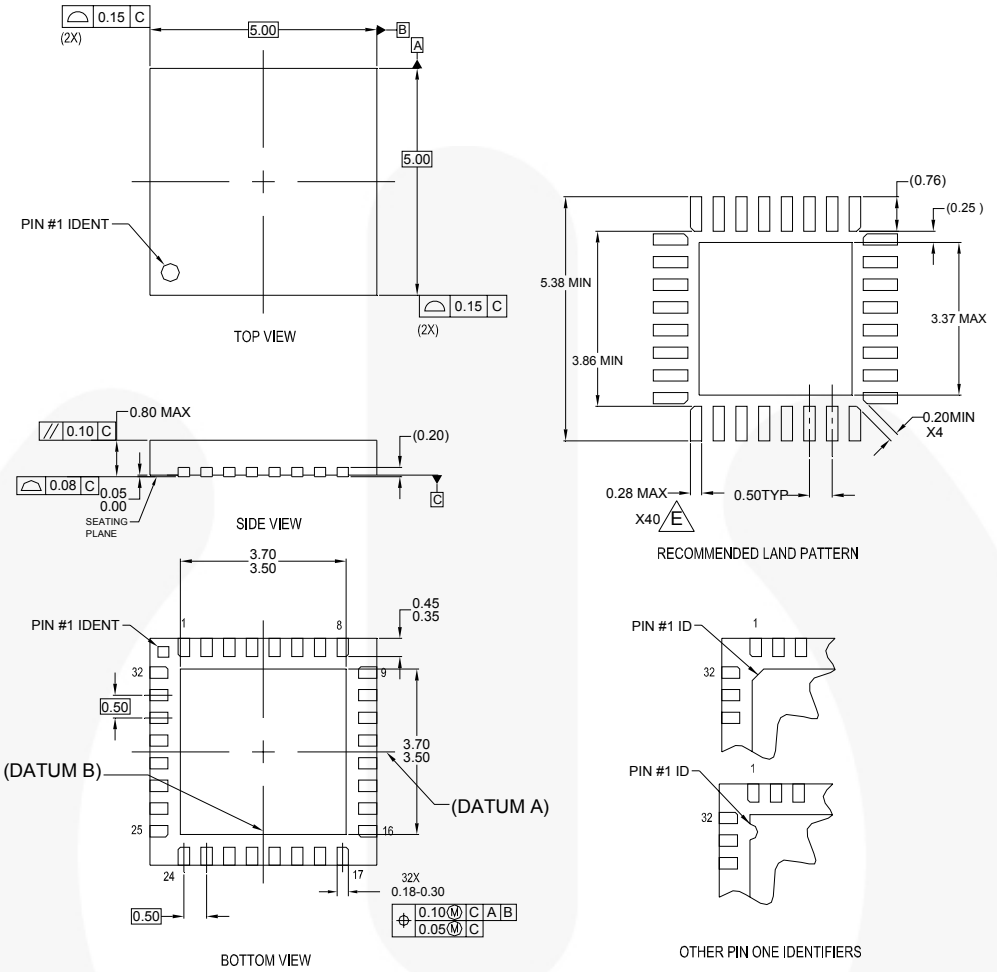




Tape Width	Dia A Max.	Dim B Min.	Dia C +0.5/-0.2	Dia D Min.	Dim N Min.	Dim W1 +2.0/-0	Dim W2	Dim W3 (LSL-USL)
8	330.0	1.5	13.0	20.2	178.0.	8.4	14.4	7.9 ~ 10.4
12	330.0	1.5	13.0	20.2	178.0.	12.4	18.4	11.9 ~ 15.4
16	330.0	1.5	13.0	20.2	178.0.	16.4	22.4	15.9 ~ 19.4

Figure 8. MLP Tape and Reel

Physical Dimensions



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-220, VARIATION WHHD-4. THIS PACKAGE IS ALSO FOOTPRINT COMPATIBLE WITH WHHD-5.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.

D. LAND PATTERN PER IPC SM-782.

E. WIDTH REDUCED TO AVOID SOLDER BRIDGING.

F. DIMENSIONS ARE NOT INCLUSIVE OF BURRS, MOLD FLASH, OR TIE BAR PROTRUSIONS.

G. DRAWING FILENAME: MKT-MLP32Arev3.

Figure 9. 32-Lead, Molded Leadless Package (MLP)

Order Number	Operating Temperature Range	Package Description	Eco Status	Packing Method
FIN210ACMLX	-30 to 70°C	32-Terminal Molded Leadless Package (MLP), Quad, JEDEC MO-220, 5mm Square	Green	Tape & Reel

For Fairchild's definition of Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.

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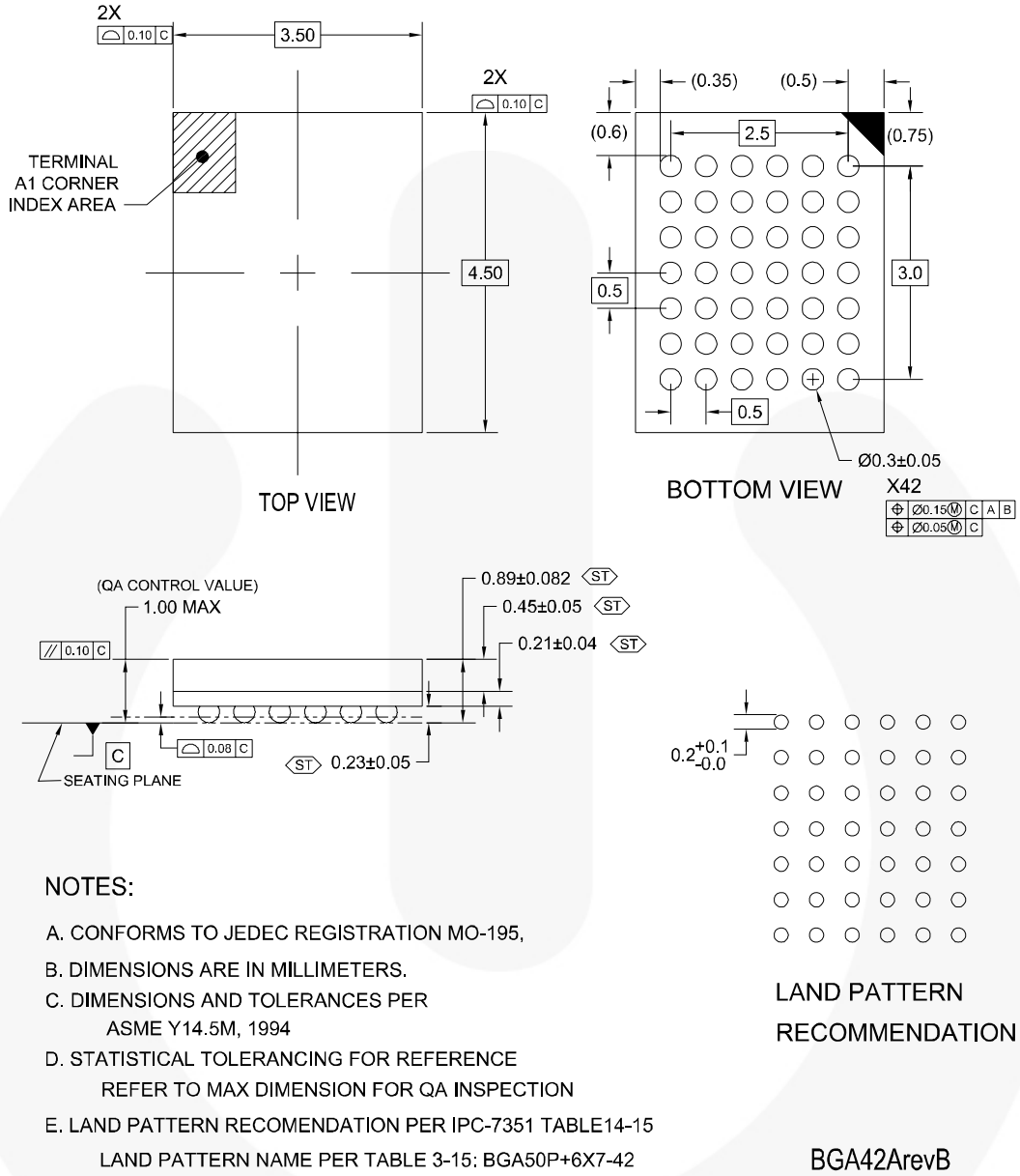
Physical Dimensions (Continued)



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-195,

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER
ASME Y14.5M, 1994

D. STATISTICAL TOLERANCING FOR REFERENCE
REFER TO MAX DIMENSION FOR QA INSPECTION

E. LAND PATTERN RECOMENDATION PER IPC-7351 TABLE14-15
LAND PATTERN NAME PER TABLE 3-15: BGA50P+6X7-42

BGA42ArevB

Figure 10. 42-Ball, Ball Grid Array (BGA) Package

Note: Click here for tape and reel specifications, available at:
http://www.fairchildsemi.com/products/analog/pdf/bga42_tr.pdf

Order Number	Operating Temperature Range	Package Description	Eco Status	Packing Method
FIN210ACGFX	-30 to 70°C	42-Ball Ultra Small-Scale Ball Grid Array (USS-BGA), JEDEC MO-195, 3.5 x 4.5mm Wide, 0.5mm Ball Pitch	RoHS	Tape & Reel

For Fairchild's definition of Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.

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