General TI High Voltage Evaluation User Safety Guidelines

Always follow TI's set-up and application instructions, including the use of all interface components within the recommended electrical rated voltage and power limits. Always use electrical safety precautions to help ensure your personal safety and the safety of those working around you. Contact TI's Product Information Center at http://support/ti./com for further information.

NOTE: Save all warnings and instructions for future reference.

Failure to follow warnings and instructions may result in personal injury, property damage, or death due to electrical shock and/or burn hazards.

The term TI HV EVM refers to an electronic device typically provided as an open framed, unenclosed PCB (printed circuit board)assembly. It is intended strictly for use in development laboratory environments, solely for qualified professional users having training, expertise, and knowledge of electrical safety risks in development and application of high-voltage electrical circuits. Any other use or application is strictly prohibited by Texas Instruments. If you are not suitably qualified, you should immediately stop from further use of the HV EVM.

- **Work Area Safety:**
  - Maintain a clean and orderly work area.
  - Qualified observer(s) must be present anytime circuits are energized.
  - Effective barriers and signage must be present in the area where the TI HV EVM and its interface electronics are energized; indicating operation of accessible high voltages may be present for the purpose of protecting inadvertent access.
  - All interface circuits, power supplies, evaluation modules, instruments, meters, scopes, and other related apparatus used in a development environment exceeding 50 VRMS/75 VDC must be electrically located within a protected Emergency Power Off (EPO) power strip.
  - Use a stable and non-conductive work surface.
  - Use adequately insulated clamps and wires to attach measurement probes and instruments. No freehand testing whenever possible.
- **Electrical Safety:**
  - As a precautionary measure, it is always a good engineering practice to assume that the entire EVM may have fully accessible and active high voltages.
  - De-energize the TI HV EVM and all its inputs, outputs, and electrical loads before performing any electrical or other diagnostic measurements. Confirm that TI HV EVM power has been safely de-energized.
  - After confirming the EVM is de-energized, proceed with the required electrical circuit configurations, wiring, measurement equipment hook-ups, and other application needs while still assuming the EVM circuit and measuring instruments are electrically live.
  - When EVM readiness is complete, energize the EVM as intended.

WARNING

While the EVM is energized, never touch the EVM or its electrical circuits as they could be at high voltages capable of causing electrical shock hazard.

- **Personal Safety:**
  - Wear personal protective equipment like latex gloves and safety glasses with side shields, or protect the EVM from accidental touch in an adequate translucent plastic box with interlocks.
- **Limitation for Safe Use:**
  - EVMs are not to be used as all or part of a production unit.

Safety and Precautions

The EVM is designed for professionals who have received the appropriate technical training and is designed to operate from an AC power supply or a high-voltage DC supply. Read this user guide and the safety-related documents that come with the EVM package before operating this EVM.

CAUTION

Do not leave the EVM powered when unattended.

WARNING

Hot surface! Contact may cause burns. Do not touch!

WARNING

High Voltage! Electric shock is possible when connecting board to live wire. Board should be handled with care by a professional.

For safety, use of isolated test equipment with overvoltage and overcurrent protection is highly recommended.

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WARNING

Before populating the EVM with a laser diode, read the out-of-the-box procedure to set the board up correctly before powering the laser diode, found in *Section 4*.

Using the LMG1020EVM-006 Nano-second LiDAR EVM

Contents

List of Figures

List of Tables

1 Introduction

The LMG1020 device is a single, low-side driver designed for driving GaN FETs and logic-level MOSFETs in high-frequency applications including LiDAR, time-of-flight, facial recognition, and any power converters involving low side drivers. The LMG1020EVM-006 is designed to evaluate the LMG1020. This EVM consists of one Gallium Nitride (GaN) enhancement mode FET driven by one LMG1020 and the drain of the GaN FET is connected to an unpopulated resistive load representing a typical laser diode load for LiDAR (Light Detection And Ranging) applications.

This User's Guide shows a circuit and the list of materials describing how to power the board up and how to configure the board. The EVM is designed to accelerate the evaluation of the LMG1020.

This EVM is not intended to be used as a standalone product but is intended to evaluate the switching performance of LMG1020.

This User's Guide describes correct operation and measurement of the EVM, as well as the EVM construction and typical performance.

2 Description

The LMG1020EVM-006 is a small, easy-to-use power stage that comes with a place to populate a resistive load, representing a typical Lidar laser diode load, as well as a place to populate a laser diode. Section 4 explains the procedure to set up the board out-of-the-box and accommodate the resistive load. The unpopulated resistive load will help achieve the applications required pulses before populating and powering the laser diode. The EVM takes a short-pulse input that can either be buffered (and shortened), or passed directly to the power stage.

The input pulse signal is used to pulse the current through the load (not populated out-of-the-box), to achieve 1-ns to 2-ns wide current pulses, which are the state-of-the-art target for LiDAR systems.

The EVM features a LMG1020, driving a single EPC2019 FET referenced to ground and with the drain connected to the unpopulated resistive load.

The board comes with a place to populate a resistive load, as well as larger pads where a laser diode of choice can be mounted. The load (when populated) is split between two current loops to reduce the effective inductance.

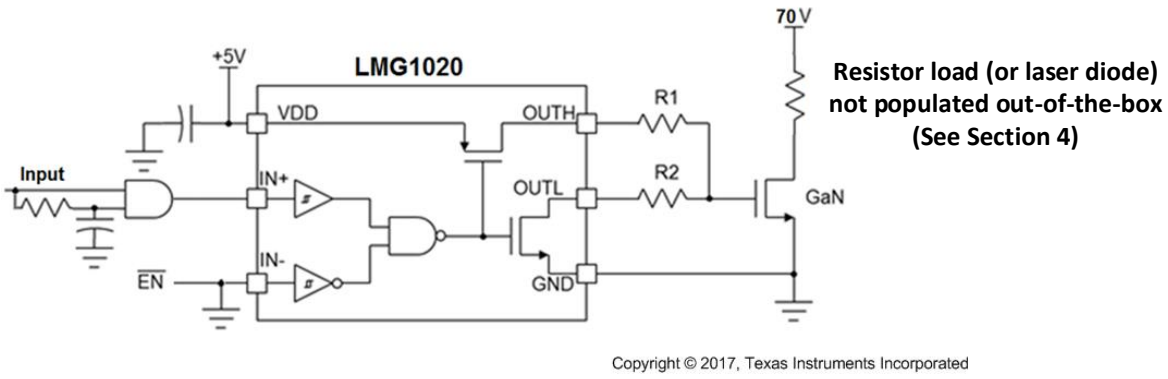

Figure 1. LiDAR Power Stage with LMG1020

The power stage can deliver up to 40 A of current to the load (when populated) at duty cycles ~0.1% and frequencies up to 2MHz. It includes adequate thermal management (case temperature should be monitored and adequate airflow should be ensured).

2.1 Typical Applications

The LMG1020 is suited for use in high frequency applications which may require nano-second pulse width. The extremely short pulse capability and short propagation delay, allow for state-of-the-art solutions.

Typical applications include:

- LiDAR power stage
- Wireless power
- VHF converters

CAUTION

High-voltage levels are present on the evaluation module whenever it is energized. Proper precautions must be taken when working with the EVM.

2.2 Features

The LMG1020 has the following features and specifications:

- Single low-side ultra-fast driver for 5-V drive GaN and silicon FETs
- Single 5-V supply
- Schmitt-trigger type CMOS inputs for robustness
- 2.5-ns typical, 4.5-ns max propagation delay
- 400-ps typical rise/fall time
- UVLO and over-temperature protection
- Minimum package 0.8 x 1.2 WCSP minimizes gate loop inductance and maximizes power density

The LMG1020EVM also includes the SN74LVC1G08, a single 2-input positive AND gate which provides the following features:

- Buffer for the LMG1020 input
- Used to shorten input pulse width by using a R-C filter on one input of the AND gate (Figure 8)
- Bypass the buffer by populating R3 with a 0-Ω resistor and removing R10 to disconnect the AND gate output.

The EVM also features a low ESL, 0.47-uF feed through capacitor (C4 in Figure 4)

- Feed through structure makes distance to GND shorter and obtains low ESL
- Low ESL to prevent ringing on VDD (5.4-V Recommended Max)
- Can be substituted with a 0201 capacitor placed as close to the pins as possible

3 Electrical Performance Specifications

Table 1. LMG1020EVM Electrical Performance Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input and Output Characteristics					
Input Voltage		0		75 (1)	VDC
Input current		0		0.1	A
Bias voltage	Iout,MAX = 100 mA	5.5		16	VDC
System Characteristics					
Switching frequency		0.1	1	50 (1)	MHz

(1) Determined by the thermal dissipation; depending on the magnitude of the current pulse and duty cycle. The thermal limitation of the resistor load, R5–R8, when populated is explained in more detail in *Section 4*.

4 EVM Operation Out-of-the-Box

The EVM, out-of-the-box, has a place to put a resistor load and a place to put a laser diode. The purpose of the resistor load is to set up the appropriate pulses required for a laser diode application. When operating the EVM, out-of-the-box, follow the procedure to properly fine tune the gate drive pulses before powering on a laser diode:

1. Size the resistor load, R5-R8, to represent the application's typical laser diode resistance
2. Populate the resistor load, R5-R8, by soldering 4 parallel 0603 size, 100 mW resistors
3. Achieve the required pulses for the laser diode application
4. Take the resistors, R5-R8, off before powering a laser diode
5. Populate a laser diode

CAUTION

Take off the resistor load, R5-R8, before powering on a laser diode.

When using LMG1020EVM out-of-the-box, the resistor load, R5 - R8, is not populated. With R5 - R8 not populated, the power loop is open and therefore the K waveform is not switching. For full functionality of the power loop without a laser diode connected, a resistor load R5 - R8 must be soldered on. The resistor load can be soldered by populating the four parallel resistors R5 - R8 as seen in Figure 3. To properly solder R5 - R8, use a soldering iron by hand and also hot air directed to the bottom of the board if needed. When selecting a resistor load, use 4 parallel 0603 size, 100 mW resistors and a typical laser diode resistance value of 1 Ω to 20 Ω. To achieve nanosecond pulses, a 1 Ω resistor load is recommended, in which four 4 Ω parallel resistors for R5 - R8 would be needed. The higher the resistor load value, the longer the switching rise and fall times as well as lower peak current. To avoid excessive power dissipation, damaging the R5 - R8 load resistors as seen in Figure 2, start by testing the EVM without a bus voltage to achieve the required pulse width, frequency, and repetition rate on the gate test point, Vg (TP4). When first testing the LMG1020EVM, start without a bus voltage. Try to achieve a short 1–2 ns gate pulse width to limit the peak current and thermal dissipation in the load resistors to a safe point when a bus voltage would be present. The on-board pulse shortener can be used to create a 1–2 ns pulse. The pulse shortener is explained in more detail in *Section 8.2*. After the required gate pulses are achieved, apply a small bus voltage. Begin with 5–10 V and gradually increase. When operating the EVM at 75 V while using the R5 - R8 resistor load, make sure to proceed with high voltage safety and caution. Operating at 75 V, the EVM can achieve high switching frequencies by using very short pulse widths and repetition rates. If the load resistors become damaged, the load resistance can be increased to an appropriate amount to limit the peak current or higher wattage resistors can be used. After achieving the required pulses on the gate, switch out the resistor load, R5-R8, for a laser diode of choice.

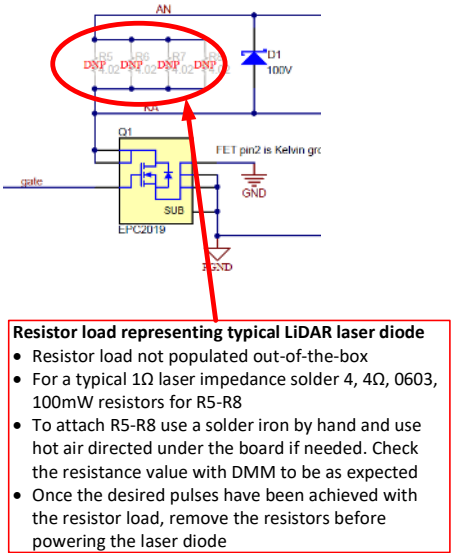

Figure 2. Schematic View of Unpopulated Load Resistors R5–R8

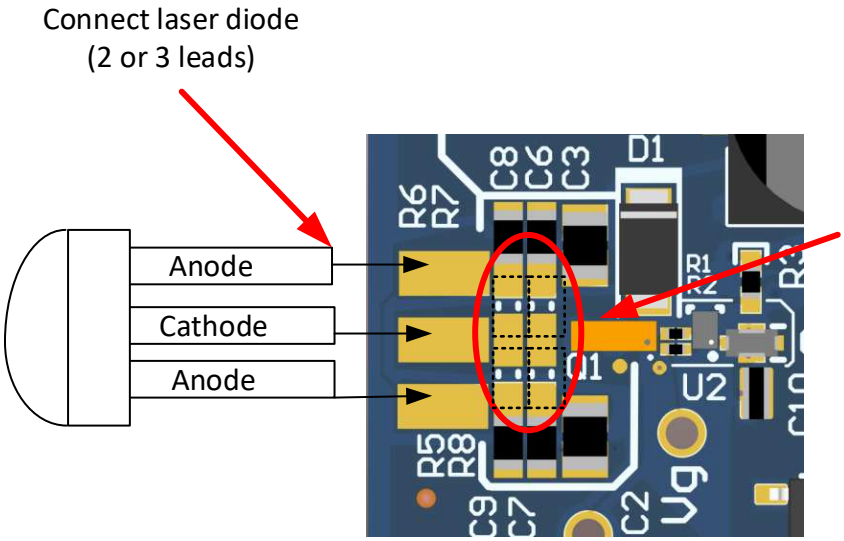

Figure 3. Populate Load Resistors R5–R8 Out-of-the-Box and Depopulate Before Testing Laser Diode

5 EVM Schematic

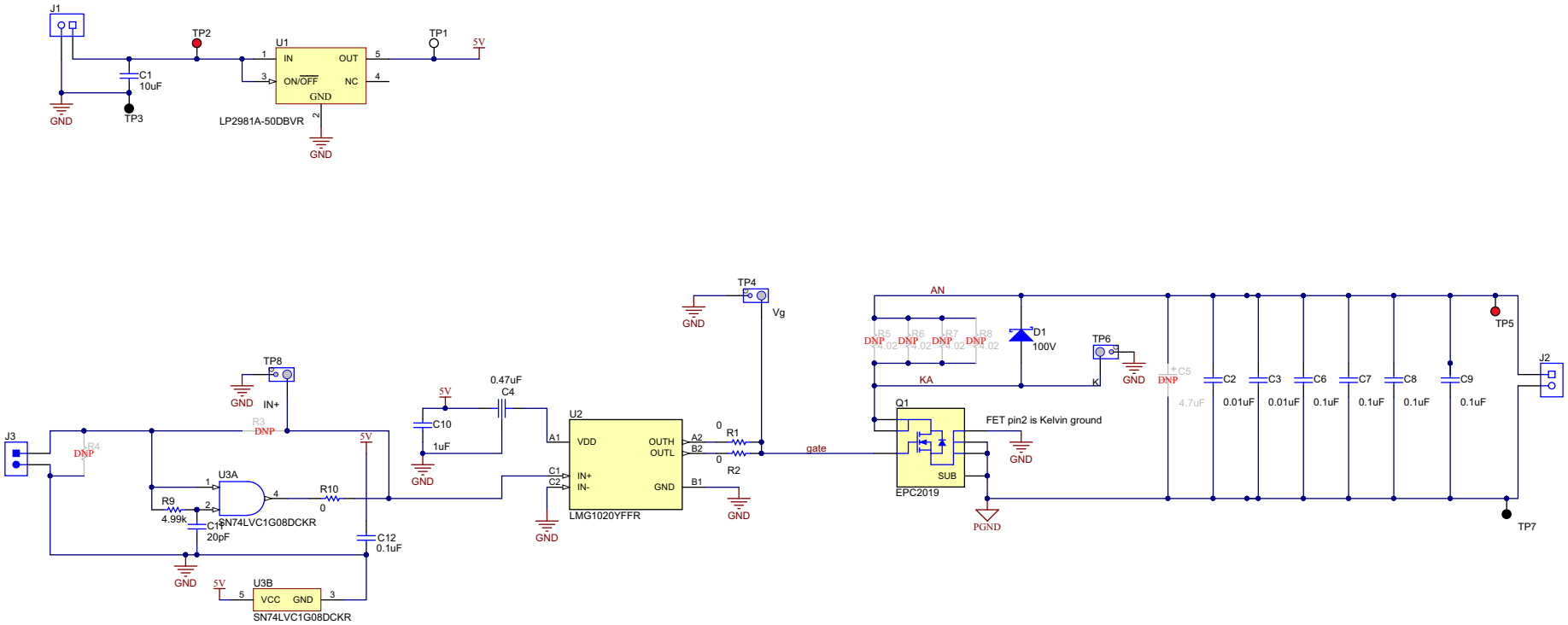

Figure 4. Power Stage Schematic (DNP = Do Not Place, Not Present On Board)

6 EVM Kit Contents

The kit contains the following:

- Using the LMG1020EVM-006 (this user's guide)
- Safety instructions
- LMG1020EVM-006 EVM PCB assembly

7 Test Setup

7.1 Test Equipment

DC Voltage Source: capable of supplying the input of the EVM up to 75 V_{DC} as desired. Capable of supplying 100 mA and supports current limiting.

DC Bias Source: capable of 5.5-V_{DC} to 15-V_{DC} output at up to 100 mA.

Oscilloscope: capable of at least 1-GHz operation, using oscilloscope probes with a “pigtail” spring ground clip instead of the standard alligator clip.

DC Multimeter(s): capable of 100-V measurement, suitable for determining operation and efficiency (if desired).

Function Generator: single output capable of at least 0-3 Vdc pulse signal (operating maximum digital input is 5 V_{DC}),1MHz frequency or higher, 50ns minimum pulse or smaller.

7.2 Recommended Test Setup

Connect the input and bias supplies as indicated in Figure 5.

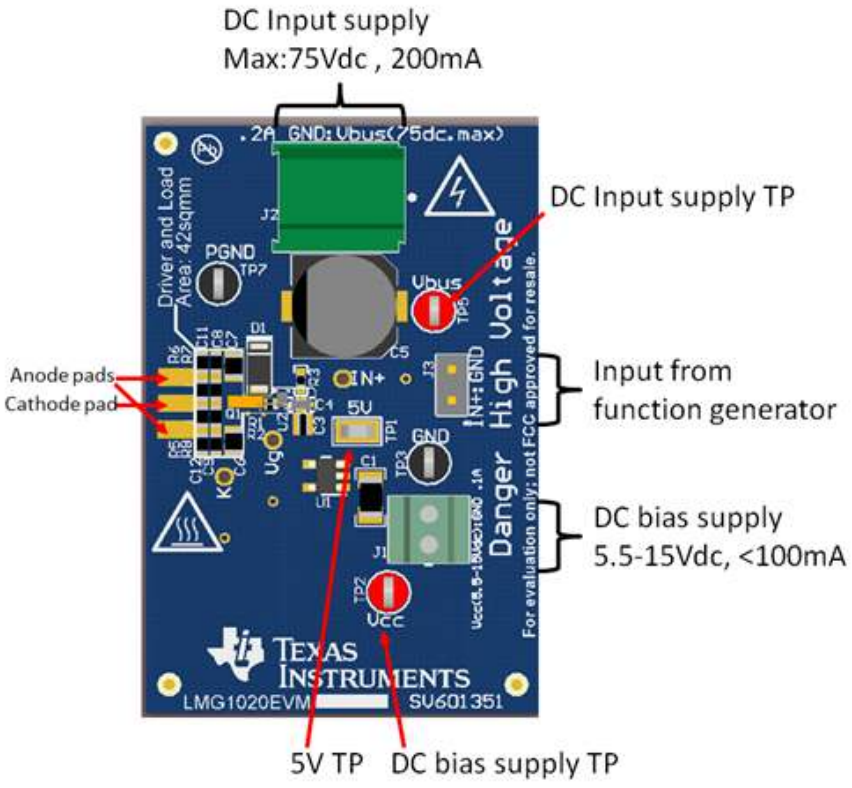

Figure 5. Recommended Connection Points and Feature Description

WARNING

High voltages that may cause injury exist on this evaluation module (EVM). Please ensure all safety procedures are followed when working on this EVM. Never leave a powered EVM unattended.

7.3 List of Test Points

The test points on this EVM have been designed for use with oscilloscope probes with the included spring-type ground connections, often called pigtails. Using the small pigtails without the probe clips will minimize measurement error and produce a cleaner signal with the fast switching GaN devices used on this EVM. The data shown in this user guide has been obtained using such a measurement method.

Table 2. Test Point Functional Description

TEST POINT	NAME	DESCRIPTION
TP1	5 V	Connected to the VDD pin of the LMG1020. This is 5Vdc nom
TP2	V_{CC}	Connected to the Vin of the on board LDO, this is the input bias supply voltage (5.5V-15Vdc)
TP3	GND	Connected to GND, the common reference for the board
TP4	Vg	Gate voltage, connected to the Gate of the GaN FET
TP5	V_{BUS}	Connected to the positive of the input supply for the power stage
TP6	K	Connected to the cathode of the laser diode, or negative of the unpopulated load. This is also the drain of the GaN FET
TP7	PGND	Connected to PGND, the common for the input supply of the power stage, internally star-connected to GND
TP8	IN+	Connected to IN+ pin of the LMG1020, this is the positive logic input.

Figure 6. Recommended Use for Ground Spring Clip Test Points

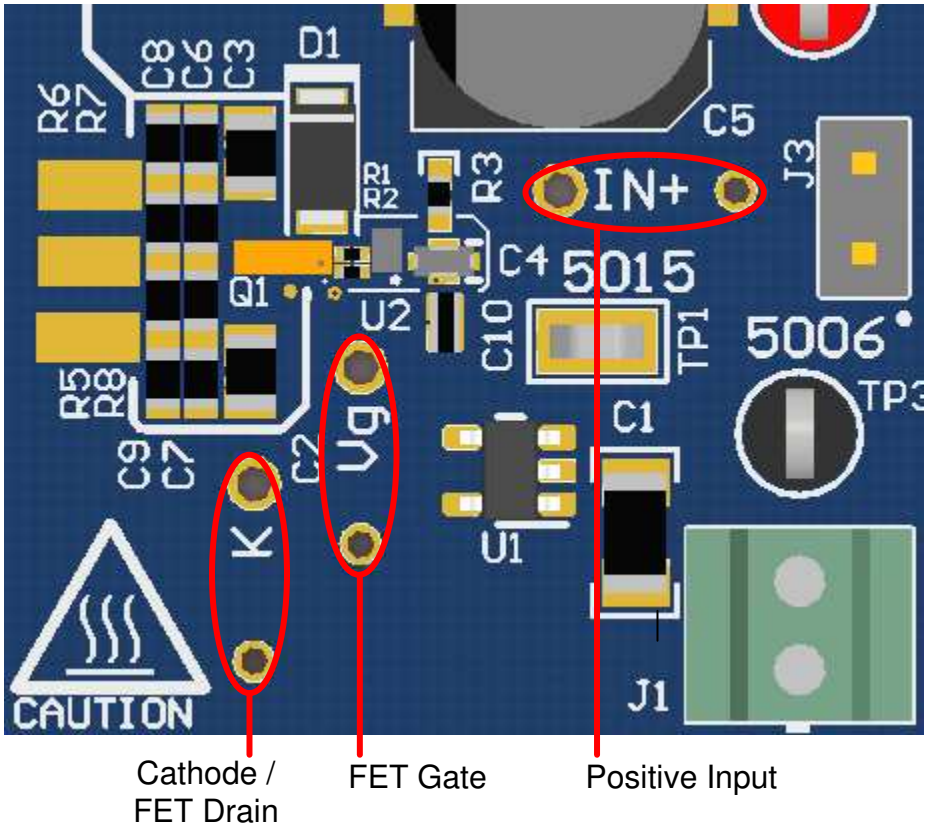

Figure 7. Visual and Description of Ground Spring Clip Test Points

7.4 List of Terminals

Table 3. List of Terminals

TERMINALS	NAME	DESCRIPTION
J1	DC Bias Supply (V_{CC})	Bias supply connection terminals (5.5-15 V_{DC}, 0.1 A)
J2	DC Input Supply (V_{BUS})	Input voltage connection terminals (MAX: 75 V_{DC}, 0.2 A)
J3	Input signal	Connector for function generator input, connected through a buffer to the positive input of the LMG1020

8 Test Procedure

WARNING

There are very high voltages present on the EVM. Some components reach temperatures above 50°C. Precautions must be taken when handling the board.

8.1 Nanosecond Pulse Measurements

WARNING

Before populating the EVM with a laser diode, read the out-of-the-box procedure to set the board up correctly before powering the laser diode, found in *Section 4*.

The following procedure is used to obtain and measure nano-second(s) pulse at the output:

1. Connect the input(J2) and bias supplies(J1) as shown in Figure 5, but do not power them on yet.
2. Power up the DC bias supply (J1) maintaining it in the 5.5 V to 15 V range and setting the current limit to 0.1 A.
3. Connect the function generator and apply the following settings:
   - Frequency to 100 kHz
   - Signal range 0 V to 3 V
   - Pulse width 100 ns
   - Enable the output
4. Power up the input supply(J2) (as shown in Figure 5) and set to the desired input voltage, but no higher than 75Vdc. Set the current limit to 0.2 A. It is recommended to begin measurements at lower voltage, such as 10 V to ensure the correct waveforms are being captured.
5. Tune the length of the pulse on the function generator, so that the Cathode voltage pulse is reduced to the desired width, this will be close to 1-2ns. **Notice that if a resistive load is populated, the rising edge of the pulse is given by the RC constant of the load in series with the COSS of the FET.**
6. Perform the desired measurements

8.2 Pulse Shortener

The digital input buffer includes the lowpass filter plus AND gate as seen in Figure 8. The combination can be used as a pulse shortener allowing a regular function generator to achieve 1-2 ns pulses on IN+. Most function generators can only output pulses as low as 10 ns, therefore the ability to create a 1-2 ns pulse can be achieved on the EVM using the AND gate input (J3). The AND gate compares the input (J3) to a RC delayed version and when both inputs are high the output will go high. The input pulse width or falling edge from the function generator can then be fine tuned in order to see the desired pulse width on IN+. When first starting to fine tune the function generator input to see the pulse on IN+, start with 100 ns then reduce the pulse width down by the nanosecond or smaller to make 1-2 ns visible on the IN+ test point. To bypass the pulse shortener populate R3 with a 0-Ω resistor and remove R9 and R10 to disconnect the AND gate input and output respectively.

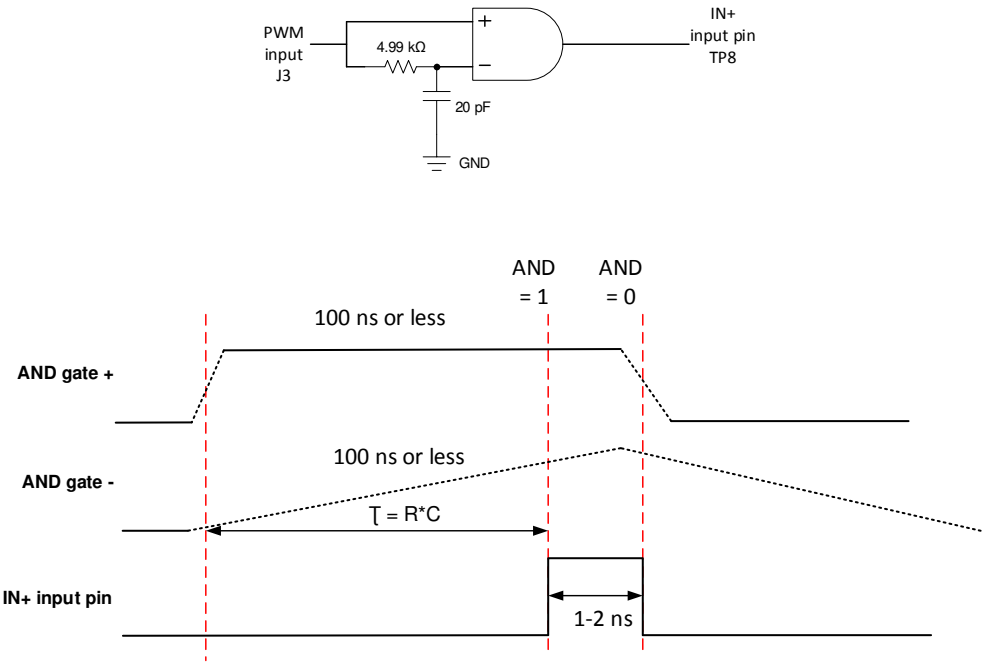

Figure 8. Pulse Shortener Yielding 1-ns to 2-ns Pulse on IN+

8.3 Shutdown Procedure

Once the desired measurements have been completed, shut down the EVM by following these steps:

1. Turn off the DC input power supply(J2)
2. Disable the function generator
3. Disable the bias supply(J1)

8.3.1 Components rating and DNPs

- All input capacitors are 100 V rated
- The EPC2019 FET is 200 V rated to withstand inductive voltage spikes
- The digital input buffer is placed to generate clean input signals on the board and to shorten the input pulse. To bypass it, the DNP resistor R3 has to be placed and resistor R10 has to be removed.
- Out-of-the-box the resistor load, R5 - R8, is not populated (DNP).

9 Performance Data and Typical Characteristics

Figure 9 through Figure 12 present typical performance curves for LMG1020EVM-006.

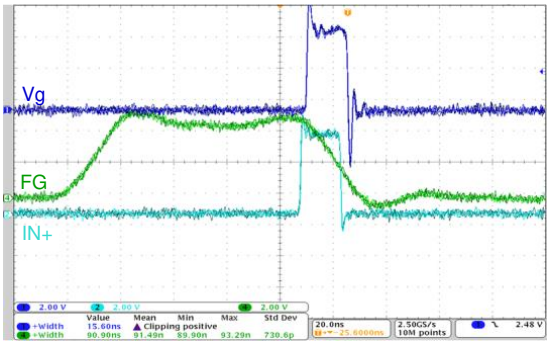

Figure 9. 90-ns Pulse from Function Generator Yielding 15-ns Pulse on the Gate

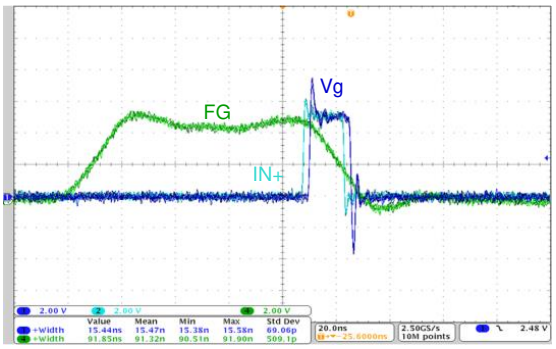

Figure 10. 90-ns Pulse from Function Generator Yielding 15-ns Pulse on the Gate

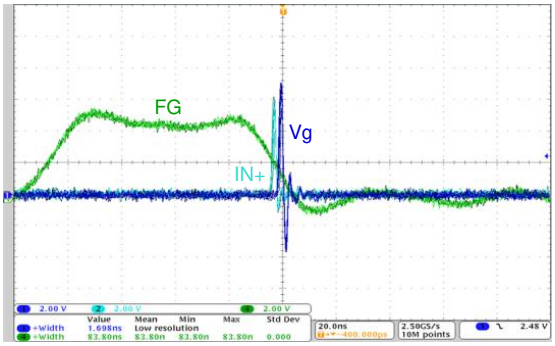

Figure 11. 84-ns Pulse from Function Generator Yielding 1.5-ns Pulse on the Gate

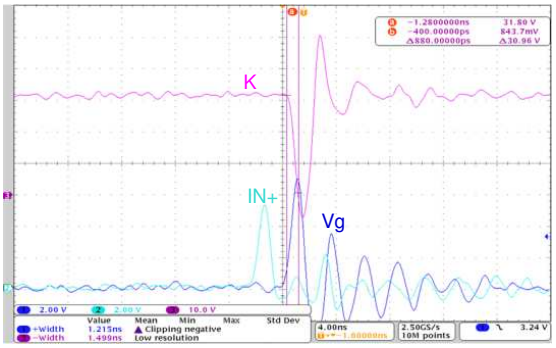

Figure 12. 1.2-ns Gate Pulse Yielding 1.5 ns, 30 V into 1-Ω Pulse (500-MHz Scope)

Figure 9 through Figure 11 show how the input stage performs and how the buffer cleans up and shortens the input pulse. This allows the use of a function generator with lower specifications.

Figure 12, taken with a 500MHz oscilloscope, shows typical operation waveforms. On the (K) waveform it is possible to see a 20V overshoot, this is due to the inductance in the power loop. Vg seems to be oscillating, but this is caused by pickup noise, which is inevitable even when using a spring ground connection. The expected resonant frequency for the gate loop is ~70-90MHz (given Gate capacitance of ~10nF and Gate inductance of 3-5nH), the oscillation observed is at 250MHz, which would imply a gate loop inductance of ~40pH. This is therefore pickup noise.

10 EVM Assembly Drawing and PCB Layout

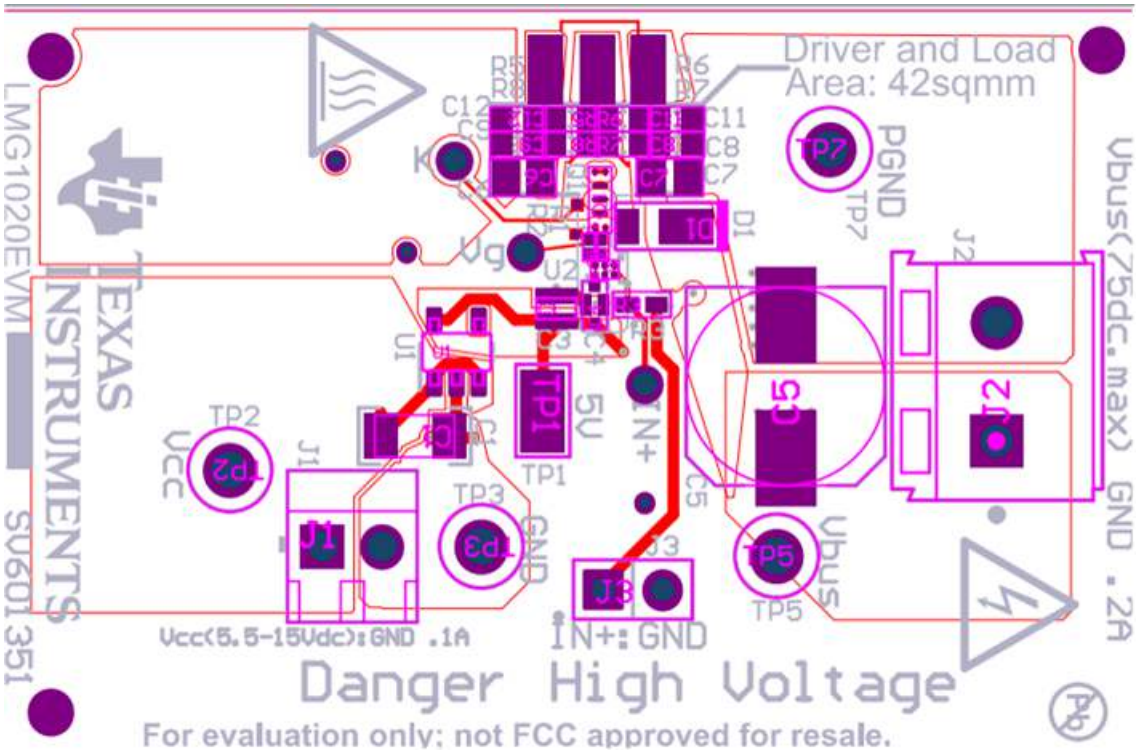

Figure 13. LMG1020EVM-006 Top Layer and Components

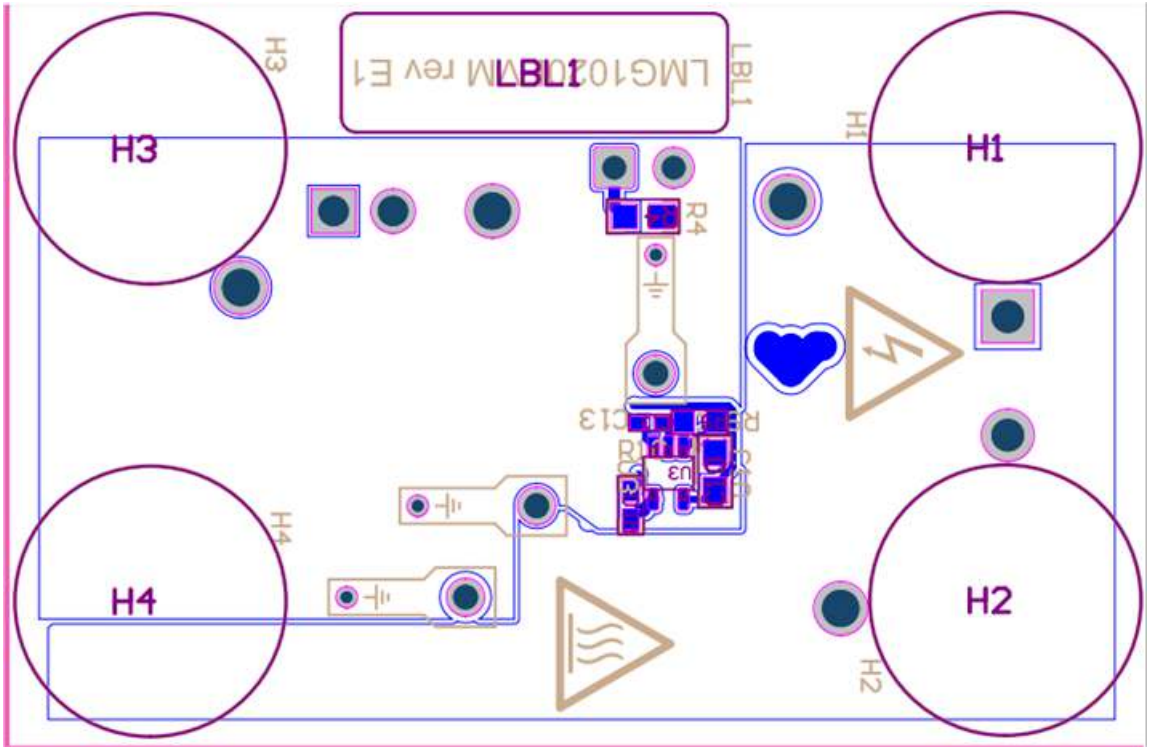

Figure 14. LMG1020EVM-006 Bottom Layer and Components

11 List of Materials

Table 4. LMG1020EVM-006 List of Materials

QUANTITY	DESIGNATOR	DESCRIPTION	PART NUMBER
1	C1	Capacitor ceramic, 10 µF, 25 V, ±10%, X7R, 1206	885012208069
2	C2, C3	Capacitor ceramic, 0.01 µF, 100 V, ±1%, C0G/NP0, 0805	C0805C103F1GACTU
1	C4	Feedthru Capacitor, 0.47 µF, 6.3V, SMD	YFF18PW0J474M
4	C6, C7 , C8, C9	Capacitor ceramic, 0.1 µF, 100 V, ±10%, X7R, 0603	GRM188R72A104KA35D
1	C10	Capacitor ceramic, 1 µF, 10V, ±20%, X5R, 0306	LWK107BJ105MV
1	C11	Capacitor ceramic, 20 pF, 50 V, +±5%, C0G/NP0, 0402	GRM1555C1H200JA01D
1	C12	Capacitor ceramic, 0.1 µF, 25 V, ±10%, X7R, 0603	GRM188R71E104KA01D
1	D1	Diode, Schottky, 100 V, 2 A, PowerDI123	DFLS2100-7
4	H1, H2, H3, H4	Bumpon, hemisphere, 0.44 X 0.20, Clear	SJ-5303 (CLEAR)
1	J1	Terminal block, 2.54 mm, 2 x 1, Brass, TH	OSTVN02A150
1	J2	Terminal block, 2 x 1, 5.08 mm, TH	282841-2
1	J3	Header, 100mil, 2 x 1, gold, TH	HTSW-102-07-G-S
1	Q1	MOSFET, N-channel, 200 V, 8.5 A, 2.766 x 0.68 mm	EPC2019
2	R1, R2	Resistor, 0, 5%, 0.05 W, 0201	ERJ-1GE0R00C
0	R5, R6, R7, R8	Resistor, 4.02 Ω, 0.5%, 0.1 W, 0603 (DNP)	RT0603DRE074R02L
1	R9	Resistor, 4.99 kΩ, 1%, 0.1 W, 0603	CR0603-FX-4991ELF
1	R10	Resistor, 0 Ω, 5%, 0.063 W, 0402	CRCW04020000Z0ED
1	TP1	Test point, miniature, SMT	5015
2	TP2, TP5	Test point, compact, red, TH	5005
2	TP3 , TP7	Test point, compact, black, TH	5006
3	TP4, TP6, TP8	Test point, pig tail	TESTPOINT_PIGTAIL
1	U1	Micropower 100 mA Ultra Low-Dropout Regulator in SOT-23 Package, DBV0005A (SOT-23-5)	LP2981A-50DBVR
1	U2	High Speed Gate Driver in WCSP Package, YFF	LMG1020YFFR
1	U3	Single 2-Input Positive-AND Gate, DCK0005A (SOT-5)	SN74LVC1G08DCKR
0	C5	Capacitor, aluminum, 4.7 µF, 100 V, ±20%, SMD	UUX2A4R7MCL1GS
0	FID1, FID2, FID3	Fiducial mark. There is nothing to buy or mount.	N/A
0	R3	Resistor, 10 Ω, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	CRCW040210R0JNED
0	R4	Resistor, 50 Ω, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060350R0FKEA

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from B Revision (May 2020) to C Revision **Page**

- Changed Description to explain the unpopulated resistor load 5

Changes from A Revision (April 2019) to B Revision **Page**

- Added EVM Operation Out-of-the-Box to include procedure of how to populate resistor load out-of-the-box. 6

Changes from Original (January 2018) to A Revision **Page**

- Added text to the introduction 5
- Changed LMG1020-HB-EVM to LMG1020EVM-006 5
- Changed 1-2MHz to 2MHz in Description section 5
- Changed 210ps to 400ps in Features section 6
- Added SN74LVC1G08 description to the features list 6
- Changed LMG1020 part # from XLMG1020A0 to LMG1020YFFR 9
- Added Pulse Shortener description to the test procedure 13

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