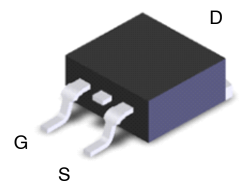
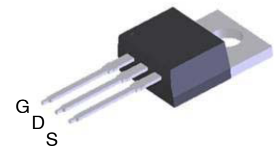
MOSFET – N-Channel, POWERTRENCH®

100 V, 32 A, 36 mΩ

FDB3682, FDP3682



D2PAK−3
(TO−263, 3−LEAD)
CASE 418AJ



TO−220−3LD
CASE 340AT

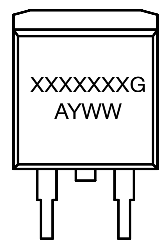
Features

- $R_{DS(on)}$ = 32 mΩ (Typ.) @ V_{GS} = 10 V, I_D = 32 A
- $Q_{G(tot)}$ = 18.5 nC (Typ.) @ V_{GS} = 10 V
- Low Miller Charge
- Low Q_{rr} Body Diode
- UIS Capability (Single Pulse and Repetitive Pulse)
- These Devices are Pb−Free and are RoHS Compliant

Applications

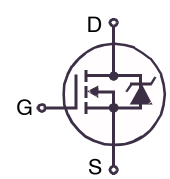
- Consumer Appliances
- Synchronous Rectification
- Battery Protection Circuit
- Motor Drives and Uninterruptible Power Supplies
- Micro Solar Inverter

MARKING DIAGRAM



XXXXXX = Specific Device Code (FDB3862 or FDP3862)
A = Assembly Location
Y = Year
WW = Work Week
G = Pb−Free Package

SCHEMATIC



ORDERING INFORMATION

See detailed ordering and shipping information on page 13 of this data sheet.

MOSFET MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Symbol	Parameter		FDB3682 / FDP3682	Unit
V_{DSS}	Drain to Source Voltage		100	V
V_{GS}	Gate to Source Voltage		±20	V
I_D	Drain Current	Continuous (T_C = 25°C, V_{GS} = 10 V)	32	A
		Continuous (T_C = 100°C, V_{GS} = 10 V)	23	A
		Continuous (T_{amb} = 25°C, V_{GS} = 10 V, $R_{\theta JA}$ = 43°C/W)	6	A
		Pulsed	Figure 4	A
E_{AS}	Single Pulse Avalanche Energy (Note 1)		55	mJ
P_D	Power Dissipation		95	W
	Derate above 25°C		0.63	mW/°C
T_J, T_{STG}	Operating and Storage Temperature		–55 to 175	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Starting T_J = 25°C, L = 0.27 mH, I_{AS} = 20 A.

THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case TO−220, TO−263, Max.	1.58	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient TO−220, TO−263 (Note 2), Max.	62	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient TO−263, 1 in^2 copper pad area, Max.	43	°C/W

2. Pulse Width = 100 s

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
OFF CHARACTERISTICS						
B_{VDSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	100			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 80 V, V_{GS} = 0 V			1	μA
		V_{DS} = 80 V, V_{GS} = 0 V, T_C = 150°C			250	
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V			±100	nA
ON CHARACTERISTICS						
$V_{GS(TH)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	2		4	V
$R_{DS(ON)}$	Drain to Source On Resistance	I_D = 32 A, V_{GS} = 10 V		0.032	0.036	Ω
		I_D = 16 V, V_{GS} = 6 V		0.040	0.060	
		I_D = 32 A, V_{GS} = 10 V, T_C = 175 °C		0.080	0.090	
DYNAMIC CHARACTERISTICS						
C_{ISS}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz		1250		pF
C_{OSS}	Output Capacitance			190		pF
C_{RSS}	Reverse Transfer Capacitance			45		pF
$Q_{g(TOT)}$	Total Gate Charge at 10 V	V_{GS} = 0 V to 10 V, V_{DD} = 50 V, I_D = 32 A, I_g = 1.0 mA		18.5	28	nC
$Q_{g(TH)}$	Threshold Gate Charge	V_{GS} = 0 V to 2 V, V_{DD} = 50 V, I_D = 32 A, I_g = 1.0 mA		2.4	3.6	nC
Q_{gs}	Gate to Source Gate Charge	V_{DD} = 50 V, I_D = 32 A, I_g = 1.0 mA		6.5		nC
Q_{gs2}	Gate Charge Threshold to Plateau			4.1		nC
Q_{gd}	Gate to Drain “Miller” Charge			4.6		nC
RESISTIVE SWITCHING CHARACTERISTICS (V_{GS} = 10 V)						
t_{ON}	Turn-On Time	V_{DD} = 50 V, I_D = 32 A, V_{GS} = 10 V, R_{GS} = 16 Ω			83	ns
$t_{d(ON)}$	Turn-On Delay Time			9		ns
t_r	Rise Time			46		ns
$t_{d(OFF)}$	Turn-Off Delay Time			26		ns
t_f	Fall Time			32		ns
t_{OFF}	Turn-Off Time				87	ns
DRAIN−SOURCE DIODE CHARACTERISTICS						
V_{SD}	Source to Drain Diode Voltage	I_{SD} = 32 A			1.25	V
		I_{SD} = 16 A			1.0	V
t_{rr}	Reverse Recovery Time	I_{SD} = 32 A, dI_{SD}/dt = 100 A/μs			55	ns
Q_{RR}	Reverse Recovered Charge	I_{SD} = 32 A, dI_{SD}/dt = 100 A/μs			90	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

(T_C = 25°C unless otherwise noted)

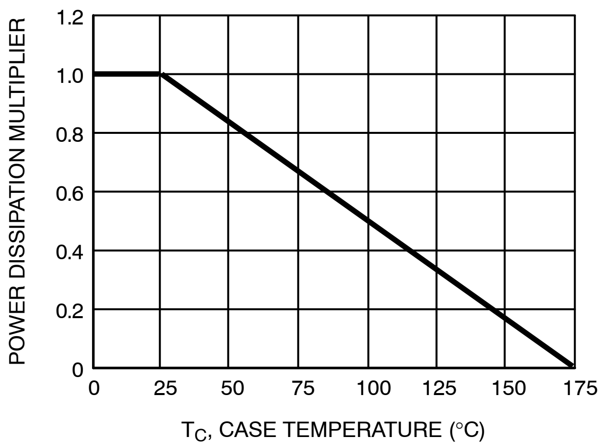


Figure 1. Normalized Power Dissipation vs. Case Temperature

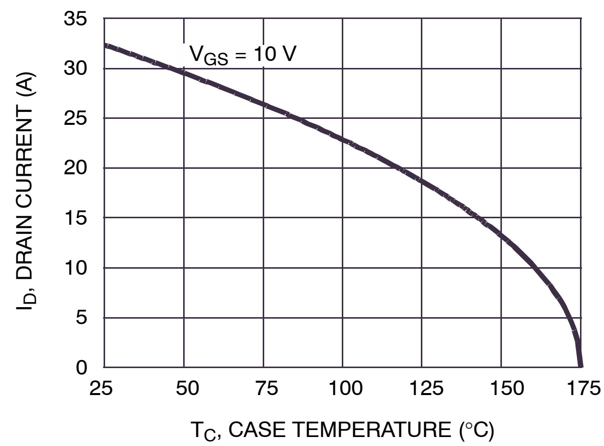


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

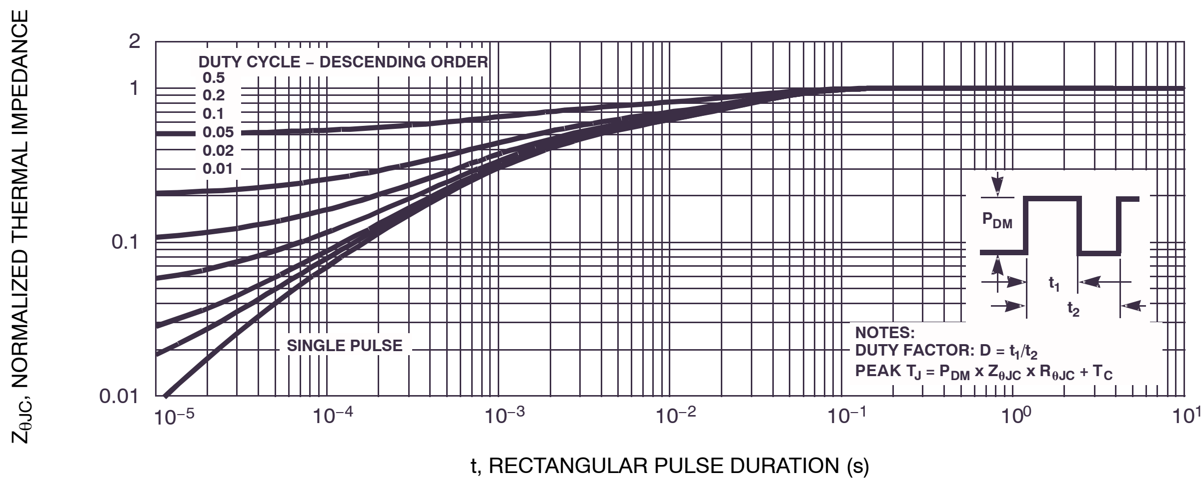


Figure 3. Normalized Maximum Transient Thermal Impedance

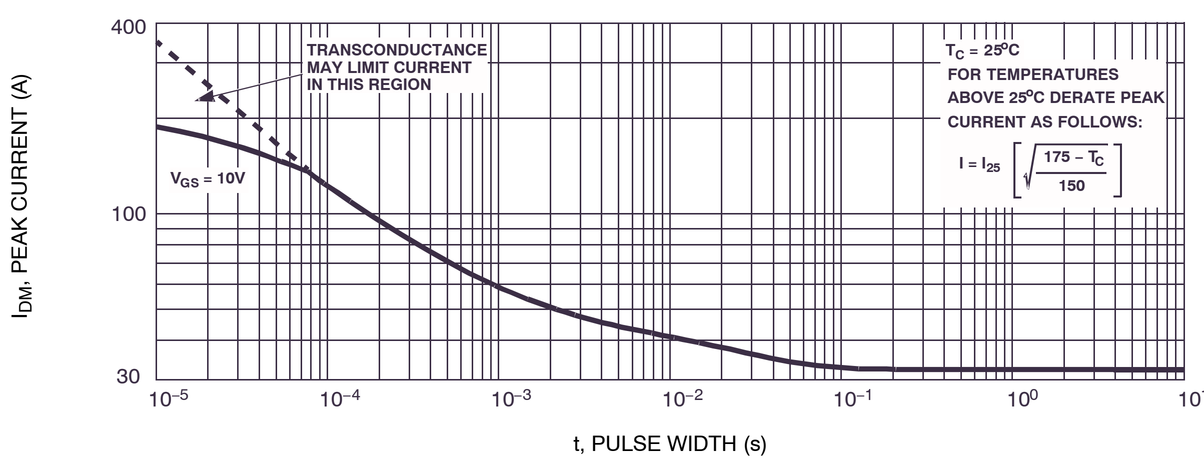


Figure 4. Peak Current Capability

TYPICAL CHARACTERISTICS

(T_C = 25°C unless otherwise noted) (continued)

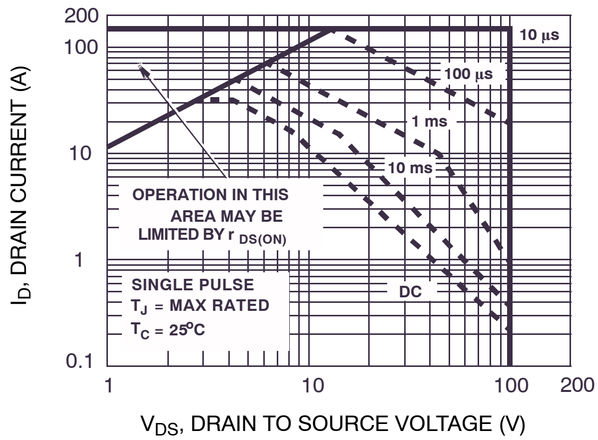
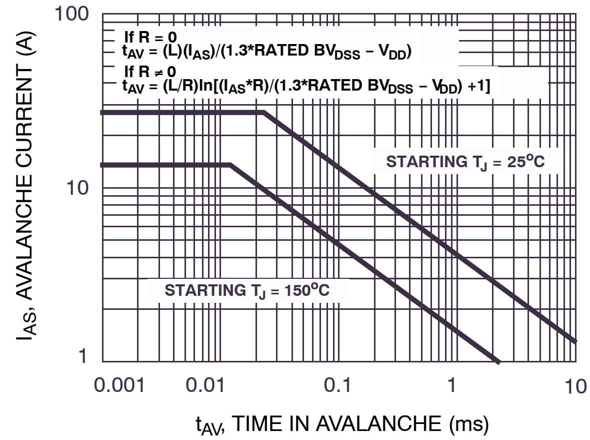


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to **onsemi** Application Notes AN–7514 and AN–7515

Figure 6. Unclamped Inductive Switching Capability

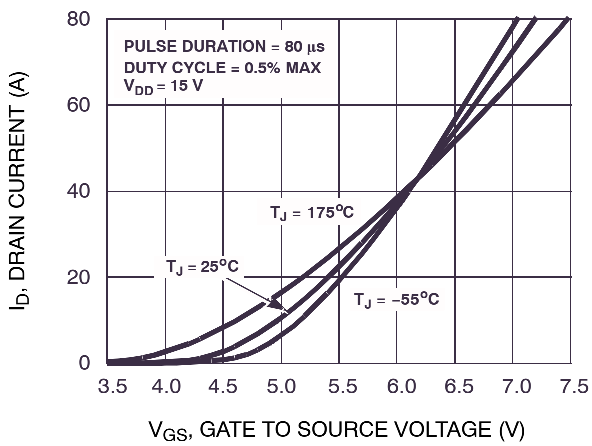


Figure 7. Transfer Characteristics

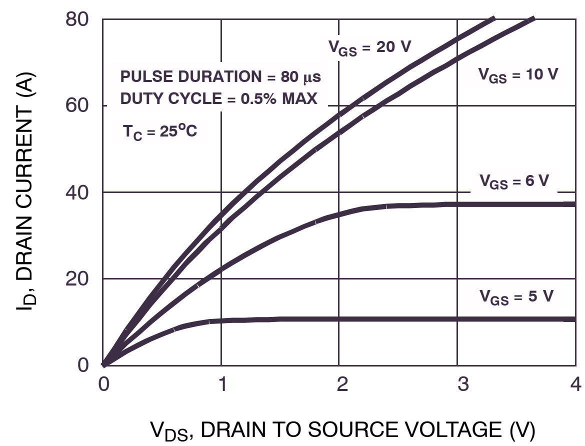


Figure 8. Saturation Characteristics

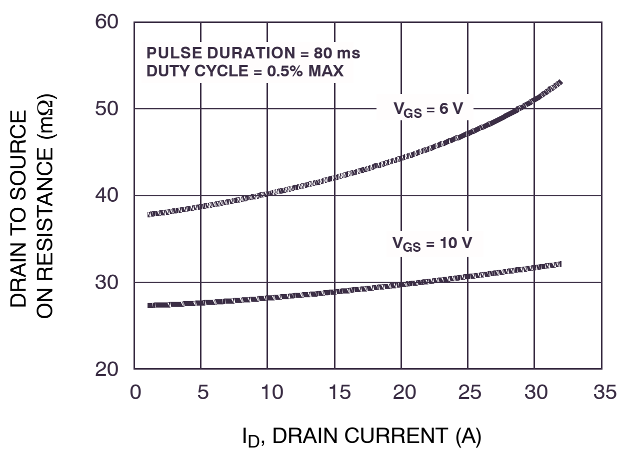


Figure 9. Drain to Source On Resistance vs. Drain Current

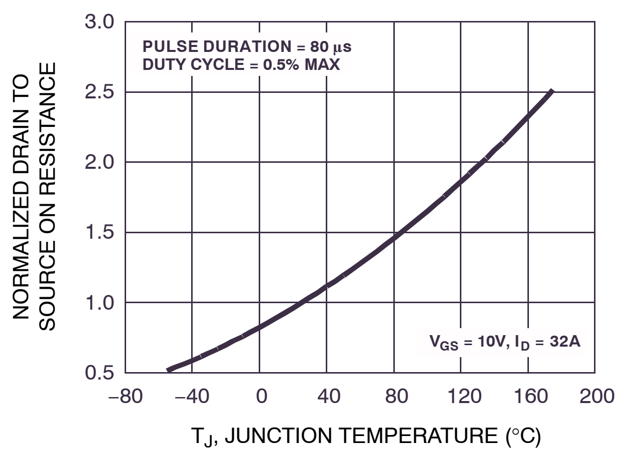


Figure 10. Normalized Drain to Source On Resistance vs. Junction Temperature

TYPICAL CHARACTERISTICS

(T_J = 25°C unless otherwise noted) (continued)

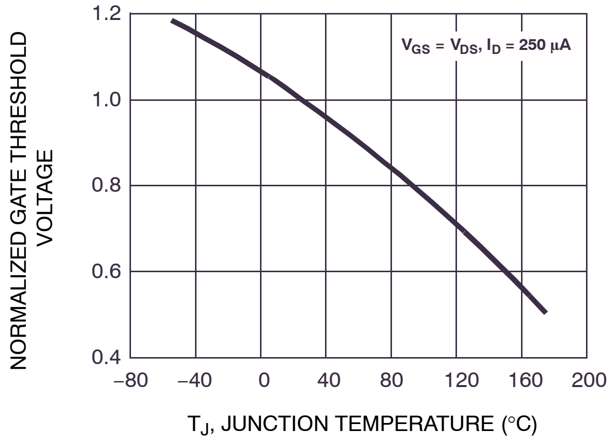


Figure 11. Normalized Gate Threshold Voltage vs. Junction Temperature

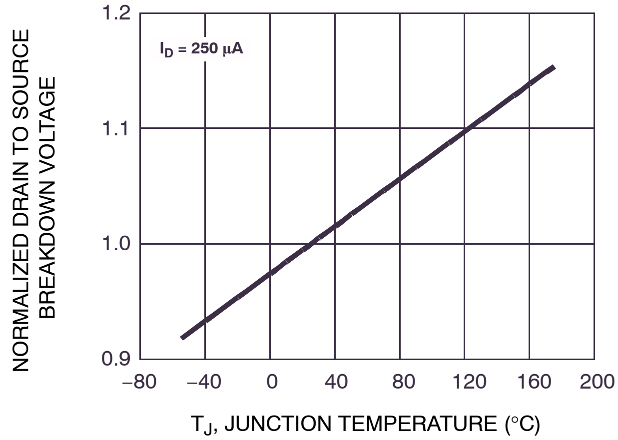


Figure 12. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

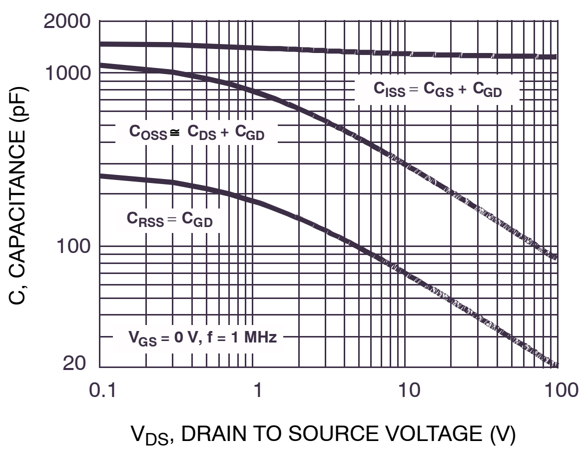


Figure 13. Capacitance vs. Drain to Source Voltage

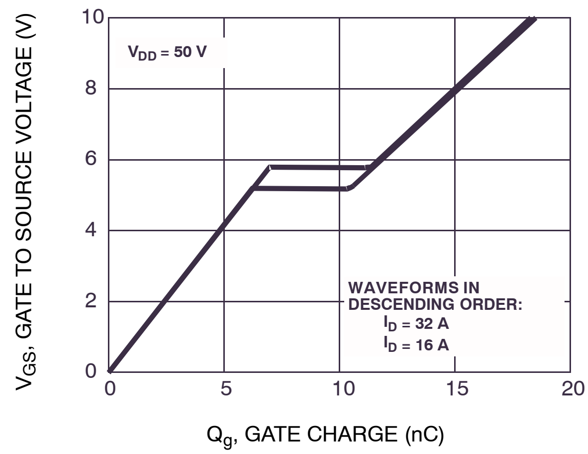


Figure 14. Gate Charge Waveforms for Constant Gate Currents

TEST CIRCUITS AND WAVEFORMS

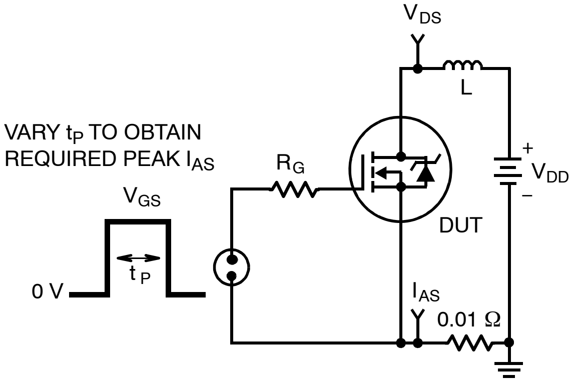


Figure 15. Unclamped Energy Test Circuit

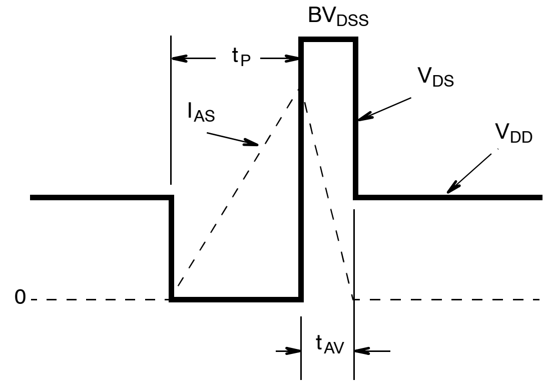


Figure 16. Unclamped Energy Waveforms

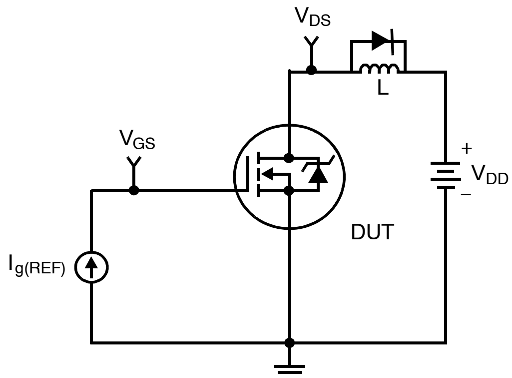


Figure 17. Gate Charge Test Circuit

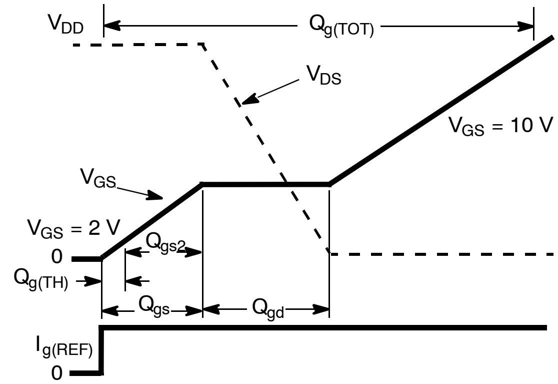


Figure 18. Gate Charge Waveforms

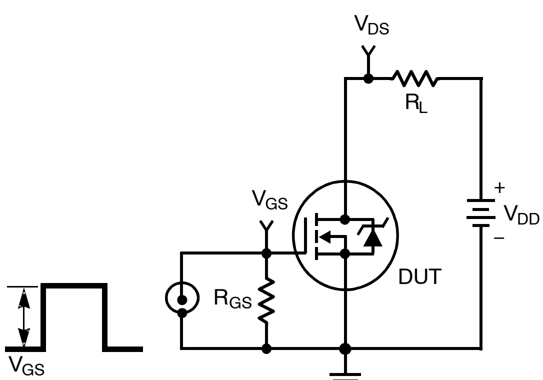


Figure 19. Switching Time Test Circuit

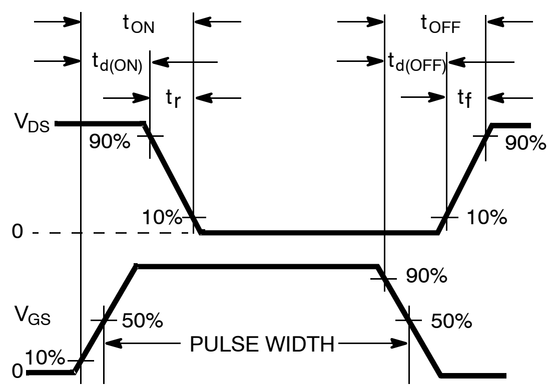


Figure 20. Switching Time Waveforms

THERMAL RESISTANCE VS. MOUNTING PAD AREA

The maximum rated junction temperature, T_{JM}, and the thermal resistance of the heat dissipating path determines the maximum allowable device power dissipation, P_{DM}, in an application. Therefore the application's ambient temperature, T_A (°C), and thermal resistance $R_{\theta JA}$ (°C/W) must be reviewed to ensure that T_{JM} is never exceeded. Equation 1 mathematically represents the relationship and serves as the basis for establishing the rating of the part.

$$P_{DM} = \frac{(T_{JM} - T_A)}{R_{\theta JA}} \qquad \text{(eq. 1)}$$

In using surface mount devices such as the TO−263 package, the environment in which it is applied will have a significant influence on the part's current and maximum power dissipation ratings. Precise determination of P_{DM} is complex and influenced by many factors:

1. Mounting pad area onto which the device is attached and whether there is copper on one side or both sides of the board.
2. The number of copper layers and the thickness of the board.
3. The use of external heat sinks.
4. The use of thermal vias.
5. Air flow and board orientation.
6. For non steady state applications, the pulse width, the duty cycle and the transient thermal response of the part, the board and the environment they are in.

onsemi provides thermal information to assist the designer's preliminary application evaluation. Figure 21 defines the $R_{\theta JA}$ for the device as a function of the top copper (component side) area. This is for a horizontally positioned FR−4 board with 1 oz copper after 1000 seconds of steady state power with no air flow. This graph provides the necessary information for calculation of the steady state junction temperature or power dissipation. Pulse applications can be evaluated using the **onsemi** device Spice thermal model or manually utilizing the normalized maximum transient thermal impedance curve.

Thermal resistances corresponding to other copper areas can be obtained from Figure 21 or by calculation using Equation 2 or 3. Equation 2 is used for copper area defined in inches square and equation 3 is for area in centimeter square. The area, in square inches or square centimeters is the top copper area including the gate and source pads.

$$R_{\theta JA} = 26.51 + \frac{19.84}{0.262 + \text{Area}} \qquad \text{(eq. 2)}$$

Area in in^2.

$$R_{\theta JA} = 26.51 + \frac{128}{1.69 + \text{Area}} \qquad \text{(eq. 3)}$$

Area in cm^2.

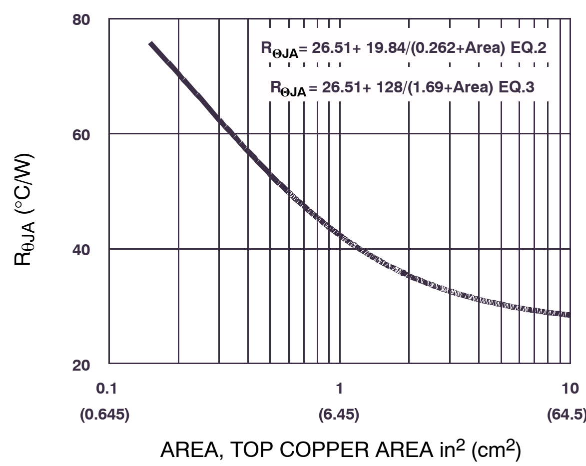


Figure 21. Thermal Resistance vs. Mounting Pad Area

PSPICE ELECTRICAL MODEL

```
.SUBCKT FDB3682 2 1 3 ;    rev May 2002
Ca 12 8 4e−10
Cb 15 14 5.5e−10
Cin 6 8 1.22e−9

Dbody 7 5 DbodyMOD
Dbreak 5 11 DbreakMOD
Dplcap 10 5 DplcapMOD

Ebreak 11 7 17 18 108
Eds 14 8 5 8 1
Egs 13 8 6 8 1
Esg 6 10 6 8 1
Evthres 6 21 19 8 1
Evtemp 20 6 18 22 1

It 8 17 1

Lgate 1 9 5.96e−9
Ldrain 2 5 1.0e−9
Lsource 3 7 3.19e−9

RLgate 1 9 59.6
RLdrain 2 5 10
RLsource 3 7 31.9

Mmed 16 6 8 8 MmedMOD
Mstro 16 6 8 8 MstroMOD
Mweak 16 21 8 8 MweakMOD

Rbreak 17 18 RbreakMOD 1
Rdrain 50 16 RdrainMOD 10.5e−3
Rgate 9 20 1.86
RSLC1 5 51 RSLCMOD 1.0e−6
RSLC2 5 50 1.0e3
Rsource 8 7 RsourceMOD 11.9e−3
Rvthres 22 8 RvthresMOD 1
Rvtemp 18 19 RvtempMOD 1
S1a 6 12 13 8 S1AMOD
S1b 13 12 13 8 S1BMOD
S2a 6 15 14 13 S2AMOD
S2b 13 15 14 13 S2BMOD

Vbat 22 19 DC 1

ESLC 51 50 VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e−6*70),2.5))}

.MODEL DbodyMOD D (IS=2.4E−12  RS=4.4e−3 TRS1=2.0e−3 TRS2=4.5e−7
+ CJO=9e−10 M=0.57 TT=2.9e−8 XTI=4.0)
.MODEL DbreakMOD D (RS=0.6 TRS1=1.4e−3 TRS2=−5.0e−5)
.MODEL DplcapMOD D (CJO=2.7e−10 IS=1.0e−30 N=10 M=0.56)

.MODEL MstroMOD NMOS (VTO=4.16 KP=32 IS=1e−30 N=10 TOX=1 L=1u W=1u)
.MODEL MmedMOD NMOS (VTO=3.48 KP=2.7 IS=1e−30 N=10 TOX=1 L=1u W=1u RG=1.86)
.MODEL MweakMOD NMOS (VTO=2.97 KP=0.04 IS=1e−30 N=10 TOX=1 L=1u W=1u RG=18.6 RS=0.1)
```

.MODEL RbreakMOD RES (TC1=1.05e−3 TC2=−1.1e−8)
.MODEL RdrainMOD RES (TC1=1.6e−2 TC2=4e−5)
.MODEL RSLCMOD RES (TC1=3.0e−3 TC2=2.9e−6)
.MODEL RsourceMOD RES (TC1=1e−3 TC2=1e−6)
.MODEL RvthresMOD RES (TC1=−4.1e−3 TC2=−1.4e−5)
.MODEL RvtempMOD RES (TC1=−3.5e−3 TC2=1.3e−6)

.MODEL S1AMOD VSWITCH (RON=1e−5 ROFF=0.1 VON=−5.0 VOFF=−2.0)
.MODEL S1BMOD VSWITCH (RON=1e−5 ROFF=0.1 VON=−2.0 VOFF=−5.0)
.MODEL S2AMOD VSWITCH (RON=1e−5 ROFF=0.1 VON=−0.4 VOFF=0.3)
.MODEL S2BMOD VSWITCH (RON=1e−5 ROFF=0.1 VON=0.3 VOFF=−0.4)

.ENDS

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub−Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.

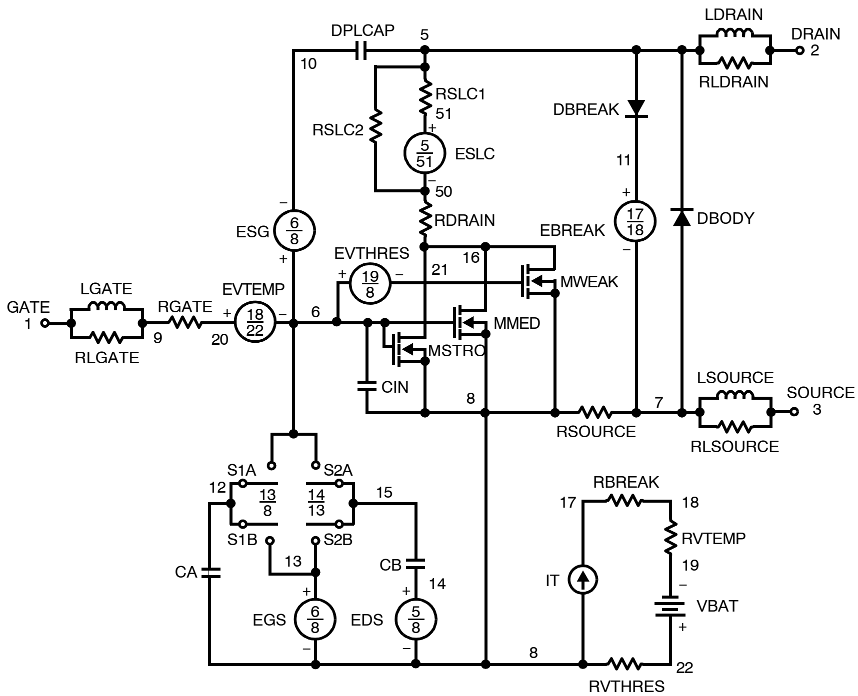


Figure 22.

SABER ELECTRICAL MODEL

```
REV May 2002
template FDB3682 n2,n1,n3
electrical n2,n1,n3
{
var i iscl
dp..model dbodymod = (isl=2.4e−12,rs=4.4e−3,trs1=2.0e−3,trs2=4.5e−7,cjo=9e−10,m=0.57,tt=2.9e−8,xti=4.0)
dp..model dbreakmod = (rs=0.6,trs1=1.4e−3,trs2=−5e−5)
dp..model dplcapmod = (cjo=2.7e−10,isl=10e−30,nl=10,m=0.56)
m..model mstrongmod = (type=_n,vto=4.16,kp=32,is=1e−30, tox=1)
m..model mmedmod = (type=_n,vto=3.48,kp=2.7,is=1e−30, tox=1)
m..model mweakmod = (type=_n,vto=2.97,kp=0.04,is=1e−30, tox=1,rs=0.1)
sw_vcsp..model s1amod = (ron=1e−5,roff=0.1,von=−5,voff=−2)
sw_vcsp..model s1bmod = (ron=1e−5,roff=0.1,von=−2,voff=−5)
sw_vcsp..model s2amod = (ron=1e−5,roff=0.1,von=−0.4,voff=0.3)
sw_vcsp..model s2bmod = (ron=1e−5,roff=0.1,von=0.3,voff=−0.4)
c.ca n12 n8 = 4e−10
c.cb n15 n14 = 5.5e−10
c.cin n6 n8 = 1.22e−9

dp.dbody n7 n5 = model=dbodymod
dp.dbreak n5 n11 = model=dbreakmod
dp.dplcap n10 n5 = model=dplcapmod

spe.ebreak n11 n7 n17 n18 = 108
spe.eds n14 n8 n5 n8 = 1
spe.egs n13 n8 n6 n8 = 1
spe.esg n6 n10 n6 n8 = 1
spe.evthres n6 n21 n19 n8 = 1
spe.evtemp n20 n6 n18 n22 = 1

i.it n8 n17 = 1

l.lgate n1 n9 = 5.96e−9
l.ldrain n2 n5 = 1.0e−9
l.lsource n3 n7 = 3.19e−9

res.rlgate n1 n9 = 59.6
res.rldrain n2 n5 = 10
res.rlsource n3 n7 = 31.9

m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u
m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u
m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u

res.rbreak n17 n18 = 1, tc1=1.05e−3,tc2=−1.1e−8
res.rdrain n50 n16 = 10.5e−3, tc1=1.6e−2,tc2=4e−5
res.rgate n9 n20 = 1.86
res.rslc1 n5 n51 = 1.0e−6, tc1=3.0e−3,tc2=2.9e−6
res.rslc2 n5 n50 = 1.0e3
res.rsource n8 n7 = 11.9e−3, tc1=1e−3,tc2=1e−6
res.rvthres n22 n8 = 1, tc1=−4.1e−3,tc2=−1.4e−5
res.rvtemp n18 n19 = 1, tc1=−3.5e−3,tc2=1.3e−6
sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod
sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod
sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod
sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod
```

```
v.vbat n22 n19 = dc=1
equations {
i (n51−>n50) +=iscl
iscl: v(n51,n50) = ((v(n5,n51)/(1e−9+abs(v(n5,n51))))*((abs(v(n5,n51)*1e6/70))** 2.5))
}
}
```

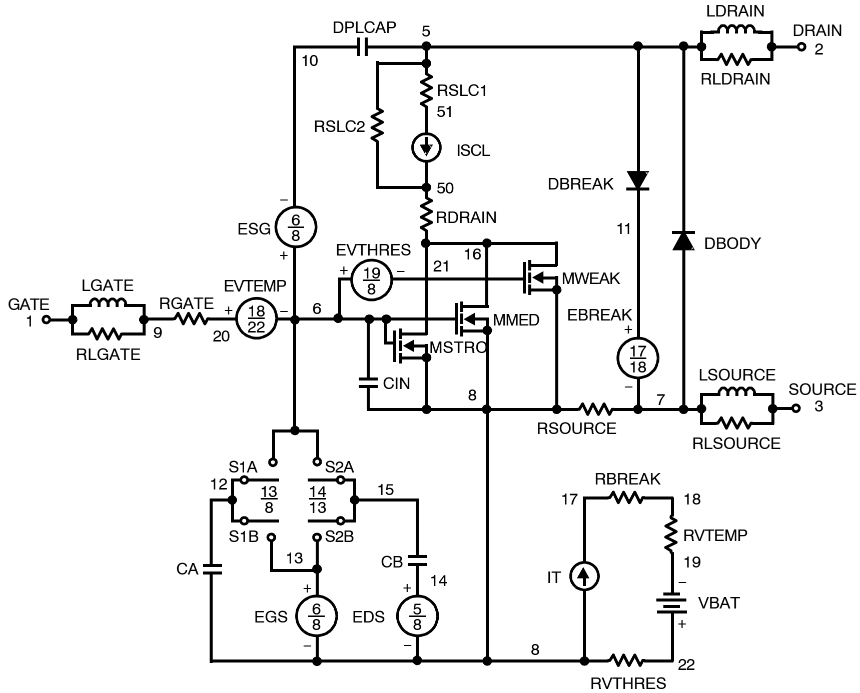


Figure 23.

SPICE THERMAL MODEL

REV 20 May 2002

FDB3682_JC TH TL

CTHERM1 TH 6 1.6e−3
CTHERM2 6 5 4.5e−3
CTHERM3 5 4 5.0e−3
CTHERM4 4 3 8.0e−3
CTHERM5 3 2 8.2e−3
CTHERM6 2 TL 4.7e−2

RTHERM1 TH 6 3.3e−2
RTHERM2 6 5 7.9e−2
RTHERM3 5 4 9.5e−2
RTHERM4 4 3 1.4e−1
RTHERM5 3 2 2.9e−1
RTHERM6 2 TL 6.7e−1

SABER THERMAL MODEL

SABER thermal model FDB3682
template thermal_model th tl
thermal_c th, tl
{
ctherm.ctherm1 th 6 =1.6e−3
ctherm.ctherm2 6 5 =4.5e−3
ctherm.ctherm3 5 4 =5.0e−3
ctherm.ctherm4 4 3 =8.0e−3
ctherm.ctherm5 3 2 =8.2e−3
ctherm.ctherm6 2 tl =4.7e−2

rtherm.rtherm1 th 6 =3.3e−2
rtherm.rtherm2 6 5 =7.9e−2
rtherm.rtherm3 5 4 =9.5e−2
rtherm.rtherm4 4 3 =1.4e−1
rtherm.rtherm5 3 2 =2.9e−1
rtherm.rtherm6 2 tl =6.7e−1
}

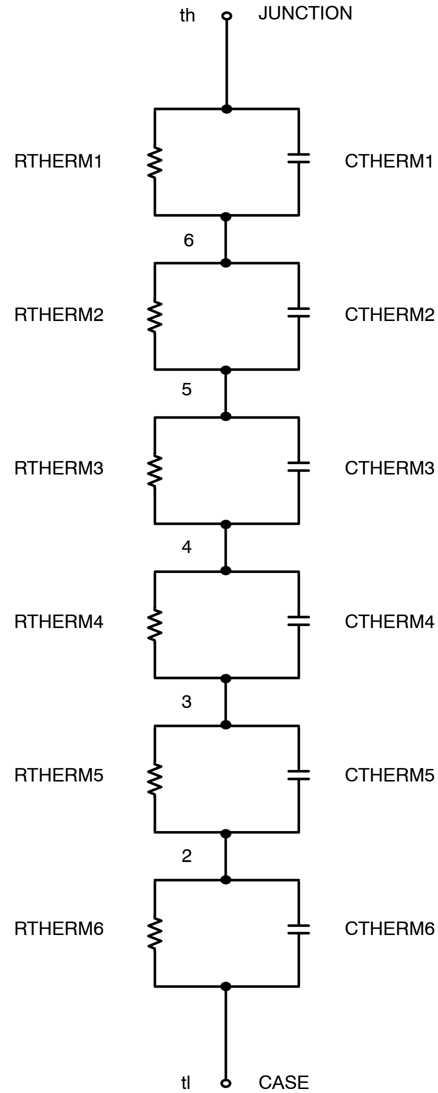
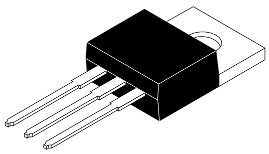


Figure 24.

PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package Type	Shipping†
FDB3682	FDB3682	D2PAK−3 (TO−263) (Pb−Free)	800 / Tape & Reel
FDP3682	FDP3682	TO−220−3LD (Pb−Free)	800 / Tube

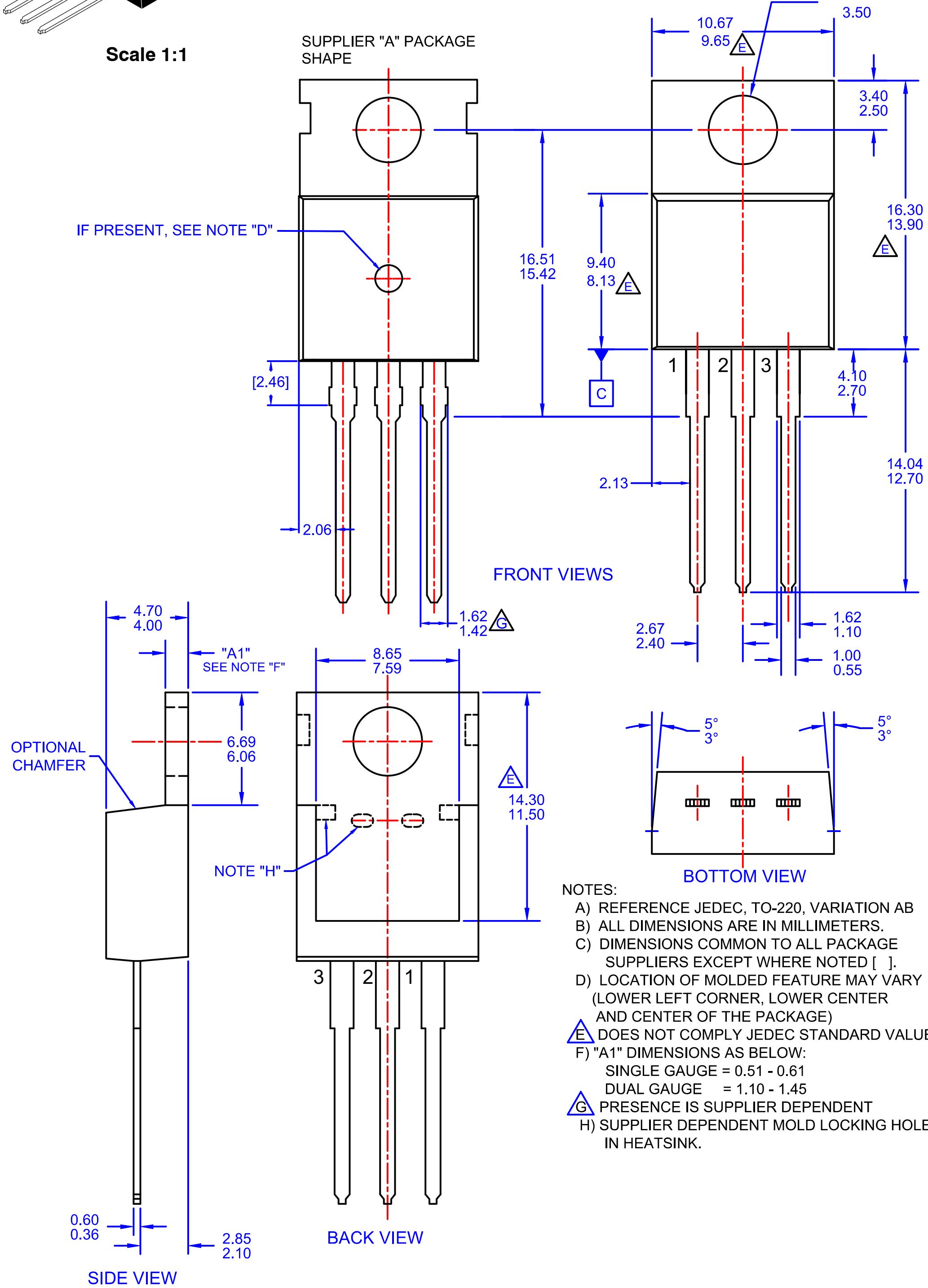
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



Scale 1:1

TO−220−3LD
CASE 340AT
ISSUE A

DATE 03 OCT 2017



NOTES:
- A) REFERENCE JEDEC, TO-220, VARIATION AB
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS COMMON TO ALL PACKAGE SUPPLIERS EXCEPT WHERE NOTED [ ].
- D) LOCATION OF MOLDED FEATURE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE)
- E) DOES NOT COMPLY JEDEC STANDARD VALUE.
- F) "A1" DIMENSIONS AS BELOW:
  - SINGLE GAUGE = 0.51 - 0.61
  - DUAL GAUGE = 1.10 - 1.45
- G) PRESENCE IS SUPPLIER DEPENDENT
- H) SUPPLIER DEPENDENT MOLD LOCKING HOLES IN HEATSINK.

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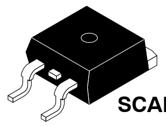
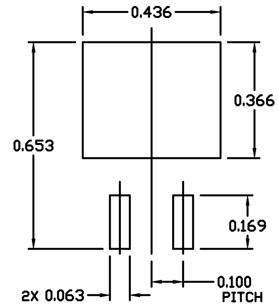
DESCRIPTION:	**TO−220−3LD**	**PAGE 1 OF 1**



SCALE 1:1

D^2PAK−3 (TO−263, 3−LEAD)
CASE 418AJ
ISSUE F

DATE 11 MAR 2021



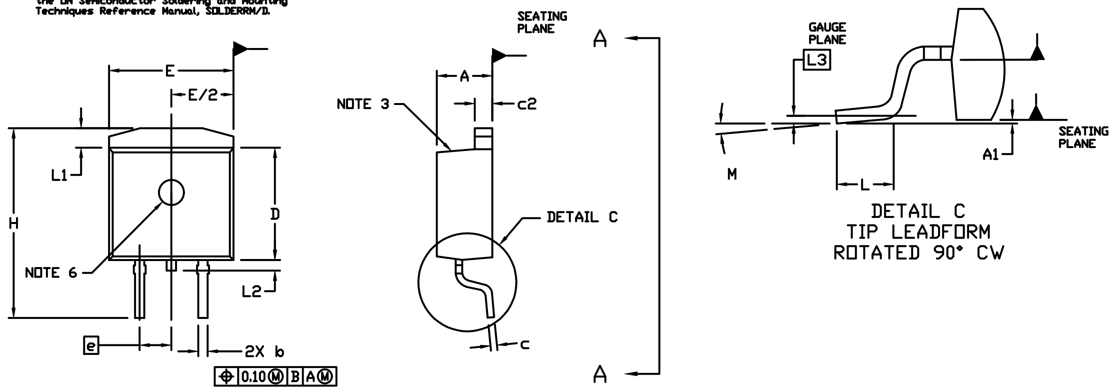
RECOMMENDED MOUNTING FOOTPRINT

* For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

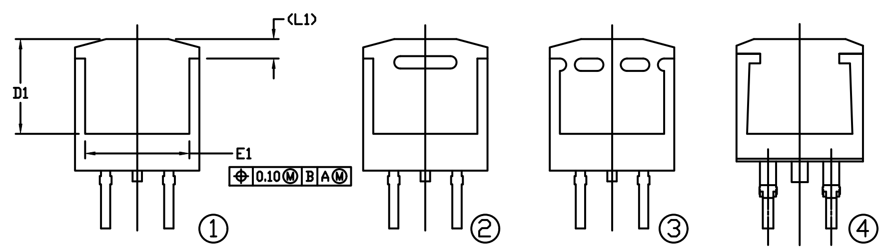
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: INCHES
3. CHAMFER OPTIONAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005 PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
5. THERMAL PAD CONTOUR IS OPTIONAL WITHIN DIMENSIONS E, L1, D1, AND E1.
6. OPTIONAL MOLD FEATURE.
7. ①, ② ... OPTIONAL CONSTRUCTION FEATURE CALL OUTS.

DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.160	0.190	4.06	4.83
A1	0.000	0.010	0.00	0.25
b	0.020	0.039	0.51	0.99
c	0.012	0.029	0.30	0.74
c2	0.045	0.065	1.14	1.65
D	0.330	0.380	8.38	9.65
D1	0.260	---	6.60	---
E	0.380	0.420	9.65	10.67
E1	0.245	---	6.22	---
e	0.100 BSC		2.54 BSC	
H	0.575	0.625	14.60	15.88
L	0.070	0.110	1.78	2.79
L1	---	0.066	---	1.68
L2	---	0.070	---	1.78
L3	0.010 BSC		0.25 BSC	
M	0°	8°	0°	8°



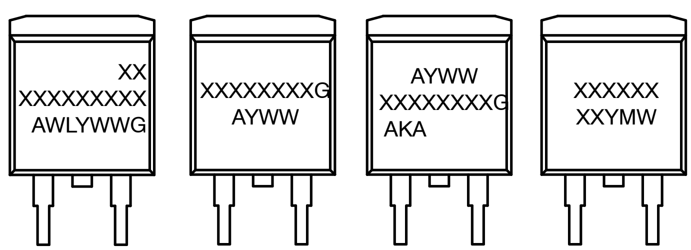
DETAIL C
TIP LEADFORM
ROTATED 90° CW



VIEW A−A

VIEW A−A
OPTIONAL CONSTRUCTIONS

GENERIC MARKING DIAGRAMS*



IC **Standard** **Rectifier** **SSG**

XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
W = Week Code (SSG)
M = Month Code (SSG)
G = Pb−Free Package
AKA = Polarity Indicator

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**D^2PAK−3 (TO−263, 3−LEAD)**	**PAGE 1 OF 1**

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