

AD7528

Advanced LinCMOS™ DUAL 8-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTER

D3112, JULY 1988

- Advanced LinCMOS™ Silicon-Gate Technology
- Easily Interfaced to Microprocessors
- On-Chip Data Latches
- Monotonic Over the Entire A/D Conversion Range
- Designed to be Interchangeable with Analog Devices AD7528 and PMI PM-7528
- Fast Control Signaling for Digital Signal Processor Applications Including Interface with TMS320

KEY PERFORMANCE SPECIFICATIONS	
Resolution	8 bits
Linearity Error	1/2 LSB
Power Dissipation at $V_{DD} = 5\text{ V}$	5 mW
Settling Time at $V_{DD} = 5\text{ V}$	100 ns
Propagation Delay at $V_{DD} = 5\text{ V}$	80 ns

description

The AD7528 is a dual 8-bit digital-to-analog converter designed with separate on-chip data latches and featuring excellent DAC-to-DAC matching. Data is transferred to either of the two DAC data latches via a common 8-bit input port. Control input $\overline{\text{DACA/DACB}}$ determines which DAC is to be loaded. The "load" cycle of the AD7528 is similar to the "write" cycle of a random-access memory, allowing easy interface to most popular microprocessor busses and output ports. Segmenting the high-order bits minimizes glitches during changes in the most significant bits, where glitch impulse is typically the strongest.

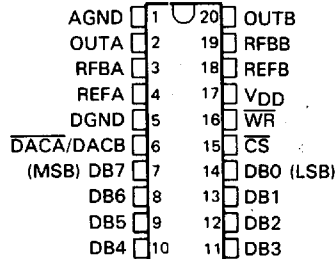
The AD7528 operates from a 5-V to 15-V power supply and dissipates less than 15 mW (typical). Excellent 2- or 4-quadrant multiplying makes the AD7528 a sound choice for many microprocessor-controlled gain-setting and signal-control applications.

The AD7528B is characterized for operation from -25°C to 85°C . The AD7528K is characterized for operation from 0°C to 70°C .

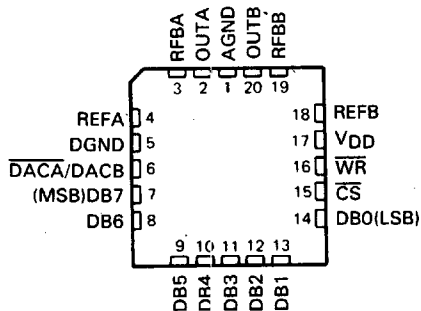
AVAILABLE OPTIONS

DEVICE	SYMBOLIZATION		OPERATING TEMPERATURE RANGE
	PACKAGE	SUFFIX	
AD7528B	FN, N		-25°C to 85°C
AD7528K	FN, N		0°C to 70°C

N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



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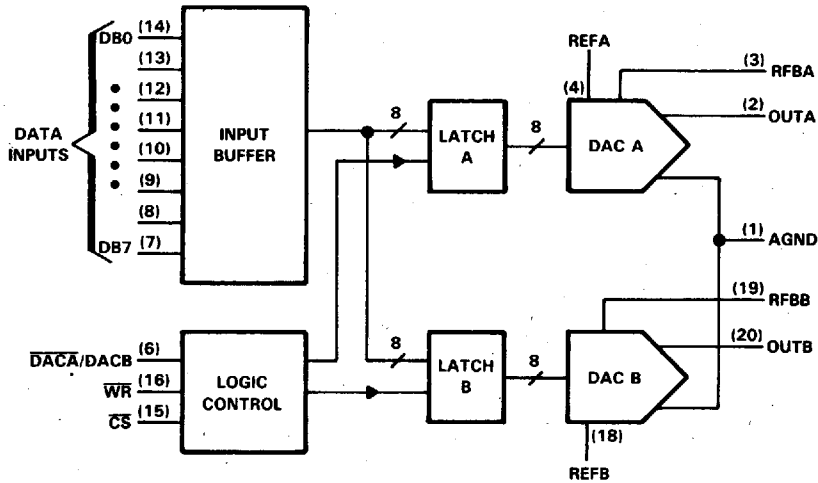
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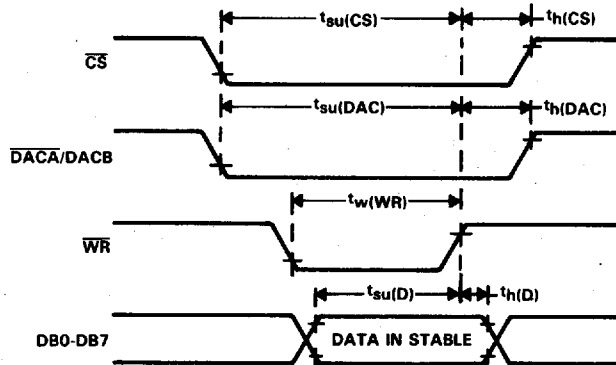
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functional block diagram



operating sequence



T-51-09-08 AD7528

Advanced LinCMOS™ DUAL 8-BIT MULTIPLYING
DIGITAL-TO-ANALOG CONVERTER**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

Supply voltage, V_{DD} (to AGND or DGND)	-0.3 V to 17 V
Voltage between AGND and DGND	$\pm V_{DD}$
Input voltage, V_I (to DGND)	-0.3 V to $V_{DD} + 0.3$ V
Reference voltage, V_{refA} or V_{refB} (to AGND)	± 25 V
Feedback voltage, V_{RFBA} or V_{RFBB} (to AGND)	± 25 V
Output voltage, V_{OA} or V_{OB} (to AGND)	± 25 V
Peak input current	10 μ A
Operating free-air temperature range: AD7528B	-25°C to 85°C
AD7528K	0°C to 70°C
Storage temperature range	-65°C to 150°C
Case temperature for 10 seconds: FN package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package	260°C

recommended operating conditions

	$V_{DD} = 4.75$ V to 5.25 V			$V_{DD} = 14.5$ V to 15.5 V			UNIT	
	MIN	NOM	MAX	MIN	NOM	MAX		
Reference voltage, V_{refA} or V_{refB}	± 10			± 10			V	
High-level input voltage, V_{IH}	2.4			13.5			V	
Low-level input voltage, V_{IL}	0.8			1.5			V	
\overline{CS} setup time, $t_{su}(CS)$	50			50			ns	
\overline{CS} hold time, $t_h(CS)$	0			0			ns	
DAC select setup time, $t_{su}(DAC)$	50			50			ns	
DAC select hold time, $t_h(DAC)$	10			10			ns	
Data bus input setup time $t_{su}(D)$	25			25			ns	
Data bus input hold time $t_h(D)$	0			0			ns	
Pulse duration, \overline{WR} low, $t_w(WR)$	50			50			ns	
Operating free-air temperature, T_A	AD7528B	-25		85		85		°C
	AD7528K	0		70		70		

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electrical characteristics over recommended operating temperature range, $V_{refA} = V_{refB} = 10\text{ V}$,
 VOA and VOB at 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		$V_{DD} = 5\text{ V}$		$V_{DD} = 15\text{ V}$		UNIT
				MIN	MAX	MIN	MAX	
I_{IH}	High-level input current	$V_I = V_{DD}$	Full Range	10	10	μA		
			25°C	1	1			
I_{IL}	Low-level input current	$V_I = 0$	Full Range	-10	-10	μA		
			25°C	-1	-1			
Reference input impedance (Pin 15 to GND)				8	15	8	15	$\text{k}\Omega$
I_{kg}	Output leakage current	OUTA	DAC data latch loaded with 00000000, $V_{refA} = \pm 10\text{ V}$	Full Range	± 400	± 200	nA	
			25°C	± 50	± 50			
	OUTB	DAC data latch loaded with 00000000, $V_{refB} = \pm 10\text{ V}$	Full Range	± 400	± 200			
		25°C	± 50	± 50				
Input resistance match (REFA to REFB)				$\pm 1\%$	$\pm 1\%$			
DC supply sensitivity $\Delta\text{gain}/\Delta V_{DD}$		$V_{DD} = \pm 10\%$	Full Range	0.04	0.02	%/%		
			25°C	0.02	0.01			
I_{DD}	Supply current	Quiescent	DB0-DB7 at V_{IHmin} or V_{ILmax}	1	1	mA		
		Standby	DB0-DB7 at 0 V or V_{DD}	Full Range	0.5		0.5	
	25°C			0.1	0.1			
C_i	Input capacitance	DB0-DB7	$V_I = 0$ or V_{DD}	10	10	pF		
		\overline{WR} , \overline{CS} ,		15	15			
		$\overline{DACA}/\overline{DACB}$						
C_o	Output capacitance (OUTA, OUTB)	DAC Data latches loaded with 00000000	50	50	pF			
		DAC Data latches loaded with 11111111	120	120				



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operating characteristics over recommended operating free-air temperature range,
 $V_{refA} = V_{refB} = 10\text{ V}$, V_{OA} and V_{OB} at 0 V (unless otherwise noted)

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PARAMETER	TEST CONDITIONS		V _{DD} = 5 V		V _{DD} = 15 V		UNIT	
			MIN	TYP	MAX	MIN		TYP
Linearity error			±1/2		±1/2		LSB	
Setting time (to 1/2 LSB)	See Note 1		100		100		ns	
Gain error	See Note 2	Full Range	±4		±3		LSB	
		25°C	±2		±2			
AC feedthrough	REFA to OUTA	See Note 3	Full Range	-65		-65		dB
	REFB to OUTB		25°C	-70		-70		
Temperature coefficient of gain			0.007		0.0035		%FSR/°C	
Propagation delay (from digital input to 90% of final analog output current)	See Note 4		80		80		ns	
Channel-to-channel isolation	REFA to OUTB	See Note 5	77		77		dB	
	REFB to OUTA	See Note 6	77		77			
Digital-to-analog glitch impulse area	Measured for code transition from 00000000 to 11111111, T _A = 25°C		160		440		nVs	
Digital crosstalk glitch impulse area	Measured for code transition from 00000000 to 11111111, T _A = 25°C		30		60		nVs	
Harmonic distortion	V _I = 6 V, f = 1 kHz, T _A = 25°C		-85		-85		dB	

- NOTES: 1. OUTA, OUTB load = 100 Ω, C_{ext} = 13 pF; \overline{WR} and \overline{CS} at 0 V; DB0-DB7 at 0 V to V_{DD} or V_{DD} to 0 V.
 2. Gain error is measured using an internal feedback resistor. Nominal Full Scale Range (FSR) = V_{ref} - 1 LSB.
 3. V_{ref} = 20 V peak-to-peak, 100-kHz sine wave; DAC data latches loaded with 0000000.
 4. V_{refA} = V_{refB} = 10 V; OUTA/OUTB load = 100 Ω, C_{ext} = 13 pF; \overline{WR} and \overline{CS} at 0 V; DB0-DB7 at 0 V to V_{DD} or V_{DD} to 0 V.
 5. Both DAC latches loaded with 11111111; V_{refA} = 20 V peak-to-peak, 100-kHz sine wave; V_{refB} = 0.
 6. Both DAC latches loaded with 11111111; V_{refB} = 20 V peak-to-peak, 100-kHz sine wave; V_{refA} = 0.

principles of operation

The AD7528 contains two identical 8-bit multiplying D/A converters, DACA and DACB. Each DAC consists of an inverted R-2R ladder, analog switches, and input data latches. Binary-weighted currents are switched between DAC output and AGND, thus maintaining a constant current in each ladder leg independent of the switch state. Most applications require only the addition of an external operational amplifier and voltage reference. A simplified D/A circuit for DACA with all digital inputs low is shown in Figure 1.

Figure 2 shows the DACA equivalent circuit. A similar equivalent circuit can be drawn for DACB. Both DACs share the analog ground pin 1 (AGND). With all digital inputs high, the entire reference current flows to OUTA. A small leakage current (I_{kg}) flows across internal junctions, and as with most semiconductor devices, doubles every 10°C. C_O is due to the parallel combination of the NMOS switches and has a value that depends on the number of switches connected to the output. The range of C_O is 50 pF to 120 pF maximum. The equivalent output resistance r_O varies with the input code from 0.8R to 3R where R is the nominal value of the ladder resistor in the R-2R network.

Interfacing the AD7528 to a microprocessor is accomplished via the data bus, \overline{CS} , \overline{WR} , and $\overline{DACA/DACB}$ control signals. When \overline{CS} and \overline{WR} are both low, the AD7528 analog output, specified by the $\overline{DACA/DACB}$ control line, responds to the activity on the DB0-DB7 data bus inputs. In this mode, the input latches are transparent and input data directly affects the analog output. When either the \overline{CS} signal or \overline{WR} signal goes high, the data on the DB0-DB7 inputs is latched until the \overline{CS} and \overline{WR} signals go low again. When \overline{CS} is high, the data inputs are disabled regardless of the state of the \overline{WR} signal.

The digital inputs of the AD7528 provide TTL compatibility when operated from a supply voltage of 5 V. The AD7528 may be operated with any supply voltage in the range from 5 V to 15 V, however, input logic levels are not TTL compatible above 5 V.

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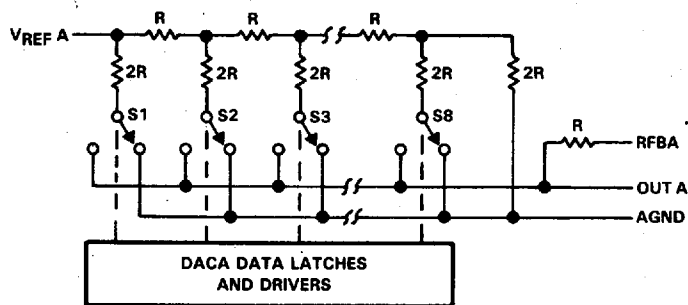


FIGURE 1. SIMPLIFIED FUNCTIONAL CIRCUIT FOR DAC A

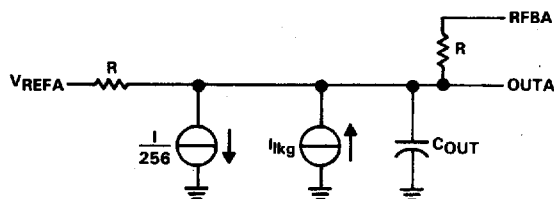


FIGURE 2. AD7528 EQUIVALENT CIRCUIT, DAC LATCH LOADED WITH 11111111.

MODE SELECTION TABLE

DACA/ DACB	CS	WR	DACA	DACB
L	L	L	WRITE	HOLD
H	L	L	HOLD	WRITE
X	H	X	HOLD	HOLD
X	X	H	HOLD	HOLD

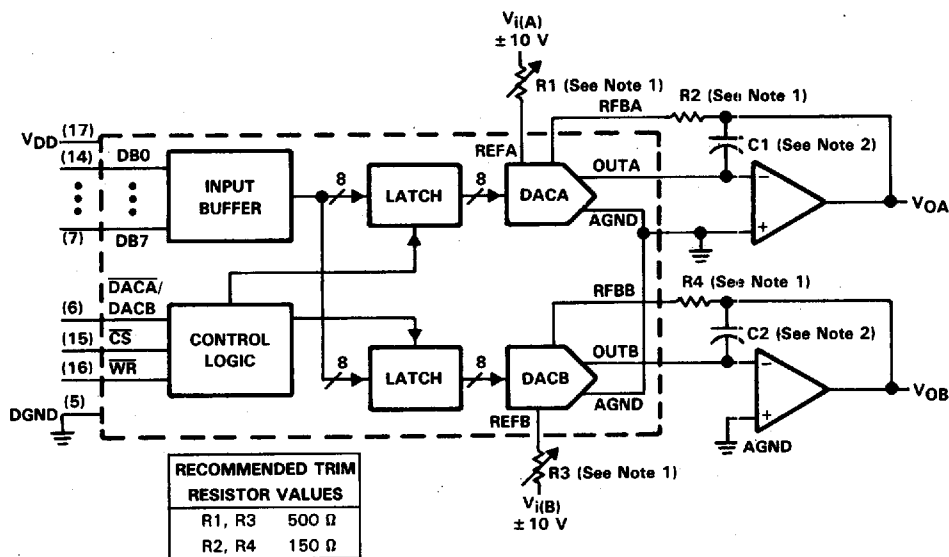
L = low level, H = high level, X = don't care

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TYPICAL APPLICATION DATA

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The AD7528 is capable of performing 2-quadrant or full 4-quadrant multiplication. Circuit configurations for 2-quadrant and 4-quadrant multiplication are shown in Figures 3 and 4. Input coding for unipolar and bipolar operation are summarized in Tables 1 and 2, respectively.



- NOTES: 1. R1, R2, R3, and R4 are used only if gain adjustment is required. See table for recommended values. Make gain adjustment with digital input of 255.
2. C1 and C2 phase compensation capacitors (10 pF to 15 pF) are required when using high-speed amplifiers to prevent ringing or oscillation.

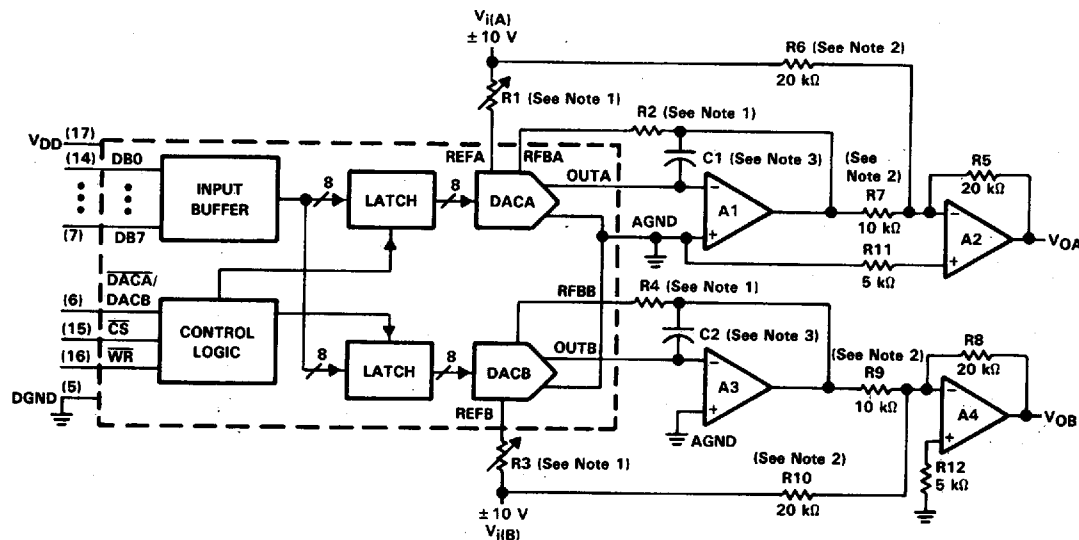
FIGURE 3. UNIPOLAR OPERATION (2-QUADRANT MULTIPLICATION)

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TYPICAL APPLICATION DATA



- NOTES: 1. R1, R2, R3, and R4 are used only if gain adjustment is required. See table in Figure 3 for recommended values. Adjust R1 for $V_{OA} = 0$ V with code 10000000 in DACA latch. Adjust R3 for $V_{OB} = 0$ V with 10000000 in DACB latch.
2. Matching and tracking are essential for resistor pairs R6, R7, R9, and R10.
3. C1 and C2 phase compensation capacitors (10 pF to 15 pF) may be required if A1 and A3 are high-speed amplifiers.

FIGURE 4. BIPOLAR OPERATION (4-QUADRANT OPERATION)

TABLE 1. UNIPOLAR BINARY CODE

DAC LATCH CONTENTS		ANALOG OUTPUT
MSB	LSB [†]	
11111111		$-V_i (255/256)$
10000001		$-V_i (129/256)$
10000000		$-V_i (128/256) = -V_i/2$
01111111		$-V_i (127/256)$
00000001		$-V_i (1/256)$
00000000		$-V_i (0/256) = 0$

$$^{\dagger} 1 \text{ LSB} = (2^{-8})V_i$$

TABLE 2. BIPOLAR (OFFSET BINARY) CODE

DAC LATCH CONTENTS		ANALOG OUTPUT
MSB	LSB [‡]	
11111111		$V_i (127/128)$
10000001		$V_i (1/128)$
10000000		0 V
01111111		$-V_i (1/128)$
00000001		$-V_i (127/128)$
00000000		$-V_i (128/128)$

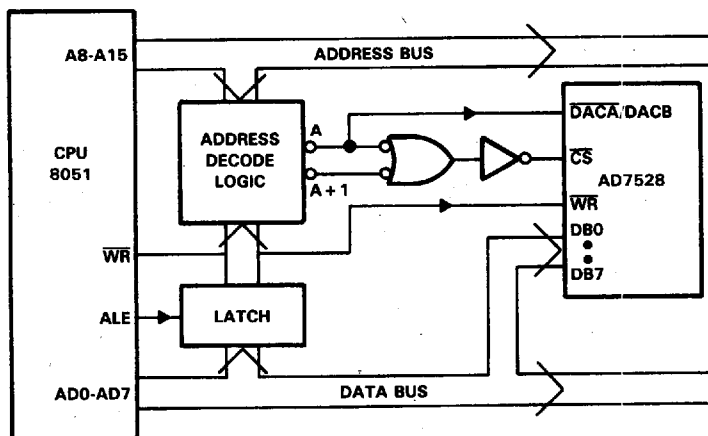
$$^{\ddagger} 1 \text{ LSB} = (2^{-7})V_i$$

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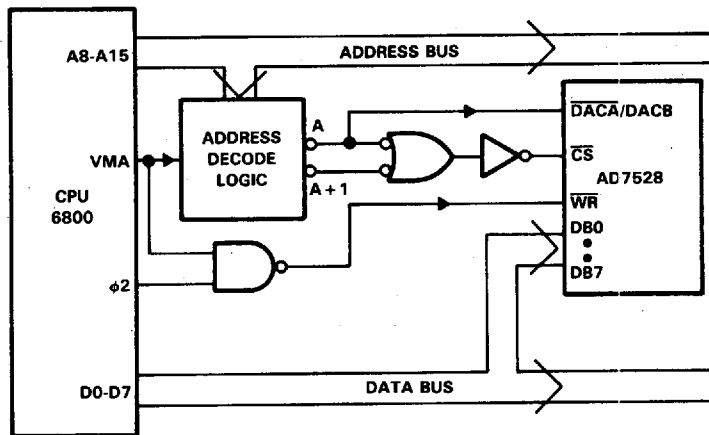
TYPICAL APPLICATION DATA

microprocessor interface information



NOTE: A = decoded address for AD7528 DACA.
 A+1 = decoded address for AD7528 DACB.

FIGURE 5. AD7528 – INTEL 8051 INTERFACE



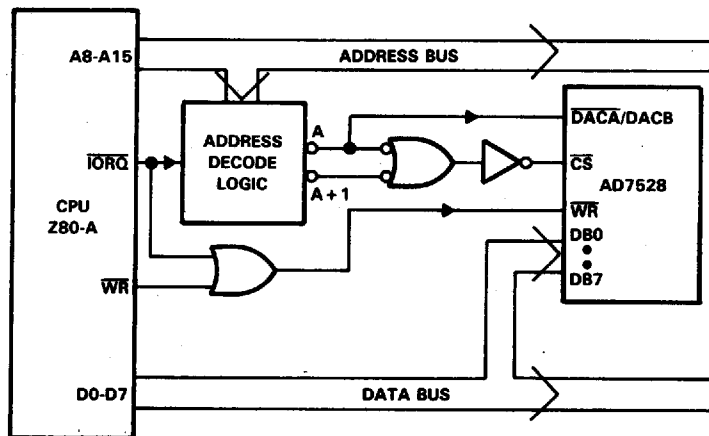
NOTE: A = decoded address for AD7528 DACA.
 A+1 = decoded address for AD7528 DACB.

FIGURE 6. AD7528 – 6800 INTERFACE

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TYPICAL APPLICATION DATA



NOTE: A = decoded address for AD7528 DACA.
 A + 1 = decoded address for AD7528 DACB.

FIGURE 7. AD7528 TO Z-80A INTERFACE

programmable window detector

The programmable window comparator shown in Figure 8 will determine if voltage applied to the DAC feedback resistors are within the limits programmed into the AD7528 data latches. Input signal range depends on the reference and polarity, that is, the test input range is 0 to $-V_{ref}$. The DACA and DACB data latches are programmed with the upper and lower test limits. A signal within the programmed limits will drive the output high.

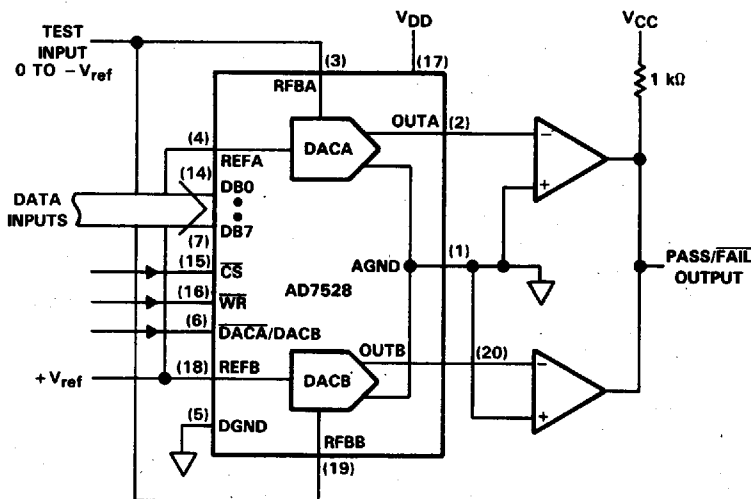


FIGURE 8. DIGITALLY PROGRAMMABLE WINDOW COMPARATOR (UPPER- AND LOWER-LIMIT TESTER)



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TYPICAL APPLICATION DATA

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digitally controlled signal attenuator

Figure 9 shows the AD7528 configured as a two-channel programmable attenuator. Applications include stereo audio and telephone signal level control. Table 3 shows input codes vs attenuation for a 0 to 15.5 dB range.

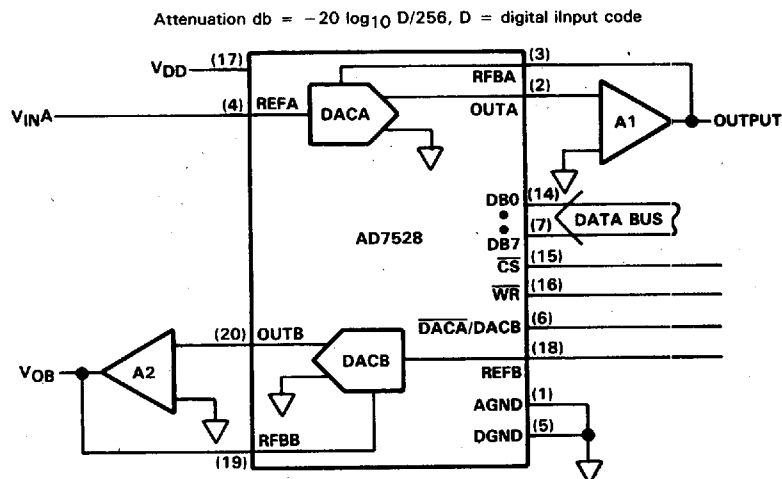


FIGURE 9. DIGITALLY CONTROLLED DUAL TELEPHONE ATTENUATOR

TABLE 3. ATTENUATION vs DACA, DACB CODE

ATTN(dB)	DAC INPUT CODE	CODE IN DECIMAL	ATTN(dB)	DAC INPUT CODE	CODE IN DECIMAL
0	11111111	255	8.0	01100110	102
0.5	11110010	242	8.5	01100000	96
1.0	11100100	228	9.0	01011011	91
1.5	11010111	215	9.5	01010110	86
2.0	11001011	203	10.0	01010001	81
2.5	11000000	192	10.5	01001100	76
3.0	10110101	181	11.0	01001000	72
3.5	10101011	171	11.5	01000100	68
4.0	10100010	162	12.0	01000000	64
4.5	10011000	152	12.5	00111101	61
5.0	10010000	144	13.0	00111001	57
5.5	10001000	136	13.5	00110110	54
6.0	10000000	128	14.0	00110011	51
6.5	01111001	121	14.5	00110000	48
7.0	01110010	114	15.0	00101110	46
7.5	01101100	108	15.5	00101011	43

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TYPICAL APPLICATION DATA

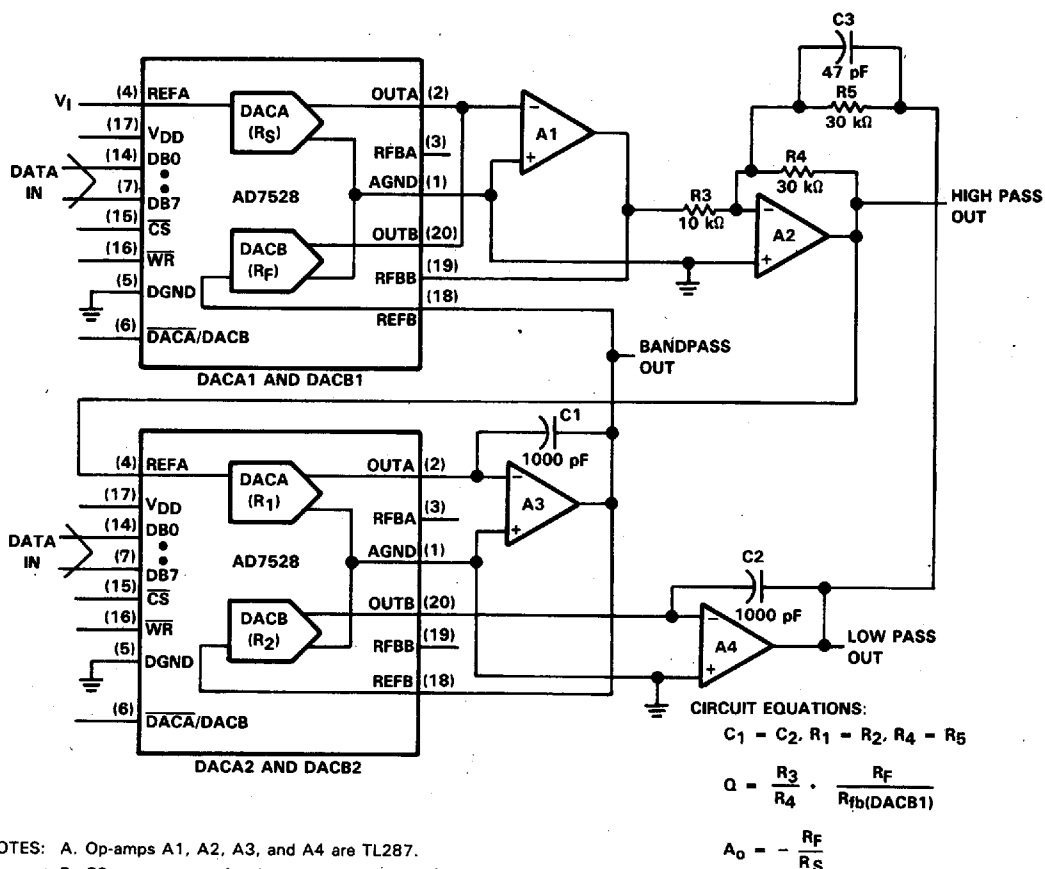
programmable state-variable filter

This programmable state-variable or universal filter configuration provides low-pass, high-pass, and band-pass outputs, and is suitable for applications in which microprocessor control of filter parameters is required.

As shown in Figure 10, DACA1 and DACB1 control the gain and Q of the filter while DACA2 and DACB2 control the cutoff frequency. Both halves of the DACA2 and DACB2 must track accurately in order for the cutoff-frequency equation to be true. With the AD7528, this is easily achieved.

$$f_c = \frac{1}{2\pi R_1 C_1}$$

The programmable range for the cutoff or center frequency is 0 to 15 kHz with a Q ranging from 0.3 to 4.5. This defines the limits of the component values.



- NOTES: A. Op-amps A1, A2, A3, and A4 are TL287.
 B. C3 compensates for the op-amp gain-bandwidth limitations.
 C. DAC equivalent resistance equals $\frac{256 \times (\text{DAC ladder resistance})}{\text{DAC digital code}}$

FIGURE 10. DIGITALLY CONTROLLED STATE-VARIABLE FILTER

