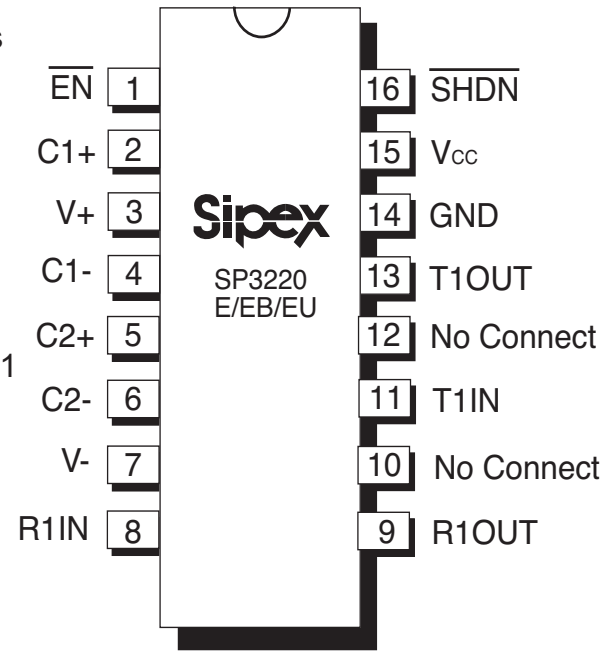
SP3220E/EB/EU

+3.0V to +5.5V RS-232 Driver/Receiver Pair

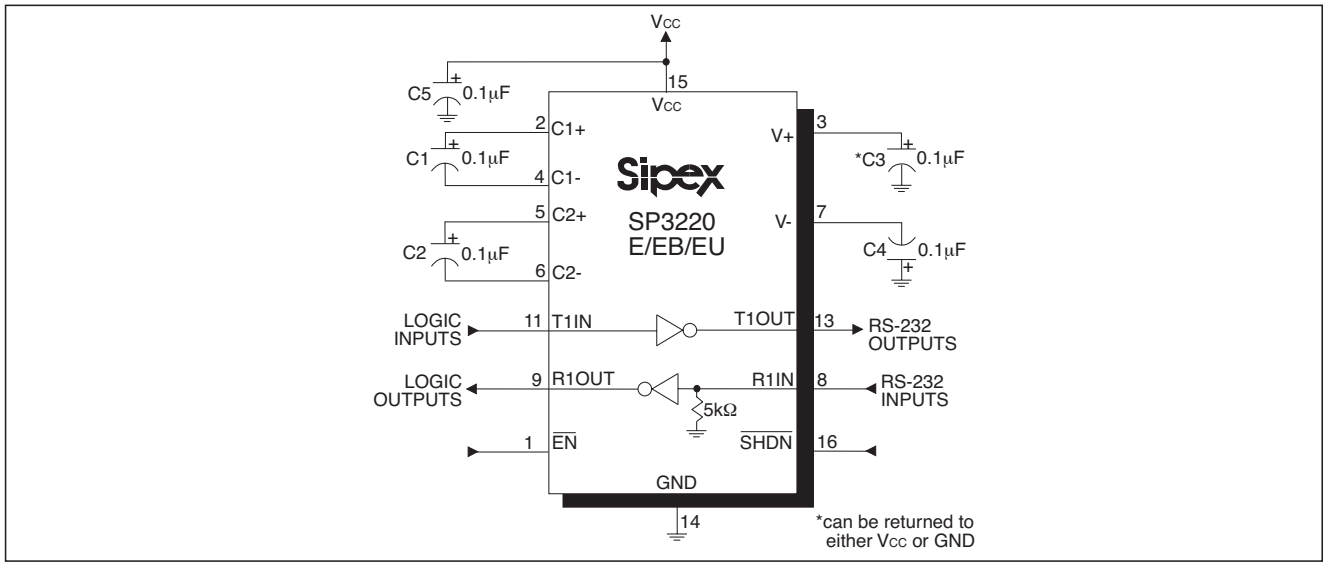
- Meets All EIA-232 and ITU V.28 Specifications from a wide +3.0V to +5.5V power supply
  - Interoperable with RS232 and V.28 at 2.7V
- Supports High Serial DataRates:
  - 120 kbps SP3220E
  - 250 kbps SP3220EB
  - 1 Mbps SP3220EU
- 1μA Low Power Shutdown Mode
- Footprint Compatible with MAX3221E, ISL3221
- 4 x 0.1μF External Charge Pump Capacitors
- Tri–State/Receiver Enable
- Improved ESD Specifications:
  - +15kV Human Body Model
  - +15kV IEC1000-4-2 Air Discharge
  - +8kV IEC1000-4-2 Contact Discharge



Available in Lead Free Packaging

DESCRIPTION

The **SP3220E** devices are RS-232 driver/receiver solutions intended for portable or hand-held applications such as palmtop computers, instrumentation and consumer products. These devices incorporate a high-efficiency charge-pump power supply that allows the **SP3220E** devices to deliver true RS-232 performance from a single power supply ranging from +3.0V to +5.0V. This charge pump requires only 0.1μF capacitors in 3.3V operation. The ESD tolerance of these devices is over ±15kV for both Human Model and IEC1000-4-2 Air discharge test methods. All devices have a low-power shutdown mode where the driver outputs and charge pumps are disabled. During shutdown, the supply current falls to less than 1μA.



ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability and cause permanent damage to the device.

V_{CC}.....-0.3V to +6.0V
V+ (NOTE 1).....-0.3V to +7.0V
V- (NOTE 1).....+0.3V to -7.0V
V+ + |V-| (NOTE 1).....+13V

I_{CC} (DC V_{CC} or GND current).....±100mA

Input Voltages
TxIN, $\overline{EN}$, $\overline{SHUTDOWN}$ ..... -0.3V to V_{CC} +0.3V
RxIN ..... ±25V

Output Voltages
TxOUT ..... ±13.2V
RxOUT ..... -0.3V to (V_{CC}+0.3V)

Short-Circuit Duration
TxOUT ..... Continuous

Storage Temperature ..... -65°C to +150°C

Power Dissipation Per Package
16-pin SSOP (derate 9.69mW/°Cabove+70°C) 775mW
16-pin TSSOP (derate 10.5mW/°C above +70°C) 840mW
16-pin Wide SOIC (derate 11.2mW/°C above+70°C) 900mW

NOTE 1: V+ and V- can have maximum magnitudes of 7V, but their absolute difference cannot exceed 13V.

SPECIFICATIONS

Unless otherwise noted, the following specifications apply for V_{CC} = +3.0V to +5.0V with T_{AMB} = T_{MIN} to T_{MAX}. Typical Values apply at V_{CC} = +3.3V or +5.0V and T_{AMB} = 25°C, C1-4=0.1µF.

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
DC CHARACTERISTICS					
Supply Current		0.3	1.0	mA	no load, T_{AMB} = +25°C, V_{CC} = 3.3V, TxIN = GND or V_{CC}
Shutdown Supply Current		1.0	10	µA	$\overline{SHDN}$ = GND, T_{AMB} = +25°C, V_{CC} = +3.3V, TxIN = GND or V_{CC}
LOGIC INPUTS AND RECEIVER OUTPUTS					
Input Logic Threshold LOW	GND		0.8	V	TxIN, $\overline{EN}$, $\overline{SHDN}$, Note 2
Input Logic Threshold HIGH	2.0			V	V_{CC} = 3.3V, Note 2
	2.4			V	V_{CC} = 5.0V, Note 2
Input Leakage Current		±0.01	±1.0	µA	TxIN, $\overline{EN}$, $\overline{SHDN}$, T_{AMB} = +25°C V_{IN} = GND to V_{CC}
Output Leakage Current		±0.05	±10	µA	Receivers Disabled V_{OUT} = GND to V_{CC}
Output Voltage LOW			0.4	V	I_{OUT} = 1.6mA
Output Voltage HIGH	V_{CC}-0.6	V_{CC}-0.1		V	I_{OUT} = -1.0mA
DRIVER OUTPUTS					
Output Voltage Swing	±5.0	±5.4		V	3kΩ load to ground at all driver outputs, T_{AMB} = +25°C
Output Resistance	300			Ω	V_{CC} = V+ = V- = GND, T_{OUT} = ±2V
Output Short-Circuit Current		±35	±60	mA	V_{OUT} = GND
Output Leakage Current			±25	µA	V_{OUT} = ±12V, V_{CC}= GND to 5.5V, drivers disabled

NOTE 2: Driver input hysteresis is typically 250mV.

SPECIFICATIONS (continued)

Unless otherwise noted, the following specifications apply for V_{CC} = +3.0V to +5.0V with T_{AMB} = T_{MIN} to T_{MAX}.
Typical Values apply at V_{CC} = +3.3V or +5.0V and T_{AMB} = 25°C, C1-4=0.1µF.

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
RECEIVER INPUTS					
Input Voltage Range	-25		+25	V	
Input Threshold LOW	0.6 0.8	1.2 1.5		V	V_{CC}=3.3V V_{CC}=5.0V
Input Threshold HIGH		1.5 1.8	2.4 2.4	V	V_{CC}=3.3V V_{CC}=5.0V
Input Hysteresis		0.3		V	
Input Resistance	3	5	7	kΩ	
TIMING CHARACTERISTICS					
Data Rate SP3220E	120	235		Kbps	R_L=3kΩ, C_L=1000pF, one driver switching
Data Rate SP3220EB	250			Kbps	R_L=3kΩ, C_L=1000pF
Data Rate SP3220EU	1000			Kbps	R_L=3kΩ, C_L= 250pF
Receiver Propagation Delay		0.15 0.15		µs µs	t_{PHL}, RxIN to RxOUT, C_L = 150pF t_{PHL}, RxIN to RxOUT, C_L = 150pF
Receiver Output Enable Time		200		ns	
Receiver Output Disable Time		200		ns	
Driver Skew		100		ns	$\lvert t_{PHL} - t_{PLH} \rvert$, T_{AMB} = 25°C
Receiver Skew		50		ns	$\lvert t_{PHL} - t_{PLH} \rvert$
Transition-Region Slew Rate		 90	30	V/µs V/µs	V_{CC} = 3.3V, R_L = 3KΩ, T_{AMB} = 25°C, measurements taken from -3.0V to +3.0V or +3.0V to -3.0V (SP3220E and EB) (SP3220EU)

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise noted, the following performance characteristics apply for V_{CC} = +3.3V, 250kbps data rates, all drivers loaded with 3kΩ, 0.1µF charge pump capacitors, and T_{AMB} = +25°C.

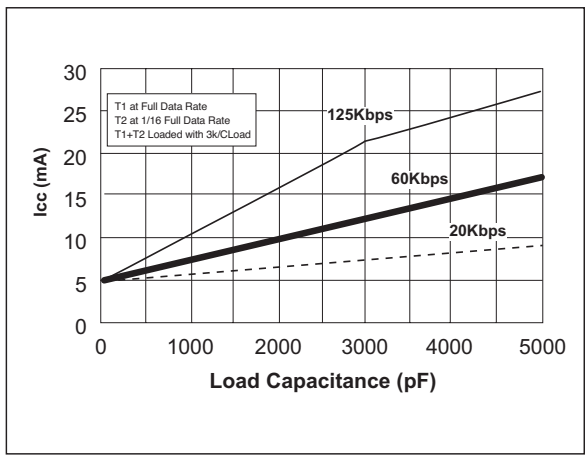


Figure 1. I_{CC} vs Load Capacitance for the SP3220EB.

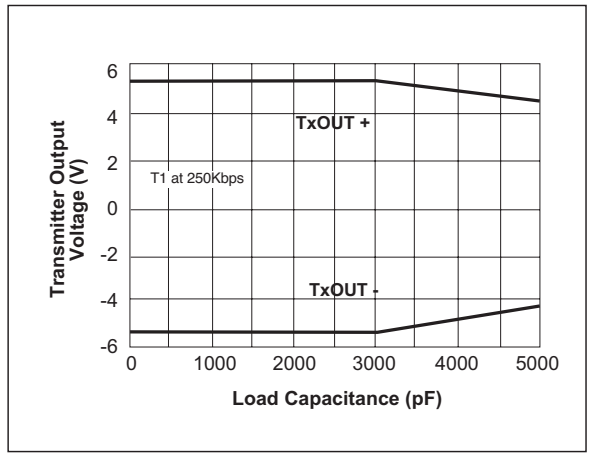


Figure 2. Transmitter Output Voltage vs Load Capacitance for the SP3220EB.

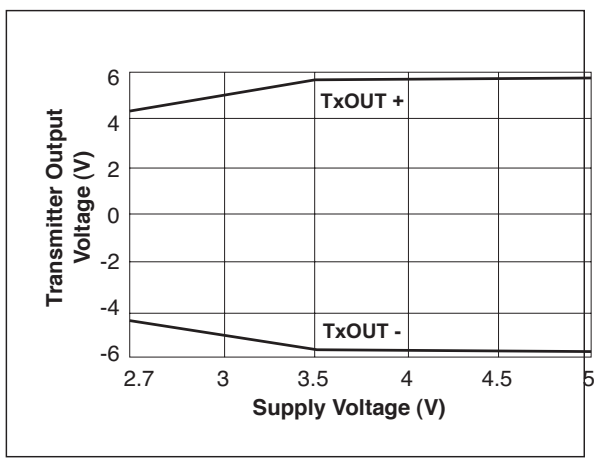


Figure 3. Transmitter Output Voltage vs Supply Voltage for the SP3220EB.

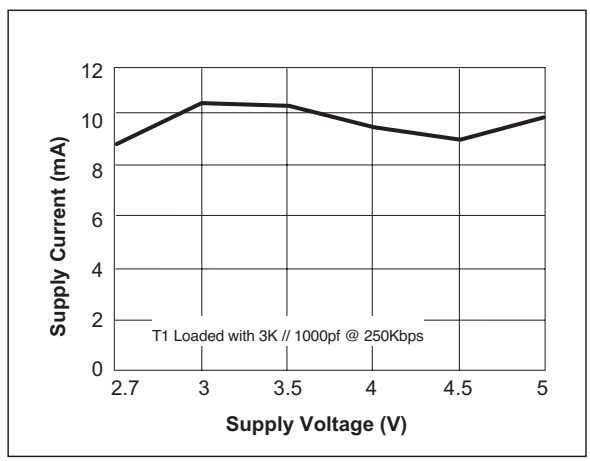


Figure 4. Supply Current vs Supply Voltage for the SP3220EB.

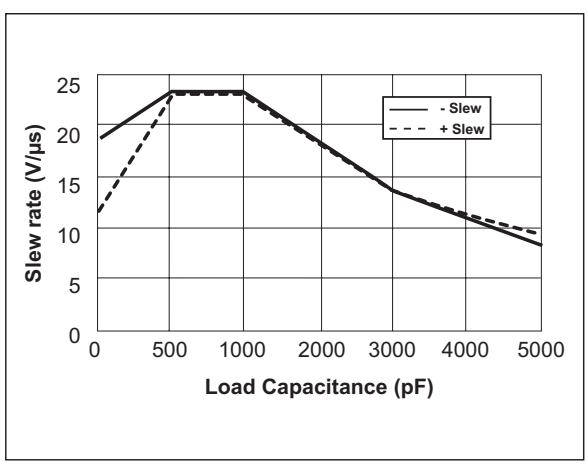


Figure 5. Slew Rate vs Load Capacitance for the SP3220EB.

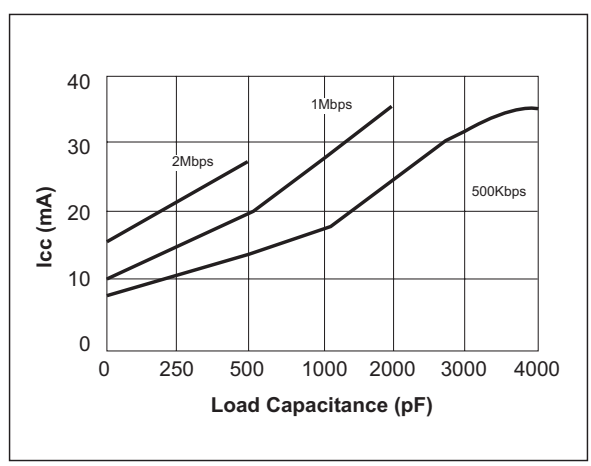


Figure 4. Supply Current vs Supply Voltage for the SP3220EU.

TYPICAL PERFORMANCE CHARACTERISTICS: Continued

Unless otherwise noted, the following performance characteristics apply for V_{CC} = +3.3V, 250kbps data rates, all drivers loaded with 3kΩ, 0.1µF charge pump capacitors, and T_{AMB} = +25°C.

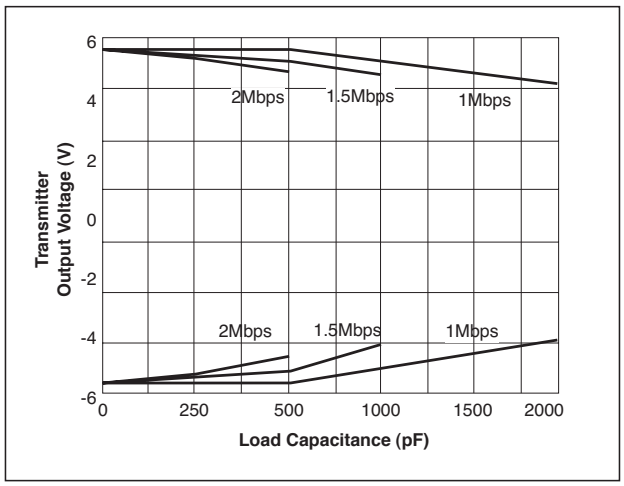


Figure 7. Transmitter Output Voltage vs Load Capacitance for the SP3220EU.

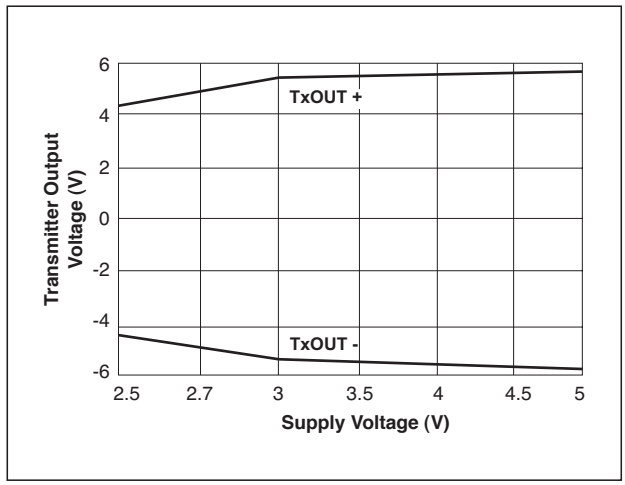


Figure 8. Transmitter Output Voltage vs Supply Voltage for the SP3220EU.

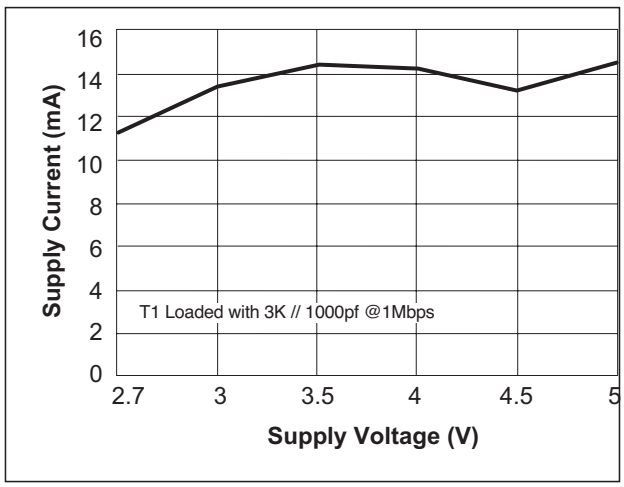


Figure 9. Supply Current vs Supply Voltage for the SP3220EU.

NAME	FUNCTION	PIN NUMBER
$\overline{EN}$	Receiver Enable Control. Drive LOW for normal operation. Drive HIGH to Tri-State the receiver outputs (high-Z state).	1
C1+	Positive terminal of the voltage doubler charge-pump capacitor.	2
V+	+5.5V generated by the charge pump.	3
C1-	Negative terminal of the voltage doubler charge-pump capacitor.	4
C2+	Positive terminal of the inverting charge-pump capacitor.	5
C2-	Negative terminal of the inverting charge-pump capacitor.	6
V-	-5.5V generated by the charge pump.	7
R1IN	RS-232 receiver input.	8
R1OUT	TTL/CMOS reciever output.	9
N.C.	No Connect.	10, 12
T1IN	TTL/CMOS driver input.	11
T1OUT	RS-232 driver output.	13
GND	Ground.	14
V_{CC}	+3.0V to +5.5V supply voltage	15
$\overline{SHDN}$	Shutdown Control Input. Drive HIGH for normal device operation. Drive LOW to shutdown the drivers (high-Z output) and the on-board charge pump power supply.	16

Table 1. Device Pin Description

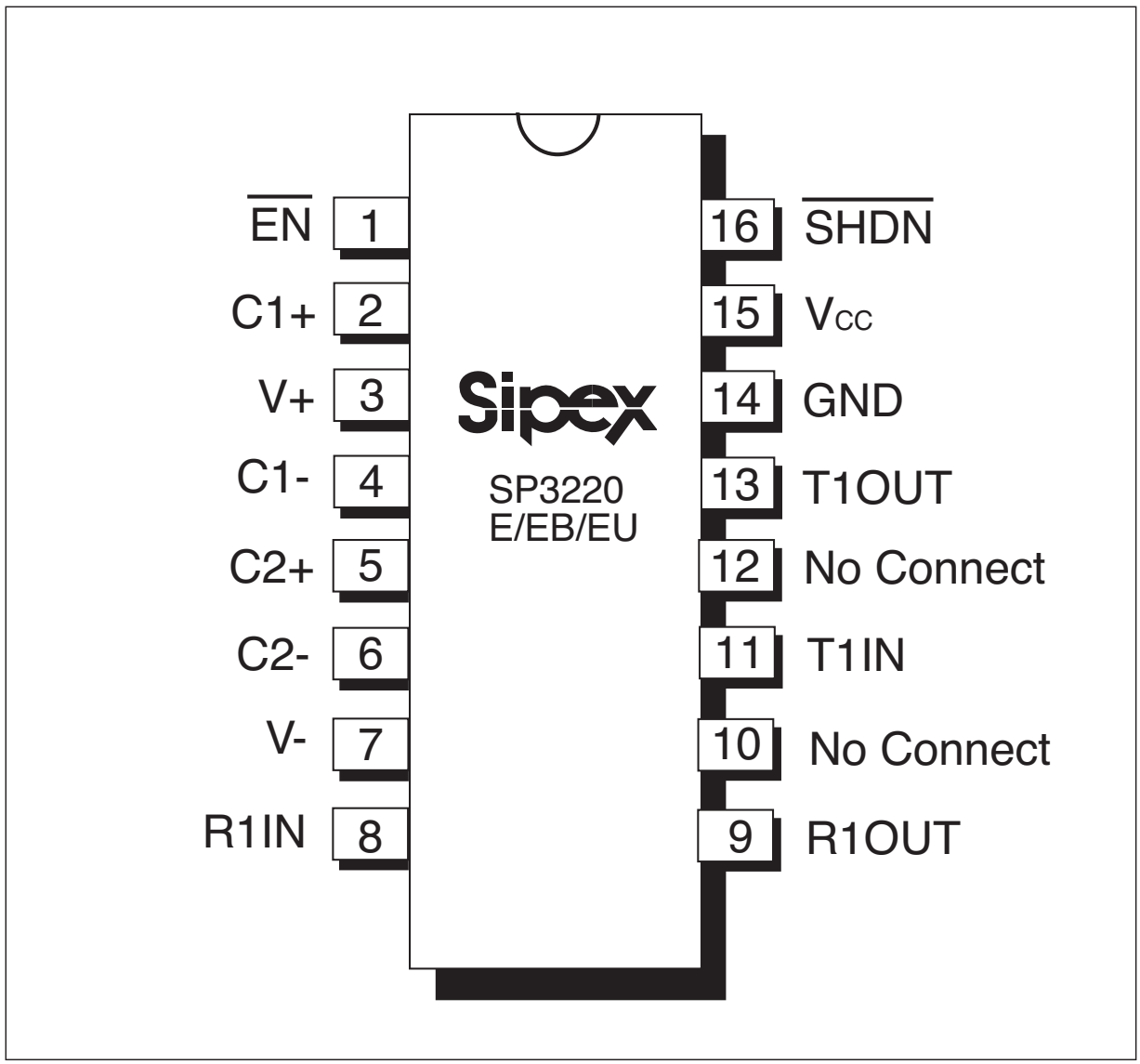


Figure 10. Pinout Configurations for the SP3220E/EB/EU

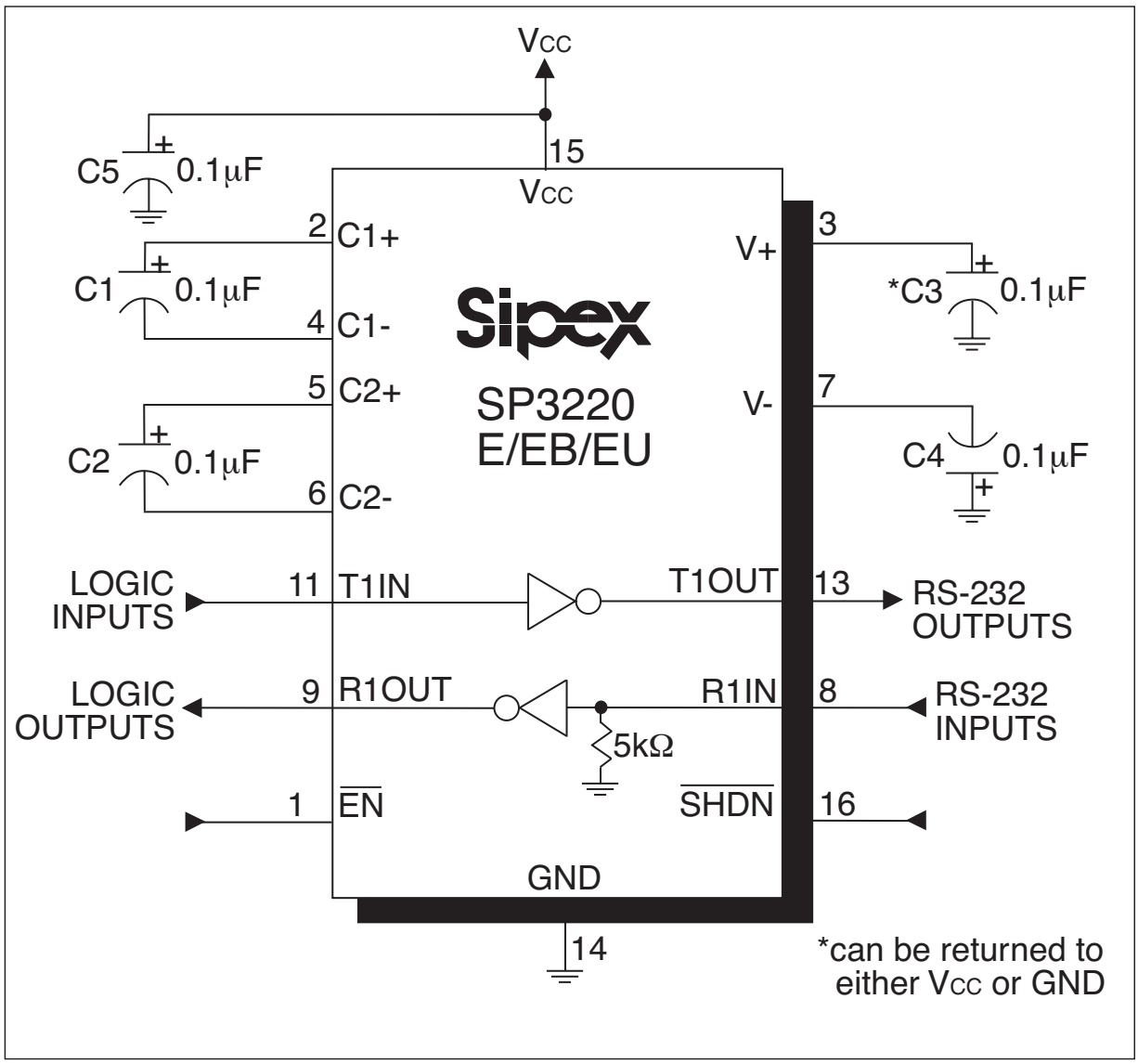


Figure 11. SP3220E/EB/EU Typical Operating Circuits

DESCRIPTION

The **SP3220E/EB/EU** devices meet the EIA/TIA-232 and V.28/V.24 communication protocols and can be implemented in battery-powered, portable, or hand-held applications such as notebook or palmtop computers. The **SP3220E/EB/EU** devices feature Sipex's proprietary on-board charge pump circuitry that generates 2 x V_{CC} for RS-232 voltage levels from a single +3.0V to +5.5V power supply. This series is ideal for +3.3V-only systems, mixed +3.0V to +5.5V systems, or +5.0V-only systems that require true RS-232 performance. The SP3220EB device has a driver that can operate at a data rate of 250Kbps fully loaded. The SP3220EU can operate at 1000Kbps; the SP3220E operates at a typical data rate of 235Kbps fully loaded.

The **SP3220E/EB/EU** is a 1-driver/1-receiver device ideal for portable or hand-held applications. The **SP3220E/EB/EU** features a 1μA shutdown mode that reduces power consumption and extends battery life in portable systems. Its receivers remains active in shutdown mode, allowing external devices to be monitored using only 1μA supply current.

THEORY OF OPERATION

The **SP3220E/EB/EU** devices are made up of three basic circuit blocks: 1. Driver, 2. Receiver, and 3. the Sipex proprietary charge pump.

Driver

The driver is an inverting level transmitter that converts TTL or CMOS logic levels to ±5.0V EIA/TIA-232 levels, inverted relative to the input logic levels. Typically, the RS-232 output voltage swing is ±5.5V with no load and at least ±5V minimum fully loaded. The driver outputs are protected against infinite short-circuits to ground without degradation in reliability. Driver outputs will meet EIA/TIA-562 levels of ±3.7V with supply voltages as low as 2.7V.

The SP3220EB driver typically can operate at a data rate of 250Kbps fully loaded with 3KΩ in parallel with 1000pF, ensuring compatibility with PC-to-PC communication software. The SP3220EU driver can guarantee a data rate of 1000Kbps fully loaded with 3Ω in parallel with 250pF.

The slew rate of the SP3220E and SP3220EB outputs are internally limited to a maximum of 30V/μs in order to meet the EIA standards (EIA RS-232D 2.1.7, Paragraph 5). The transition of the loaded output from HIGH to LOW also meets the monotonicity requirements of the standard. The slew rate of the SP3220EU is not internally limited. This allows it to transmit at much faster data rates.

Figure 12 shows a loopback circuit used to test the RS-232 driver. *Figure 13* shows the test results of the loopback circuit with the SP3220EB driver active at 250Kbps with an RS-232 load in parallel with a 1000pF capacitor. *Figure 14* shows the test results where the SP3220EU driver was active at 1000Kbps and loaded with an RS-232 receiver in parallel with a 250pF capacitor. A solid RS-232 data transmission rate of 250Kbps provides compatibility with many designs in personal computer peripherals and LAN applications.

The **SP3220E/EB/EU** driver's output stage is turned off (high-Z) when the device is in shutdown mode. When the power is off, the **SP3220E/EB/EU** device permits the outputs to be driven up to ±12V. The driver's input does not have pull-up resistors. Designers should connect an unused input to V_{CC} or GND.

In the shutdown mode, the supply current falls to less than 1μA, where $\overline{SHDN}$ = LOW. When the **SP3220E/EB/EU** device is shut down, the device's driver output is disabled (high-Z) and the charge pump is turned off with V+ pulled down to V_{CC} and V- pulled to GND. The time required to exit shutdown is typically 100ms. Connect $\overline{SHDN}$ to V_{CC} if the shutdown mode is not used. $\overline{SHDN}$ has no effect on RxOUT. Note that the driver is enabled only when the magnitude of V- exceeds approximately 3V.

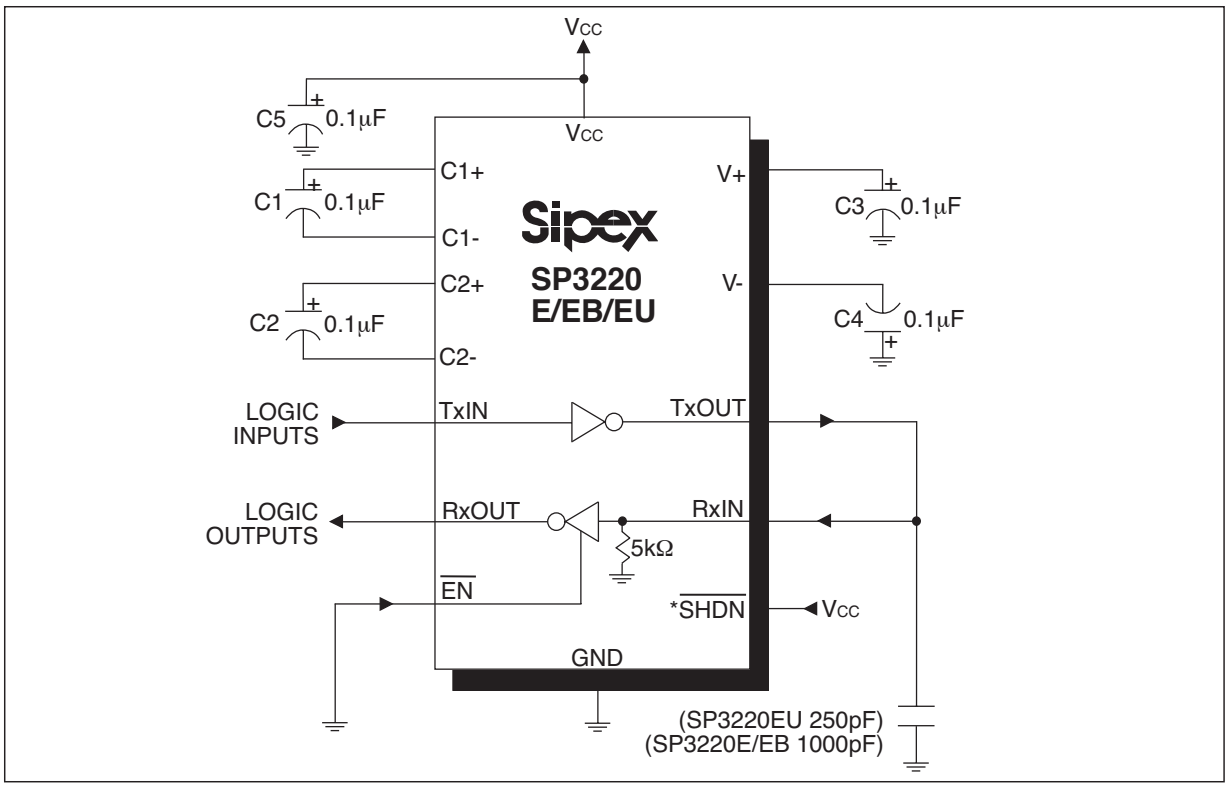


Figure 12. SP3220E/EB/EU Driver Loopback Test Circuit

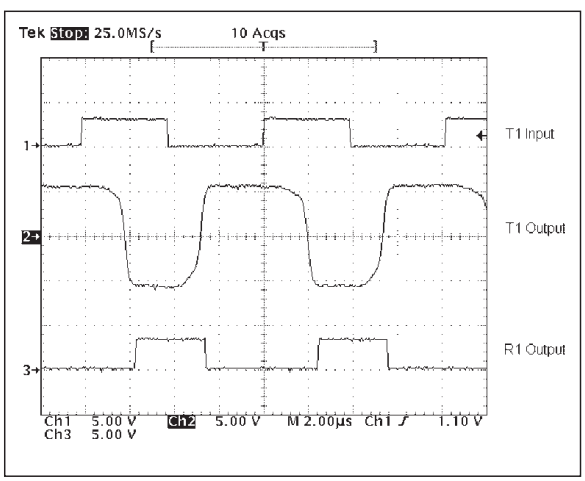


Figure 13. SP3220EB Driver Loopback Test Results at 250Kbps

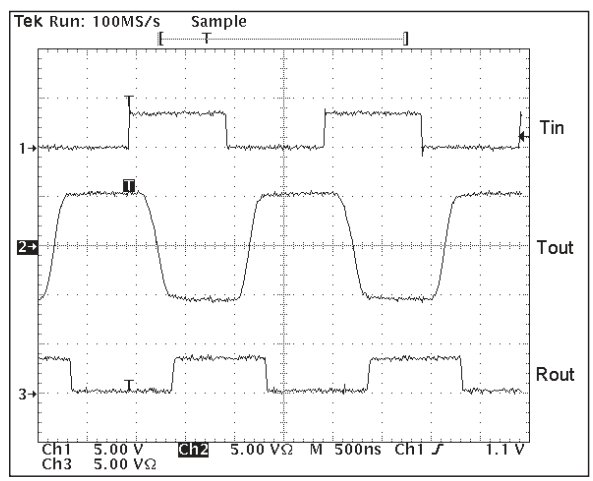


Figure 14. SP3220EU Driver Loopback Test Results at 1Mbps

Receivers

The receiver converts EIA/TIA-232 levels to TTL or CMOS logic output levels. The receiver has an inverting high-impedance output. This receiver output (RxOUT) is at high-impedance when the enable control $\overline{EN}$ = HIGH. In the shutdown mode, the receiver can be active or inactive. $\overline{EN}$ has no effect on TxOUT. The truth table logic of the **SP3220E/EB/EU** driver and receiver outputs can be found in *Table 2*.

Since receiver input is usually from a transmission line where long cable lengths and system interference can degrade the signal, the inputs have a typical hysteresis margin of 300mV. This ensures that the receiver is virtually immune to noisy transmission lines. Should an input be left unconnected, a 5kΩ pulldown resistor to ground will commit the output of the receiver to a HIGH state.

CHARGE PUMP

The charge pump is a **Sipex**–patented design (U.S. 5,306,954) and uses a unique approach compared to older less–efficient designs. The charge pump still requires four external capacitors, but uses a four–phase voltage shifting technique to attain symmetrical 5.5V power supplies. The internal power supply consists of a regulated dual charge pump that provides output voltages 5.5V regardless of the input voltage (V_{CC}) over the +3.0V to +5.5V range.

$\overline{SHDN}$	$\overline{EN}$	TxOUT	RxOUT
0	0	Tri-state	Active
0	1	Tri-state	Tri-state
1	0	Active	Active
1	1	Active	Tri-state

Table 2. Truth Table Logic for Shutdown and Enable Control

In most circumstances, decoupling the power supply can be achieved adequately using a 0.1μF bypass capacitor at C5 (*refer to Figure 11*). In applications that are sensitive to power-supply noise, decouple V_{CC} to ground with a capacitor of the same value as charge-pump capacitor C1. Physically connect bypass capacitors as close to the IC as possible.

The charge pumps operate in a discontinuous mode using an internal oscillator. If the output voltages are *less than* a magnitude of 5.5V, the charge pumps are *enabled*; if the output voltages *exceed* a magnitude of 5.5V, the charge pumps are *disabled*. This oscillator controls the four phases of the voltage shifting. A description of each phase follows.

Phase 1

— V_{SS} charge storage — During this phase of the clock cycle, the positive side of capacitors C_1 and C_2 are initially charged to V_{CC}. C_1^+ is then switched to GND and the charge in C_1^- is transferred to C_2^-. Since C_2^+ is connected to V_{CC}, the voltage potential across capacitor C_2 is now 2 times V_{CC}.

Phase 2

— V_{SS} transfer — Phase two of the clock connects the negative terminal of C_2 to the V_{SS} storage capacitor and the positive terminal of C_2 to GND. This transfers a negative generated voltage to C_3. This generated voltage is regulated to a minimum voltage of -5.5V. Simultaneous with the transfer of the voltage to C_3, the positive side of capacitor C_1 is switched to V_{CC} and the negative side is connected to GND.

Phase 3

— V_{DD} charge storage — The third phase of the clock is identical to the first phase — the charge transferred in C_1 produces $-V_{CC}$ in the negative terminal of C_1, which is applied to the negative side of capacitor C_2. Since C_2^+ is at V_{CC}, the voltage potential across C_2 is 2 times V_{CC}.

Phase 4

— V_{DD} transfer — The fourth phase of the clock connects the negative terminal of C_2 to GND, and transfers this positive generated voltage across C_2 to C_4, the V_{DD} storage capacitor. This voltage is regulated to +5.5V. At this voltage, the internal oscillator is disabled. Simultaneous with the transfer of the voltage to C_4, the positive side of capacitor C_1 is switched to V_{CC} and the negative side is connected to GND, allowing the charge pump cycle to begin again. The charge pump cycle will continue as long as the operational conditions for the internal oscillator are present.

In a no–load condition V^+ and V^- will be symmetrical, since both V^+ and V^- are separately generated from V_{CC}. Older charge pump approaches that generate V^- from V^+ will show a decrease in the magnitude of V^- compared to V^+ due to the inherent inefficiencies in the design.

CHARGE PUMP DESIGN GUIDELINES

The charge pump operates with 0.1μF capacitors for 3.3V operation. For other supply voltages, see the table for required capacitor values. Do not use values smaller than those listed. Increasing the capacitor values (e.g., by doubling in value) reduces ripple on the transmitter outputs and may slightly reduce power consumption. C2, C3, and C4 may be increased without changing C1's value.

Minimum recommended charge pump capacitor value	
Input Voltage Vcc	Charge pump Capacitor value for SP3220E/EB/EU
3.0V to 3.6V	C1 – C4 = 0.1uF
3.0V to 5.5V	C1 – C4 = 0.22uF

The charge pump oscillator typically operates at greater than 250kHz allowing the pump to run efficiently with small 0.1μF capacitors. Efficient operation depends on rapidly charging and discharging C_1 and C_2, therefore capacitors should be mounted close to the IC and have low ESR (equivalent series resistance).

Low cost surface mount ceramic capacitors (such as are widely used for power-supply decoupling) are ideal for use on the charge pump. However the charge pumps are designed to be able to function properly with a wide range of capacitor styles and values. If polarized capacitors are used the positive and negative terminals should be connected as shown in the Typical Operating Circuit.

Voltage potential across any of the capacitors will never exceed 2 x V_{CC}. Therefore capacitors with working voltages as low as 6.3V rating may be used with a 3.0V V_{CC} supply. The reference terminal of the V+ capacitor may be connected either to V_{CC} or ground, but if connected to ground a minimum 10V working voltage is required. Higher working voltages and/or capacitance values may be advised if operating at higher V_{CC} or to provide greater stability as the capacitors age.

Under lightly loaded conditions the intelligent pump oscillator maximizes efficiency by running only as needed to maintain V+ and V^-. Since interface transceivers often spend much of their time at idle, this power-efficient innovation can greatly reduce total power consumption. This improvement is made possible by the independent phase sequence of the **Sipex** charge-pump design.

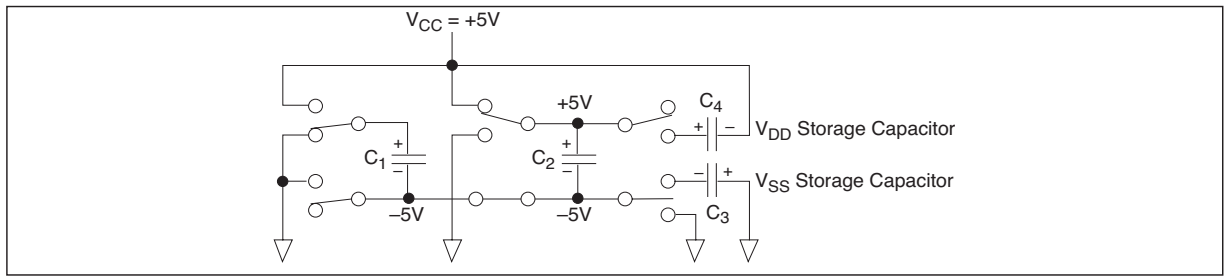


Figure 15. Charge Pump — Phase 1

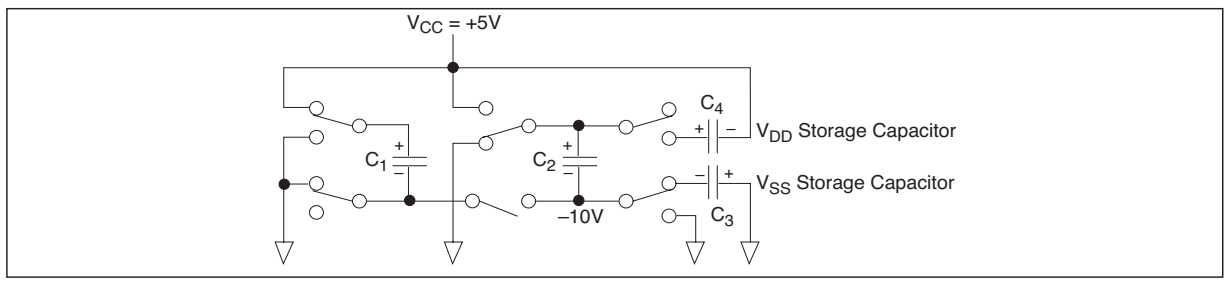


Figure 16. Charge Pump — Phase 2

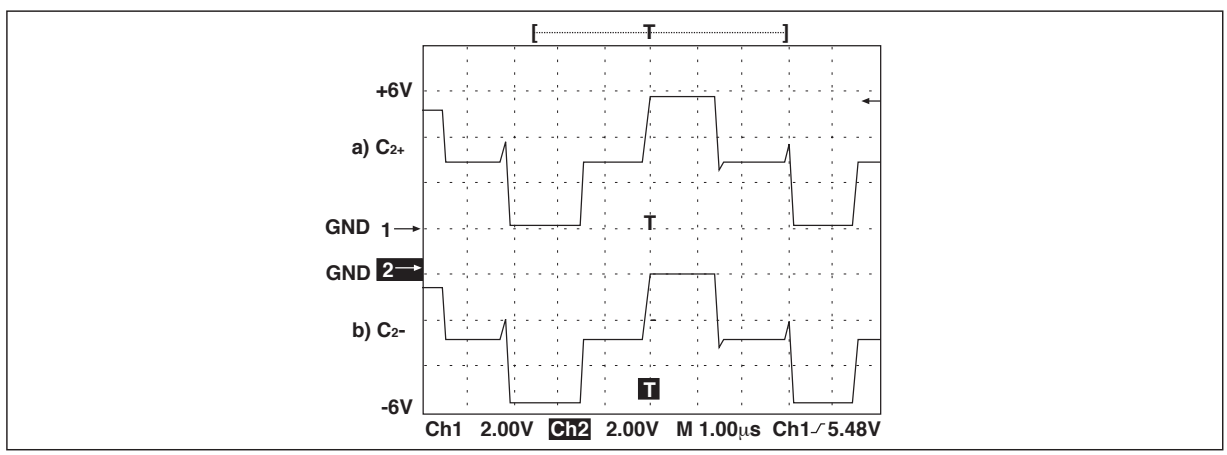


Figure 17. Charge Pump Waveforms

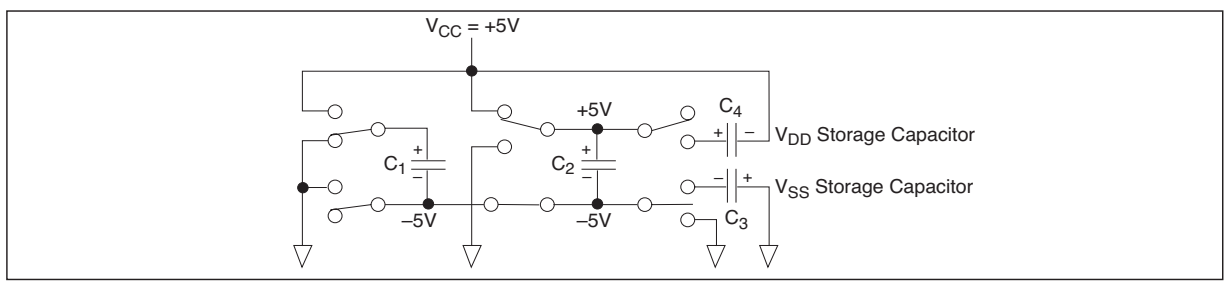


Figure 18. Charge Pump — Phase 3

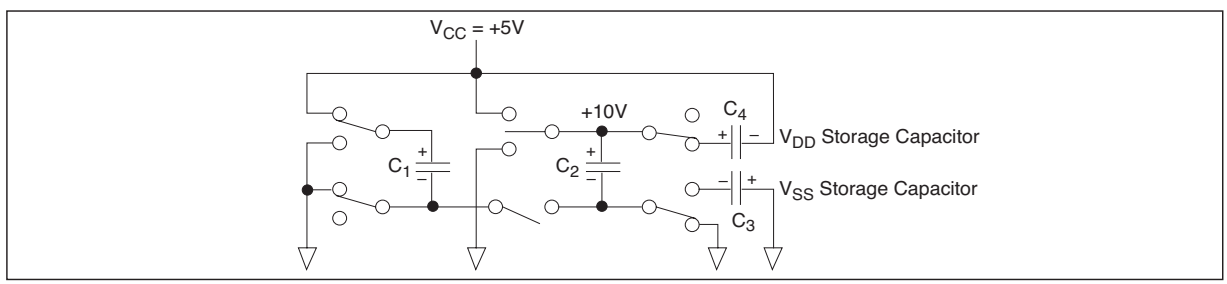


Figure 19. Charge Pump — Phase 4

ESD TOLERANCE

The **SP3220E/EB/EU** device incorporates ruggedized ESD cells on all driver output and receiver input pins. The ESD structure is improved over our previous family for more rugged applications and environments sensitive to electro-static discharges and associated transients. The improved ESD tolerance is at least ±15kV without damage nor latch-up.

There are different methods of ESD testing applied:

a) MIL-STD-883, Method 3015.7
b)IEC1000-4-2 Air Discharge
c)IEC1000-4-2 Direct Contact

The Human Body Model has been the generally accepted ESD testing method for semiconductors. This method is also specified in MIL-STD-883, Method 3015.7 for ESD testing. The premise of this ESD test is to simulate the human body's potential to store electro-static energy and discharge it to an integrated circuit. The simulation is performed by using a test model as shown in *Figure 20*. This method will test the IC's capability to withstand an ESD transient during normal handling such as in manufacturing areas where the ICs tend to be handled frequently.

The IEC-1000-4-2, formerly IEC801-2, is generally used for testing ESD on equipment and system manufacturers; they must guarantee a certain amount of ESD protection since the system itself is exposed to the outside environment and human presence. The premise with IEC1000-4-2 is that the system is required to withstand an amount of static electricity when ESD is applied to points and surfaces of the equipment that are accessible to personnel during normal usage. The transceiver IC receives most of the ESD current when the ESD source is applied to the connector pins. The test circuit for IEC-1000-4-2 is shown in *Figure 21*. There are two methods within IEC-4-2: the Air Discharge method and the Contact Discharge method.

With the Air Discharge Method, an ESD voltage is applied to the equipment under test (EUT) through air. This simulates an electrically charged person ready to connect a cable onto the rear of the system only to find an unpleasant zap just before the person touches the back panel. The high energy potential on the person discharges through an arcing path to the rear panel system before he or she even touches the system. This energy, whether discharged directly or through air, is predominantly a function of the discharge current rather than the discharge voltage.

Variables with an air discharge -- such as approach speed of the object carrying the ESD potential to the system and humidity -- will tend to change the discharge current. For example, the rise time of the discharge current varies with the approach speed.

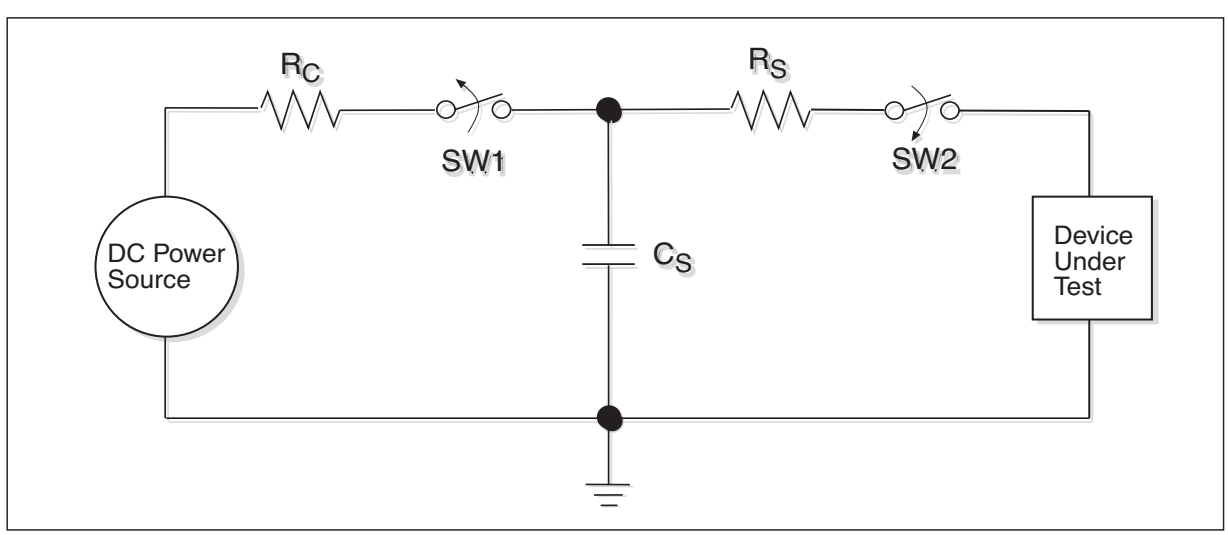


Figure 20. ESD Test Circuit for Human Body Model

The Contact Discharge Method applies the ESD current directly to the EUT. This method was devised to reduce the unpredictability of the ESD arc. The discharge current rise time is constant since the energy is directly transfered without the air-gap arc. In situations such as hand held systems, the ESD charge can be directly discharged to the equipment from a person in contact with the equipment. The current is transferred on to the keypad or the serial port of the equipment directly and then travels through the PCB and finally to the IC.

The circuit models in *Figure 20 and 21* represent the typical ESD testing circuits used for all three methods. The C_S is initially charged with the DC power supply when the first switch (SW1) is on. Now that the capacitor is charged, the second switch (SW2) is on while SW1 switches off. The voltage stored in the capacitor is then applied through R_S, the current limiting resistor, onto the device under test (DUT). In ESD tests, the SW2 switch is pulsed so that the device under test recives a duration of voltage.

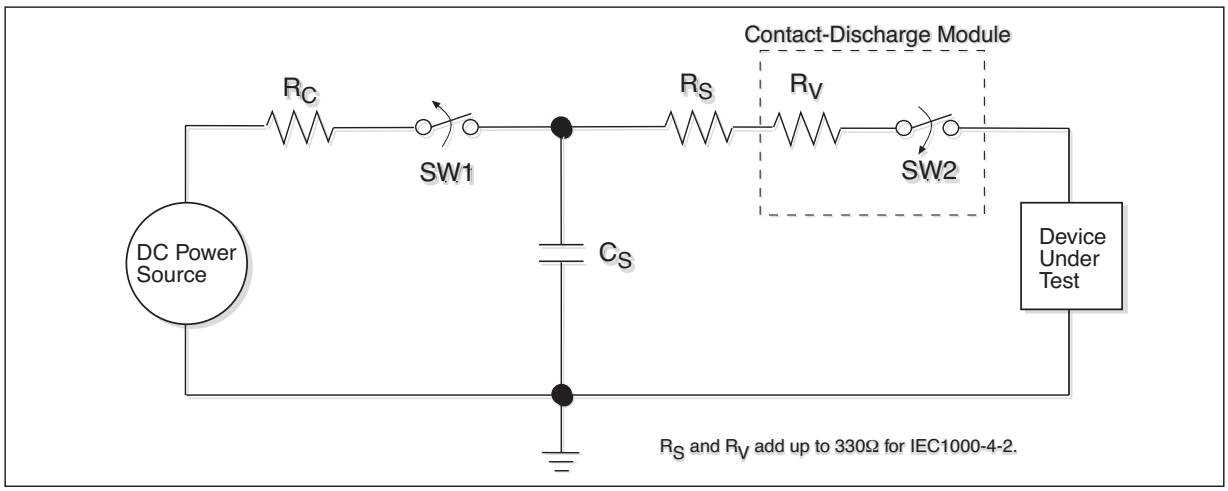


Figure 21. ESD Test Circuit for IEC1000-4-2

For the Human Body Model, the current limiting resistor (R_S) and the source capacitor (C_S) are 1.5kΩ and 100pF, respectively. For IEC-1000-4-2, the current limiting resistor (RS) and the source capacitor (CS) are 330Ω and 150pF, respectively.

The higher CS value and lower RS value in the IEC1000-4-2 model are more stringent than the Human Body Model. The larger storage capacitor injects a higher voltage to the test point when SW2 is switched on. The lower current limiting resistor increases the current charge onto the test point.

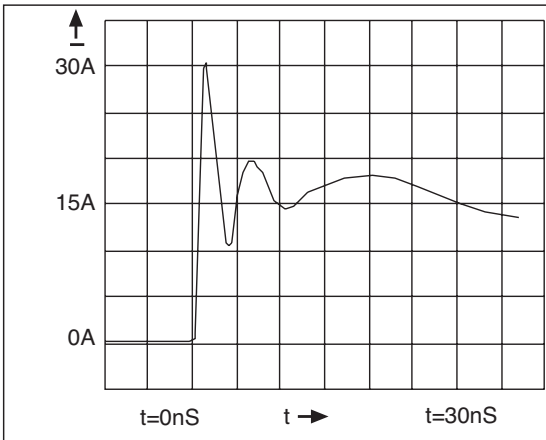
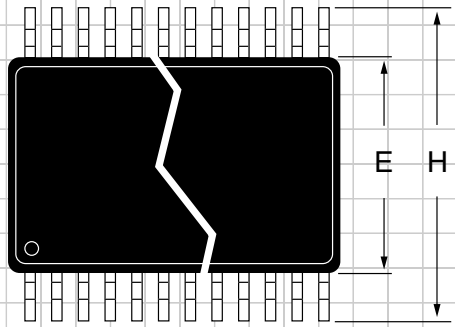
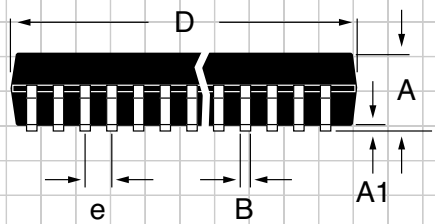


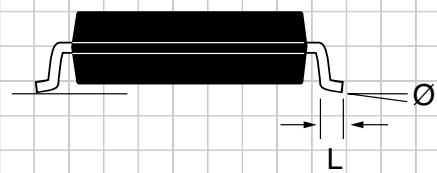
Figure 22. ESD Test Waveform for IEC1000-4-2

Device Pin Tested	Human Body Model	IEC1000-4-2		
		Air Discharge	Direct Contact	Level
Driver Ouputs	±15kV	±15kV	±8kV	4
Receiver Inputs	±15kV	±15kV	±8kV	4

PACKAGE: PLASTIC SHRINK SMALL OUTLINE (SSOP)

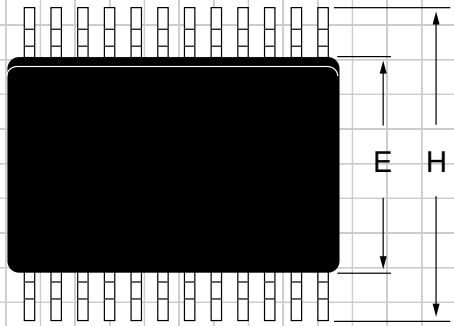


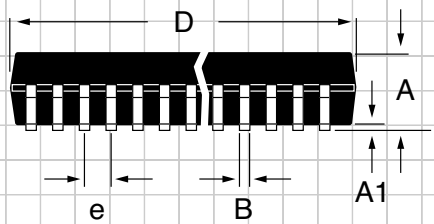


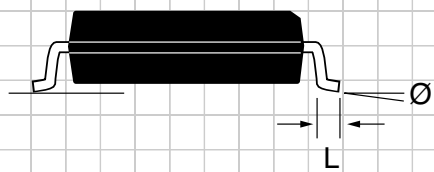


DIMENSIONS (Inches) Minimum/Maximum (mm)	16–PIN	20–PIN	24–PIN	28–PIN
A	0.068/0.078 (1.73/1.99)	0.068/0.078 (1.73/1.99)	0.068/0.078 (1.73/1.99)	0.068/0.078 (1.73/1.99)
A1	0.002/0.008 (0.05/0.21)	0.002/0.008 (0.05/0.21)	0.002/0.008 (0.05/0.21)	0.002/0.008 (0.05/0.21)
B	0.010/0.015 (0.25/0.38)	0.010/0.015 (0.25/0.38)	0.010/0.015 (0.25/0.38)	0.010/0.015 (0.25/0.38)
D	0.239/0.249 (6.07/6.33)	0.278/0.289 (7.07/7.33)	0.317/0.328 (8.07/8.33)	0.397/0.407 (10.07/10.33)
E	0.205/0.212 (5.20/5.38)	0.205/0.212 (5.20/5.38)	0.205/0.212 (5.20/5.38)	0.205/0.212 (5.20/5.38)
e	0.0256 BSC (0.65 BSC)	0.0256 BSC (0.65 BSC)	0.0256 BSC (0.65 BSC)	0.0256 BSC (0.65 BSC)
H	0.301/0.311 (7.65/7.90)	0.301/0.311 (7.65/7.90)	0.301/0.311 (7.65/7.90)	0.301/0.311 (7.65/7.90)
L	0.022/0.037 (0.55/0.95)	0.022/0.037 (0.55/0.95)	0.022/0.037 (0.55/0.95)	0.022/0.037 (0.55/0.95)
Ø	0°/8° (0°/8°)	0°/8° (0°/8°)	0°/8° (0°/8°)	0°/8° (0°/8°)

PACKAGE: PLASTIC SMALL OUTLINE (SOIC)

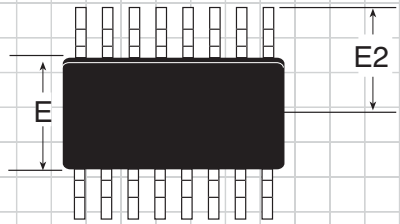


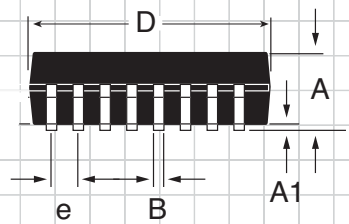


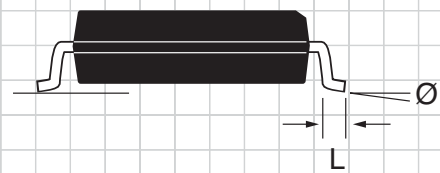


DIMENSIONS (Inches) Minimum/Maximum (mm)	16–PIN	18–PIN
A	0.090/0.104 (2.29/2.649)	0.090/0.104 (2.29/2.649))
A1	0.004/0.012 (0.102/0.300)	0.004/0.012 (0.102/0.300)
B	0.013/0.020 (0.330/0.508)	0.013/0.020 (0.330/0.508)
D	0.398/0.413 (10.10/10.49)	0.447/0.463 (11.35/11.74)
E	0.291/0.299 (7.402/7.600)	0.291/0.299 (7.402/7.600)
e	0.050 BSC (1.270 BSC)	0.050 BSC (1.270 BSC)
H	0.394/0.419 (10.00/10.64)	0.394/0.419 (10.00/10.64)
L	0.016/0.050 (0.406/1.270)	0.016/0.050 (0.406/1.270)
Ø	0°/8° (0°/8°)	0°/8° (0°/8°)

PACKAGE: PLASTIC THIN SMALL OUTLINE (TSSOP)







DIMENSIONS in inches (mm) Minimum/Maximum	16–PIN	20–PIN
A	- /0.043 (- /1.10)	- /0.043 (- /1.10)
A1	0.002/0.006 (0.05/0.15)	0.002/0.006 (0.05/0.15)
B	0.007/0.012 (0.19/0.30)	0.007/0.012 (0.19/0.30)
D	0.193/0.201 (4.90/5.10)	0.252/0.260 (6.40/6.60)
E	0.169/0.177 (4.30/4.50)	0.169/0.177 (4.30/4.50)
e	0.026 BSC (0.65 BSC)	0.026 BSC (0.65 BSC)
E2	0.126 BSC (3.20 BSC)	0.126 BSC (3.20 BSC)
L	0.020/0.030 (0.50/0.75)	0.020/0.030 (0.50/0.75)
Ø	0°/8°	0°/8°

RECOMMENDED UPGRADES

Contact factory for availability of the following legacy part numbers. For long term availability Sipex recommends upgrades as listed below. All upgrade part numbers shown are fully pinout and function compatible with legacy part numbers. Upgrade part numbers may contain feature and/or performance enhancements or other changes to datasheet parameters.

Legacy Part Number	Recommended Upgrade
SP3220CA	SP3220ECA
SP3220CA-L	SP3220ECA-L
SP3220CT	SP3220ECT
SP3220CY	SP3220ECY
SP3220EA	SP3220EEA
SP3220ET	SP3220EET
SP3220EY	SP3220EEY
SP3220BCA	SP3220EBCA
SP3220BCT	SP3220EBCT
SP3220BCY	SP3220EBCY
SP3220BEA	SP3220EBEA
SP3220BET	SP3220EBET
SP3220BEY	SP3220EBEY
SP3220UCA	SP3220EUCA
SP3220UCT	SP3220EUCT
SP3220UCY	SP3220EUCY
SP3220UEA	SP3220EUEA
SP3220UET	SP3220EUET
SP3220UEY	SP3220EUEY

ORDERING INFORMATION

Model	Temperature Range	Package Type
SP3220EBCA	0˚C to +70˚C	16-Pin SSOP
SP3220EBCA/TR	0˚C to +70˚C	16-Pin SSOP
SP3220EBCT	0˚C to +70˚C	16-Pin Wide SOIC
SP3220EBCT/TR	0˚C to +70˚C	16-Pin Wide SOIC
SP3220EBCY	0˚C to +70˚C	16-Pin TSSOP
SP3220EBCY/TR	0˚C to +70˚C	16-Pin TSSOP
SP3220EBEA	-40˚C to +85˚C	16-Pin SSOP
SP3220EBEA/TR	-40˚C to +85˚C	16-Pin SSOP
SP3220EBET	-40˚C to +85˚C	16-Pin Wide SOIC
SP3220EBET/TR	-40˚C to +85˚C	16-Pin Wide SOIC
SP3220EBEY	-40˚C to +85˚C	16-Pin TSSOP
SP3220EBEY/TR	-40˚C to +85˚C	16-Pin TSSOP
SP3220ECA	0˚C to +70˚C	16-Pin SSOP
SP3220ECA/TR	0˚C to +70˚C	16-Pin SSOP
SP3220ECT	0˚C to +70˚C	16-Pin WSOIC
SP3220ECT/TR	0˚C to +70˚C	16-Pin WSOIC
SP3220ECY	0˚C to +70˚C	16-Pin TSSOP
SP3220ECY/TR	0˚C to +70˚C	16-Pin TSSOP

Available in lead free packaging. To order add “-L” suffix to part number.

Example: SP3220ECA/TR = standard; SP3220ECA-L/TR = Lead Free

/TR = Tape and Reel

Pack quantity is 1,500 for WSOIC, or SSOP; pack quantity is 2,500 for 16-pin TSSOP.

Sipex Corporation

ANALOG EXCELLENCE

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Billerica, MA 01821
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FAX: (978) 670-9001
e-mail: sales@sipex.com

ORDERING INFORMATION

Model	Temperature Range	Package Type
SP3220EEA	-40°C to +85°C	16-Pin SSOP
SP3220EEA/TR	-40°C to +85°C	16-Pin SSOP
SP3220EET	-40°C to +85°C	16-Pin WSOIC
SP3220EET/TR	-40°C to +85°C	16-Pin WSOIC
SP3220EEY	-40°C to +85°C	16-Pin TSSOP
SP3220EEY/TR	-40°C to +85°C	16-Pin TSSOP
SP3220EUCA	0°C to +70°C	16-Pin SSOP
SP3220EUCA/TR	0°C to +70°C	16-Pin SSOP
SP3220EUCT	0°C to +70°C	16-Pin Wide SOIC
SP3220EUCT/TR	0°C to +70°C	16-Pin Wide SOIC
SP3220EUCY/TR	0°C to +70°C	16-Pin TSSOP
SP3220EUCY	0°C to +70°C	16-Pin TSSOP
SP3220EUEA	-40°C to +85°C	16-Pin SSOP
SP3220EUEA/TR	-40°C to +85°C	16-Pin SSOP
SP3220EUET	-40°C to +85°C	16-Pin Wide SOIC
SP3220EUET/TR	-40°C to +85°C	16-Pin Wide SOIC
SP3220EUEY	-40°C to +85°C	16-Pin TSSOP
SP3220EUEY/TR	-40°C to +85°C	16-Pin TSSOP

Available in lead free packaging. To order add "-L" suffix to part number.

Example: SP3220ECA/TR = standard; SP3220ECA-L/TR = Lead Free

/TR = Tape and Reel

Pack quantity is 1,500 for WSOIC, or SSOP; pack quantity is 2,500 for 16-pin TSSOP.

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