XA-SK-SDRAM Slice Card hardware Guide

REV A

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XMOS

Table of Contents

1 Slice Card Overview

IN THIS CHAPTER

1.1 Pack Contents

- One XA-SK-SDRAM Slice Card

1.2 Random Access Memory

This slice provides 8 Megebytes of random access memory via an ISSI 6400 Synchronous DRAM. It is suitable for burst access only, random access is possible but performance will be very significantly degraded. The associated SDRAM Controll xSOFTip component can operate this memory at clock speeds up to 40 MHz, yielding an aggregate performance of 80 MBytes/sec.

1.3 Reduced Pinout

The SDRAM slice uses a technique of reusing the same XCore GPIO pins for both Address and Data. This optimisation is made possible tahnks to the soft nature of the associated xSOFTip sdram controller component. In addition, a NOR gate on the slice generates the data strobes (UDQM and LDQM on the memory chip) from CAS# and WE#. These features are described more fully in the SDRAM Controller xSOFTip component documentation.

Taken together, these features permit the addition of a high performance SDRAM subsystem to any XCore application using only 20 pins.

2 XA-SK-SDRAM Functional Pins

This table shows the port mapping for each of the Slice Card Signal IO, and the Slicekit Slot connector pin it is located on.

Function	STAR	TRIANGLE	SQUARE	PIN	Description
SD_WE	1C	1K	1C	B10	SDRAM Write Enable
SD_CAS	1B	1J	1B	A8	SDRAM CAS
SD_RAS	1G	1I	1G	B15	SDRAM RAS
SD_CLK	1F	1L	1F	A15	SDRAM Clock drivern from XCore
SD_ADQ0	A0	B0	A0	B6	SDRAM Address and Data
SD_ADQ1	A1	B1	A1	B7	SDRAM Address and Data
SD_ADQ2	A2	B2	A2	B9	SDRAM Address and Data
SD_ADQ3	A3	B3	A3	B11	SDRAM Address and Data
SD_ADQ4	A4	B4	A4	A9	SDRAM Address and Data
SD_ADQ5	A5	B5	A5	A11	SDRAM Address and Data
SD_ADQ6	A6	B6	A6	A6	SDRAM Address and Data
SD_ADQ7	A7	B7	A7	A7	SDRAM Address and Data
SD_ADQ8	A8	B8	A8	B12	SDRAM Address and Data
SD_ADQ9	A9	B9	A9	B13	SDRAM Address and Data
SD_ADQ10	A10	B10	A10	B17	SDRAM Address and Data
SD_ADQ11	A11	B11	A11	B18	SDRAM Address and Data
SD_ADQ12	A12	B12	A12	A17	SDRAM Address and Data
SD_DQ13/BA0	A13	B13	A13	A18	SDRAM Bank Address and Data
SD_DQ14/BA1	A14	B14	A14	A12	SDRAM Bank Address and Data
SD_DQ15	A15	B15	A15	A13	SDRAM Data