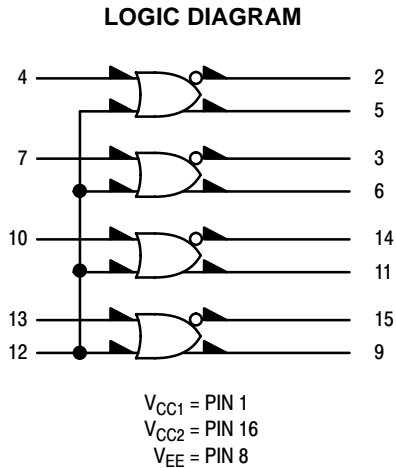


# MC10101

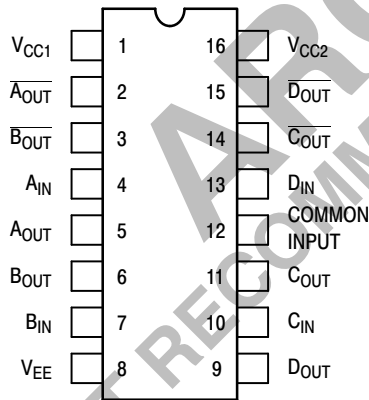
## Quad OR/NOR Gate

The MC10101 is a quad 2-input OR/NOR gate with one input from each gate common to pin 12.

- $P_D = 25 \text{ mW typ/gate (No Load)}$
- $t_{pd} = 2.0 \text{ ns typ}$
- $t_r, t_f = 2.0 \text{ ns typ (20\%–80\%)}$



**DIP  
PIN ASSIGNMENT**

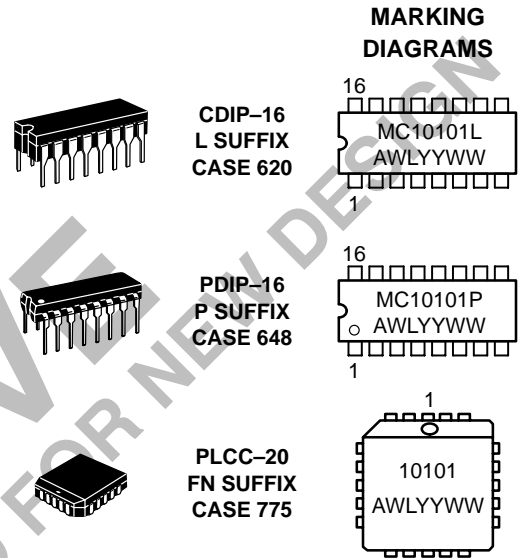


Pin assignment is for Dual-in-Line Package.  
 For PLCC pin assignment, see the Pin Conversion Tables on page 18  
 of the ON Semiconductor MECL Data Book (DL122/D).



**ON Semiconductor**

<http://onsemi.com>



A = Assembly Location  
 WL = Wafer Lot  
 YY = Year  
 WW = Work Week

**ORDERING INFORMATION**

Device	Package	Shipping
MC10101L	CDIP-16	25 Units / Rail
MC10101P	PDIP-16	25 Units / Rail
MC10101FN	PLCC-20	46 Units / Rail

# MC10101

## ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits						Unit	
			-30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min		Max
Power Supply Drain Current	$I_E$	8		29		20	26		29	mAdc
Input Current	$I_{inH}$	4		425			265		265	$\mu$ Adc
		12		850			535		535	
	$I_{inL}$	4	0.5		0.5			0.3		$\mu$ Adc
		12	0.5		0.5			0.3		
Output Voltage Logic 1	$V_{OH}$	5	-1.060	-0.890	-0.960		-0.810	-0.890	-0.700	Vdc
		5	-1.060	-0.890	-0.960		-0.810	-0.890	-0.700	
		2	-1.060	-0.890	-0.960		-0.810	-0.890	-0.700	
		2	-1.060	-0.890	-0.960		-0.810	-0.890	-0.700	
Output Voltage Logic 0	$V_{OL}$	5	-1.890	-1.675	-1.850		-1.650	-1.825	-1.615	Vdc
		5	-1.890	-1.675	-1.850		-1.650	-1.825	-1.615	
		2	-1.890	-1.675	-1.850		-1.650	-1.825	-1.615	
		2	-1.890	-1.675	-1.850		-1.650	-1.825	-1.615	
Threshold Voltage Logic 1	$V_{OHA}$	5	-1.080		-0.980			-0.910		Vdc
		5	-1.080		-0.980			-0.910		
		2	-1.080		-0.980			-0.910		
		2	-1.080		-0.980			-0.910		
Threshold Voltage Logic 0	$V_{OLA}$	5		-1.655			-1.630		-1.595	Vdc
		5		-1.655			-1.630		-1.595	
		2		-1.655			-1.630		-1.595	
		2		-1.655			-1.630		-1.595	
Switching Times (50 $\Omega$ Load)									ns	
Propagation Delay	$t_{4+2-}$	2	1.0	3.1	1.0	2.0	2.9	1.0	3.3	
		2	1.0	3.1	1.0	2.0	2.9	1.0	3.3	
		5	1.0	3.1	1.0	2.0	2.9	1.0	3.3	
		5	1.0	3.1	1.0	2.0	2.9	1.0	3.3	
Rise Time (20 to 80%)	$t_{2+}$	2	1.1	3.6	1.1	2.0	3.3	1.1	3.7	
		5	1.1	3.6	1.1	2.0	3.3	1.1	3.7	
Fall Time (20 to 80%)	$t_{5-}$	2	1.1	3.6	1.1	2.0	3.3	1.1	3.7	
		5	1.1	3.6	1.1	2.0	3.3	1.1	3.7	

# MC10101

## ELECTRICAL CHARACTERISTICS (continued)

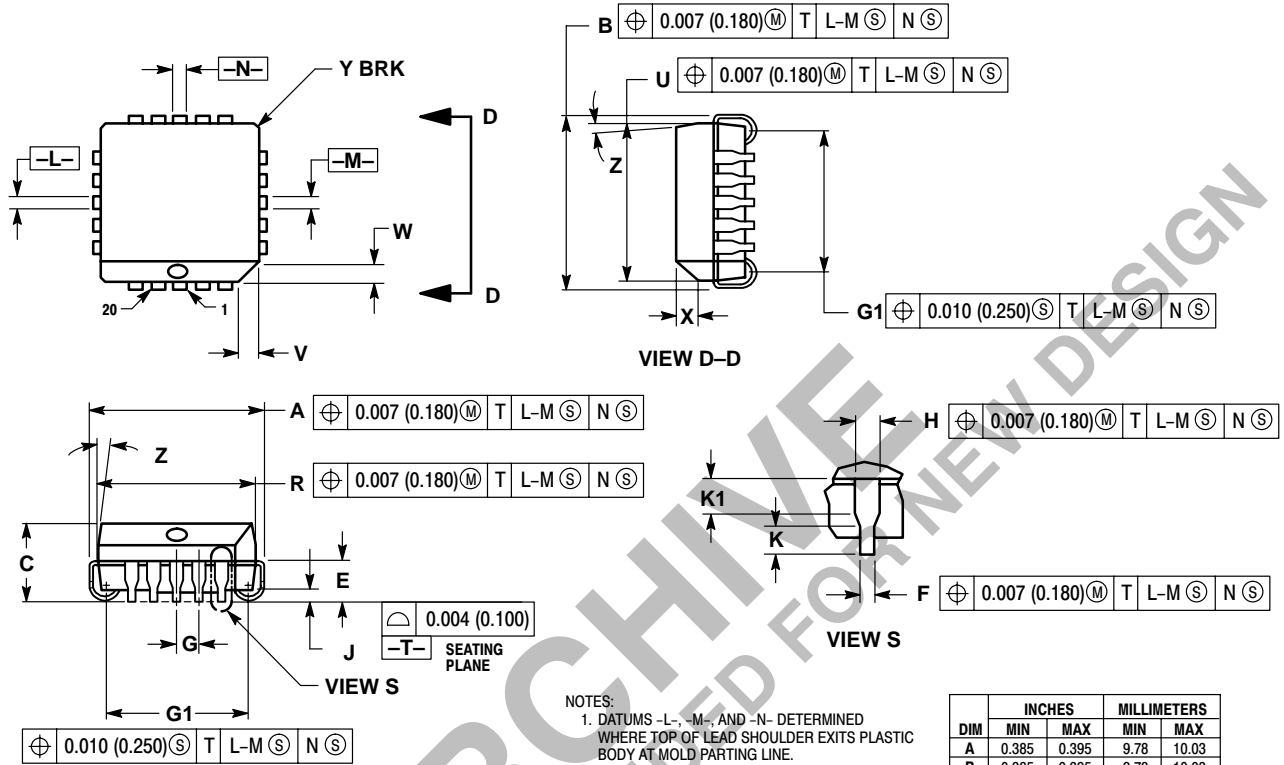
			TEST VOLTAGE VALUES (Volts)					(V <sub>CC</sub> ) Gnd	
			V <sub>IHmax</sub>	V <sub>ILmin</sub>	V <sub>IHAmin</sub>	V <sub>ILAmax</sub>	V <sub>EE</sub>		
			-30°C	-0.890	-1.890	-1.205	-1.500		-5.2
			+25°C	-0.810	-1.850	-1.105	-1.475		-5.2
			+85°C	-0.700	-1.825	-1.035	-1.440	-5.2	
Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW						
			V <sub>IHmax</sub>	V <sub>ILmin</sub>	V <sub>IHAmin</sub>	V <sub>ILAmax</sub>	V <sub>EE</sub>		
Power Supply Drain Current	I <sub>E</sub>	8					8	1, 16	
Input Current	I <sub>inH</sub>	4	4				8	1, 16	
		12	12				8	1, 16	
	I <sub>inL</sub>	4		4			8	1, 16	
		12		12			8	1, 16	
Output Voltage	Logic 1	V <sub>OH</sub>	5	12				8	1, 16
			5	4				8	1, 16
			2					8	1, 16
			2					8	1, 16
Output Voltage	Logic 0	V <sub>OL</sub>	5					8	1, 16
			5					8	1, 16
			2	12				8	1, 16
			2	4				8	1, 16
Threshold Voltage	Logic 1	V <sub>OHA</sub>	5		12			8	1, 16
			5		4			8	1, 16
			2			12		8	1, 16
			2			4		8	1, 16
Threshold Voltage	Logic 0	V <sub>OLA</sub>	5			12		8	1, 16
			5			4		8	1, 16
			2		12			8	1, 16
			2		4			8	1, 16
Switching Times	(50Ω Load)				Pulse In	Pulse Out	-3.2 V	+2.0 V	
Propagation Delay		t <sub>4+2-</sub>	2			4	2	8	1, 16
		t <sub>4-2+</sub>	2			4	2	8	1, 16
		t <sub>4+5+</sub>	5			4	5	8	1, 16
		t <sub>4-5-</sub>	5			4	5	8	1, 16
Rise Time	(20 to 80%)	t <sub>2+</sub>	2			4	2	8	1, 16
		t <sub>5+</sub>	5			4	5	8	1, 16
Fall Time	(20 to 80%)	t <sub>2-</sub>	2			4	2	8	1, 16
		t <sub>5-</sub>	5			4	5	8	1, 16

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

# MC10101

## PACKAGE DIMENSIONS

PLCC-20  
FN SUFFIX  
PLASTIC PLCC PACKAGE  
CASE 775-02  
ISSUE C



### NOTES:

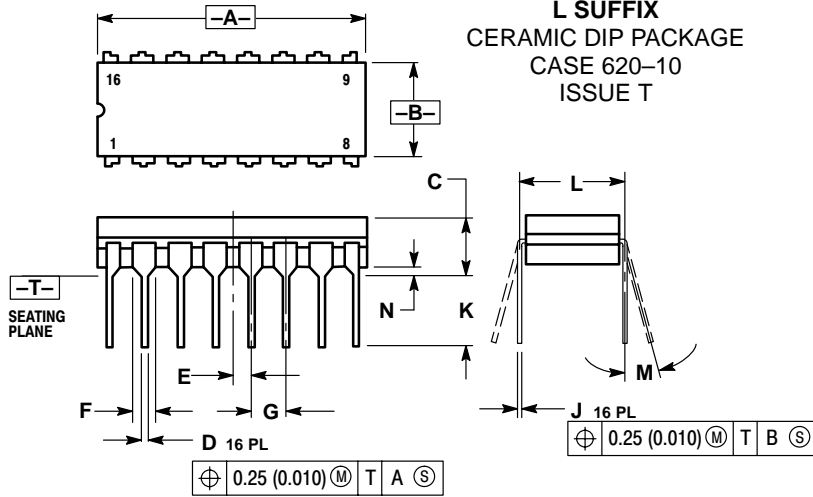
- DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
- DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
- DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
- THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH. TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
- DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.385	0.395	9.78	10.03
B	0.385	0.395	9.78	10.03
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	---	0.51	---
K	0.025	---	0.64	---
R	0.350	0.356	8.89	9.04
U	0.350	0.356	8.89	9.04
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	---	0.020	---	0.50
Z	2°	10°	2°	10°
G1	0.310	0.330	7.88	8.38
K1	0.040	---	1.02	---

# MC10101

## PACKAGE DIMENSIONS

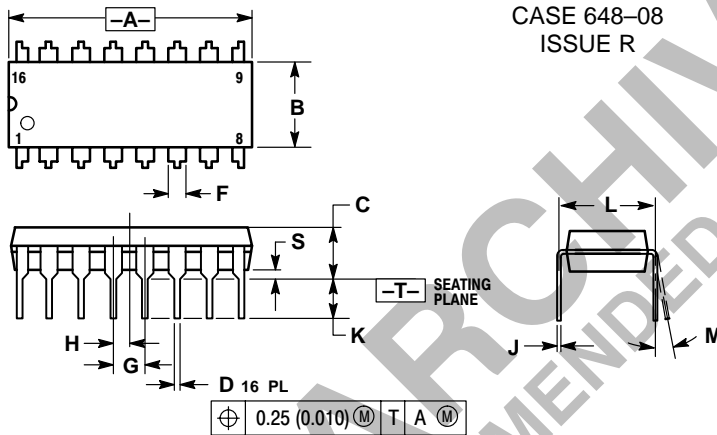
### CDIP-16 L SUFFIX CERAMIC DIP PACKAGE CASE 620-10 ISSUE T



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
  4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	---	0.200	---	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

### PDIP-16 P SUFFIX PLASTIC DIP PACKAGE CASE 648-08 ISSUE R



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
  4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
  5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01


Notes

ARCHIVE  
DEVICE NOT RECOMMENDED FOR NEW DESIGN

Notes

ARCHIVE  
DEVICE NOT RECOMMENDED FOR NEW DESIGN

ARCHIVE  
 RECOMMENDED FOR NEW DESIGN

**ON Semiconductor** and  are trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer.

## PUBLICATION ORDERING INFORMATION

### Literature Fulfillment:

Literature Distribution Center for ON Semiconductor  
 P.O. Box 5163, Denver, Colorado 80217 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** ONlit@hibbertco.com

**N. American Technical Support:** 800-282-9855 Toll Free USA/Canada

**JAPAN:** ON Semiconductor, Japan Customer Focus Center  
 4-32-1 Nishi-Gotanda, Shinagawa-ku, Tokyo, Japan 141-0031  
**Phone:** 81-3-5740-2700  
**Email:** r14525@onsemi.com

**ON Semiconductor Website:** <http://onsemi.com>

For additional information, please contact your local Sales Representative.