DATA SHEET

AAT2630: Wireless Data Card PMIC 10-Channel DC-DC Converter

Applications

- Wireless mini, or half-mini PCI express cards
- Express cards
- USB wireless modules
- SDIO modules
- On-board wireless modems

Features

- V_{IN} range: 3.0 V to 5.5 V
- Two 1.92 MHz synchronous step-down converters:
  - 180° out-of-phase operation
  - Buck1: 1.375 V, 500 mA output
  - Buck2: 2.1 V, 500 mA output
  - Light load, low noise switching mode
- Eight LDO regulators:
  - Two with 300 mA output:
    LDO1 for MSME: 1.8 V
    LDO3 for MSMA: 2.6 V
  - Three with 150 mA output:
    LDO2 for MSMP: 2.6 V
    LDO4 for MMC: 3.0 V
    LDO8 for RFRX: 2.75 V
  - Three with 50mA output:
    LDO5 for RUIM: 1.8 V/3.0 V
    LDO6 for TCXO: 2.85 V
    LDO7 for USB: 3.1 V
  - High PSRR (70 dB @1 KHz)
- Over-current and over-temperature protection
- Power-on reset
- Power up with defined sequence
- 1.25 V voltage reference
- 19.2 MHz clock buffer
- 32.7645 kHz frequency output
- WLCSP (49-bump, 3 mm × 3 mm) package (MSL1, 260 ºC per JEDEC J-STD-020)

Description

The AAT2630 contains two fully integrated, step-down converters, eight low-dropout (LDO) regulators, a 1.25 V voltage reference, a 19.2 MHz clock buffer, a 32 kHz frequency output, and three LED drivers in a 3 mm × 3 mm Wafer Level Chip Scale Package (WLCSP), making it ideal for wireless data cards or modules and on-board modems.

The two step-down converters are synchronous with internal compensation. Switching at 1.92 MHz, they operate 180° out of phase to minimize the number and size of the external components and to provide efficiencies higher than 90%.

The eight LDOs are high PSRR type, requiring only a small output ceramic capacitor for stability.

Power-on reset and automatic power-up sequence, which are common in system architectures involving a processor, are defined for the supplies. The AAT2630 also includes over-current and over-temperature protection.

The AAT2630 is available in a 49-bump, 3 mm × 3 mm WLCSP package.

A typical application circuit is shown in Figure 1. The pin configurations are shown in Figure 2. Signal pin assignments descriptions are provided in Table 1.

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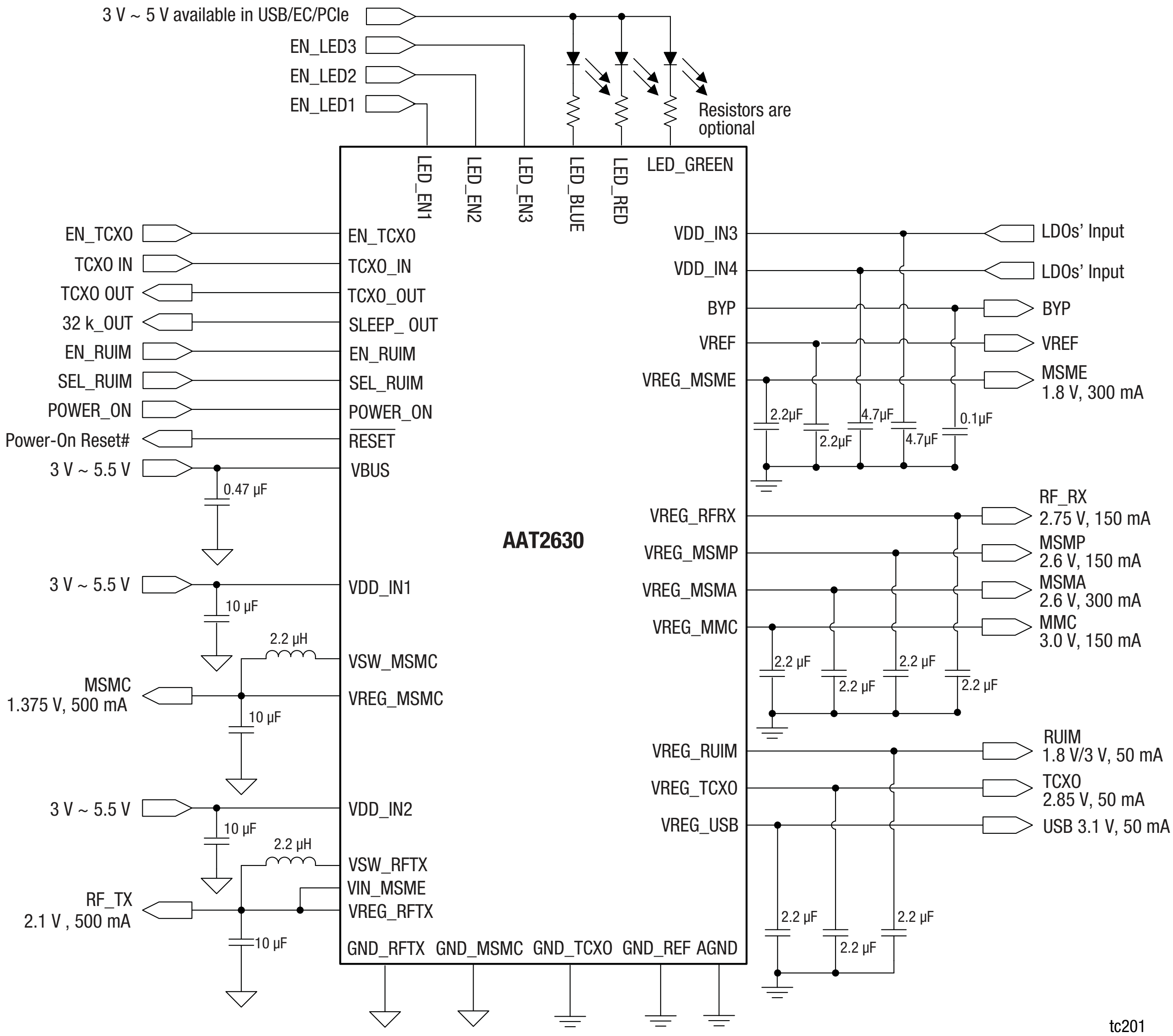

Figure 1. AAT2630 Typical Application Circuit

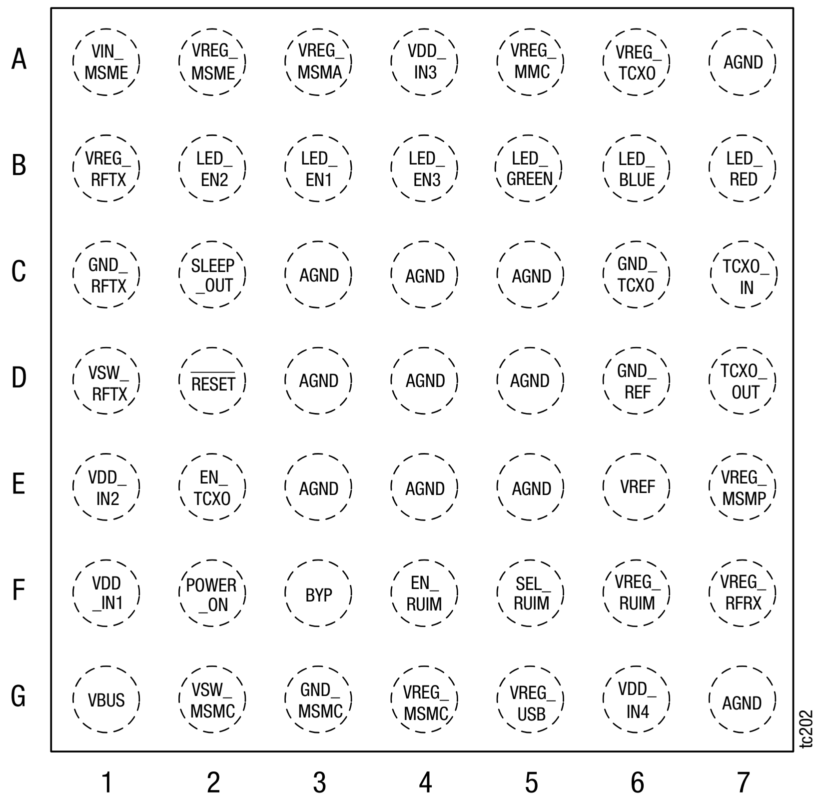

Figure 2. AAT2630 Pinout – 49-Bump, 3 mm × 3 mm WLCSP (Top View)

Table 1. AAT2630 Signal Descriptions (1 of 2)

Pin	Name	Type	Description
A1	VIN_MSME	PWR	Supply voltage for LDO MSME.
A2	VREG_MSME	O	LDO1 output for MSME.
A3	VREG_MSMA	O	LDO3 output for MSMA.
A4	VDD_IN3	PWR	Supply voltage for LDO3/4/6 = VREG_MSMA/VREG_MMC/VREG_TCXO and internal analog blocks such as band-gap. UVLO senses VDD_IN3.
A5	VREG_MMC	O	LDO4 output for MMC.
A6	VREG_TCXO	O	LDO6 output for TCXO.
A7	AGND	GND	Analog ground.
B1	VREG_RFTX	O	Buck2 output for RFTX.
B2	LED_EN2	I	Active high LED2 driver enable for red.
B3	LED_EN1	I	Active high LED1 driver enable for blue.
B4	LED_EN3	I	Active high LED3 driver enable for green.
B5	LED_GREEN	O	LED3 driver output for green.
B6	LED_BLUE	O	LED1 driver output for blue.
B7	LED_RED	O	LED2 driver output for red.
C1	GND_RFTX	GND	Switching current return path of Buck2 for RFTX.
C2	SLEEP_OUT	O	32 kHz frequency signal output.
C3	AGND	GND	Ground.

Table 1. AAT2630 Signal Descriptions (2 of 2)

Pin	Name	Type	Description
C4	AGND	GND	Ground.
C5	AGND	GND	Ground.
C6	GND_TCXO	GND	GND for the 19.2 MHz buffer.
C7	TCXO_IN	I	19.2 MHz frequency signal buffer input.
D1	VSW_RFTX	O	Switching node of Buck2 for RFTX, connect to an inductor.
D2	$\overline{\text{RESET}}$	O	System power on reset (Active low) with 100 kΩ pull up resistor to VREG_MSMP internally.
D3	AGND	GND	Ground.
D4	AGND	GND	Ground.
D5	AGND	GND	Ground.
D6	GND_REF	GND	Reference ground.
D7	TCXO_OUT	O	19.2 MHz frequency signal buffer output.
E1	VDD_IN2	PWR	Supply voltage of the Buck2 power switches for RFTX.
E2	EN_TCXO	I	19.2 MHz frequency signal buffer enable input (active high) with internal 1.5 MΩ pull down resistor.
E3	AGND	GND	Ground.
E4	AGND	GND	Ground.
E5	AGND	GND	Ground.
E6	VREF	O	1.25 V reference voltage output.
E7	VREG_MSMP	O	LDO2 output for MSMP.
F1	VDD_IN1	PWR	Supply voltage of the Buck1 power switches for MSMC.
F2	POWER_ON	I	Active high PMU power on with internal 1.5 MΩ pull down resistor.
F3	BYP	I	Bypass pin.
F4	EN_RUIM	I	Enable LDO5 input (Active High) for RUIM with internal 1.5 MΩ pull down resistor.
F5	SEL_RUIM	I	LDO5 voltage select for RUIM High = 3.0 V, Low = 1.8 V with 1.5 MΩ pull down resistor.
F6	VREG_RUIM	O	LDO5 output for RUIM.
F7	VREG_RFRX	O	LDO8 output for RFRX.
G1	VBUS	I	Supply voltage for VREG_USB and buck converter control blocks. VBUS must be shorted to VDD_IN1 and VDD_IN2.
G2	VSW_MSMC	O	Switching node of Buck1 for MSMC, connect to an inductor.
G3	GND_MSMC	GND	Switching current return path of Buck1 for MSMC.
G4	VREG_MSMC	O	Buck1 output for MSMC.
G5	VREG_USB	O	LDO7 output for USB.
G6	VDD_IN4	PWR	Supply voltage for LDO2/5/8 = VREG_MSMP/VREG_RUIM/VREG_RFRX.
G7	AGND	GND	Analog ground.

Electrical and Mechanical Specifications

The absolute maximum ratings of the AAT2630 are provided in Table 2, the thermal information is listed in Table 3, and electrical specifications are provided in Table 4.

Table 2. AAT2630Absolute Maximum Ratings (Note 1)

Parameter	Symbol	Minimum	Typical	Maximum	Units
VDD_IN1 to GND_MSMC, VDD_IN2 to GND_RFTX, LED_BLUE, LED_RED, LED_GREEN, VDD_IN3, VDD_IN4, RESET to AGND	V_{IN_ABS}	–0.3		6.5	V
VSW_MSMC to GND_MSMC, VSW_RFTX to GND_RFTX	V_{P_ABS}	–0.3		V_{DD_IN1} + 0.3	V
All other input pins other than VDD_IN1, VDD_IN2, LED_BLUE, LED_RED, LED_GREEN, VDD_IN3, VDD_IN4, RESET, VSW_MSMC, VSW_RFTX to AGND	V_{N_ABS}	–0.3		V_{DD_IN1} + 0.3	V
GND_MSMC and GND_RFRX to AGND	V_{G_ABS}	–0.3		0.3	V
Operating temperature range	T_J	–40		125	ºC
Storage temperature range	T_S	–65		150	ºC
Maximum soldering temperature (at leads, 10 sec)	T_{LEAD}		300		ºC

Note 1: Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed may result in permanent damage to the device.

Table 3. AAT2630 Thermal Information (Note 1)

Parameter	Symbol	Value	Units
Thermal resistance	θ_{JA}	52.5	ºC/W
Maximum power dissipation	P_D	1.9	W

Note 1: Mounted on an FR4 board.

CAUTION: *Although this device is designed to be as robust as possible, electrostatic discharge (ESD) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions should be used at all times.*

Table 4. AAT2630 Electrical Specifications (1 of 5) (Note 1)
(V_{BUS} = V_{DD_IN1} = V_{DD_IN2} = V_{DD_IN3} = V_{DD_IN4} = 3.6 V, V_{POWER_ON} = 3.6 V, V_{EN_TCXO} = V_{EN_RUIM} = 3.6 V, V_{SEL_RUIM} = 3.6 V, C_{INB} = 10 μF, C_{OUTB} = 10 μF, C_{VREF} = 2.2 μF, C_{INL} = 4.7 μF, C_{OUTL} = 2.2 μF, C_{BYP} = 0.1 μF, C_{VBUS} = 0.47 μF, T_A = –40 °C to +85 °C, Typical Values are T_A = 25 °C, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Operation						
Normal operating buck input voltage range	V_{DD_IN1}, V_{DD_IN2}, V_{BUS}		3.0		5.5	V
Normal operating ldo input voltage range	V_{DD_IN3}, V_{DD_IN4}		2.9		4.0	V
Input under voltage lockout	V_{UVLO}	V_{DD_IN3} falling	2.3	2.55	2.8	V
		Hysteresis		200		mV
		Blanking time		1		μs
Operating current	I_{OP}	I_{OUTB} = 0 mA, I_{OUT} = 0 mA, TCXO_IN = 0		8		mA
Standby supply current	I_{STDBY}	V_{POWER_ON} = 0 V		110		μA
VREF						
Nominal VREF voltage	V_{REF}			1.25		V
Temperature coefficient	ΔV_{REF}/ºC			±100		ppm/°C
Absolute error	$\Delta V_{REF}/V_{REF}$	All conditions	–0.7		+0.7	%
Nominal output current	I_{REF}			300		μA
Step-Down Buck Regulators (Buck1 and Buck2)						
Buck1 output voltage	V_{REG_MSMC}	I_{OUTB1} = 10 mA, T_A = 25 °C	1.30	1.375	1.45	V
Buck2 output voltage	V_{REG_RFTX}	I_{OUTB2} = 10 mA, T_A = 25 °C	2.00	2.1	2.45	V
Buck output voltage temperature coefficient	ΔV_{OUTB}/°C			±100		ppm/°C
Buck nominal output current	I_{OUTB1}, I_{OUTB2}			500		mA
P-channel current limit	I_{LIMB1}, I_{LIMB2}		1000			mA
Switching frequency	f_{SW}			1.92		MHz
Efficiency	η	I_{OUTB1} = 300 mA		90		%
		I_{OUTB1} = 500 mA		87		%
		I_{OUTB1} = 600 mA		86		%
		I_{OUTB2} = 300 mA		92		%
		I_{OUTB2} = 500 mA		91		%
		I_{OUTB2} = 600 mA		90		%
Settling time	Transient Response	To within 1% of final value		40		μs
Overshoot		I_{OUTB} = 300 mA to 10 mA in 1 μs		100		mV
Undershoot		I_{OUTB} = 10 mA to 300 mA in 1 μs		100		mV
Load regulation		I_{OUTB} = 10 mA to 500 mA		0.65		%
Line regulation		V_{DD_IN1} = V_{DD_IN2} = 3 V to 5 V, I_{OUTB} = 100 mA		0.2		%/V

Table 4. AAT2630 Electrical Specifications (2 of 5) (Note 1)
(V_{BUS} = V_{DD_IN1} = V_{DD_IN2} = V_{DD_IN3} = V_{DD_IN4} = 3.6 V, V_{POWER_ON} = 3.6 V, V_{EN_TCXO} = V_{EN_RUIM} = 3.6 V, V_{SEL_RUIM} = 3.6 V, C_{INB} = 10 μF, C_{OUTB} = 10 μF, C_{VREF} = 2.2 μF, C_{INL} = 4.7 μF, C_{OUTL} = 2.2 μF, C_{BYP} = 0.1 μF, C_{VBUS} = 0.47 μF, T_A = –40 °C to +85 °C, Typical Values are T_A = 25 °C, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
LDO1 (MSME)						
Normal operating input voltage range	V_{IN_MSME}			V_{OUTB2}		V
Output voltage	V_{OUT1}	I_{OUT1} = 10 mA	1.75	1.8	1.85	V
Temperature coefficient	ΔV_{OUT1}/°C			±100		ppm/°C
Maximum output current	I_{OUT1}		300	450		mA
Dropout voltage	V_{LDO1_DO}	I_{OUT1} = 300 mA		150	300	mV
Load regulation		I_{OUT1} = 10 mA to 300 mA		6	50	mV
Line regulation		V_{IN_MSME} = 2.0 V to 2.2 V, I_{OUT1} = 50 mA		0.1		%/V
	V_{NOISE}	I_{OUT1} = 50 mA, 10 Hz to 10 kHz		350		μV_{RMS}
		I_{OUT1} = 50 mA, 10 Hz to 10 kHz, C_{BYP} = 1 μF		60		μV_{RMS}
Power supply rejection ratio	$PSRR_{OUT1}$	f = 1 kHz, I_{OUT1} = 50 mA, V_{IN_MSME} = 2.1 V		70		dB
		f = 10 kHz, I_{OUT1} = 50 mA, V_{IN_MSME} = 2.1 V		50		dB
LDO2 (MSMP)						
Output voltage	V_{OUT2}	I_{OUT2} = 10 mA	2.52	2.6	2.68	V
Temperature coefficient	ΔV_{OUT2}/°C			±100		ppm/°C
Maximum output current	I_{OUT2}		300	500		mA
Dropout voltage	V_{LDO2_DO}	I_{OUT2} = 150 mA		150	300	mV
Load regulation		I_{OUT2} = 10 mA to 150 mA		5	50	mV
Line regulation		V_{DD_IN4} = 3.0 V to 4.0 V, I_{OUT2} = 50 mA		0.1		%/V
	V_{NOISE}	I_{OUT2} = 50 mA, 10 Hz to 10 kHz		350		μV_{RMS}
		I_{OUT2} = 50 mA, 10 Hz to 10 kHz, C_{BYP} = 1 μF		60		μV_{RMS}
Power supply rejection ratio	$PSRR_{OUT2}$	f = 1 kHz, I_{OUT2} = 50 mA, V_{DD_IN4} = 2.1 V		70		dB
		f = 10 kHz, I_{OUT2} = 50 mA, V_{DD_IN4} = 2.1 V		50		dB
LDO3 (MSMA)						
Output voltage	V_{OUT3}	I_{OUT3} = 10 mA	2.52	2.6	2.68	V
Temperature coefficient	ΔV_{OUT3}/°C			±100		ppm/°C
Maximum output current	I_{OUT3}		300	550		mA
Dropout voltage	V_{LDO3_DO}	I_{OUT3} = 300 mA		200	400	mV
Load regulation		I_{OUT3} = 10 mA to 300 mA		5	50	mV
Line regulation		V_{DD_IN4} = 3.0 V to 4.0 V, I_{OUT3} = 50 mA		0.1		%/V
	V_{NOISE}	I_{OUT3} = 50 mA, 10 Hz to 10 kHz		350		μV_{RMS}
		I_{OUT3} = 50 mA, 10 Hz to 10 kHz, C_{BYP} = 1 μF		60		μV_{RMS}
Power supply rejection ratio	$PSRR_{OUT3}$	f = 1 kHz, I_{OUT3} = 50 mA, V_{DD_IN3} = V_{OUT3} + 1 V		70		dB
		f = 10 kHz, I_{OUT3} = 50 mA, V_{DD_IN3} = V_{OUT3} + 1 V		50		dB

Table 4. AAT2630 Electrical Specifications (3 of 5) (Note 1)
(V_{BUS} = V_{DD_IN1} = V_{DD_IN2} = V_{DD_IN3} = V_{DD_IN4} = 3.6 V, V_{POWER_ON} = 3.6 V, V_{EN_TCXO} = V_{EN_RUIM} = 3.6 V, V_{SEL_RUIM} = 3.6 V, C_{INB} = 10 μF, C_{OUTB} = 10 μF, C_{VREF} = 2.2 μF, C_{INL} = 4.7 μF, C_{OUTL} = 2.2 μF, C_{BYP} = 0.1 μF, C_{VBUS} = 0.47 μF, T_A = –40 °C to +85 °C, Typical Values are T_A = 25 °C, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
LDO4 (MMC)						
Output voltage	V_{OUT4}	I_{OUT4} = 10 mA	2.9	3.0	3.1	V
Temperature coefficient	ΔV_{OUT4}/°C			±100		ppm/°C
Maximum output current	I_{OUT4}		300	550		mA
Dropout voltage	V_{LDO4_DO}	I_{OUT4} = 150 mA		100	300	mV
Load regulation		I_{OUT4} = 10 mA to 150 mA		5	50	mV
Line regulation		V_{DD_IN3} = 3.0 V to 4.0 V, I_{OUT4} = 50 mA		0.1		%/V
	V_{NOISE}	I_{OUT4} = 50 mA, 10 Hz to 10 kHz		350		$μV_{RMS}$
		I_{OUT4} = 50 mA, 10 Hz to 10 kHz, C_{BYP} = 1 μF		60		$μV_{RMS}$
Power supply rejection ratio	$PSRR_{OUT4}$	f = 1 kHz, I_{OUT4} = 50 mA, V_{DD_IN3} = V_{OUT4} + 1 V		70		dB
		f = 10 kHz, I_{OUT4} = 50 mA, V_{DD_IN3} = V_{OUT4} + 1 V		50		dB
LDO5 (RUIM)						
Output voltage	V_{OUT5}	I_{OUT5} = 10 mA, SEL_RUIM = 3.6 V	2.9	3.0	3.1	V
		I_{OUT5} = 10 mA, SEL_RUIM = 0 V	1.75	1.8	1.85	V
Temperature coefficient	ΔV_{OUT5}/°C			±100		ppm/°C
Maximum output current	I_{OUT5}		300	550		mA
Dropout voltage	V_{LDO5_DO}	I_{OUT5} = 50 mA		40	300	mV
Load regulation		I_{OUT5} = 10 mA to 50 mA		3	50	mV
Line regulation		V_{DD_IN3} = 3.0 V to 4.0 V, I_{OUT5} = 50 mA		0.1		%/V
	V_{NOISE}	I_{OUT5} = 50 mA, 10 Hz to 10 kHz		350		$μV_{RMS}$
		I_{OUT5} = 50 mA, 10 Hz to 10 kHz, C_{BYP} = 1 μF		60		$μV_{RMS}$
Power supply rejection ratio	$PSRR_{OUT5}$	f = 1 kHz, I_{OUT5} = 50 mA, V_{DD_IN3} = V_{OUT5} + 1 V		70		dB
		f = 10 kHz, I_{OUT5} = 50 mA, V_{DD_IN4} = V_{OUT5} + 1 V		50		dB
LDO6 (TCXO)						
Output voltage	V_{OUT6}	I_{OUT6} = 10 mA	2.77	2.85	2.93	V
Temperature coefficient	ΔV_{OUT6}/°C			±100		ppm/°C
Maximum output current	I_{OUT6}		300	500		mA
Dropout voltage	V_{LDO6_DO}	I_{OUT6} = 50 mA		50	150	mV
Load regulation		I_{OUT6} = 10 mA to 50 mA		3	50	mV
Line regulation		V_{DD_IN3} = 3.0 V to 4.0 V, I_{OUT6} = 50 mA		0.1		%/V
	V_{NOISE}	I_{OUT6} = 50 mA, 10 Hz to 10 kHz		350		$μV_{RMS}$
		I_{OUT6} = 50 mA, 10 Hz to 10 kHz, C_{BYP} = 1 μF		60		$μV_{RMS}$
Power supply rejection ratio	$PSRR_{OUT6}$	f = 1 kHz, I_{OUT6} = 50 mA, V_{DD_IN3} = V_{OUT6} + 1 V		70		dB
		f = 10 kHz, I_{OUT6} = 50 mA, V_{DD_IN3} = V_{OUT6} + 1 V		50		dB

Table 4. AAT2630 Electrical Specifications (4 of 5) (Note 1)
(V_{BUS} = V_{DD_IN1} = V_{DD_IN2} = V_{DD_IN3} = V_{DD_IN4} = 3.6 V, V_{POWER_ON} = 3.6 V, V_{EN_TCXO} = V_{EN_RUIM} = 3.6 V, V_{SEL_RUIM} = 3.6 V, C_{INB} = 10 μF, C_{OUTB} = 10 μF, C_{VREF} = 2.2 μF, C_{INL} = 4.7 μF, C_{OUTL} = 2.2 μF, C_{BYP} = 0.1 μF, C_{VBUS} = 0.47 μF, T_A = –40 °C to +85 °C, Typical Values are T_A = 25 °C, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
LDO7 (USB)						
Output voltage	V_{OUT7}	I_{OUT7} = 10 mA	3.00	3.10	3.20	V
Temperature coefficient	ΔV_{OUT7}/°C			±100		ppm/°C
Maximum output current	I_{OUT7}		75	150		mA
Dropout voltage	V_{LDO7_DO}	I_{OUT7} = 50 mA		80	150	mV
Load regulation		I_{OUT7} = 10 mA to 50 mA		3	50	mV
Line regulation		V_{DD_IN4} = 3.6 V to 5.0 V, I_{OUT7} = 50 mA		0.1		%/V
	V_{NOISE}	I_{OUT7} = 50 mA, 10 Hz to 10 kHz		350		μV_{RMS}
		I_{OUT7} = 50 mA, 10 Hz to 10 kHz, C_{BYP} = 1 μF		60		μV_{RMS}
Power supply rejection ratio	$PSRR_{OUT7}$	f = 1 kHz, I_{OUT7} = 50 mA, V_{BUS} = V_{OUT7} + 1 V		70		dB
		f = 10 kHz, I_{OUT7} = 50 mA, V_{BUS} = V_{OUT7} + 1 V		50		dB
LDO8 (RFRX)						
Output voltage	V_{OUT8}	I_{OUT8} = 10 mA	2.67	2.75	2.83	V
Temperature coefficient	ΔV_{OUT8}/°C			±100		ppm/°C
Maximum output current	I_{OUT8}		300	550		mA
Dropout voltage	V_{LDO8_DO}	I_{OUT8} = 150 mA		150	300	mV
Load regulation		I_{OUT8} = 10 mA to 150 mA		5	50	mV
Line regulation		V_{DD_IN4} = 3.6 V to 5.0 V, I_{OUT8} = 50 mA		0.1		%/V
	V_{NOISE}	I_{OUT8} = 50 mA, 10 Hz to 10 kHz		350		μV_{RMS}
		I_{OUT8} = 50 mA, 10 Hz to 10 kHz, C_{BYP} = 1 μF		60		μV_{RMS}
Power supply rejection ratio	$PSRR_{OUT8}$	f = 1 kHz, I_{OUT8} = 50 mA, V_{DD_IN4} = V_{OUT8} + 1 V		70		dB
		f = 10 kHz, I_{OUT8} = 50 mA, V_{DD_IN4} = V_{OUT8} + 1 V		50		dB
LED Driver						
LED supply voltage	V_{LED}			3.6	5	V
LED drive current	I_{LED}				10	mA
LED1, LED2, LED3 output low	V_{OL_LED}	I_{LED} = 5 mA			0.5	V

Table 4. AAT2630 Electrical Specifications (5 of 5) (Note 1)
(V_{BUS} = V_{DD_IN1} = V_{DD_IN2} = V_{DD_IN3} = V_{DD_IN4} = 3.6 V, V_{POWER_ON} = 3.6 V, V_{EN_TCXO} = V_{EN_RUIM} = 3.6 V, V_{SEL_RUIM} = 3.6 V, C_{INB} = 10 μF, C_{OUTB} = 10 μF, C_{VREF} = 2.2 μF, C_{INL} = 4.7 μF, C_{OUTL} = 2.2 μF, C_{BYP} = 0.1 μF, C_{VBUS} = 0.47 μF, T_A = –40 °C to +85 °C, Typical Values are T_A = 25 °C, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
TCXO Buffer						
19 M clock period	t_{TCXO_IN}			52.083		ns
19 M frequency	f_{TCXO_IN}			19.2		MHz
Start-up time (Note 2)	t_{EN_TCXO}	From EN_TCXO assertion		0.1	3.0	ms
Input amplitude	$V_{PP(TCXO\_IN)}$	At TCXO_IN, sine wave with 1000 pF coupling capacitor	0.5		2.0	V_{PP}
Input impedance	$Z_{IN(TCXO\_IN)}$	Parallel resistance	50			kΩ
		Parallel capacitance		2.0		pF
Output logic high	V_{OH}	I_{OH} = 5 mA	V_{OUT2} – 0.45			V
Output logic low	V_{OL}	I_{OL} = 5 mA			0.45	V
Output duty cycle (Note 2)		Sinusoid at TCXO_IN	43.5	50	56.5	%
High level, TCXO outputs	I_{OH_TCXO}		6.0			mA
Low level, TCXO outputs	I_{OL_TCXO}				-6.0	mA
Output rise time (Note 2)	$t_{RISE(TCXO\_OUT)}$	10% to 90%, C_{LOAD} < 25 pF	2	5	10	ns
Output fall time (Note 2)	$t_{FALL(TCXO\_OUT)}$	90% to 10%, C_{LOAD} < 25 pF	2	5	10	ns
Standby current of clock buffer (Note 2)	$I_{SBY(TCXO)}$	V_{EN_TCXO} = 0 V		500	1000	μA
32 kHz Clock						
32 kHz clock period (Note 2)	t_{SLEEP_OUT}		16.667	30.518	33.333	μs
32 kHz frequency	f_{SLEEP_OUT}			32.7645		kHz
Output logic high	V_{OH}	I_{OH} = 5 mA	V_{OUT2} – 0.45			V
Output logic low	V_{OL}	I_{OL} = 5 mA			0.45	V
Output duty cycle (Note 2)		Sinusoid at TCXO_IN	15	50	85	%
Output amplitude	$V_{PP(SLEEP\_OUT)}$		1.5		3.0	V_{PP}
Logic (LED_EN1, LED_EN2, LED_EN3, POWER_ON, EN_RUIM, SEL_RUIM, $\overline{RESET}$)						
Input logic high	V_{IH}		1.4			V
Input logic low	V_{IL}				0.4	V
OD output leakage	I_{OH}	Pull up to VREG_MSMP, leakage into output, $\overline{RESET}$			1	μA
Output logic low	V_{OL}	I_{OL} = 1 mA, $\overline{RESET}$			0.4	V
Power On Sequence						
Power-on event to MSMC enable	t1	Refer to Figure 14 for the power-on sequence on page 14.		6		ms
Regulator Settling Time	t2			122		μs
Delay between regulator turns on	t3			122		μs
Last LDO(VREF) on to $\overline{RESET}$ = High	t4			60		ms
$\overline{RESET}$ active to LDO(USB/MMC) on (Note 2)	t5			2.5	5	ms
Thermal						
Shutdown temperature	T_{SD}	Rising		140		°C
Hysteresis temperature	T_{HYS}	Falling		15		°C

Note 1: Performance is guaranteed only under the conditions listed in this table.

Note 2: Guaranteed by design.

Typical Performance Characteristics

V_{BUS} = V_{DD_IN1} = V_{DD_IN2} = V_{DD_IN3} = V_{DD_IN4} = 3.6 V, V_{POWER_ON} = 3.6 V, V_{EN_TCXO} = V_{EN_RUIM} = 3.6 V, V_{SEL_RUIM} = 3.6 V, C_{INB} = 10 μF, C_{OUTB} = 10 μF, C_{VREF} = 2.2 μF, C_{INL} = 4.7 μF, C_{OUTL} = 2.2 μF, C_{BYP} = 0.1 μF, C_{VBUS} = 0.47 μF, T_A = –40 °C to +85 °C, Typical Values are T_A = 25 °C, Unless Otherwise Noted

Typical performance characteristics of the AAT2630 are illustrated in Figures 3 through 12.

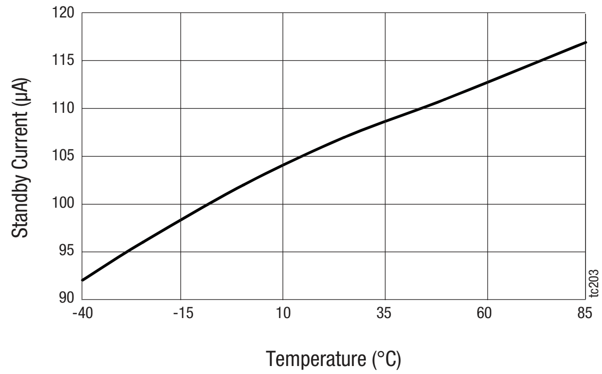

Figure 3. Standby Current vs Temperature (V_{IN} = 3.6 V)

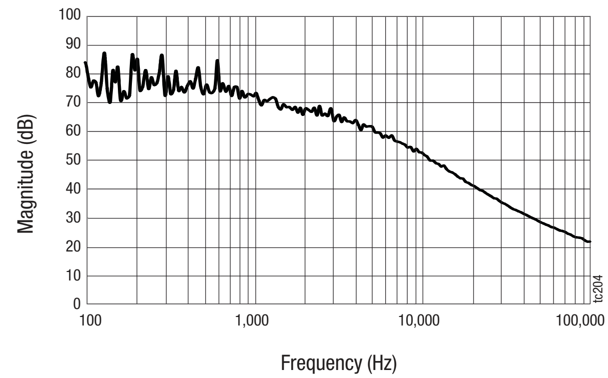

Figure 4. LDO Power Supply Rejection Ratio, PSRR (I_{OUT} = 50 mA)

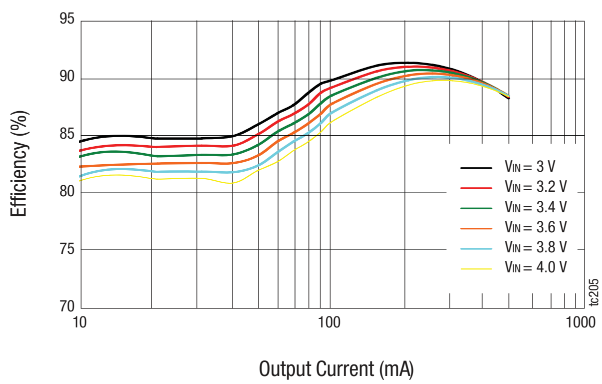

Figure 5. Buck1 Efficiency vs Output Current

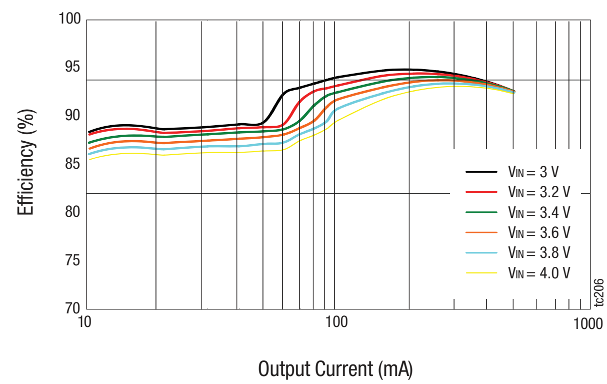

Figure 6. Buck2 Efficiency vs Output Current

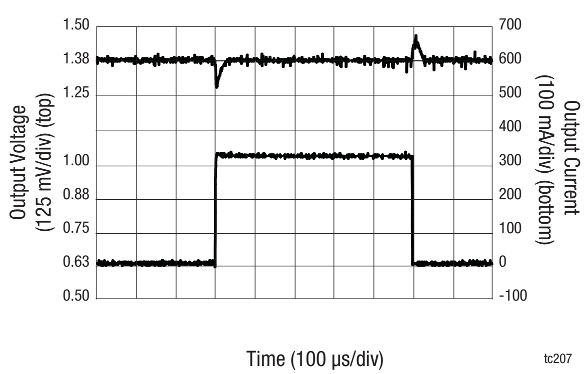

Figure 7. Buck1 Load Transient Response (V_{IN} = 3.6 V; I_{OUT} is 10 mA to 300 mA, V_{OUT} = 1.375 V; C_{OUT} = 4.7 μF)

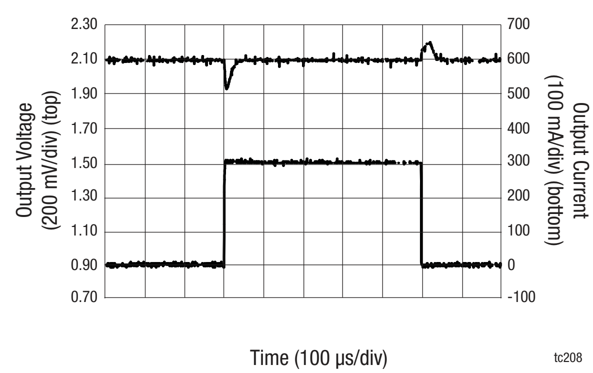

Figure 8. Buck2 Load Transient Response (V_{IN} = 3.6 V; I_{OUT} is 10 mA to 300 mA, V_{OUT} = 2.1 V; C_{OUT} = 4.7 μF)

Typical Performance Characteristics

V_{BUS} = V_{DD_IN1} = V_{DD_IN2} = V_{DD_IN3} = V_{DD_IN4} = 3.6 V, V_{POWER_ON} = 3.6 V, V_{EN_TCXO} = V_{EN_RUIM} = 3.6 V, V_{SEL_RUIM} = 3.6 V, C_{INB} = 10 μF, C_{OUTB} = 10 μF, C_{VREF} = 2.2 μF, C_{INL} = 4.7 μF, C_{OUTL} = 2.2 μF, C_{BYP} = 0.1 μF, C_{VBUS} = 0.47 μF, T_A = –40 °C to +85 °C, Typical Values are T_A = 25 °C, Unless Otherwise Noted

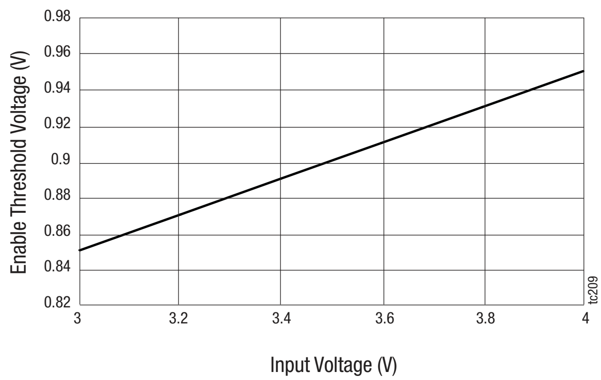

Figure 9. Power-On Threshold Voltage vs Input Voltage

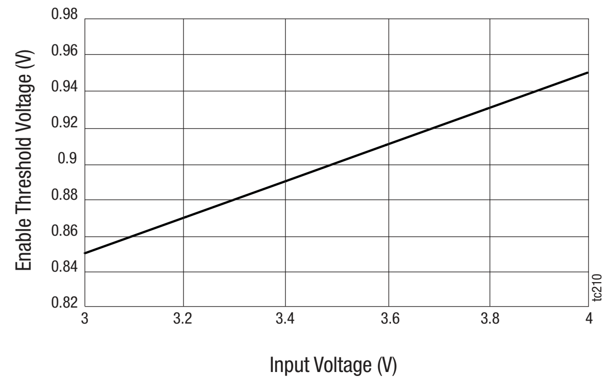

Figure 10. EN_RUIM Threshold Voltage vs Input Voltage

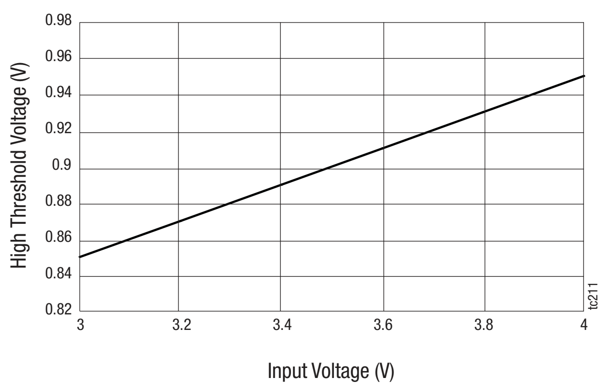

Figure 11. SEL_RUIM Threshold Voltage vs Input Voltage

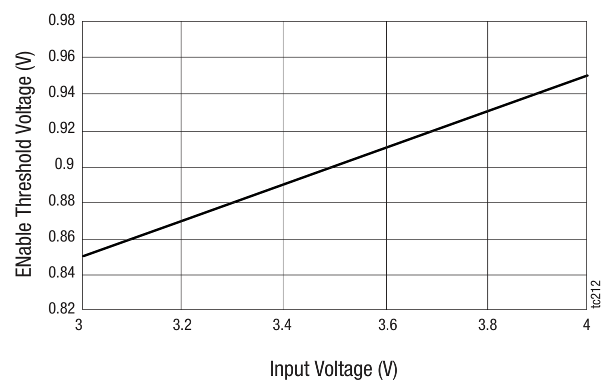

Figure 12. LED_EN Threshold Voltage vs Input Voltage

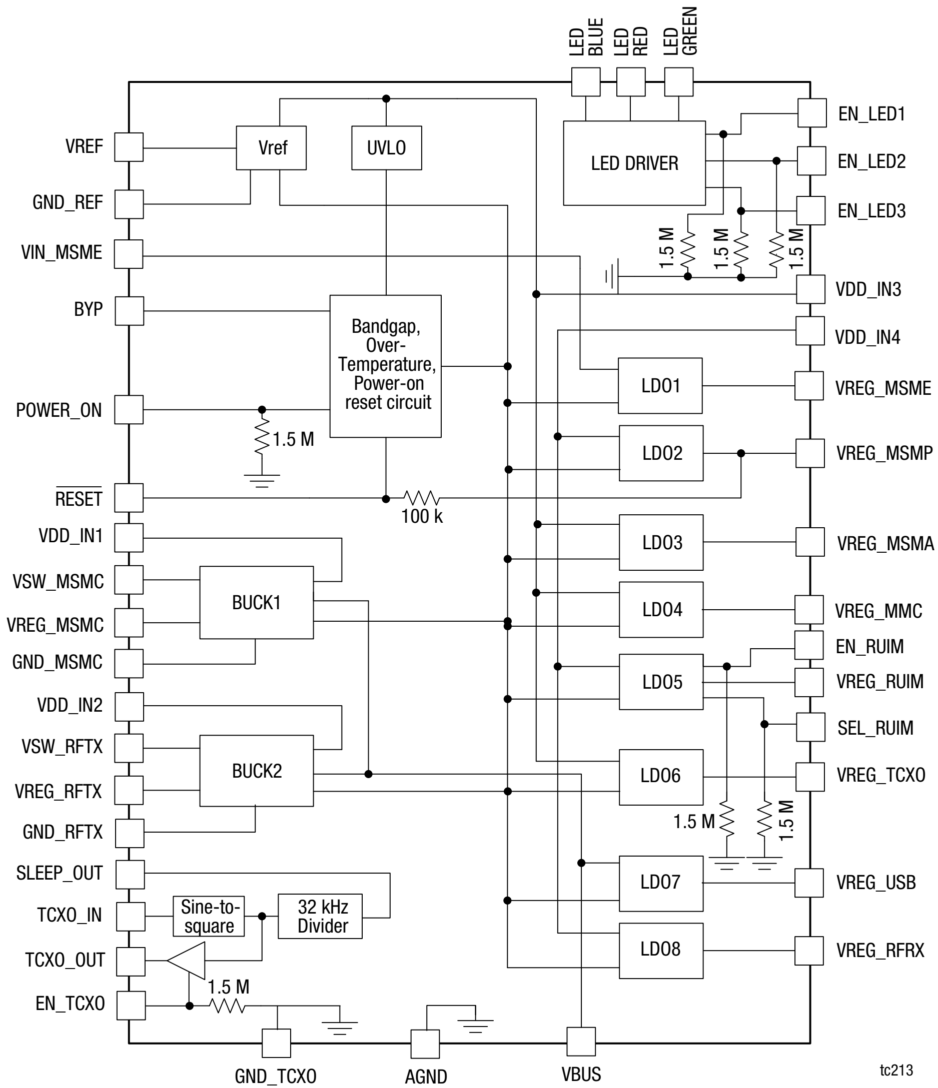

Figure 13. AAT2630 Functional Block Diagram

Functional Description

The AAT2630 is targeted for data cards, data modules, and on-board circuit blocks for wireless communication function. It is designed for half or mini-half PCI Express cards, Express Card modules, USB dongles and SDIO modules. The AAT2630 is sourced from a 3 V to 5.5 V power supply with supply currents ranging from 500 mA for USB 2.0, up to 2.7 A for half or mini-half PCI express cards. It has two high efficiency step-down converters to reduce power dissipation in space restricted modules. Automatic power-up and shutdown sequence feature is used in card slots without a power switch.

Figure 13 shows the functional block diagram for the AAT2630.

Enable and Selection Functions

The AAT2630 features five enable/disable functions for the three LEDs, LDO5 (REG_RUIM) and TCXO output that are controlled by LED_EN1, LED_EN2, LED_EN3, EN_RUIM and EN_TCXO. These signals are active high and are compatible with CMOS logic. The EN pin voltage level must be greater than 1.4 V to turn on the LED. The LED will turn off when the voltage on the EN pin falls below 0.4 V.

The AAT2630 also features a LDO regulator voltage selection function (SEL_RUIM) for LDO5 (REG_RUIM). With SEL_RUIM = 1 (high logic) the LDO5 output (REG_RUIM) will be set to 3V. When SEL_RUIM = 0 (low logic), the LDO5 output (REG_RUIM) is set to 1.8 V.

Power-on and Shutdown Sequence

The AAT2630 POWER_ON pin is used for power-on reset.

The AAT2630 starts the power on procedure when the POWER_ON pin is asserted. Upon POWER_ON assertion, Buck1 and Buck2 are enabled in sequence. When Buck2 is within 10%

of its' final regulation voltage, LDO_MSME, LDO_RFRX, LDO_MSMP, LDO_MSMA, LDO_TCXO and VREF are sequenced in cascade fashion – where each regulator is enabled after the previous regulator is within 10% of its final voltage.

After VREF is within 10% of its final voltage and the RESET delay expires, the RESET pin is released (RESET goes high). When RESET is de-asserted (High), LDO_USB and LDO_MMC are enabled. Note that once RESET is de-asserted it is latched in the high state, regardless of any of the regulators falling out of regulation, until the power on procedure starts again. The power on and shutdown sequence is shown in Figure 14.

TCXO Sequence

1. Once the AAT2630 LDO2 for MSMP starts to output 2.6 V, the external oscillator (TCXO) starts to generate a 19.2 MHz sine wave input signal. The setup time of the external oscillator is less than 6 ms.
2. After the 6 ms set-up time, the TCXO buffer can be enabled.
3. The 32.7645 kHz signal is generated from the 19.2 MHz signal in the AAT2630. There is no additional delay from 19.2 MHz input to the 32 kHz output.

The TCXO sequence is shown in Figure 15.

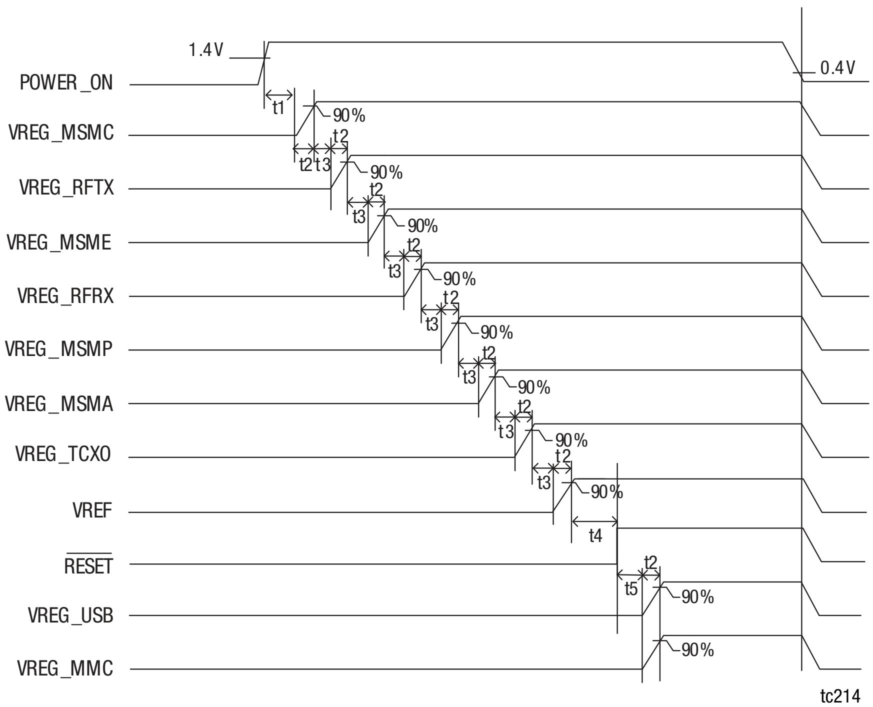

Figure 14. AAT2630 Power-On and Shutdown Timing Sequence

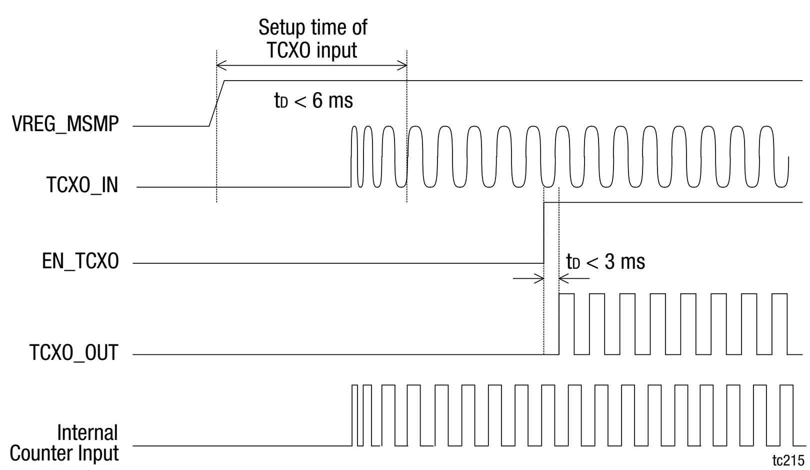

Figure 15. AAT2630 TCXO Timing Sequence

Application Information

The AAT2630 contains two buck regulators in close proximity and switching at high frequency. Its pad arrangement is carefully designed for easy placement and layout. Chip inductors should be placed in different directions to reduce the coupling between the regulators.

$\overline{\text{RESET}}$

$\overline{\text{RESET}}$ is an open-drain output with 100 kΩ pull up resistor to VREG_MSMP internally.

LED Indication

LED1 (LED_BLUE), LED2 (LED_RED) and LED3 (LED_GREEN) are open drain outputs which sink up to 10 mA current. This is a high current level for most LEDs. Optional resistors in series with the LEDs can restrict the current to a preferable level for specific LED selections.

Step-down Converter

Input Capacitor

Select a 10 μF X7R or X5R ceramic capacitor for the input. To estimate the required input capacitor size, determine the acceptable input ripple voltage level (V_{PP}) and solve for C using the equations shown below. The calculated value varies with input voltage and is a maximum when V_{IN} is double the output voltage.

$$C_{IN} = \frac{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}{\left(\frac{V_{PP}}{I_{OUT}} - ESR\right) \times f_{SW}}$$

$$C_{IN(MIN)} = \frac{1}{4 \times \left(\frac{V_{PP}}{I_{OUT}} - ESR\right) \times f_{SW}}$$

C_{IN} is the input capacitance, V_{IN} is the input voltage, V_{OUT} is the output voltage, f_{SW} is the switching frequency, I_{OUT} is the output current, and ESR is the equivalent series resistor of the input capacitor.

The maximum input capacitor RMS current is:

$$I_{RMS} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The input capacitor RMS ripple current varies with the input and output voltages and is always less than or equal to half of the total DC load current.

$$I_{RMS(MAX)} = \frac{I_{OUT}}{2}$$

The maximum input voltage ripple also appears at 50% duty cycle.

The input capacitor provides a low impedance loop for the edges of pulsed current drawn by the AAT2630. Low ESR/ESL X7R and X5R ceramic capacitors are ideal for this function. To minimize parasitic inductances, the capacitor should be placed as close as possible to the IC. This keeps the high frequency content of the input current localized, minimizing EMI and input voltage ripple.

The proper placement of the input capacitors (C2, C4) is shown in the evaluation board layout in Figure 18.

A laboratory test setup typically consists of two long wires running from the bench power supply to the evaluation board input voltage pins. The inductance of these wires, along with the low-ESR ceramic input capacitor, can create a high Q network that may affect converter performance, in the form of excessive ringing in the output voltage during load transients. Errors can also result in the loop phase and gain measurements. Since the inductance of a short PCB trace feeding the input voltage is significantly lower than the power leads from the bench power supply, most applications do not exhibit this problem.

In applications where the input power source lead inductance cannot be reduced to a level that does not affect the converter performance, place a high ESR tantalum or aluminum electrolytic capacitor in parallel with the low ESR/ESL bypass ceramic capacitor. This dampens the high Q network and stabilizes the system.

Output Capacitor

The output capacitor limits the output voltage ripple and provides holdup during large load transitions. A 4.7 μF X5R or X7R ceramic capacitor typically provides sufficient bulk capacitance to stabilize the output during large load transitions and has the ESR and ESL characteristics necessary for low output ripple voltage.

The output voltage droop due to a load transient is dominated by the capacitance of the ceramic output capacitor. During a step increase in load current, the ceramic output capacitor alone supplies the load current until the loop responds. Within two or three switching cycles, the loop responds and the inductor current increases to match the load current demand. The relationship of the output voltage droop during the three switching cycles to the output capacitance can be estimated by:

$$C_{OUT} = \frac{3 \times \Delta I_{LOAD}}{V_{DROOP} \times f_{SW}}$$

Once the average inductor current increases to the DC load level, the output voltage recovers. The above equation establishes a limit on the minimum value for the output capacitor with respect to load transients.

Output Inductor

For most designs, the AAT2630 operates with inductor values of 2.2 μH to 4.7 μH. Inductors with low inductance values are physically smaller but generate higher inductor current ripple leading to higher output voltage ripple. The inductor value can be derived from the following equation:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_{LOAD} \times f_{SW}}$$

Where ΔI_{LOAD} is inductor ripple current. Large value inductors result in lower ripple current and small value inductors result in high ripple current. Choose inductor ripple current approximately 30% of the maximum load current 0.5 A, or

$$\Delta I_{LOAD} = 150mA$$

Manufacturer's specifications list both the inductor DC current rating, which is a thermal limitation, and the peak current rating, which is determined by the saturation characteristics. The inductor should not show any appreciable saturation under normal load conditions. The DC current rating of the inductor should be at least equal to the maximum load current plus half the inductor ripple current to prevent core saturation (0.5 A + 150 mA).

Some inductors may meet the peak and average current ratings yet result in excessive losses due to a high DCR.

Always consider the losses associated with the DCR and its effect on the total converter efficiency when selecting an inductor.

Table 5 lists the recommended inductors.

Table 5. Recommended Inductors

Part	L (μH)	Max DCR (mΩ)	Rated DC Current (A)	Size W × L × H (mm)
Murata	2.2	73	1.25	3.0 × 3.0 × 1.4
	3.3	92	1.0	
	4.7	130	0.88	

Thermal Calculations

There are three types of losses associated with the AAT2630 step-down converters: switching losses (P_{SW}), conduction losses (P_{COND}), and quiescent current losses (P_{QC}). Conduction losses are associated with the $R_{DS(ON)}$ characteristics whereas switching losses are dominated by the gate charge of the power output switching devices. At full load, with continuous conduction mode (CCM), a simplified form of the losses is given by:

$$P_{BUCK} = P_{SW} + P_{COND} + P_{QC}$$

The three components of the total continuos conduction mode are given by:

$$P_{SW} = t_{SW} \times f_{SW} \times I_{OUT} \times V_{IN}$$

$$P_{COND} = I_{OUT}^2 \times \left[R_{DS(ON)P} \times \frac{V_{OUT}}{V_{IN}} + R_{DS(ON)N} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \right]$$

$$P_{QC} = I_{OUT} \times V_{IN}$$

Where I_Q is the step-down converter quiescent current, t_{SW} is the switching time, $R_{DS(ON)P}$ and $R_{DS(ON)N}$ are the high side and low side switching MOSFETs' on-resistance. V_{IN}, V_{OUT} and I_{OUT} are the input voltage, the output voltage and the load current.

Since $R_{DS(ON)}$, quiescent current and switching losses vary with input voltage, the total losses should be investigated over the complete input voltage range.

Given the total losses, the maximum junction temperature can be derived from the θ_{JA} for the package.

$$T_{J(MAX)} = P_{TOTAL} \times \theta_{JA} + T_A$$

Thermal Shutdown

Thermal overload protection limits the total power dissipation of the AAT2630. When internal thermal sensors detect a die temperature in excess of 140 °C all buck outputs are immediately shut down to allow the IC to cool. When the die temperature has dropped below the 15 °C hysteresis, the buck outputs automatically turn on again in sequence.

Low Drop Out Regulator

Input Capacitor

Typically, a 4.7 μF or larger capacitor is recommended for C_{IN} in most applications. A C_{IN} capacitor is not required for basic LDO regulator operation. However, if the LDO is physically located more than 1 or 2 centimeters from the input power source, a C_{IN} capacitor is needed for stable operation. C_{IN} should be located as close to the device input pin as practically possible. C_{IN} values greater than 4.7 μF offer superior input line transient response and assist in maximizing the power supply ripple rejection.

Ceramic, tantalum, or aluminum electrolytic capacitors may be selected for C_{IN} because there is no specific capacitor ESR requirement. For better performance, ceramic capacitors are recommended for C_{IN} due to their inherent capability over tantalum capacitors to withstand input current surges from low impedance sources such as batteries in portable devices.

Output Capacitor

For proper load voltage regulation and operational stability, a capacitor, C_{OUT}, is required between pins V_{OUT} and GND. The C_{OUT} capacitor connection to the LDO regulator ground pin should be made as direct as practically possible for maximum device performance. Although the AAT2630 LDOs have been specifically designed to function with very low ESR ceramic capacitors, the device is stable over a very wide range of capacitor ESR. The AAT2630 also works with some higher ESR tantalum or aluminum electrolytic capacitors. For best performance, ceramic capacitors are recommended.

The value of C_{OUT} typically ranges from 1 μF to 10 μF; however, 2.2 μF is sufficient for most operating conditions.

Short-Circuit and Thermal Protection

The AAT2630 LDOs are protected by both current limit and over-temperature protection circuitry. The internal short-circuit current limit is designed to activate when the output load demand exceeds the maximum rated output. If a short-circuit condition continually draws more than the current limit threshold, the LDO regulator's output voltage drops to a level necessary to supply the current demanded by the load. Under short-circuit or other over-current operating conditions, the output voltage drops, and the AAT2630's die temperature rapidly increases. Once the regulator's power dissipation capacity has been exceeded and the internal die temperature reaches approximately 140 °C, the system thermal protection circuit becomes active. The internal thermal protection circuit actively turns off the LDO regulator output pass device to prevent the possibility of over-temperature damage. The LDO regulator output remains in a shutdown state until the internal die temperature falls back below the 125 °C trip point.

The interaction between short circuit and thermal protection systems allows the LDO regulator to withstand indefinite short-circuit conditions without sustaining permanent damage.

No-Load Stability

The AAT2630 LDO is designed to maintain output voltage regulation and stability under operational no-load conditions. This is an important characteristic for applications where the output current may drop to zero. An output capacitor is required for stability under no-load operating conditions. Refer to the Output Capacitor section of this datasheet for recommended typical output capacitor values.

LDO Minimum Input Voltage

The power supply of the LDO has to be at least the V_{OUT} (nominal) + V_{LDOX_DO} to regulate the output voltage. If the power supply is lower than the V_{OUT} (nominal) value, the output voltage will be $V_{IN} - V_{LDOX\_DO}$.

For example, if the LDO output is 3.3V, V_{LDOX_DO} = 150 mV, V_{IN} should be larger than 3.3 + 0.150 = 3.45 (V). If V_{IN} = 3.2 V, then V_{OUT} is 3.2 – 0.15 = 3.05 (V).

Figure 16 indicates the typical applications.

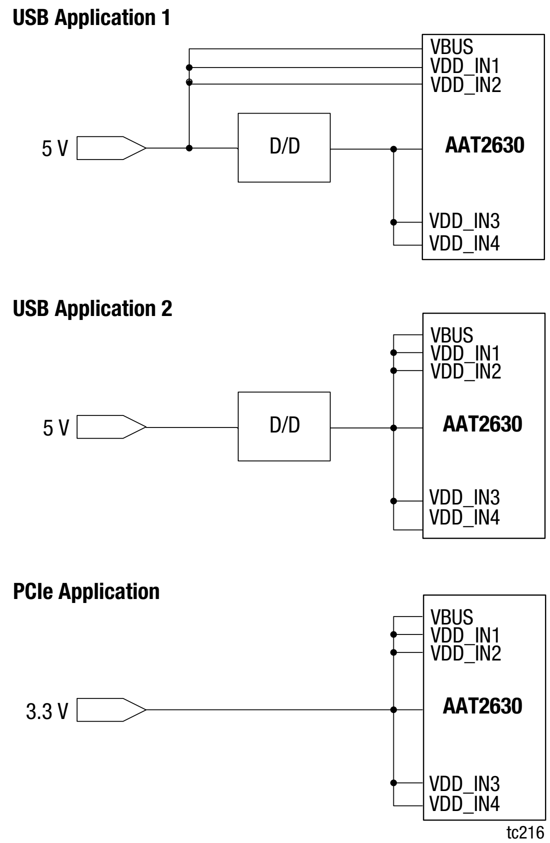

Figure 16. AAT2630 Typical Application Conditions

Layout Considerations

The suggested PCB layout for the AAT2630 is shown in Figures 5 to 10. The following guidelines are recommended to ensure a proper layout:

- Keep the power traces (GND, LX, IN) short, direct, and wide to allow large current flow. Place sufficient multiple-layer pads when needed to change the trace layer.
- Connect the output capacitors C3, C5 and inductors L1, L2 as close as possible. Keep the connection of L1, L2 to the LX1, LX2 pins as short as possible and route no signal lines under the inductors.
- Separate OUT pins (B1, G4) from any power trace and connect as close as possible to the load point. Sensing along a high-current load trace will degrade DC load regulation.
- Keep the resistance of the trace from the load returns to PGND to a minimum. This will help to minimize any error in DC regulation due to differences in the potential of the internal signal ground and the power ground.
- Connect the ground pin to PGND with a single point to decrease the effect of large power ground noise on the analog ground.

Evaluation Board Description

The AAT2630 Evaluation Board is used to test the performance of the AAT2630. An Evaluation Board schematic diagram is provided in Figure 17. Layer details for the Evaluation Board are shown in Figure 18. The Evaluation Board has additional components for easy evaluation; the actual bill of materials required for the system is shown in Table 6. Table 7 explains the terms and acronyms.

Package Information

Package dimensions for the 49-bump WLCSP package are shown in Figure 19.

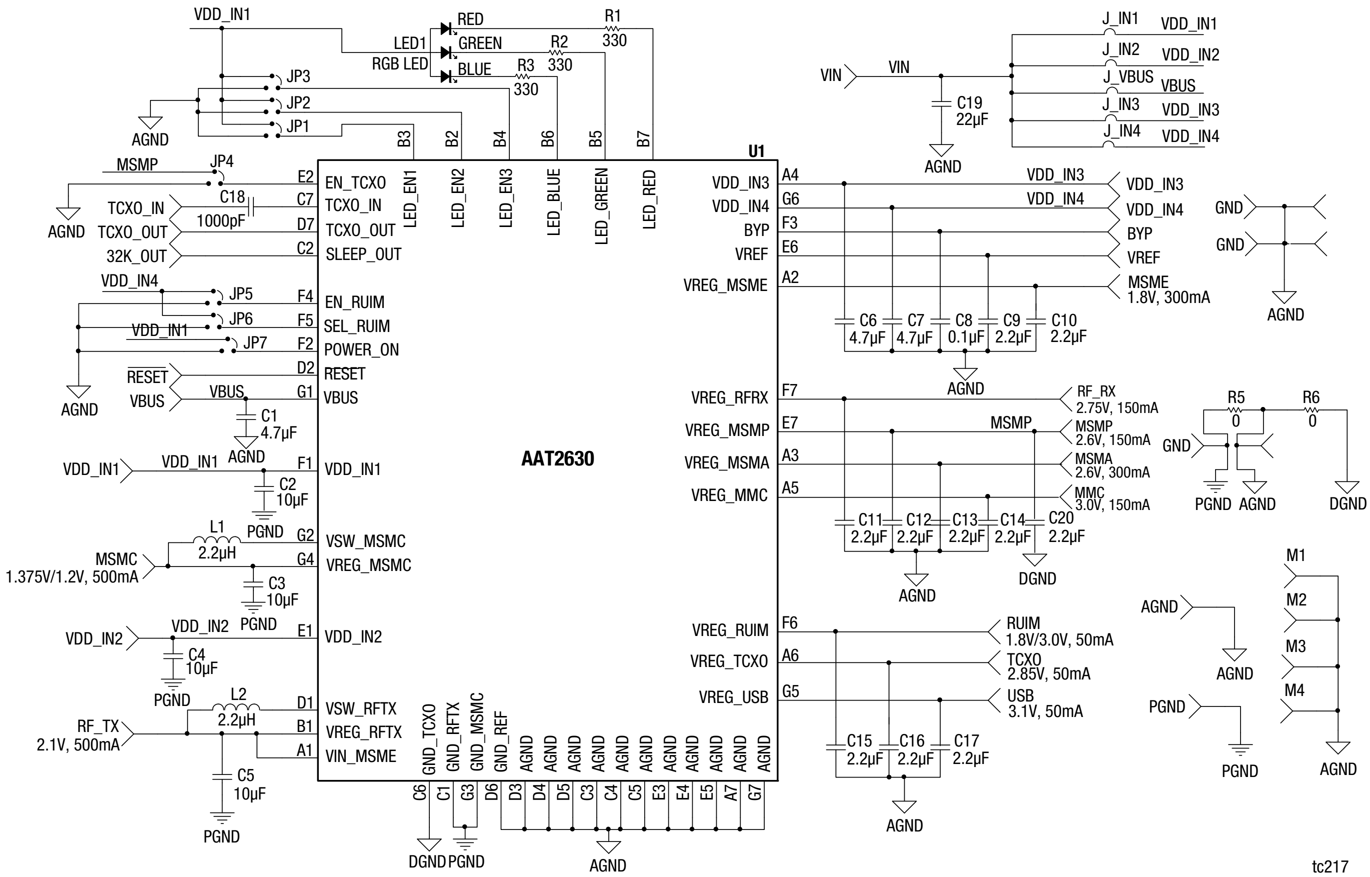

Figure 17. AAT2630 Evaluation Board Schematic

Table 6. AAT2630 Evaluation Board Bill of Materials (BOM)

Component	Part number	Description	Manufacturer
U1	AAT2630	10-channel DC-DC converter	Skyworks
C1, C6, C7	GRM188R60J475KE19	Ceramic capacitor, 4.7 μF, 0603 X5R, 6.3 V 10%	Murata
C2, C3, C4, C5	GRM21BR71A106KE51	Ceramic capacitor, 10 μF, 0805 X7R, 10 V 10%	Murata
C8	GRM188R71E104KA01	Ceramic capacitor, 0.1 μF, 0603 X7R, 25 V 10%	Murata
C9 ~ C17, C20	GCM188R70J225KE22	Ceramic capacitor, 2.2 μF, 0603, X7R, 6.3 V,10%	Murata
C18	GRM188R71H102KA01	Ceramic capacitor, 1000 pF, 0603 X7R, 50 V 10%	Murata
C19	GRM31CR71A226ME15	Ceramic capacitor, 22 μF, 1206 X7R, 10 V 10%	Murata
L1, L2	LQH3NPN2R2MM0L	2.2 μH, 73 mΩ, 1.25 A, 20%	Murata
R1, R2, R3	Chip resistor	RES 330 Ω, 1/10 W, 1% 0603 SMD	Yageo
LED1	1615LPCFC-A	Common anode type RGB LED	Lasemtech

Table 7. Terms and Acronyms

Term or Acronym	Definition
MMC	Multi-media card
MSMA	Mobile station modem analog
MSMC	Mobile station modem core
MSMP	Mobile station modem peripheral
RFTX	Radio frequency transmitter
RFRX	Radio frequency receiver
RUIM	Removable user identity module
TCXO	Temperature-compensated crystal oscillator
USB	Universal serial bus

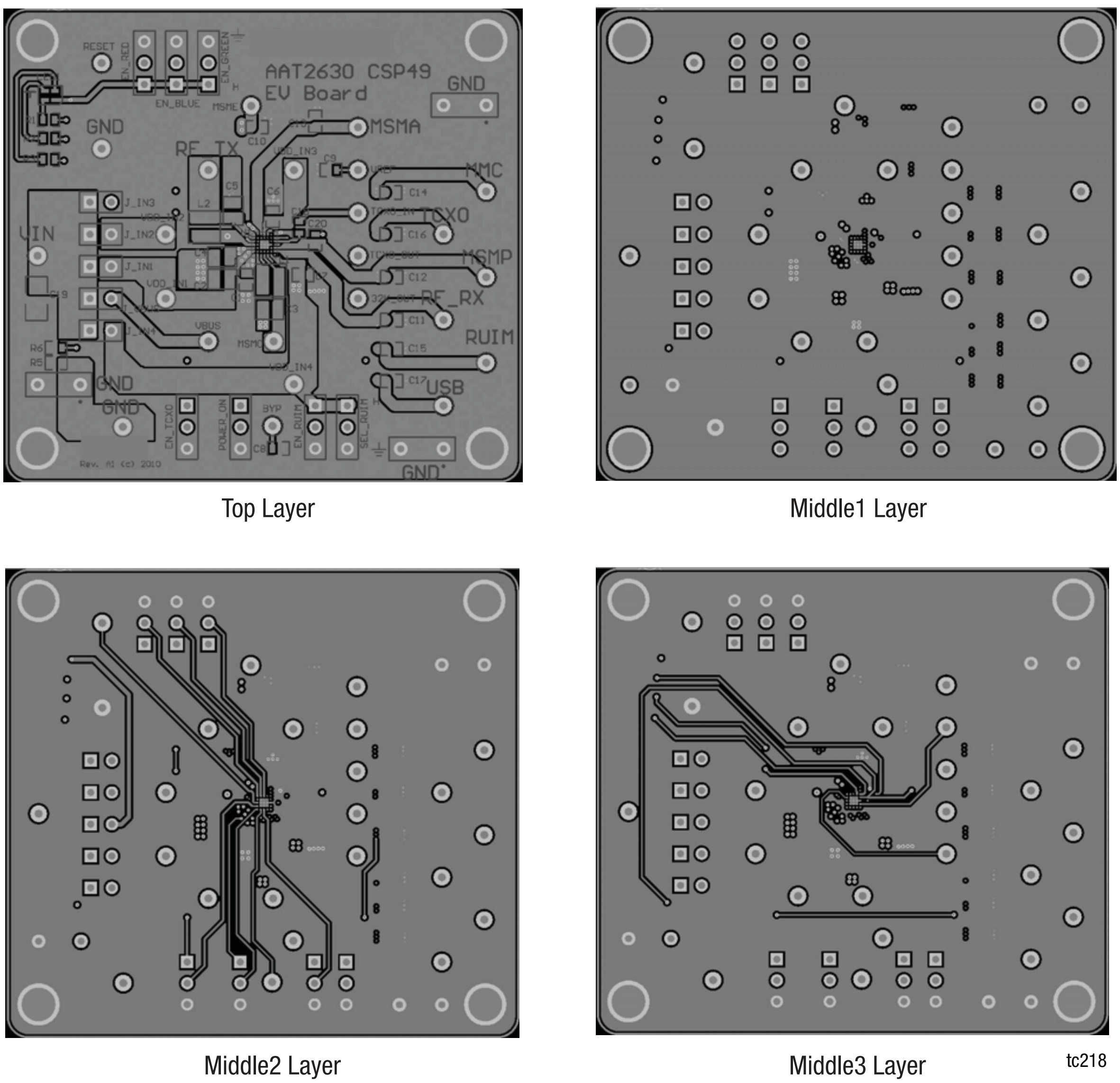

Figure 18. AAT2630 Evaluation Board Layer Details

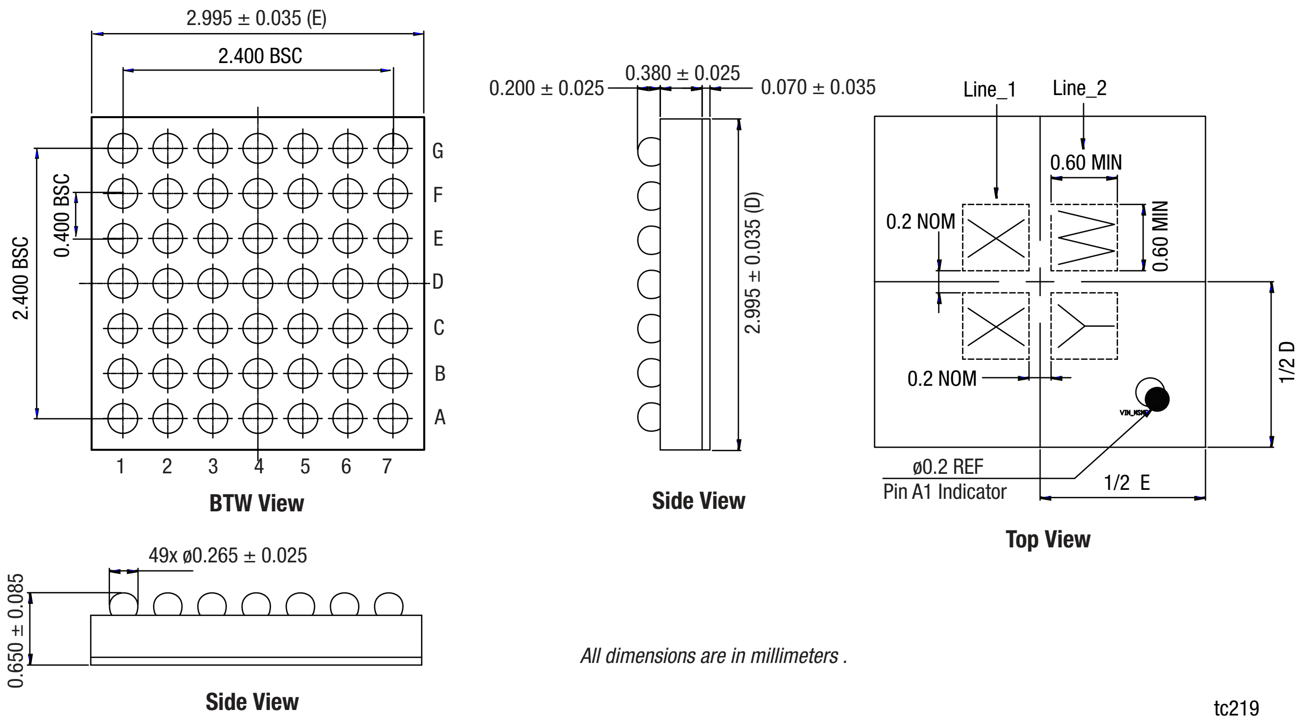

Figure 19. AAT2630 49-bump WLCSP Package Dimensions

Ordering Information

Model Name	Part Marking (Note 1)	Manufacturing Part Number (Note 2)	Evaluation Board Part Number
AAT2630 wireless data card PMIC 10-channel DC/DC converter	P8XY	**AAT2630IUA-T1**	AAT2630IUA-EVB

Note 1: XY = assembly and date code.

Note 2: Sample stock is generally held on part numbers listed in **BOLD**.