NOT RECOMMENDED FOR NEW DESIGNS
POSSIBLE SUBSTITUTE PRODUCTS
(ISL6614, ISL6614A, and ISL6614B)

Dual Channel Synchronous Rectified Buck MOSFET Driver

The HIP6602A is a high frequency, two power channel MOSFET driver specifically designed to drive four power N-Channel MOSFETs in a synchronous rectified buck converter topology. This device is available in either a 14 lead SOIC or a 16 lead QFN package with a PAD to thermally enhance the package. These drivers combined with a HIP63xx or ISL65xx series of Multi-Phase Buck PWM controllers and MOSFETs form a complete core voltage regulator solution for advanced microprocessors.

The HIP6602A drives both upper and lower gates over a range of 5V to 12V. This drive-voltage flexibility provides the advantage of optimizing applications involving trade-offs between switching losses and conduction losses.

The output drivers in the HIP6602A have the capacity to efficiently switch power MOSFETs at high frequencies. Each driver is capable of driving a 3000pF load with a 30ns propagation delay and 50ns transition time. This device implements bootstrapping on the upper gates with only a single external capacitor required for each power channel. This reduces implementation complexity and allows the use of higher performance, cost effective, N-Channel MOSFETs. Adaptive shoot-through protection is integrated to prevent both MOSFETs from conducting simultaneously.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. DWG #
HIP6602ACB	0 to 85	14 Ld SOIC	M14.15
HIP6602ACB-T	14 Ld SOIC Tape and Reel		
HIP6602ACR	0 to 85	16 Ld 5x5 QFN	L16.5x5
HIP6602ACR-T	16 Ld 5x5 QFN Tape and Reel		

Features

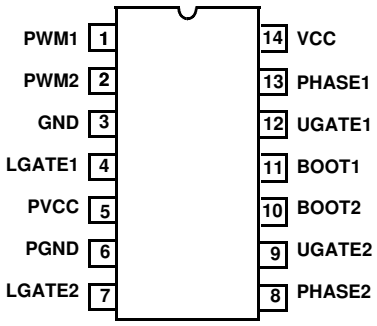
- Drives Four N-channel MOSFETs
- Adaptive Shoot-Through Protection
- Internal Bootstrap Devices
- Supports High Switching Frequency
  - Fast Output Rise Time
  - Propagation Delay 30ns
- Small 14-Lead SOIC Package
- Smaller 16-Lead QFN Thermally Enhanced Package
- 5V to 12V Gate-Drive Voltages for Optimal Efficiency
- Three-State Input for Bridge Shutdown
- Supply Under-Voltage Protection

Applications

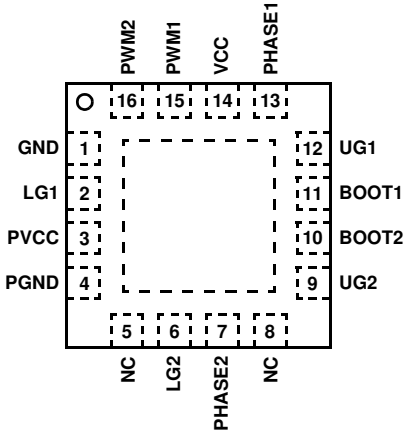
- Core Voltage Supplies for Intel Pentium® III and AMD® Athlon™ Microprocessors.
- High Frequency Low Profile DC/DC Converters
- High Current Low Voltage DC/DC Converters

Pinout

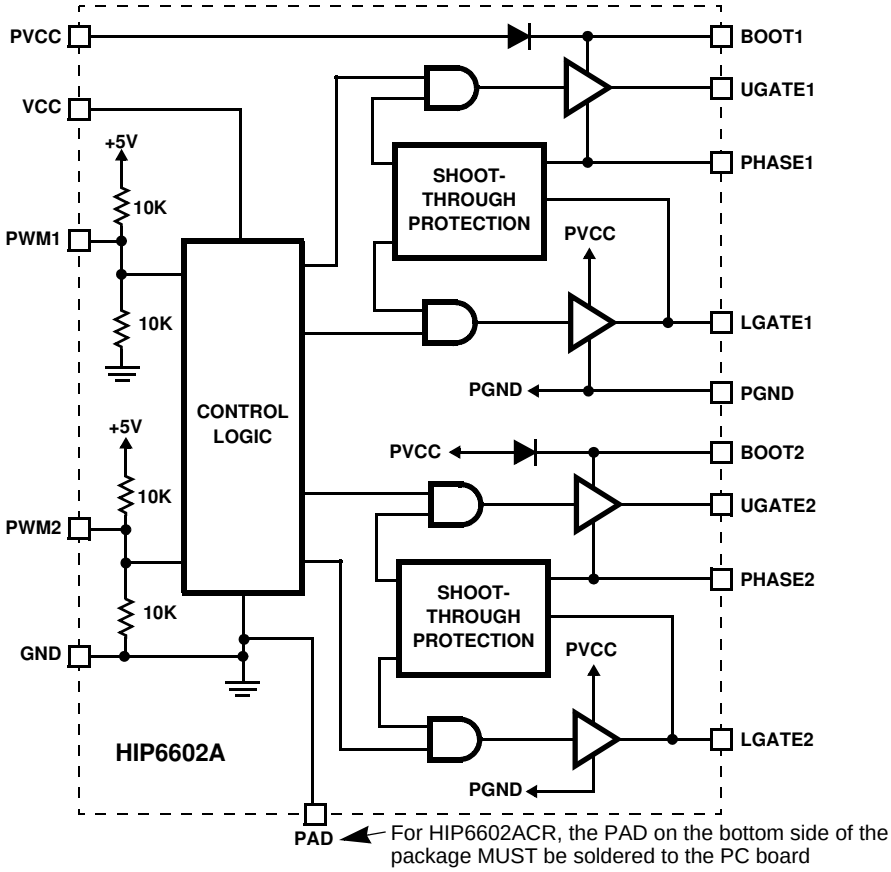
HIP6602ACB (SOIC)
TOP VIEW



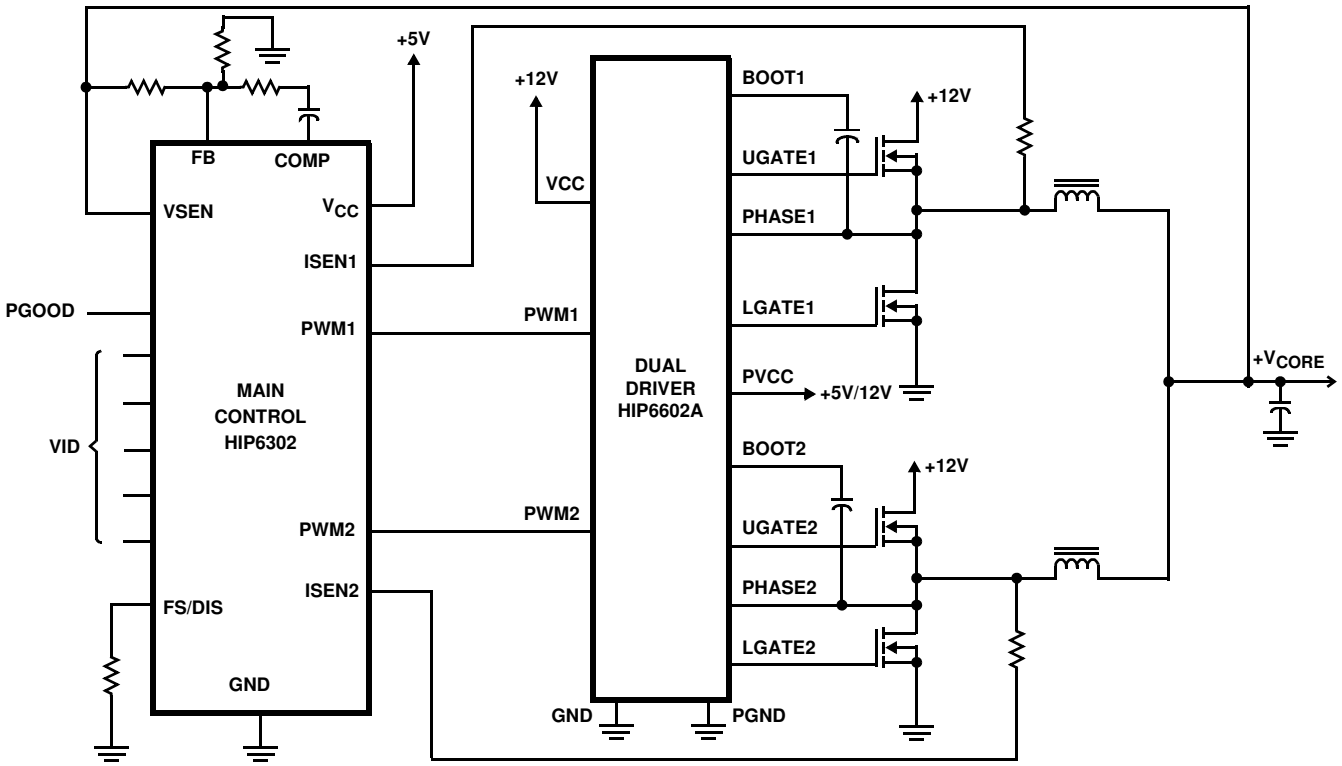
HIP6602ACR (16 LEAD QFN)
TOP VIEW



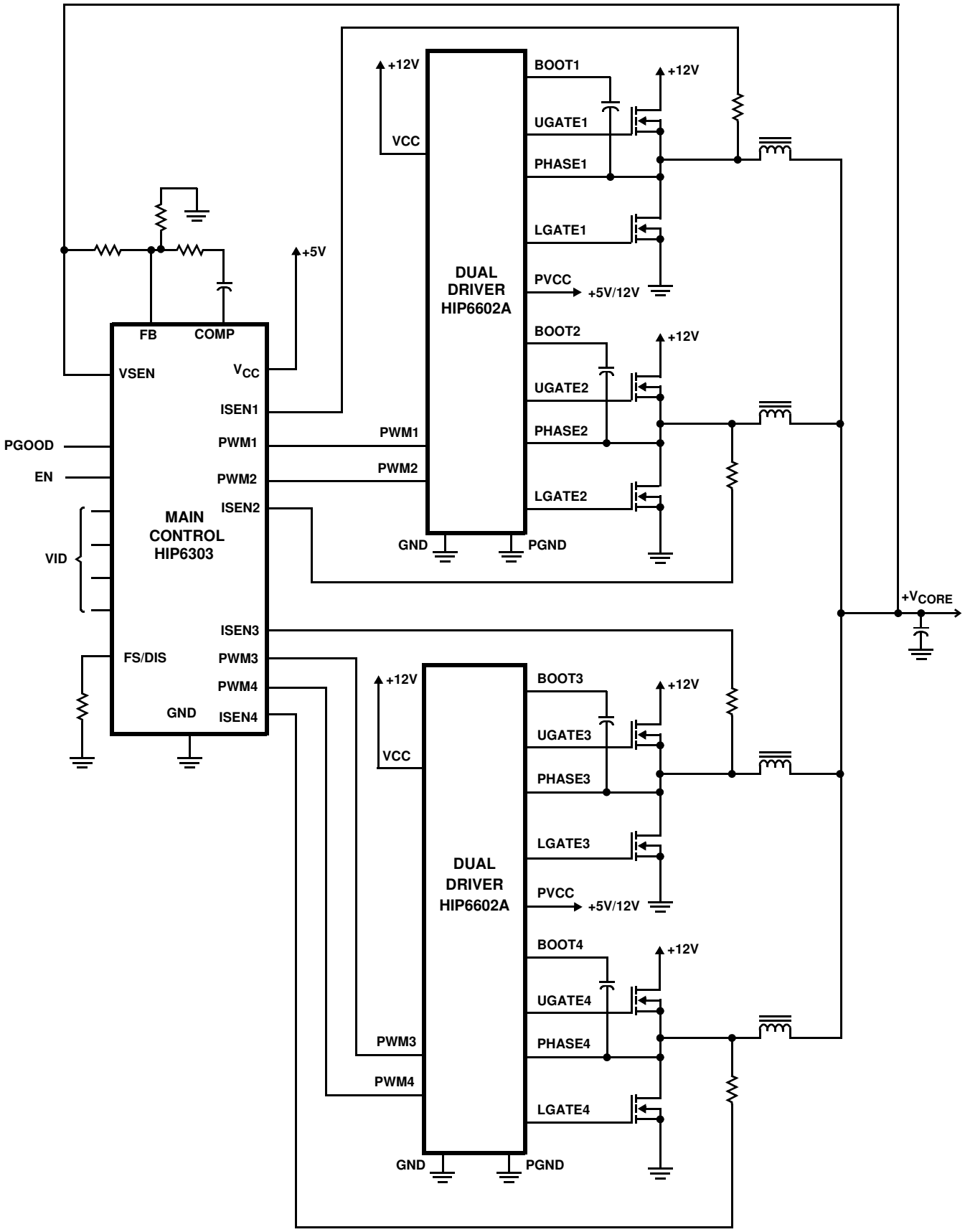
Block Diagram



Typical Application - 2 Channel Converter Using a HIP6302 and a HIP6602A Gate Driver



Typical Application - 4 Channel Converter Using a HIP6303 and HIP6602A Gate Driver



Absolute Maximum Ratings

Supply Voltage (VCC) 15V
Supply Voltage (PVCC) . . . . . VCC + 0.3V
BOOT Voltage (V_{BOOT} - V_{PHASE}) 15V
Input Voltage (VPWM) . . . . . GND - 0.3V to 7V
UGATE. . . . . V_{PHASE} - 0.3V to V_{BOOT} + 0.3V
LGATE . . . . . GND - 0.3V to V_{PVCC} + 0.3V
ESD Rating
Human Body Model (Per MIL-STD-883 Method 3015.7) 3kV
Machine Model (Per EIAJ ED-4701 Method C-111) 200V

Operating Conditions

Ambient Temperature Range. . . . . 0°C to 85°C
Maximum Operating Junction Temperature. . . . . .125°C
Supply Voltage, VCC . . . . . 12V ±10%
Supply Voltage Range PVCC . . . . . 5V to 12V

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
SOIC Package (Note 1)	68	NA
QFN Package (Note 2).	36	6

Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)
For Recommended soldering conditions see Tech Brief TB389.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
2. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. θ_{JC}, the "case temp" is measured at the center of the exposed metal pad on the package underside. See Tech Brief TB379.

Electrical Specifications Recommended Operating Conditions, Unless Otherwise Noted

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VCC SUPPLY CURRENT						
Bias Supply Current	I_{VCC}	f_{PWM} = 500kHz, V_{PVCC} = 12V	-	3.7	5.0	mA
Power Supply Current	I_{PVCC}	f_{PWM} = 500kHz, V_{PVCC} = 12V	-	2.0	4.0	mA
POWER-ON RESET						
VCC Rising Threshold			9.7	9.95	10.4	V
VCC Falling Threshold			9.0	9.2	9.5	V
PWM INPUT						
Input Current	I_{PWM}	V_{PWM} = 0 or 5V (See Block Diagram)	-	500	-	µA
PWM Rising Threshold		V_{PVCC} = 12V	3.45	3.6	-	V
PWM Falling Threshold		V_{PVCC} = 12V	-	1.45	1.55	V
UGATE Rise Time	TR_{UGATE}	V_{PVCC} = V_{VCC} = 12V, 3nF Load	-	20	-	ns
LGATE Rise Time	TR_{LGATE}	V_{PVCC} = V_{VCC} = 12V, 3nF Load	-	50	-	ns
UGATE Fall Time	TF_{UGATE}	V_{PVCC} = V_{VCC} = 12V, 3nF Load	-	20	-	ns
LGATE Fall Time	TF_{LGATE}	V_{PVCC} = V_{VCC} = 12V, 3nF Load	-	20	-	ns
UGATE Turn-Off Propagation Delay	$TPDL_{UGATE}$	V_{PVCC} = V_{VCC} = 12V, 3nF Load	-	30	-	ns
LGATE Turn-Off Propagation Delay	$TPDL_{LGATE}$	V_{PVCC} = V_{VCC} = 12V, 3nF Load	-	20	-	ns
Shutdown Window			1.4	-	3.6	V
Shutdown Holdoff Time			-	230	-	ns
OUTPUT						
Upper Drive Source Impedance	R_{UGATE}	V_{VCC} = 12V, V_{PVCC} = 5V	-	1.7	3.0	Ω
		V_{VCC} = V_{PVCC} = 12V	-	3.0	5.0	Ω
Upper Drive Sink Impedance	R_{UGATE}	V_{VCC} = 12V, V_{PVCC} = 5V	-	2.3	4.0	Ω
		V_{VCC} = V_{PVCC} = 12V	-	1.1	2.0	Ω
Lower Drive Source Current	I_{LGATE}	V_{VCC} = 12V, V_{PVCC} = 5V	400	580	-	mA
		V_{VCC} = V_{PVCC} = 12V	500	730	-	mA
Lower Drive Sink Impedance	R_{LGATE}	V_{VCC} = 12V, V_{PVCC} = 5V or 12V	-	1.6	4.0	Ω

Functional Pin Descriptions

PWM1 (Pin 1) and PWM2 (Pin 2)

The PWM signal is the control input for the driver. The PWM signal can enter three distinct states during operation, see the three-state PWM Input section under DESCRIPTION for further details. Connect this pin to the PWM output of the controller.

GND (Pin 3)

Bias and reference ground. All signals are referenced to this node.

LGATE1 (Pin 4) and LGATE2 (Pin 7)

Lower gate drive outputs. Connect to gates of the low-side power N-Channel MOSFETs.

PVCC (Pin 5)

This pin supplies the upper and lower gate drivers bias. Connect this pin from +12V down to +5V.

PGND (Pin 6)

This pin is the power ground return for the lower gate drivers.

PHASE2 (Pin 8) and PHASE1 (Pin 13)

Connect these pins to the source of the upper MOSFETs and the drain of the lower MOSFETs. The PHASE voltage is monitored for adaptive shoot-through protection. These pins also provide a return path for the upper gate drive.

UGATE2 (Pin 9) and UGATE1 (Pin 12)

Upper gate drive outputs. Connect to gate of high-side power N-Channel MOSFETs.

BOOT 2 (Pin 10) and BOOT 1 (Pin 11)

Floating bootstrap supply pins for the upper gate drivers. Connect the bootstrap capacitor between these pins and the PHASE pin. The bootstrap capacitor provides the charge to turn on the upper MOSFETs. See the Internal Bootstrap Device section under DESCRIPTION for guidance in choosing the appropriate capacitor value.

VCC (Pin 14)

Connect this pin to a +12V bias supply. Place a high quality bypass capacitor from this pin to GND. To prevent forward biasing an internal diode, this pin should be more positive then PVCC during converter start-up.

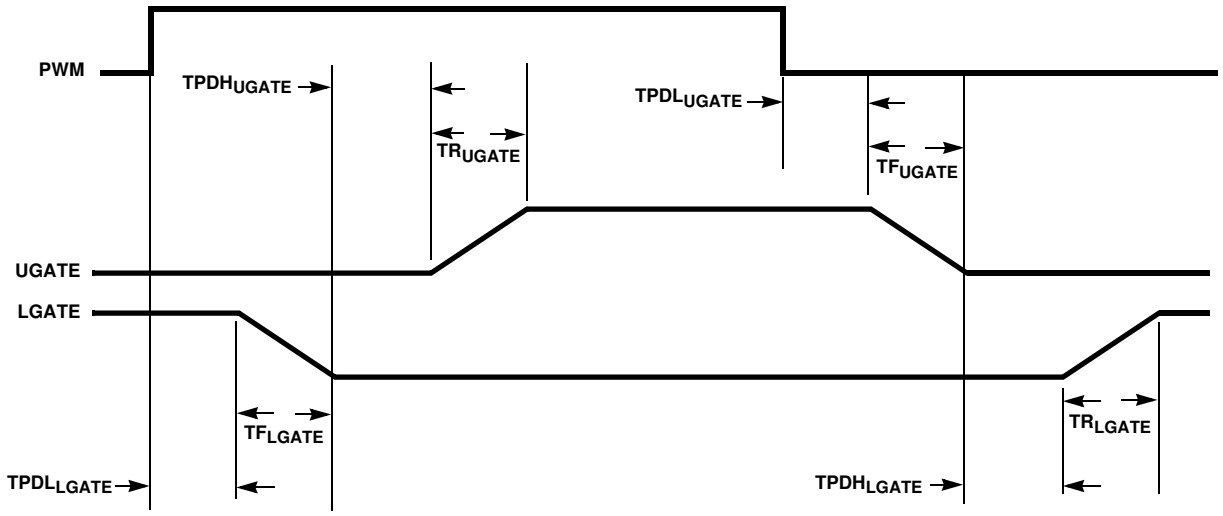
Description

Operation

Designed for versatility and speed, the HIP6602A two channel, dual MOSFET driver controls both high-side and low-side N-Channel FETs from two externally provided PWM signals.

The upper and lower gates are held low until the driver is initialized. Once the VCC voltage surpasses the VCC Rising Threshold (See Electrical Specifications), the PWM signal takes control of gate transitions. A rising edge on PWM initiates the turn-off of the lower MOSFET (see Timing Diagram). After a short propagation delay [$TPDL_{LGATE}$], the lower gate begins to fall. Typical fall times [TF_{LGATE}] are provided in the Electrical Specifications section. Adaptive shoot-through circuitry monitors the LGATE voltage and determines the upper gate delay time [$TPDH_{UGATE}$] based on how quickly the LGATE voltage drops below 2.2V. This prevents both the lower and upper MOSFETs from conducting simultaneously or shoot-through. Once this delay period is complete the upper gate drive begins to rise [TR_{UGATE}] and the upper MOSFET turns on.

Timing Diagram



A falling transition on PWM indicates the turn-off of the upper MOSFET and the turn-on of the lower MOSFET. A short propagation delay [$TPDL_{UGATE}$] is encountered before the upper gate begins to fall [TF_{UGATE}]. Again, the adaptive shoot-through circuitry determines the lower gate delay time, $TPDH_{LGATE}$. The PHASE voltage is monitored and the lower gate is allowed to rise after PHASE drops below 0.5V. The lower gate then rises [TR_{LGATE}], turning on the lower MOSFET.

Three-State PWM Input

A unique feature of the HIP6602A drivers is the addition of a shutdown window to the PWM input. If the PWM signal enters and remains within the shutdown window for a set holdoff time, the output drivers are disabled and both MOSFET gates are pulled and held low. The shutdown state is removed when the PWM signal moves outside the shutdown window. Otherwise, the PWM rising and falling thresholds outlined in the ELECTRICAL SPECIFICATIONS determine when the lower and upper gates are enabled.

Adaptive Shoot-Through Protection

The drivers incorporate adaptive shoot-through protection to prevent upper and lower MOSFETs from conducting simultaneously and shorting the input supply. This is accomplished by ensuring the falling gate has turned off one MOSFET before the other is allowed to rise.

During turn-off of the lower MOSFET, the LGATE voltage is monitored until it reaches a 2.2V threshold, at which time the UGATE is released to rise. Adaptive shoot-through circuitry monitors the PHASE voltage during UGATE turn-off. Once PHASE has dropped below a threshold of 0.5V, the LGATE is allowed to rise. If the PHASE does not drop below 0.5V within 250ns, LGATE is allowed to rise. This is done to generate the bootstrap refresh signal. PHASE continues to be monitored during the lower gate rise time. If the PHASE voltage exceeds the 0.5V threshold during this period and remains high for longer than 2µs, the LGATE transitions low. This is done to make the lower MOSFET emulate a diode. Both upper and lower gates are then held low until the next rising edge of the PWM signal.

Power-On Reset (POR) Function

During initial start-up, the VCC voltage rise is monitored and gate drives are held low until a typical VCC rising threshold of 9.95V is reached. Once the rising VCC threshold is exceeded, the PWM input signal takes control of the gate drives. If VCC drops below a typical VCC falling threshold of 9.2V during operation, then both gate drives are again held low. This condition persists until the VCC voltage exceeds the VCC rising threshold.

Internal Bootstrap Device

Both drivers feature an internal bootstrap device. Simply adding an external capacitor across the BOOT and PHASE pins completes the bootstrap circuit.

The bootstrap capacitor must have a maximum voltage rating above PVCC + 5V. The bootstrap capacitor can be chosen from the following equation:

$$C_{BOOT} \geq \frac{Q_{GATE}}{\Delta V_{BOOT}}$$

Where Q_{GATE} is the amount of gate charge required to fully charge the gate of the upper MOSFET. The ΔV_{BOOT} term is defined as the allowable droop in the rail of the upper drive.

As an example, suppose a HUF76139 is chosen as the upper MOSFET. The gate charge, Q_{GATE}, from the data sheet is 65nC for a 10V upper gate drive. We will assume a 200mV droop in drive voltage over the PWM cycle. We find that a bootstrap capacitance of at least 0.325µF is required. The next larger standard value capacitance is 0.33µF.

Gate Drive Voltage Versatility

The HIP6602A provides the user flexibility in choosing the gate drive voltage. Simply applying a voltage from 5V up to 12V on PVCC will set both driver rail voltages.

Power Dissipation

Package power dissipation is mainly a function of the switching frequency and total gate charge of the selected MOSFETs. Calculating the power dissipation in the driver for a desired application is critical to ensuring safe operation. Exceeding the maximum allowable power dissipation level will push the IC beyond the maximum recommended operating junction temperature of 125°C. The maximum allowable IC power dissipation for the 14 lead SOIC package is approximately 1000mW. Improvements in thermal transfer may be gained by increasing the PC board copper area around the HIP6602A. Adding a ground pad under the IC to help transfer heat to the outer peripheral of the board will help. Also keeping the leads to the IC as wide as possible and widening this these leads as soon as possible to further enhance heat transfer will also help.

When designing the driver into an application, it is recommended that the following calculation be performed to ensure safe operation at the desired frequency for the selected MOSFETs. The total chip power dissipation is approximated as:

$$P = 1.05 \times f_{SW} \times V_{PVCC} \left[\frac{3}{2}(Q_{U1} + Q_{U2}) + (Q_{L1} + Q_{L2})\right] + I_{DDQ} \times VCC$$

where f_{SW} is the switching frequency of the PWM signal. Q_U and Q_L is the upper and lower gate charge determined by MOSFET selection and any external capacitance added to the gate pins. The I_{DDQ} VCC product is the quiescent power of the driver and is typically 40mW.

The 1.05 term is a correction factor derived from the following characterization. The base circuit for characterizing the drivers for different loading profiles and frequencies is provided. C_U and C_L are the upper and lower gate load capacitors. Decoupling capacitors [0.15µF] are added to the PVCC and VCC pins. The bootstrap capacitor value in the test circuit is 0.01µF.

The power dissipation approximation is a result of power transferred to and from the upper and lower gates. But, the internal bootstrap device also dissipates power on-chip during the refresh cycle. Expressing this power in terms of the upper MOSFET total gate charge is explained below.

The bootstrap device conducts when the lower MOSFET or its body diode conducts and pulls the PHASE node toward GND. While the bootstrap device conducts, a current path is formed that refreshes the bootstrap capacitor. Since the upper gate is driving a MOSFET, the charge removed from the bootstrap capacitor is equivalent to the total gate charge of the MOSFET. Therefore, the refresh power required by the bootstrap capacitor is equivalent to the power used to charge the gate capacitance of the upper MOSFETs.

$$P_{REFRESH} = f_{SW}Q_{LOSS}V_{PVCC} = f_{SW}Q_{U}V_{PVCC}$$

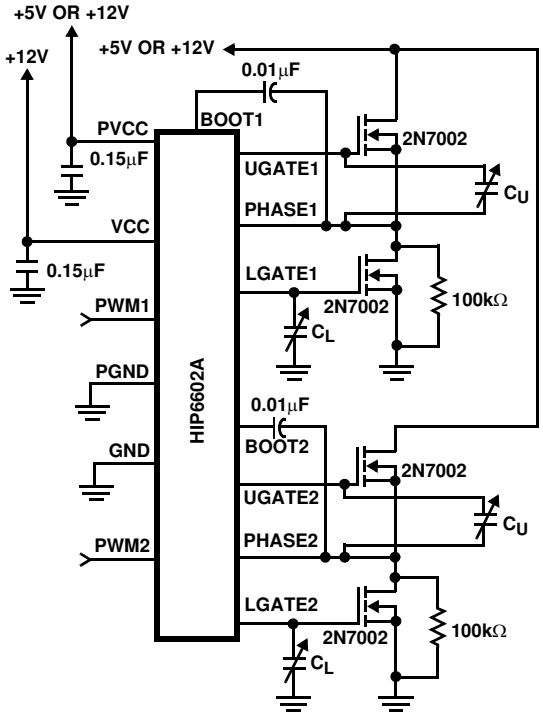
where Q_{LOSS} is the total charge removed from the bootstrap capacitors and provided to the upper gate loads.

In Figure 1, C_U and C_L values are the same and frequency is varied from 10kHz to 2MHz. PVCC and VCC are tied together to a +12V supply.

Figure 2 shows the dissipation in the driver with 1nF loading on both gates and each individually. Figure 3 is the same as Figure 2 except the capacitance is increased to 3nF.

The impact of loading on power dissipation is shown in Figure 4. Frequency is held constant while the gate capacitors are varied from 1nF to 5nF. VCC and PVCC are tied together and to a +12V supply. Figures 5 through 7 show the same characterization for PVCC tied to +5V instead of +12V. The gate supply voltage, PVCC, within the HIP6602A sets both upper and lower gate driver supplies at the same 5V level for the last three curves.

Test Circuit



Typical Performance Curves

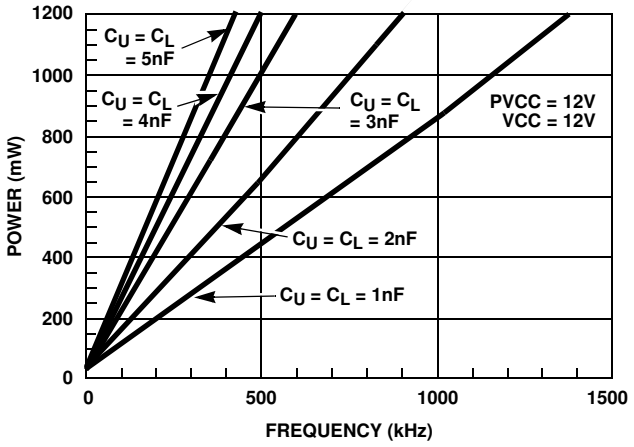


FIGURE 1. POWER DISSIPATION vs FREQUENCY

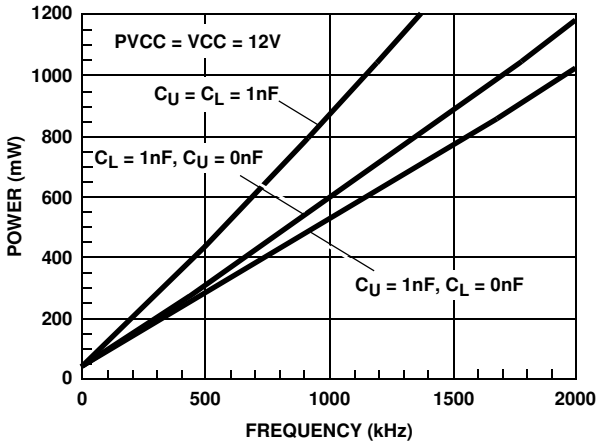


FIGURE 2. 1nF LOADING PROFILE

Typical Performance Curves (Continued)

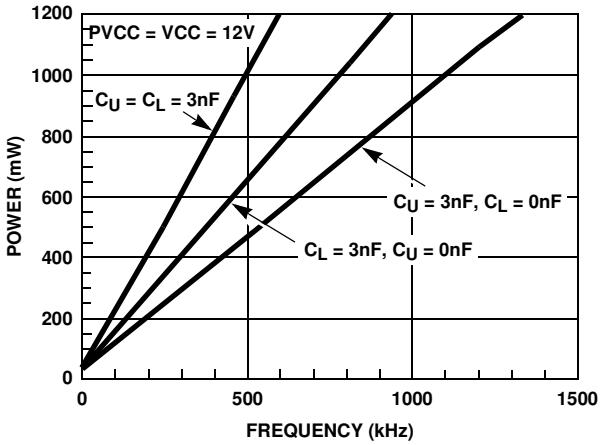


FIGURE 3. 3nF LOADING PROFILE

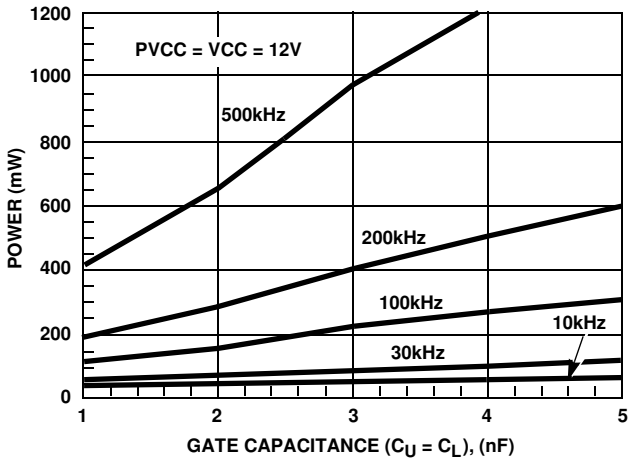


FIGURE 4. POWER DISSIPATION vs LOADING

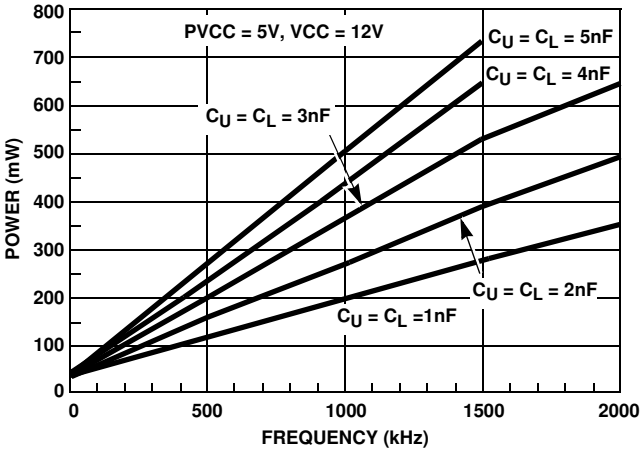


FIGURE 5. POWER DISSIPATION vs FREQUENCY, PVCC = 5V

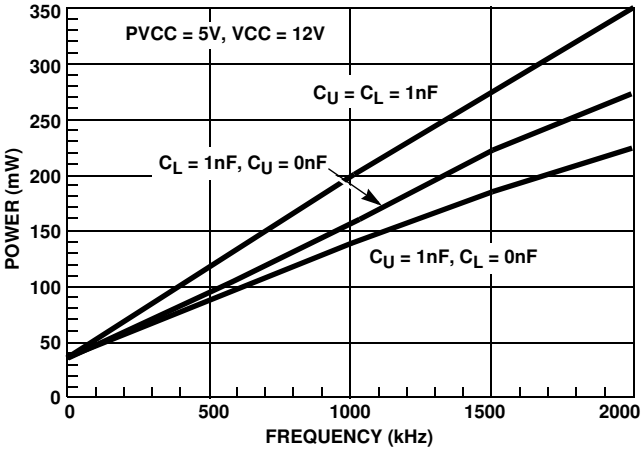


FIGURE 6. POWER DISSIPATION vs FREQUENCY, PVCC = 5V

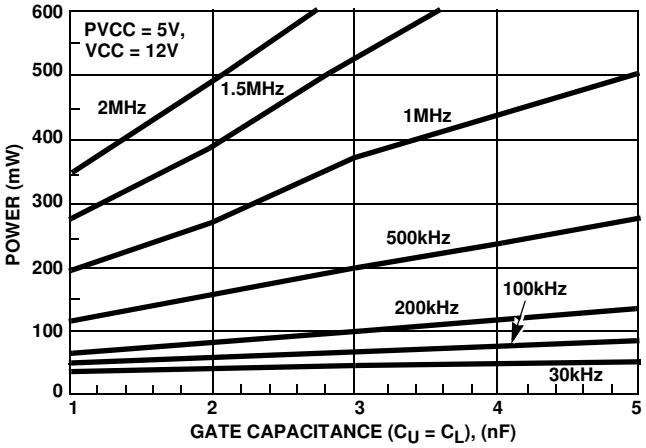
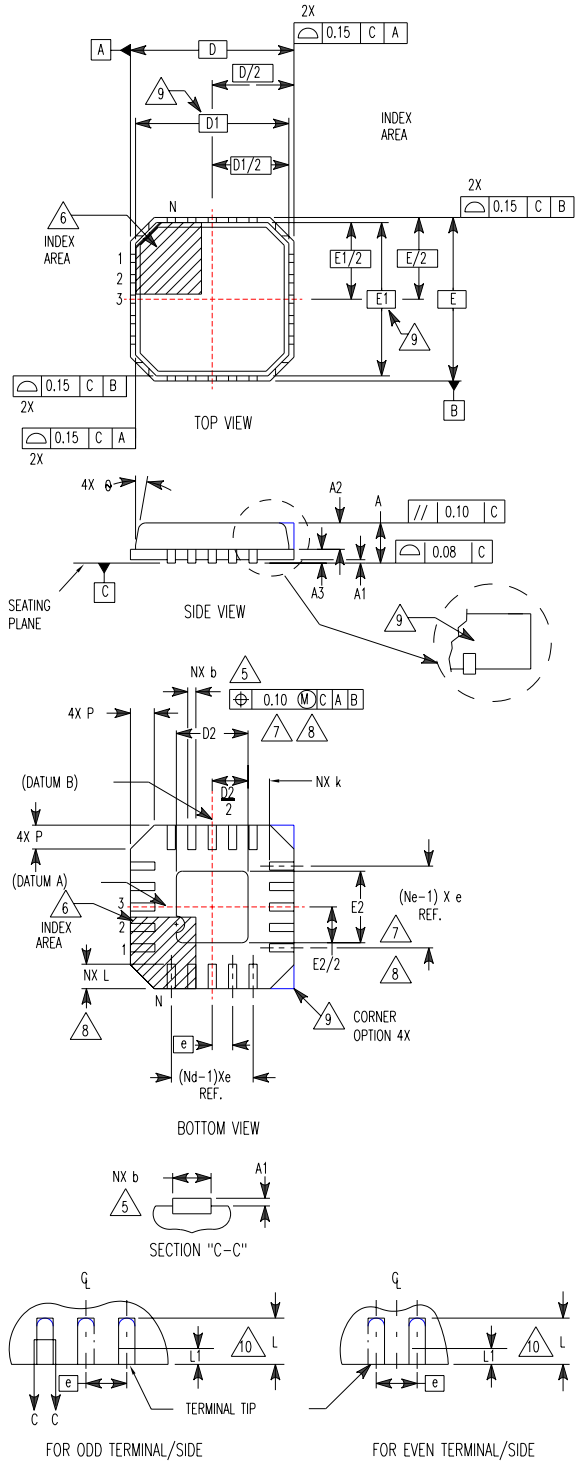


FIGURE 7. POWER DISSIPATION vs LOADING, PVCC = 5V

Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)



L16.5x5

16 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220VHHB ISSUE C)

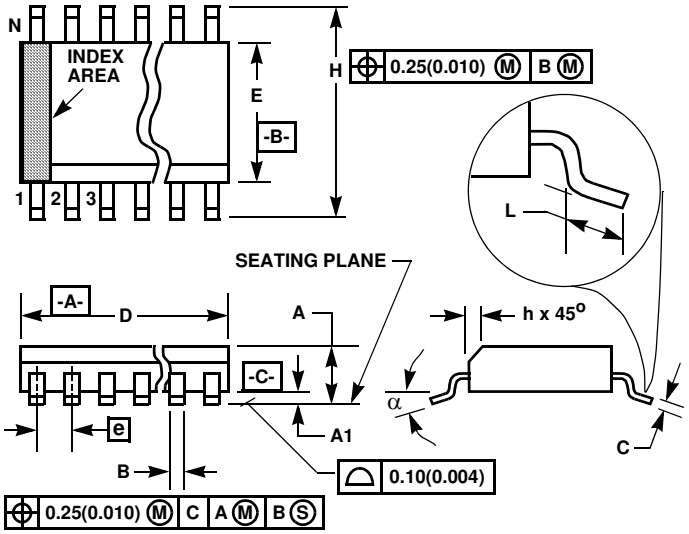
SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3		0.20 REF		9
b	0.28	0.33	0.40	5, 8
D		5.00 BSC		-
D1		4.75 BSC		9
D2	2.55	2.70	2.85	7, 8
E		5.00 BSC		-
E1		4.75 BSC		9
E2	2.55	2.70	2.85	7, 8
e		0.80 BSC		-
k	0.25	-	-	-
L	0.35	0.60	0.75	8
L1	-	-	0.15	10
N		16		2
Nd		4		3
Ne	4	4		3
P	-	-	0.60	9
θ	-	-	12	9

Rev. 2 10/02

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.

Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M14.15 (JEDEC MS-012-AB ISSUE C)
14 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.3367	0.3444	8.55	8.75	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	14		14		7
α	0^o	8^o	0^o	8^o	-

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