

# N-Channel 60 V (D-S) MOSFET



PRODUCT SUMMARY				
V <sub>DS</sub> (V)	60			
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 10 \text{ V}$	0.0118			
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 7.5 \text{ V}$	0.0150			
Q <sub>g</sub> typ. (nC)	8.9			
I <sub>D</sub> (A) <sup>a</sup>	42.8			
Configuration	Single			

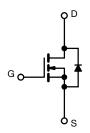
#### **FEATURES**

- TrenchFET® Gen IV power MOSFET
- Very low R<sub>DS</sub> Q<sub>q</sub> figure-of-merit (FOM)
- Tuned for the lowest R<sub>DS</sub> Q<sub>oss</sub> FOM
- 100 % R<sub>a</sub> and UIS tested
- Material categorization: for definitions of compliance please see <a href="https://www.vishav.com/doc?99912">www.vishav.com/doc?99912</a>



#### **APPLICATIONS**

- · Synchronous rectification
- · Primary side switch
- DC/DC converter
- · Motor drive switch
- · Battery and load switch
- Industrial



N-Channel MOSFET

ORDERING INFORMATION			
Package	PowerPAK SO-8		
Lead (Pb)-free and halogen-free	SIR4608DP-T1-GE3		

PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-source voltage		V <sub>DS</sub>	60	V	
Gate-source voltage		V <sub>GS</sub>	± 20	V	
Continuous drain current (T <sub>J</sub> = 150 °C)	T <sub>C</sub> = 25 °C		42.8		
	T <sub>C</sub> = 70 °C	1 , $\square$	34.3		
	T <sub>A</sub> = 25 °C	I <sub>D</sub>	13.1 <sup>b, c</sup>		
	T <sub>A</sub> = 70 °C		10.5 <sup>b, c</sup>	^	
Pulsed drain current (t = 100 μs)		I <sub>DM</sub>	100	A	
Continuous source-drain diode current	T <sub>C</sub> = 25 °C		35.5		
	T <sub>A</sub> = 25 °C	l <sub>S</sub>	3.3 b, c		
Single pulse avalanche current	I 0.1 mll	I <sub>AS</sub>	15		
Single pulse avalanche energy	L = 0.1 mH	E <sub>AS</sub>	11.25	mJ	
Maximum power dissipation	T <sub>C</sub> = 25 °C		39		
	T <sub>C</sub> = 70 °C	1 , —	25	14/	
	T <sub>A</sub> = 25 °C	P <sub>D</sub>	3.6 b, c	W	
	T <sub>A</sub> = 70 °C		2.3 b, c		
Operating junction and storage temperature range		T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C	
Soldering recommendations (peak temperature) d, e			260		

THERMAL RESISTANCE RATINGS							
PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT			
Maximum junction-to-ambient <sup>b</sup>	t ≤ 10 s	R <sub>thJA</sub>	24	34	°C/W		
Maximum junction-to-case (drain)	Steady state	$R_{th,IC}$	2.5	3.2	]		

### Notes

- a.  $T_C = 25 \,^{\circ}C$
- b. Surface mounted on 1" x 1" FR4 board
- c. t = 10 s
- d. See solder profile (<u>www.vishay.com/doc?73257</u>). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- f. Maximum under steady state conditions is 70 °C/W

# Vishay Siliconix

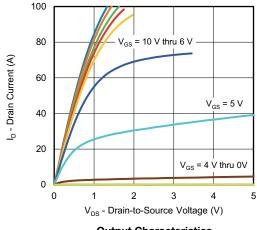
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static					•		
Drain-source breakdown voltage	V <sub>DS</sub>	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	60	-	-	V	
V <sub>DS</sub> temperature coefficient	$\Delta V_{DS}/T_{J}$	I <sub>D</sub> = 10 mA	-	34	-		
V <sub>GS(th)</sub> temperature coefficient	$\Delta V_{GS(th)}/T_J$	I <sub>D</sub> = 250 μA	-	-5.7	-	mV/°C	
Gate-source threshold voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_{D} = 250 \mu\text{A}$	2	-	4	V	
Gate-source leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$	-	-	100	nA	
Zero gate voltage drain current		$V_{DS} = 60 \text{ V}, V_{GS} = 0 \text{ V}$	-	-	1	<b>T</b> ,	
	I <sub>DSS</sub>	$V_{DS} = 60 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 70 \text{ °C}$	-	-	15	μA	
Drain-source on-state resistance <sup>a</sup>	_	$V_{GS} = 10 \text{ V}, I_D = 10 \text{ A}$	-	0.0099	0.0118	Ω	
	R <sub>DS(on)</sub>	$V_{GS} = 7.5 \text{ V}, I_D = 10 \text{ A}$	-	0.0115	0.0150		
Forward transconductance <sup>a</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 10 A	-	31	-	S	
Dynamic <sup>b</sup>					•		
Input capacitance	C <sub>iss</sub>		-	740	-	pF	
Output capacitance	C <sub>oss</sub>	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	-	195	-		
Reverse transfer capacitance	C <sub>rss</sub>		-	7	-		
Tabella de alcada a c	0	$V_{DS} = 30 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 10 \text{ A}$	-	11.7	18		
Total gate charge	Qg		-	8.9	13.5	nC	
Gate-source charge	$Q_{gs}$	$V_{DS} = 30 \text{ V}, V_{GS} = 7.5 \text{ V}, I_D = 10 \text{ A}$	-	4.2	-		
Gate-drain charge	Q <sub>gd</sub>		-	1.9	-		
Output charge	Q <sub>oss</sub>	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V		12.2	-	İ	
Gate resistance	$R_g$	f = 1 MHz	0.7	1.5	2.6	Ω	
Turn-on delay time	t <sub>d(on)</sub>		-	10	20		
Rise time	t <sub>r</sub>	$V_{DD} = 30 \text{ V}, R_L = 3 \Omega, I_D \cong 10 \text{ A},$	-	4	8		
Turn-off delay time	t <sub>d(off)</sub>	$V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$	-	14	28		
Fall time	t <sub>f</sub>		-	4	8		
Turn-on delay time	t <sub>d(on)</sub>		-	11	22	ns	
Rise time	t <sub>r</sub>	$V_{DD} = 30 \text{ V}, R_L = 3 \Omega, I_D \cong 10 \text{ A},$	-	5	10	1	
Turn-off delay time	t <sub>d(off)</sub>	$V_{GEN} = 7.5 \text{ V}, R_g = 1 \Omega$	-	13	26		
Fall time	t <sub>f</sub>		-	4	8		
<b>Drain-Source Body Diode Characteristi</b>	cs					•	
Continuous source-drain diode current	Is	T <sub>C</sub> = 25 °C	-	-	35.5	^	
Pulse diode forward current	I <sub>SM</sub>		-	-	100	A	
Body diode voltage	$V_{SD}$	I <sub>S</sub> = 5 A, V <sub>GS</sub> = 0 V	-	0.82	1.1	V	
Body diode reverse recovery time	t <sub>rr</sub>		-	20	40	ns	
Body diode reverse recovery charge	Q <sub>rr</sub>	1 10 A 4:/44 100 A/ T 05 00	-	12	24	nC	
Reverse recovery fall time	ta	$I_F = 10 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu\text{s}, T_J = 25 ^{\circ}\text{C}$	-	12	-		
Reverse recovery rise time	t <sub>b</sub>		-	8	-	ns	

#### Notes

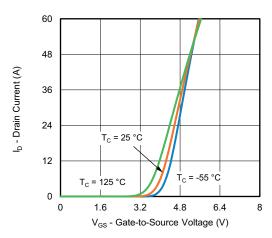
- a. Pulse test; pulse width  $\leq 300~\mu s,\,duty~cycle \leq 2~\%$
- b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

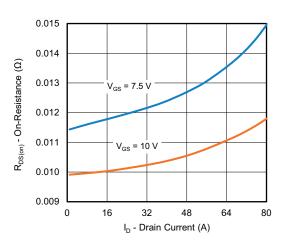




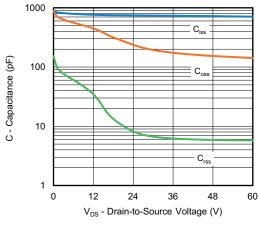
**Output Characteristics** 



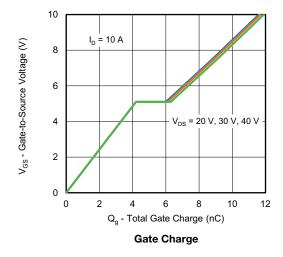
**Transfer Characteristics** 

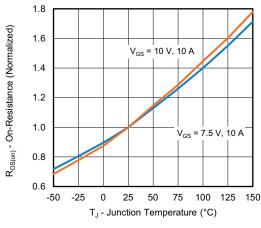


On-Resistance vs. Drain Current and Gate Voltage



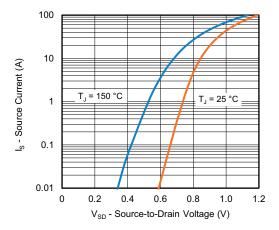
Capacitance



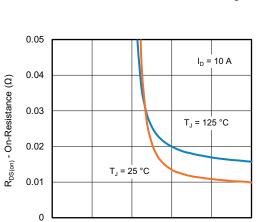


On-Resistance vs. Junction Temperature





Source-Drain Diode Forward Voltage



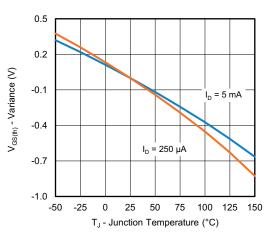
2

0

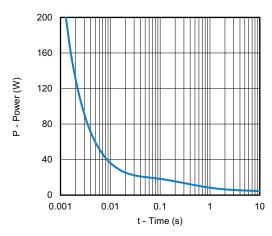
 $V_{\rm GS}$  - Gate-to-Source Voltage (V) On-Resistance vs. Gate-to-Source Voltage

6

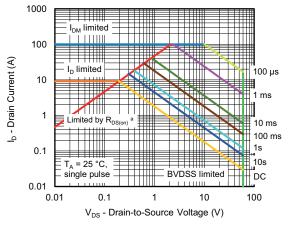
10



**Threshold Voltage** 



Single Pulse Power, Junction-to-Ambient

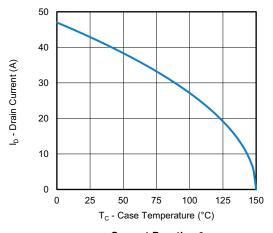


Safe Operating Area, Junction-to-Ambient

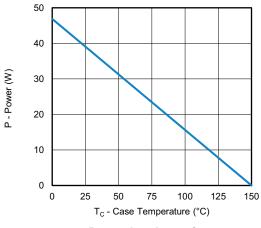
#### Note

a.  $V_{GS}$  > minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

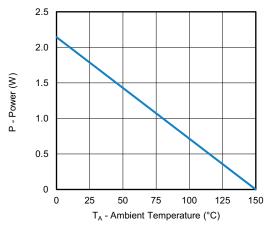




Current Derating a





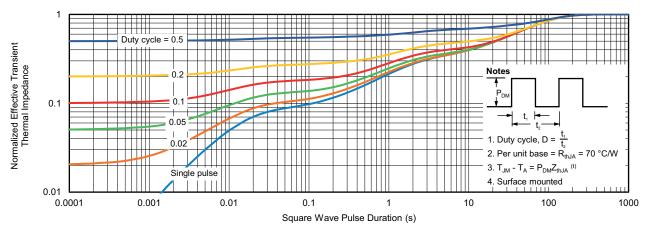


Power, Junction-to-Ambient

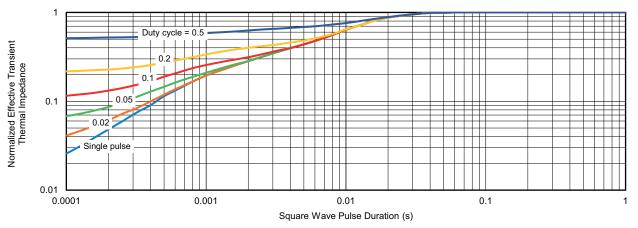
#### Note

a. The power dissipation P<sub>D</sub> is based on T<sub>J</sub> max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit





Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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