

## Half-Bridge IPM for Low Voltage Applications

***μ*IPM™**

**30A, 100V**

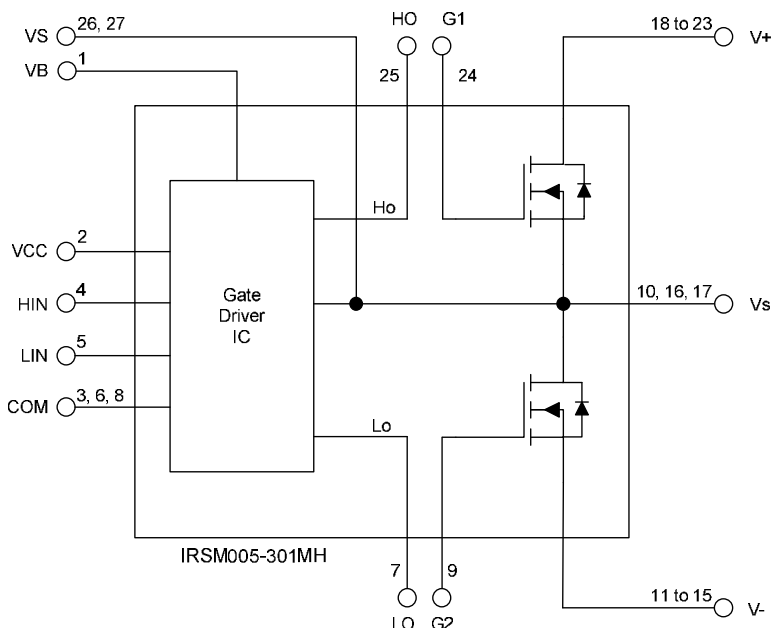
### Description

The IRSM005-301MH is a general purpose half-bridge with integrated gate driver in an attractive 7x8mm PQFN package. It is a general purpose building block suitable for a variety of low voltage applications where power density is of critical importance. Typical examples would be advanced motor drives, dc-to-ac and dc-to-dc converters.

### Features

- Package with low thermal resistance and minimal parasitics
- Low on-resistance HEXFETs: 16 mΩ typ.
- Undervoltage lockout on Vcc and Vbs
- Independent gate drive in phase with logic input
- Gate drive supply range from 10V to 20V
- Propagation delay matched to defined spec
- 3.3V, 5V and 15V logic input compatible
- RoHS compliant

### Internal Electrical Schematic



### Ordering Information

Orderable Part Number	Package Type	Form	Quantity
IRSM005-301MH	PQFN 7x8mm	Tray	1300
IRSM005-301MHTR	PQFN 7x8mm	Tape and Reel	2000

## Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the module may occur. These are not tested at manufacturing. All voltage parameters are absolute voltages referenced to  $V_{SS}$  unless otherwise stated in the table. The thermal resistance rating is measured under board mounted and still air conditions.

Symbol	Description	Min	Max	Unit
$V_{DS}$	MOSFET Drain-to-Source Voltage	---	100	V
$I_O$	Maximum DC current per MOSFET @ $T_C=25^\circ\text{C}$ (Note1)	---	30	A
$P_d$	Maximum Power dissipation per MOSFET @ $T_C=100^\circ\text{C}$	---	13.5	W
$T_J$ (MOSFET & IC)	Maximum Operating Junction Temperature	---	150	$^\circ\text{C}$
$T_S$	Storage Temperature Range	-40	150	$^\circ\text{C}$
$V_B$	High side floating supply voltage	-0.3	$V_S + 20$	V
$V_S$	High side floating supply offset voltage	$V_B - 20$	$V_B + 0.3$	V
$V_{CC}$	Low Side fixed supply voltage	-0.3	20	V
$V_{IN}$	Logic input voltage LIN, HIN	-0.3	$V_{CC} + 0.3V$	V

Note1: Calculated based on maximum junction temperature. Bond wires current limit is 20A

## Inverter Static Electrical Characteristics

$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS}$ )=15V,  $T_J=25^\circ\text{C}$ , unless otherwise specified.

Symbol	Description	Min	Typ	Max	Units	Conditions	
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	100	---	---	V	$H_{IN}=L_{IN}=0V$ , $I_D=250\mu\text{A}$	
$V_{GS(TH)}$	Gate Threshold Voltage	2.0	3.0	4.0	V	$I_D=100\mu\text{A}$	
$R_{DS(ON)}$	Drain-to-Source Voltage	---	16	21	m $\Omega$	$I_D=10A$ , $T_J=25^\circ\text{C}$	
		---	35	---		$I_D=10A$ , $T_J=150^\circ\text{C}$	
$I_{DSS}$	Zero Gate Voltage Drain Current	---	20	---	$\mu\text{A}$	$H_{IN}=L_{IN}=0V$ , $V^+=100V$	
		---	250	---		$H_{IN}=L_{IN}=0V$ , $V^+=100V$ , $T_J=125^\circ\text{C}$	
$V_{SD}$	MOSFET Diode Forward Voltage Drop	--	0.7	0.82	V	$I_F=10A$	
		---	0.6	---		$I_F=10A$ , $T_J=125^\circ\text{C}$	
$I_{GSS}$	Gate to Source leakage	---	---	+/-100	nA	$V_{GS}=+/-20V$	
RBSOA	Reverse Bias Safe Operating Area	FULL SQUARE, limited by $T_{Jmax}$				$V^+=100V$ , $V_{CC}=+15V$ to 0V	
$Q_G$	Total gate charge	---	36	54	nC	$I_D=26A$ $V_{DS}=20V$ $V_{GS}=10V$	
$Q_{GS}$	Gate to source charge	---	7	---			
$Q_{GD}$	Gate to drain charge	---	11	---			
EAS	Single Pulse Avalanche Energy	6.1	-		mJ		

## Recommended Operating Conditions Driver Function

For proper operation the device should be used within the recommended conditions. All voltages are absolute referenced to COM. The VS offset is tested with all supplies biased at 15V differential. For more details, see IRS2005 data sheet.

Symbol	Definition	Min	Typ	Max	Units
V <sub>B</sub>	High side floating supply voltage	V <sub>S</sub> +10	V <sub>S</sub> +15	V <sub>S</sub> +20	V
V <sub>S</sub>	High side floating supply offset voltage	Note 1	---	100	V
V <sub>CC</sub>	Low side and logic fixed supply voltage	10	15	20	V
V <sub>IN</sub>	Logic input voltage LIN, HIN	COM	---	V <sub>CC</sub>	V
HIN	High side PWM pulse width	1	---	---	μs
Deadtime	Suggested dead time between HIN and LIN	0.3	0.5	---	μs

## Static Electrical Characteristics Driver Function

V<sub>BIAS</sub> (V<sub>CC</sub>, V<sub>BS</sub>)=15V, T<sub>J</sub>=25°C, unless otherwise specified. The V<sub>IN</sub>, and I<sub>IN</sub> parameters are referenced to COM

Symbol	Definition	Min	Typ	Max	Units
V <sub>IN,th+</sub>	Positive going input threshold for LIN, HIN	2.5	---	---	V
V <sub>IN,th-</sub>	Negative going input threshold for LIN, HIN	---	---	0.8	V
V <sub>BSUV+</sub>	V <sub>BS</sub> supply undervoltage, Positive going threshold	8.0	8.9	9.8	V
V <sub>BSUV-</sub>	V <sub>BS</sub> supply undervoltage, Negative going threshold	7.4	8.2	9.0	V
V <sub>BSUVH</sub>	V <sub>BS</sub> supply undervoltage lock-out hysteresis	---	0.8	---	V
V <sub>CCUV+</sub>	V <sub>CC</sub> supply undervoltage, Positive going threshold	8.0	8.9	9.8	V
V <sub>CCUV-</sub>	V <sub>CC</sub> supply undervoltage, Negative going threshold	7.4	8.2	9.0	V
V <sub>CCUVH</sub>	V <sub>CC</sub> supply undervoltage lock-out hysteresis	---	0.8	---	V
I <sub>QBS</sub>	Quiescent V <sub>BS</sub> supply current	---	30	75	μA
I <sub>QCC</sub>	Quiescent V <sub>CC</sub> supply current	---	150	520	μA
I <sub>LK</sub>	Offset Supply Leakage Current	---	---	50	μA
I <sub>O+</sub>	IC high output short circuit current	200	290	---	VO=0V VIN=Logic "1" PW<10us
I <sub>O-</sub>	IC low output short circuit current	420	600	---	VO=15V VIN=Logic "0" PW<10us
I <sub>IN+</sub>	Input bias current V <sub>IN</sub> =5V for LIN, HIN	---	4	10	μA
I <sub>IN-</sub>	Input bias current V <sub>IN</sub> =0V for LIN, HIN	---	0.5	1	μA

### Dynamic Electrical Characteristics Driver Function

$V_{BIAS} (V_{CC}, V_{BS})=15V$ ,  $T_J=25^{\circ}C$ ,  $C_L=1000pF$  unless otherwise specified. Driver only timing unless otherwise specified.

Symbol	Description	Min	Typ	Max	Units	Conditions
$T_{ON}$	Input to Output propagation turn-on delay time (see fig.3)	---	160	220	ns	
$T_{OFF}$	Input to Output propagation turn-off delay time (see fig. 3)	---	150	220	ns	
$T_R$	Input to Output turn-on rise time (see fig.3)	---	70	170	ns	
$T_F$	Input to Output turn-off fall time (see fig. 3)	---	35	95	ns	
MT	Delay matching, HS and LS turn-on/off	---	---	50	ns	

### Thermal and Mechanical Characteristics

Symbol	Description	Min	Typ	Max	Units	Conditions
$R_{th(J-B)}$	Thermal resistance, junction to mounting pad, each MOSFET	---	3.8	---	$^{\circ}C/W$	Standard reflow-solder process
$R_{th(J-A)}$	Thermal resistance, junction to ambient, each MOSFET	---	40	---	$^{\circ}C/W$	Mounted on $50mm^2$ of four-layer FR4 with 28 vias

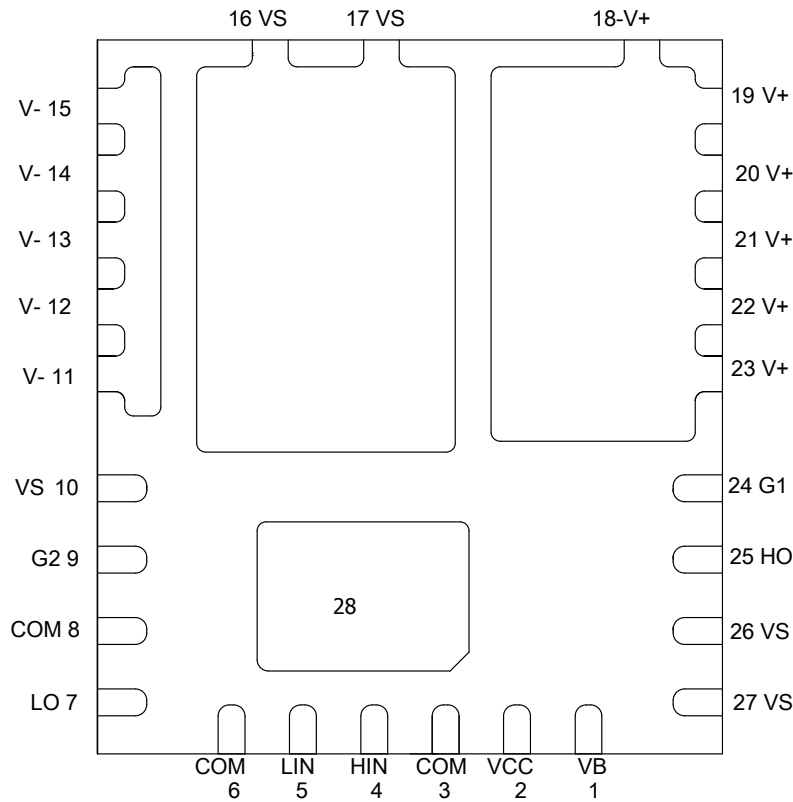
### Input-Output Logic Level Table

HIN	LIN	U,V,W
HI	HI	Shoot-through
LO	LO	**
HI	LO	V+
LO	HI	0

\* V+ if motor current is flowing into VS, 0 if current is flowing out of VS into the motor winding

**Module Pin-Out Description**

Pin	Name	Description
3, 6, 8	COM	Low Side Gate Driver Return
2	V <sub>CC</sub>	15V Gate Drive Supply
4	HIN	Logic Input for High Side (Active High)
5	LIN	Logic Input for Low Side (Active High)
7	LO	Low Side Gate Drive Output
9	G2	Low Side FET Gate
10, 16, 17	V <sub>S</sub>	Phase Output
11 to 15	V-	Low Side Source Connection
18 to 23	V+	DC Bus
24	G1	High Side FET Gate
25	HO	High Side Gate Drive Output
26, 27	V <sub>S</sub>	Phase Output (-ve of Bootstrap Cap Connection)
1	V <sub>B</sub>	High Side Floating Supply (+ve Bootstrap Cap Connection)


**BOTTOM OF PACKAGE VIEW**

Exposed pad (Pin 28) has to be connected to COM for better electrical performance

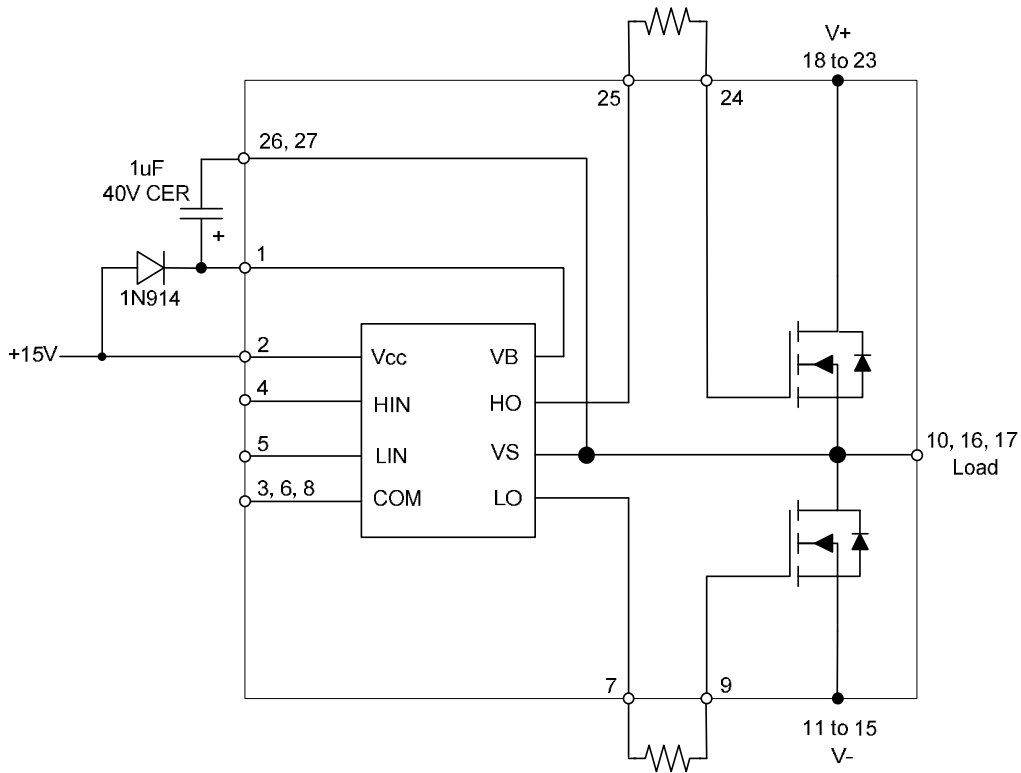


Figure 1: Typical Application Connection

1. Bus capacitors should be mounted as close to the module bus terminals as possible to reduce ringing and EMI problems. Additional high frequency ceramic capacitor mounted close to the module pins will further improve performance.
2. Value of the boot-strap capacitors depends upon the switching frequency. Their selection should be made based on IR Design tip DT04-4 or application note AN-1044.

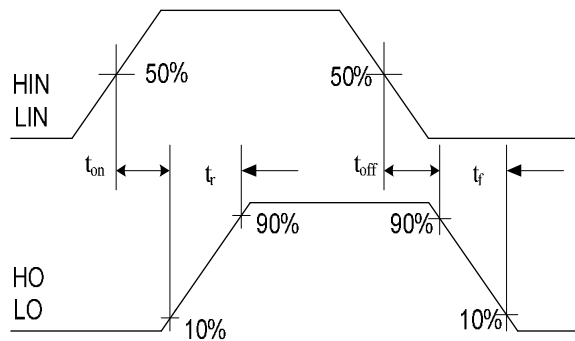


Figure 2. IC switching waveforms definitions.

**Qualification**

<b>Qualification Level</b>		Industrial <sup>††</sup> (per JEDEC JESD 47E)
<b>Moisture Sensitivity Level</b>		MSL3 <sup>†††</sup> (per IPC/JEDEC J-STD-020C)
<b>ESD</b>	Machine Model	Class A (±200V) (per JEDEC standard JESD22-A115A)
	Human Body Model	Class 2 (±2000V) (per EIA/JEDEC standard EIA/JES-001A-2011)
<b>RoHS Compliant</b>		Yes

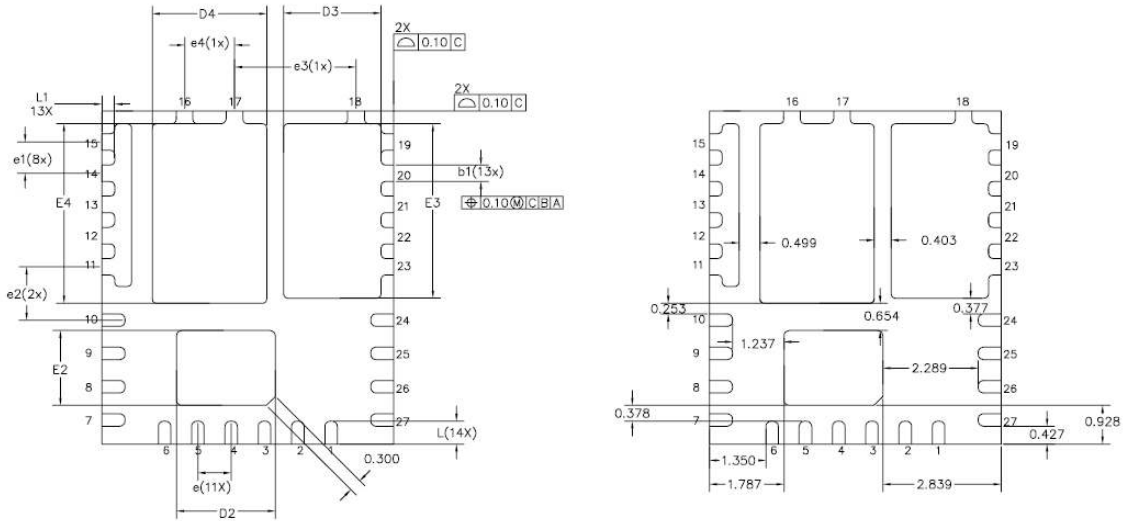
† Qualification standards can be found at International Rectifier's web site <http://www.irf.com/>

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information.

††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.



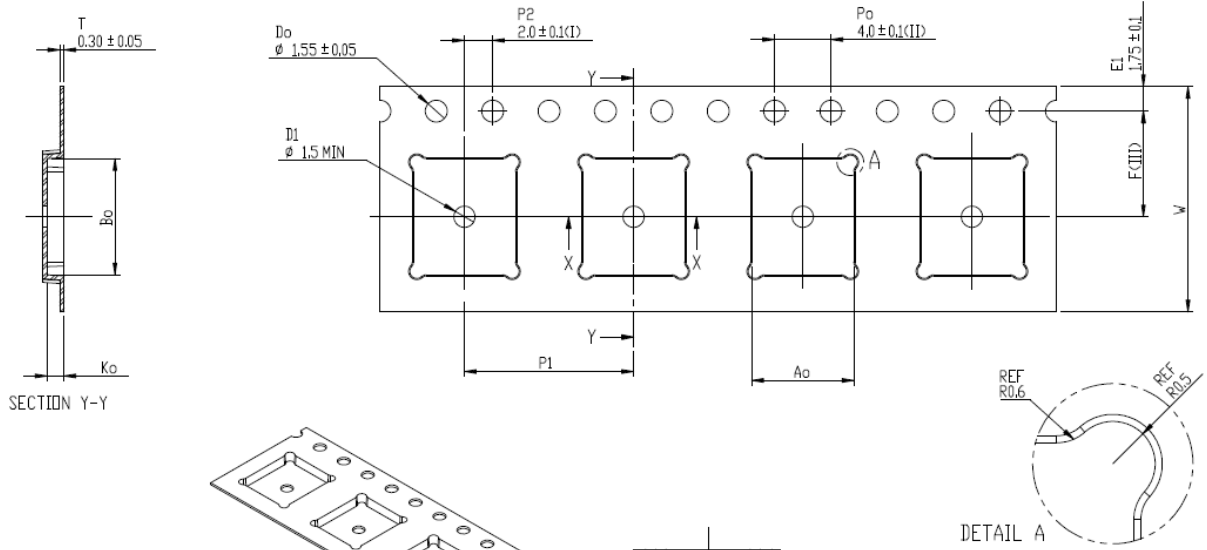


**Package Outline (Bottom View, 1 of 2)**
PACKAGE BOTTOM VIEW


DIMENSION	DIMENSIONS IN MILLIMETER		
	MIN.	NOM.	MAX.
A	0.800	0.900	1.000
A1	0.000	—	0.050
A3	0.203 REF.		
b	0.250	0.300	0.350
b1	0.350	0.400	0.450
D	6.900	7.000	7.100
E	7.900	8.000	8.100
D2	2.323	2.373	2.423
E2	1.748	1.798	1.848
D3	2.290	2.340	2.390
E3	4.144	4.194	4.244
D4	2.698	2.748	2.798
E4	4.267	4.317	4.367
e	0.800 BSC		
e1	0.750 BSC		
e2	1.281 BSC		
e3	2.918 BSC		
e4	1.200 BSC		
L	0.500	0.550	0.600
L1	0.253	0.303	0.353

1. For mounting instruction see AN-1168.
2. For recommended PCB via design see AN-1091.
3. For recommended design, solder profile, integration and rework guidelines see AN-1028.
4. For board inspection guidelines see AN-1133.

### Tape and Reel Details



Ao	7.25	+/- 0.1
Bo	8.25	+/- 0.1
Ko	1.20	+/- 0.1
F	7.50	+/- 0.1
P 1	12.00	+/- 0.1
W	16.00	+/- 0.3

- (I) Measured from centreline of sprocket hole to centreline of pocket.
  - (II) Cumulative tolerance of 10 sprocket holes is  $\pm 0.20$ .
  - (III) Measured from centreline of sprocket hole to centreline of pocket.
  - (IV) Other material available.
  - (V) Typical SR of form tape Max  $10^{-3}$  OHM/SQ
- ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED.

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