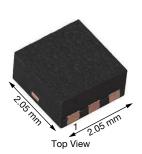
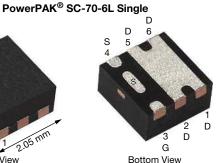


# Vishay Siliconix

# N-Channel 30 V (D-S) MOSFET

PRODUCT SUMMARY									
V <sub>DS</sub> (V)	$R_{DS(on)}$ ( $\Omega$ )	I <sub>D</sub> (A) b, c	Q <sub>g</sub> (TYP.)						
30	0.0200 at V <sub>GS</sub> = 10 V	10.1	5.6						
	0.0240 at V <sub>GS</sub> = 4.5 V	9.2	5.0						



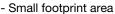


Marking Code: A L **Ordering Information:** 

SiA432DJ-T1-GE3 (Lead (Pb)-free and Halogen-free) SiA432DJ-T4-GE3 (Lead (Pb)-free and Halogen-free)

#### **FEATURES**

- TrenchFET® power MOSFET
- Thermally enhanced PowerPAK® SC-70 package





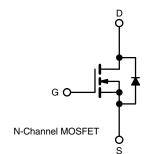
• Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

#### **APPLICATIONS**

Load Switch







ABSOLUTE MAXIMUM RATING	(1 <sub>A</sub> – 20 °C, a	1	Y Company of the Comp		
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-Source Voltage		$V_{DS}$	30	V	
Gate-Source Voltage		$V_{GS}$	± 20	v	
	T <sub>C</sub> = 25 °C		12 <sup>a</sup>		
O	T <sub>C</sub> = 70 °C	1 .	12 <sup>a</sup>		
Continuous Drain Current (T <sub>J</sub> = 150 °C)	T <sub>A</sub> = 25 °C	I <sub>D</sub>	10.1 <sup>b, c</sup>		
	T <sub>A</sub> = 70 °C		8.1 <sup>b, c</sup>	A	
Pulsed Drain Current		I <sub>DM</sub>	30	7 ^	
Continuous Common Dunio Diodo Commont	T <sub>C</sub> = 25 °C		12 <sup>a</sup>		
Continuous Source-Drain Diode Current	T <sub>A</sub> = 25 °C	l <sub>S</sub>	2.9 b, c		
Single-Pulse Avalanche Current	L = 0.1 mH	I <sub>AS</sub>	15.5		
Single-Pulse Avalanche Energy	L = 0.1 IIIH	E <sub>AS</sub>	12	mJ	
	T <sub>C</sub> = 25 °C		19.2		
Mayimum Dawar Dissination	T <sub>C</sub> = 70 °C		12.3	١٨/	
Maximum Power Dissipation	T <sub>A</sub> = 25 °C	P <sub>D</sub>	3.5 b, c	W	
	T <sub>A</sub> = 70 °C		2.2 <sup>b, c</sup>		
Operating Junction and Storage Temperatur	re Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to 150	00	
Soldering Recommendations (Peak Tempera	ature) <sup>d, e</sup>		260	°C	

THERMAL RESISTANCE RATINGS									
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT				
Maximum Junction-to-Ambient b, f	t ≤ 5 s	$R_{thJA}$	28	36	°C/W				
Maximum Junction-to-Case (Drain)	Steady State	R <sub>thJC</sub>	5.3	6.5	C/VV				

- a. Package limited.
- b. Surface mounted on 1" x 1" FR4 board.
- d. See solder profile (<u>www.vishay.com/doc?73257</u>). The PowerPAK SC-70 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- e. Rework conditions: Manual soldering with a soldering iron is not recommended for leadless components.
- f. Maximum under steady state conditions is 80 °C/W.



# Vishay Siliconix

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static			•			
Drain-Source Breakdown Voltage	$V_{DS}$	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	30	-	-	V
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$	1 0504	-	35	-	mV/°C
V <sub>GS(th)</sub> Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I <sub>D</sub> = 250 μA	-	-5.6	-	
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}$ , $I_D = 250 \mu A$	1	-	3	V
Gate-Source Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$	-	-	± 100	nA
Zaura Carta Valta via Duniu Communi	_	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V	-	-	1	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C	-	-	10	μΑ
On-State Drain Current a	I <sub>D(on)</sub>	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	20	-	-	Α
D : 0		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 6 A	-	0.0158	0.0200	
Drain-Source On-State Resistance a	R <sub>DS(on)</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 5 A	-	0.0190	0.0240	Ω
Forward Transconductance a	g <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 6 A	-	22	-	S
Dynamic <sup>b</sup>				1	<u> </u>	
Input Capacitance	C <sub>iss</sub>		-	800	-	pF
Output Capacitance	Coss	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 V, f = 1 MHz	-	115	-	
Reverse Transfer Capacitance	C <sub>rss</sub>		-	54	-	
	Qg	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 10 A	-	13	20	nC
Total Gate Charge			-	5.6	9	
Gate-Source Charge	Q <sub>gs</sub>	$V_{DS} = 15 \text{ V}, V_{GS} = 4.5 \text{ V}, I_{D} = 10 \text{ A}$	-	2	-	
Gate-Drain Charge	Q <sub>gd</sub>	ı		1.4	-	1
Gate Resistance	Rg	f = 1 MHz	-	3	-	Ω
Turn-On Delay Time	t <sub>d(on)</sub>	(on)		15	25	<b>†</b>
Rise Time	t <sub>r</sub>	$V_{DD} = 15 \text{ V}, R_{L} = 1.9 \Omega$	-	11	17	ns
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D \cong 8 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_g = 1 \Omega$	-	15	25	
Fall Time	t <sub>f</sub>		-	10	15	
Turn-On Delay Time	t <sub>d(on)</sub>		-	8	15	
Rise Time	t <sub>r</sub>	$V_{DD} = 15 \text{ V}, R_{L} = 1.9 \Omega$	-	8	15	
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D \cong 8 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$	-	15	25	
ıll Time t <sub>f</sub>			-	8	15	1
Drain-Source Body Diode Characteristic	s		•	1		<u> </u>
Continuous Source-Drain Diode Current	Is	T <sub>C</sub> = 25 °C	-	-	12	_
Pulse Diode Forward Current	e Diode Forward Current I <sub>SM</sub>		-	-	30	A
Body Diode Voltage	V <sub>SD</sub>	I <sub>S</sub> = 5 A, V <sub>GS</sub> = 0 V	-	0.8	1.2	V
Body Diode Reverse Recovery Time t <sub>rr</sub>			-	16	30	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>		-	8	15	nC
Reverse Recovery Fall Time	ta	I <sub>F</sub> = 8 A, dl/dt = 100 A/μs, T <sub>J</sub> = 25 °C	-	9.8	-	ns
Reverse Recovery Rise Time	t <sub>b</sub>		_	6.2	_	

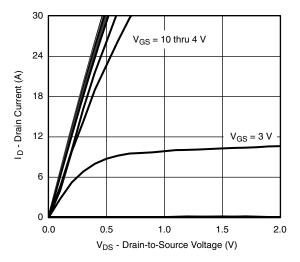
#### Notes

- a. Pulse test; pulse width  $\leq 300~\mu s,$  duty cycle  $\leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.

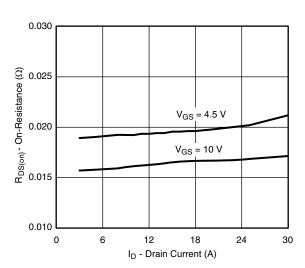
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ARE SUBJECT TO SPECIFIC DISCLAIMERS, SET FORTH AT www.vishay.com/doc?91000

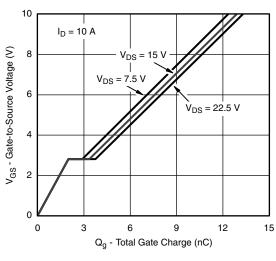




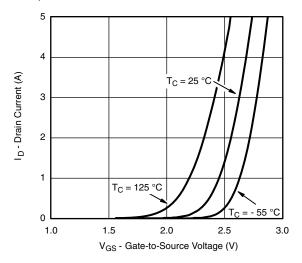
#### **Output Characteristics**



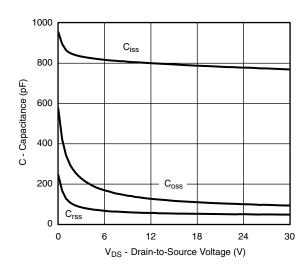
On-Resistance vs. Drain Current and Gate Voltage



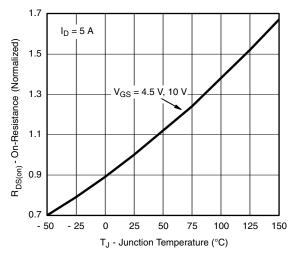
**Gate Charge** 



**Transfer Characteristics** 

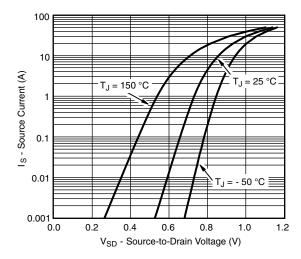


Capacitance

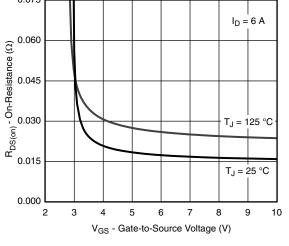


On-Resistance vs. Junction Temperature

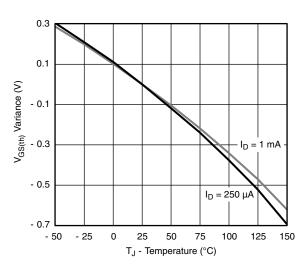




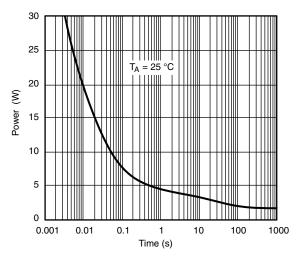
Source-Drain Diode Forward Voltage



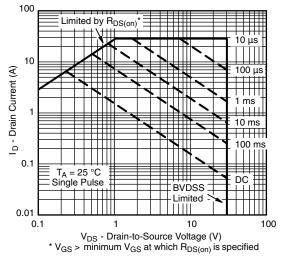
On-Resistance vs. Gate-to-Source Voltage



**Threshold Voltage** 

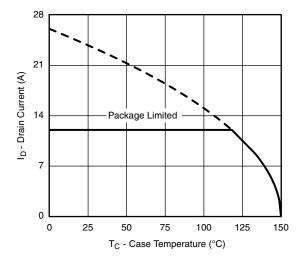


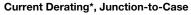
Single Pulse Power (Junction-to-Ambient)

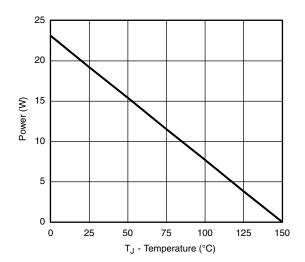


Safe Operating Area, Junction-to-Ambient





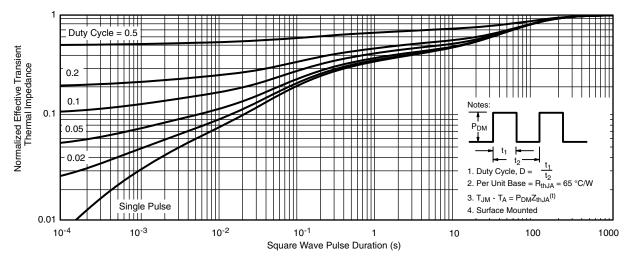




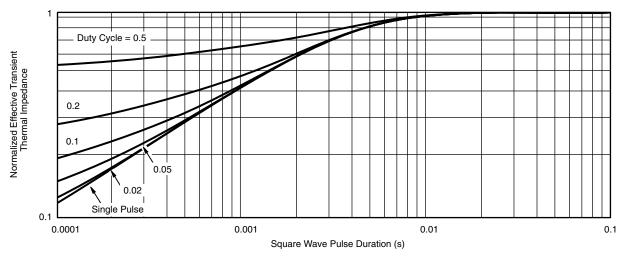
**Power Derating** 

<sup>\*</sup> The power dissipation P<sub>D</sub> is based on T<sub>J (max.)</sub> = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.





Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

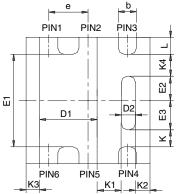
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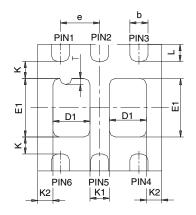




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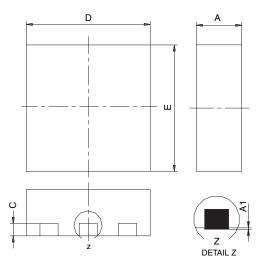
# PowerPAK® SC70-6L





BACKSIDE VIEW OF SINGLE

BACKSIDE VIEW OF DUAL



- All dimensions are in millimeters
  Package outline exclusive of mold flash and metal burr
  Package outline inclusive of plating

	SINGLE PAD						DUAL PAD					
DIM	M	ILLIMETER	RS		INCHES		М	ILLIMETER	RS		INCHES	
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max
Α	0.675	0.75	0.80	0.027	0.030	0.032	0.675	0.75	0.80	0.027	0.030	0.032
<b>A</b> 1	0	-	0.05	0	-	0.002	0	-	0.05	0	-	0.002
b	0.23	0.30	0.38	0.009	0.012	0.015	0.23	0.30	0.38	0.009	0.012	0.015
С	0.15	0.20	0.25	0.006	0.008	0.010	0.15	0.20	0.25	0.006	0.008	0.010
D	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
D1	0.85	0.95	1.05	0.033	0.037	0.041	0.513	0.613	0.713	0.020	0.024	0.028
D2	0.135	0.235	0.335	0.005	0.009	0.013						
Е	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
E1	1.40	1.50	1.60	0.055	0.059	0.063	0.85	0.95	1.05	0.033	0.037	0.041
E2	0.345	0.395	0.445	0.014	0.016	0.018						
E3	0.425	0.475	0.525	0.017	0.019	0.021						
е		0.65 BSC			0.026 BSC	;		0.65 BSC			0.026 BSC	
K		0.275 TYP			0.011 TYP	1	0.275 TYP		0.011 TYP			
K1		0.400 TYP			0.016 TYP		0.320 TYP		0.013 TYP			
K2		0.240 TYP		0.009 TYP		0.252 TYP		0.010 TYP				
К3		0.225 TYP		0.009 TYP								
K4		0.355 TYP		0.014 TYP								
L	0.175	0.275	0.375	0.007	0.011	0.015	0.175	0.275	0.375	0.007	0.011	0.015
Т							0.05	0.10	0.15	0.002	0.004	0.006
ECN: C O	2.07421											

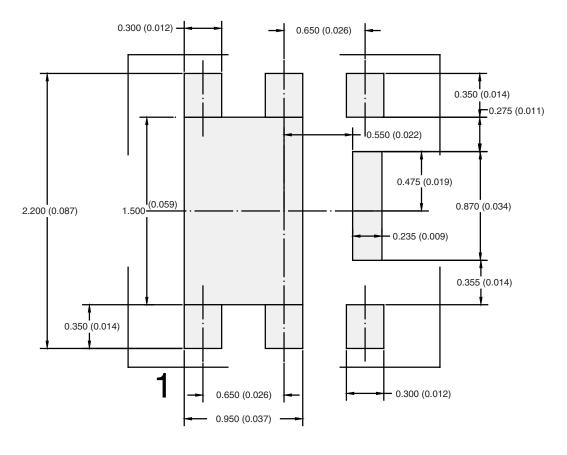
ECN: C-07431 - Rev. C, 06-Aug-07

DWG: 5934

Document Number: 73001 06-Aug-07



## RECOMMENDED PAD LAYOUT FOR PowerPAK® SC70-6L Single



Dimensions in mm/(Inches)

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ATTLICA ION NOI



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Vishay

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