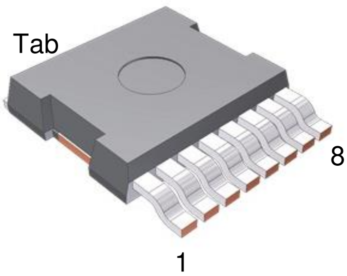
OptiMOS™-5 Power-Transistor

Product Summary

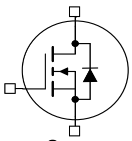
V_{DS}	80	V
$R_{DS(on)}$	1.9	mΩ
I_D	240	A

PG-HSOG-8-1



Features

- N-channel - Enhancement mode
- AEC qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green product (RoHS compliant)
- Ultra low Rds(on)
- 100% Avalanche tested



Type	Package	Marking
IAUS240N08S5N019	PG-HSOG-8-1	A08S5N19

Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	T_C=25°C, V_{GS}=10V[1]	240	A
		T_C=100 °C, V_{GS}=10 V[2]	173	
Pulsed drain current[2]	$I_{D,pulse}$	T_C=25 °C	960	
Avalanche energy, single pulse[2]	E_{AS}	I_D=120 A	400	mJ
Avalanche current, single pulse	I_{AS}	-	240	A
Gate source voltage	V_{GS}	-	±20	V
Power dissipation	P_{tot}	T_C=25 °C	230	W
Operating and storage temperature	T_j, T_{stg}	-	-55 ... +175	°C
IEC climatic category; DIN IEC 68-1	-	-	55/175/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics[2]						
Thermal resistance, junction - case	R_{thJC}	-	-	-	0.65	K/W
Electrical characteristics, at T_j=25 °C, unless otherwise specified						
Static characteristics						
Drain-source breakdown voltage[2]	$V_{(BR)DSS}$	V_{GS}=0 V, I_D=1 mA	80	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=160 µA	2.2	3	3.8	
Zero gate voltage drain current[2]	I_{DSS}	V_{DS}=80 V, V_{GS}=0 V, T_j=25 °C	-	0.1	1	µA
		V_{DS}=40 V, V_{GS}=0 V, T_j=85 °C[2]	-	1	20	
Gate-source leakage current	I_{GSS}	V_{GS}=20 V, V_{DS}=0 V	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=6 V, I_D=60 A	-	2.0	3.0	mΩ
		V_{GS}=10 V, I_D=100 A	-	1.5	1.9	

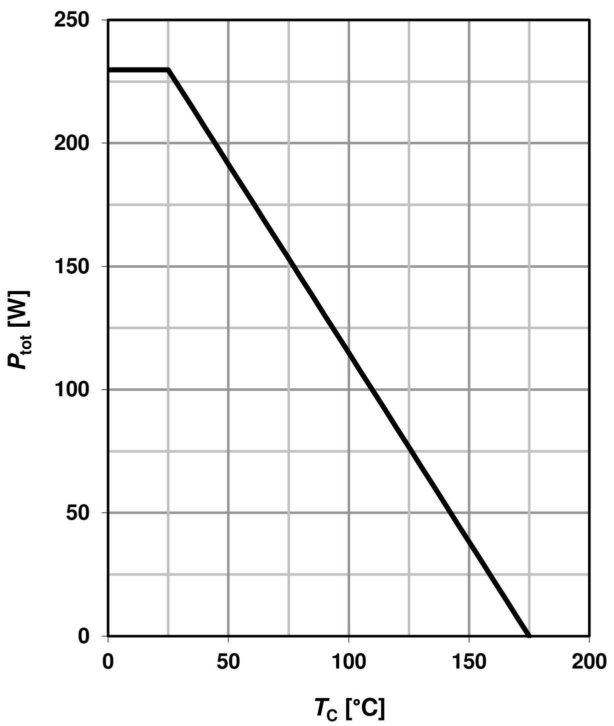
Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics[2]						
Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=40 V, f=1 MHz	-	7126	9264	pF
Output capacitance	C_{oss}		-	1152	1498	
Reverse transfer capacitance	C_{rss}		-	51	76	
Turn-on delay time	$t_{d(on)}$	V_{DD}=40 V, V_{GS}=10 V, I_D=100 A, R_G=3.5 Ω	-	18	-	ns
Rise time	t_r		-	12	-	
Turn-off delay time	$t_{d(off)}$		-	35	-	
Fall time	t_f		-	36	-	
Gate Charge Characteristics[2]						
Gate to source charge	Q_{gs}	V_{DD}=40 V, I_D=100 A, V_{GS}=0 to 10 V	-	32	42	nC
Gate to drain charge	Q_{gd}		-	22	33	
Gate charge total	Q_g		-	100	130	
Gate plateau voltage	$V_{plateau}$		-	4.7	-	V
Reverse Diode						
Diode continous forward current[2]	I_S	T_C=25 °C	-	-	240	A
Diode pulse current[2]	$I_{S,pulse}$		-	-	960	
Diode forward voltage	V_{SD}	V_{GS}=0 V, I_F=100 A, T_j=25 °C	-	0.9	1.2	V
Reverse recovery time[2]	t_{rr}	V_R=40 V, I_F=50A, di_F/dt=100 A/µs	-	71	-	ns
Reverse recovery charge[2]	Q_{rr}		-	126	-	nC

[1] Current is limited by bondwire; with an R_{thJC} = 0.65 K/W the chip is able to carry 246A at 25°C.

[2] Defined by design. Not subject to production test.

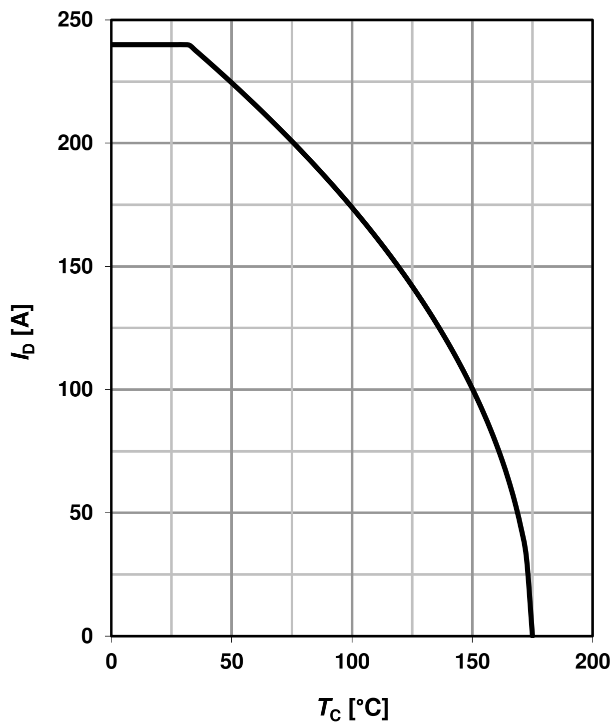
1 Power dissipation

$P_{tot} = f(T_C)$; $V_{GS} \geq 6$ V



2 Drain current

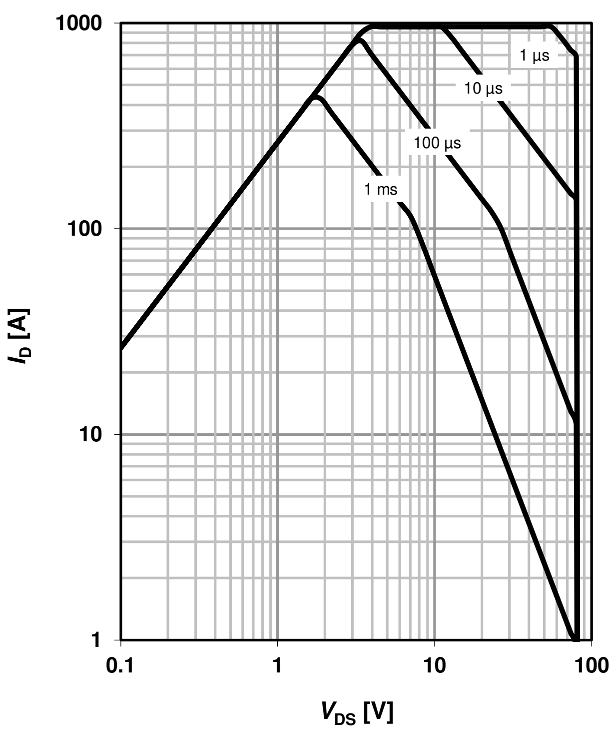
$I_D = f(T_C)$; $V_{GS} \geq 6$ V



3 Safe operating area

$I_D = f(V_{DS})$; $T_C = 25$ °C; $D = 0$

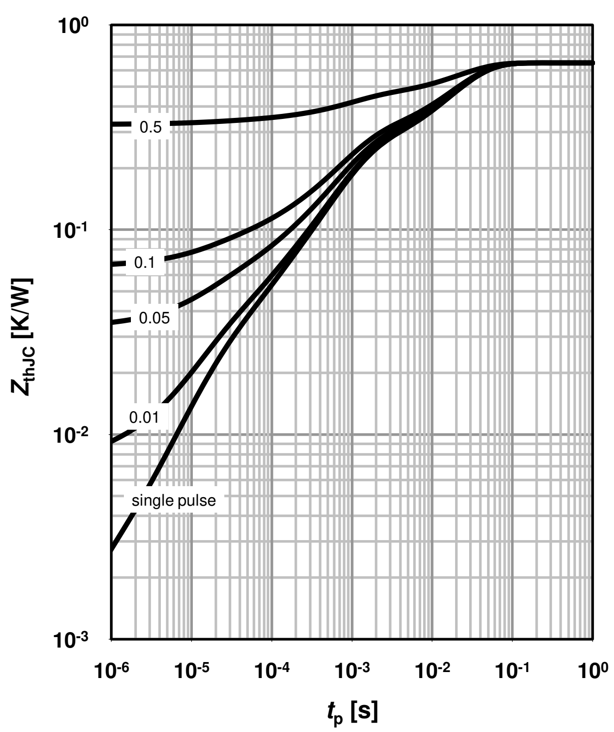
parameter: t_p



4 Max. transient thermal impedance

$Z_{thJC} = f(t_p)$

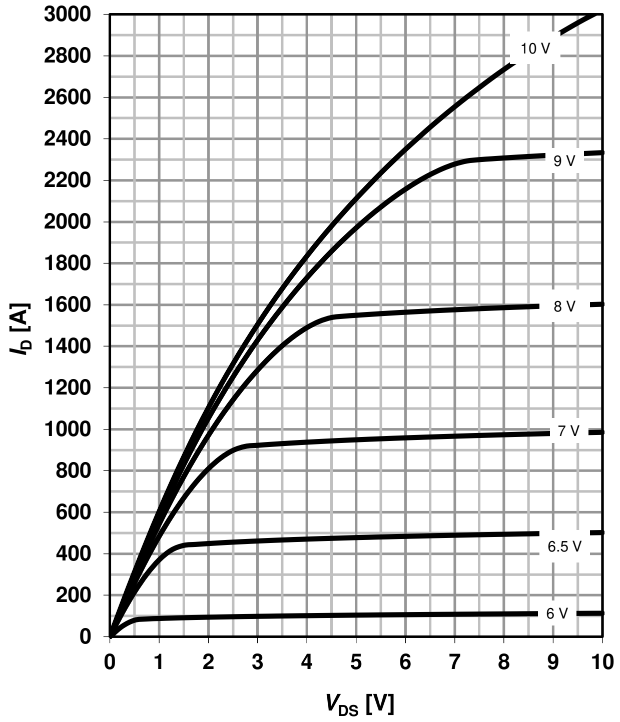
parameter: $D=t_p/T$



5 Typ. output characteristics

$I_D = f(V_{DS})$; $T_j = 25$ °C

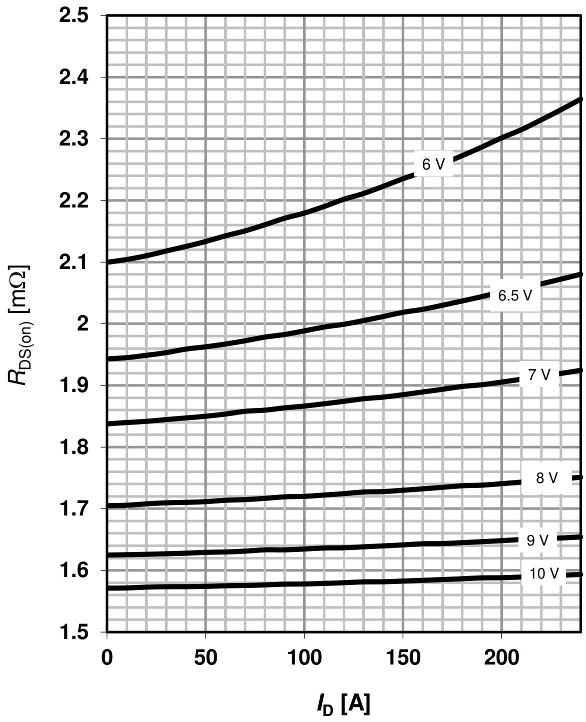
parameter: V_{GS}



6 Typ. drain-source on-state resistance

$R_{DS(on)} = f(I_D)$; $T_j = 25$ °C

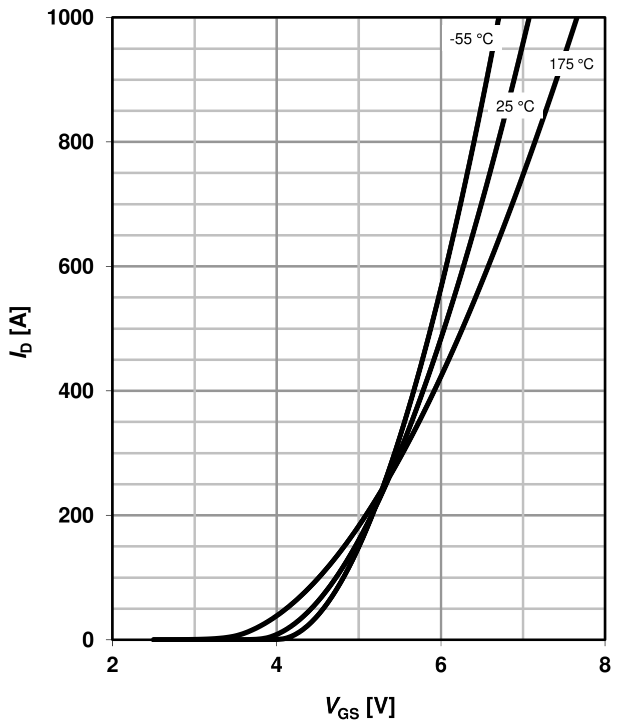
parameter: V_{GS}



7 Typ. transfer characteristics

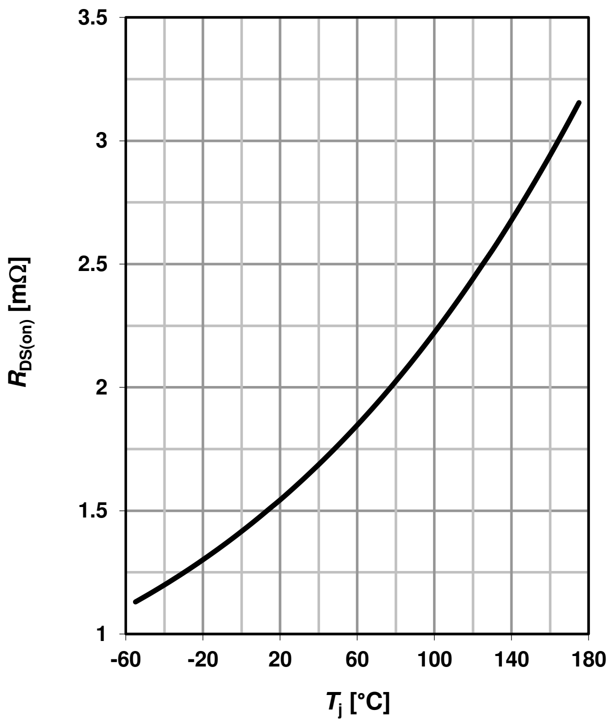
$I_D = f(V_{GS})$; $V_{DS} = 6$V

parameter: T_j



8 Typ. drain-source on-state resistance

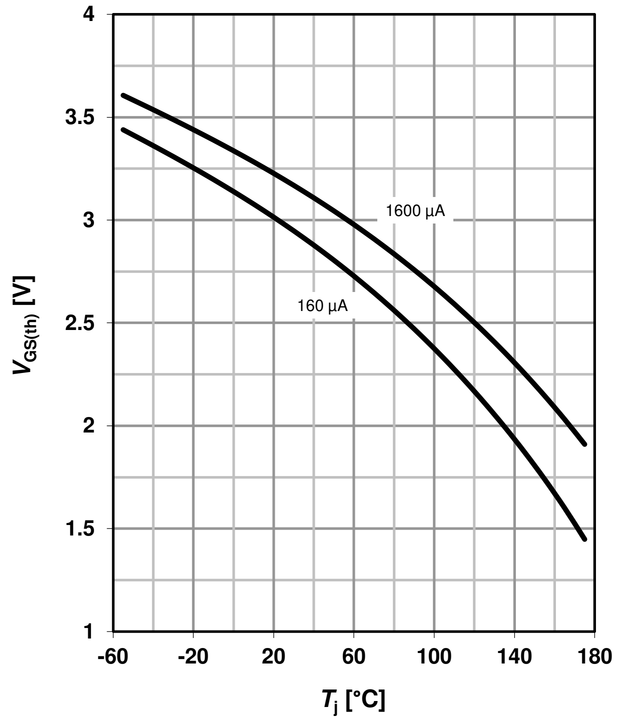
$R_{DS(on)} = f(T_j)$; $I_D = 100$ A; $V_{GS} = 10$ V



9 Typ. gate threshold voltage

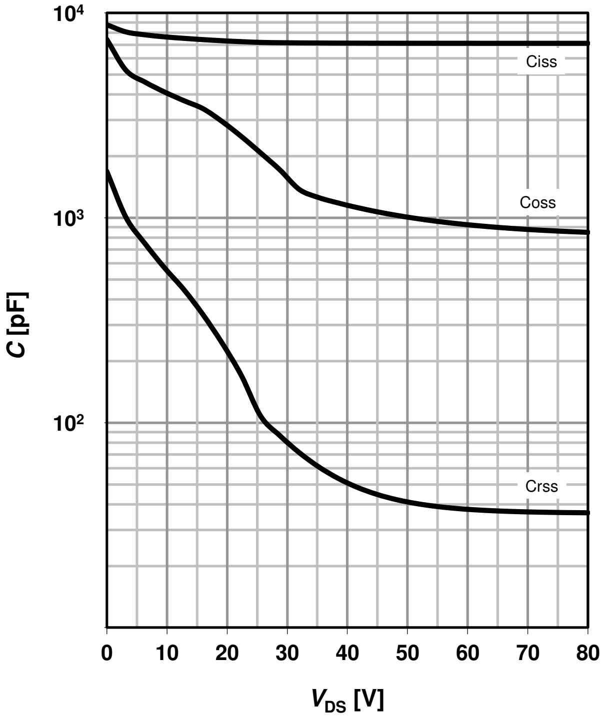
$V_{GS(th)} = f(T_j)$; $V_{GS} = V_{DS}$

parameter: I_D



10 Typ. capacitances

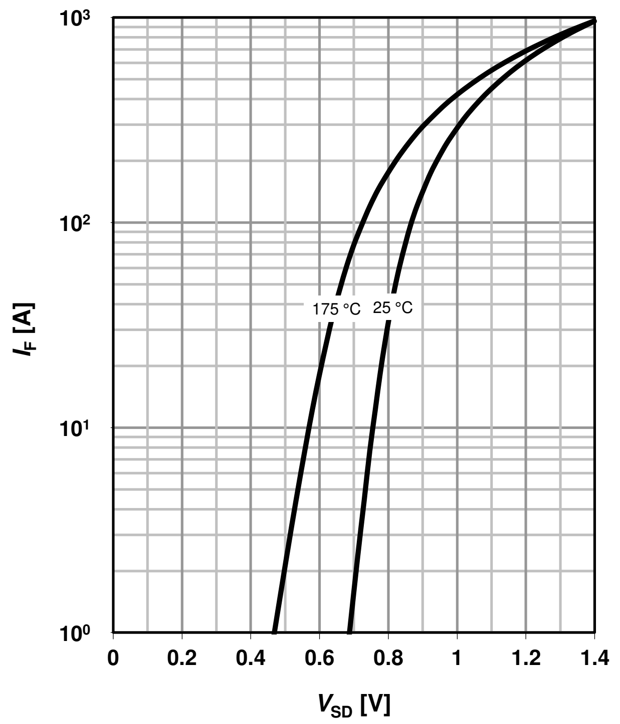
$C = f(V_{DS})$; $V_{GS} = 0$ V; $f = 1$ MHz



11 Typical forward diode characteristics

IF = f(V_{SD})

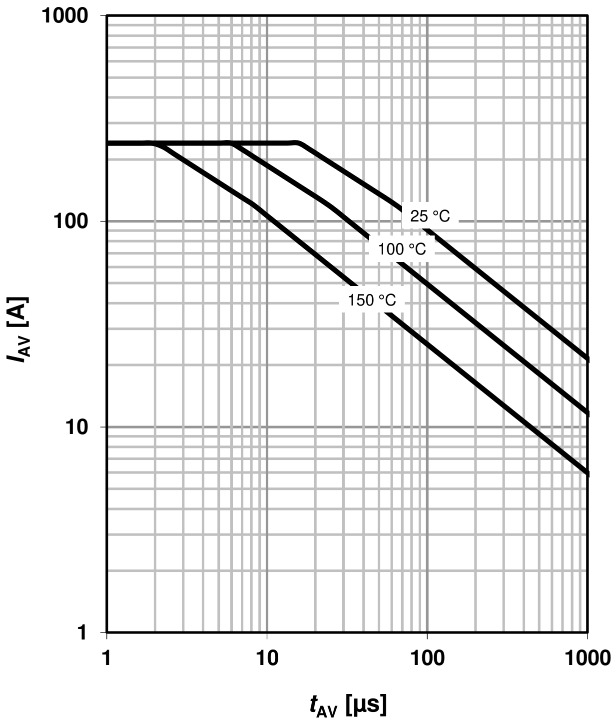
parameter: T_j



12 Typ. avalanche characteristics

$I_{AS} = f(t_{AV})$

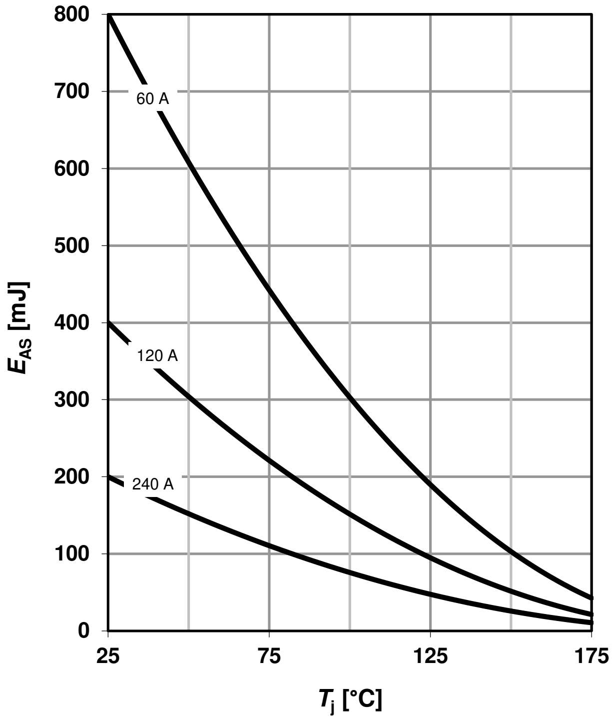
parameter: $T_{j(start)}$



13 Typical avalanche energy

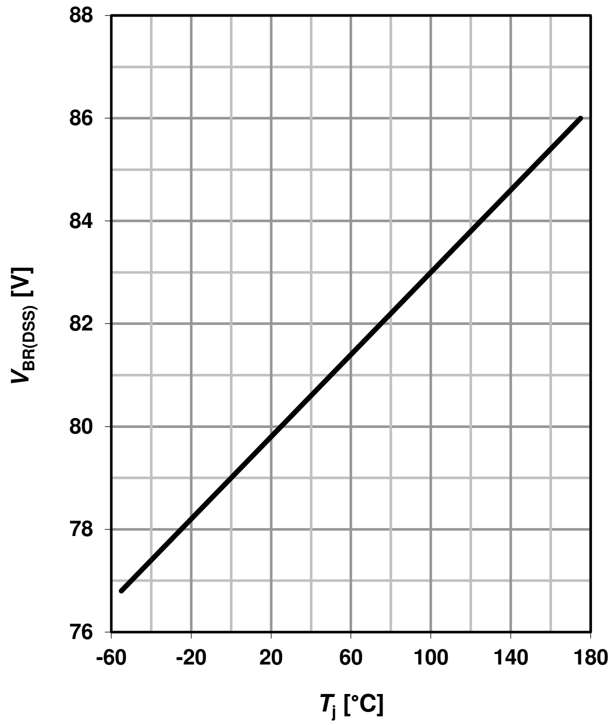
$E_{AS} = f(T_j)$

parameter: I_D



14 Drain-source breakdown voltage

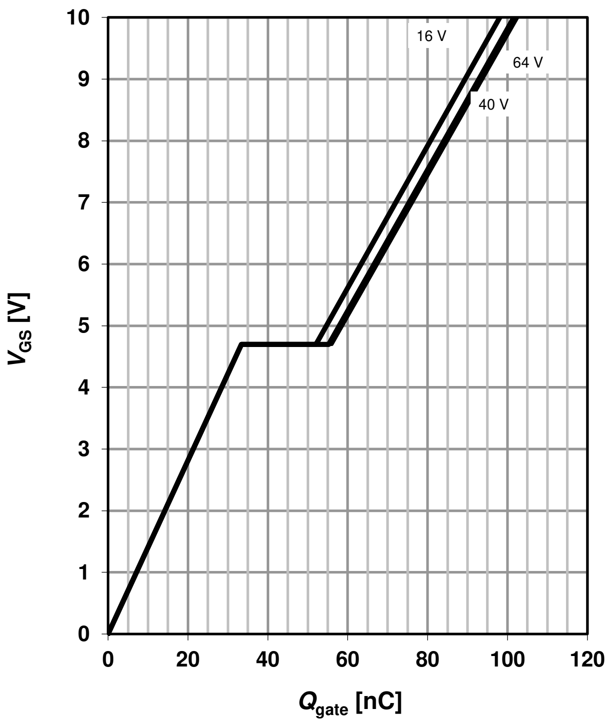
$V_{BR(DSS)} = f(T_j)$; $I_{D\_typ} = 1$ mA



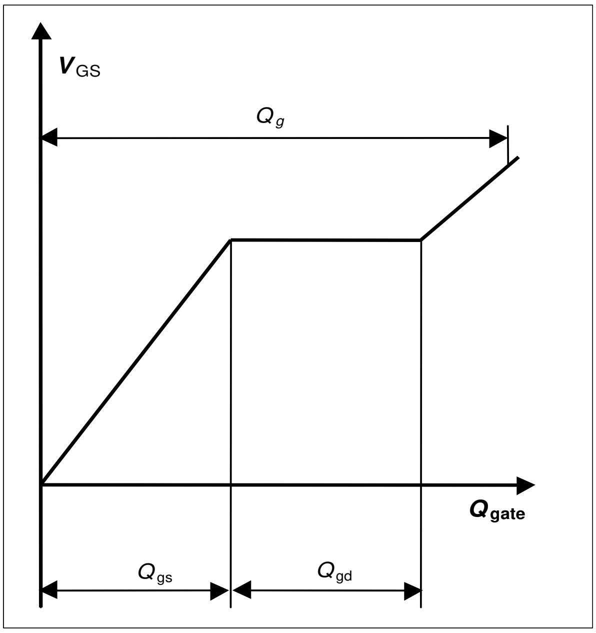
15 Typ. gate charge

$V_{GS} = f(Q_{gate})$; $I_D = 100$ A pulsed

parameter: V_{DD}



16 Gate charge waveforms



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If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

Revision History

Version	Date	Changes
Version 1.0	25.05.2018	Final Data Sheet