LOW PHASE NOISE ZERO DELAY BUFFER ICS571

Description

The ICS571 is a high speed, high output drive, low phase noise Zero Delay Buffer (ZDB) which integrates IDT's proprietary analog/digital Phase Locked Loop (PLL) techniques. IDT introduced the world standard for these devices in 1992 with the debut of the AV9170, and updated that with the ICS570. The ICS571, part of IDT's ClockBlocks™ family, was designed to operate at higher frequencies, with faster rise and fall times, and with lower phase noise. The zero delay feature means that the rising edge of the input clock aligns with the rising edges of both outputs, giving the appearance of no delay through the device. There are two outputs on the chip, one being a low-skew divide by two of the other.

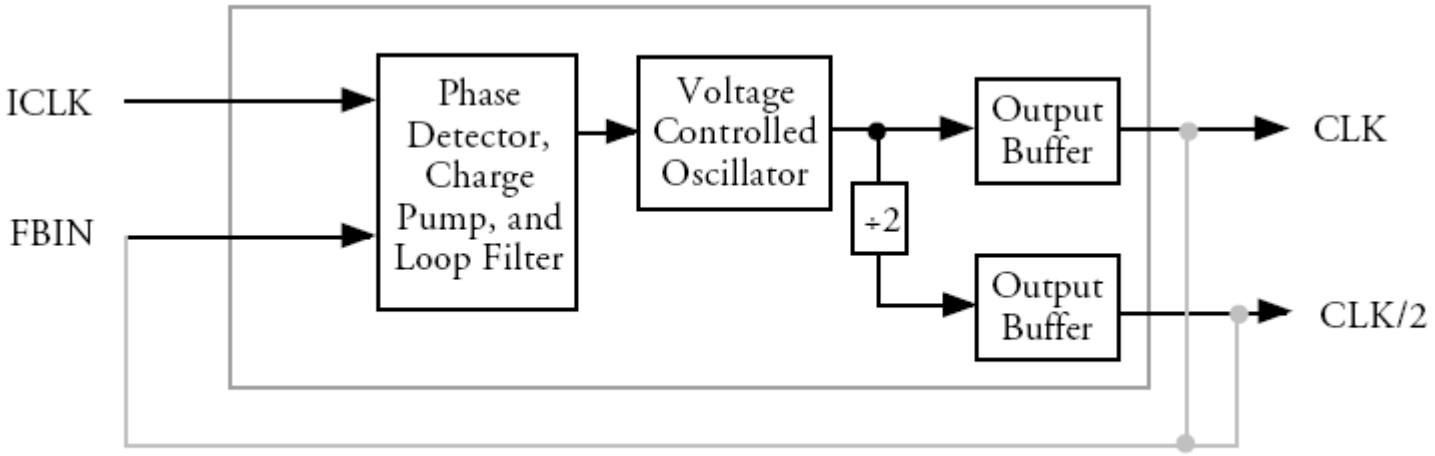
The chip is ideal for synchronizing outputs in a large variety of systems, from personal computers to data communications to video. By allowing offchip feedback paths, the ICS571 can eliminate the delay through other devices. The use of dividers in the feedback path will enable the part to multiply by more than two.

Features

- Packaged in 8-pin SOIC (Pb free available)
- Can function as low phase noise x2 multiplier
- Low skew outputs. One is ÷2 of other
- Input clock frequency up to 160 MHz at 3.3 V
- Phase noise of better than -100 dBc/Hz from 1 kHz to 1 MHz offset from carrier
- Can recover poor input clock duty cycle
- Output clock duty cycle of 45/55 at 3.3 V
- High drive strength for >100 MHz outputs
- Full CMOS clock swings with 25 mA drive capability at TTL levels
- Advanced, low power CMOS process
- Operating voltages of 3.0 to 5.5 V

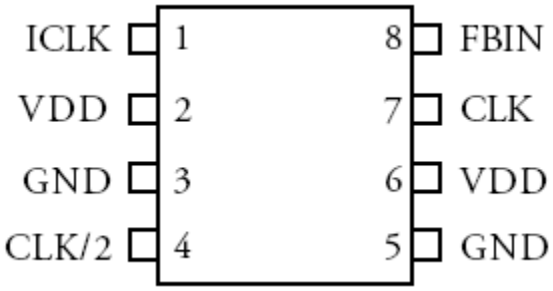
NOTE: EOL for non-green parts to occur on 5/13/10 per PDN U-09-01

Block Diagram



External feedback can come from CLK or CLK/2 (see table on page 2).

Pin Assignment



Feedback Configuration Table and Frequency Ranges (at 3.3 V)

Feedback From	CLK	CLK/2	Input Range
CLK	Input clock frequency	Input clock frequency/2	20 to 160 MHz
CLK/2	2x Input clock frequency	Input clock frequency	10 to 80 MHz

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	ICLK	CI	Reference clock input.
2	VDD	P	Connect to +3.3 V or +5 V. Must be same as other VDD.
3	GND	P	Connect to ground.
4	CLK/2	O	Clock output per table above. Low skew divide by two of pin 7 clock.
5	GND	P	Connect to ground.
6	VDD	P	Connect to +3.3 V or +5 V. Must be same as other VDD.
7	CLK	O	Clock output per table above.
8	FBIN	CI	Feedback clock input. Connect to CLK or CLK/2 per table above.

Key: CI = clock input; I = input; O = output; P = power supply connection.

External Components

The ICS571 requires a minimum number of external components for proper operation.

A decoupling capacitor of 0.01µF must be connected between VDD and GND on each side of the chip (between pins 2 and 3, and between pins 6 and 5). They must be connected close to the ICS571 to minimize lead inductance. No external power supply filtering is required for this device. A 33Ω terminating resistor can be used next to each output pin.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS571. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD, referenced to GND	7 V
Inputs, referenced to GND	-0.5 V to VDD+0.5 V
Clock Output, referenced to GND	-0.5 V to VDD+0.5 V
Storage Temperature	-65 to +150° C
Soldering Temperature, max of 10 seconds	260° C
Ambient Operating Temperature	0 to +70° C

DC Electrical Characteristics

Unless stated otherwise, **VDD = 5.0 V or 3.3 V**, Ambient Temperature 0 to +70° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Supply Voltage	VDD		3		5.5	V
Input High Voltage	V_{IH}	ICLK, FBIN (pins 1 and 8)	VDD/2+1	VDD/2		V
Input Low Voltage	V_{IL}	ICLK, FBIN (pins 1 and 8)		VDD/2	VDD/2-1	V
Output High Voltage, CMOS level	V_{OH}	I_{OH} = -4 mA	VDD-0.4			V
Output High Voltage	V_{OH}	I_{OH} = -25 mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 25 mA			0.4	V
IDD Operating Supply Current, 133 in, 133 out		No load, 3.3 V		34		mA
IDD Operating Supply Current, 50 in, 100 out		No load, 3.3 V		26		mA
Short Circuit Current	I_{OS}	Each output		±100		mA
Input Capacitance	C_{IN}	ICLK, FBIN		5		pF

AC Electrical Characteristics

Unless stated otherwise, **VDD = 5.0 V or 3.3 V**, Ambient Temperature 0 to +70° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency, clock input	f_{IN}	FB from CLK	20		160	MHz
Input Frequency, clock input	f_{IN}	FB from CLK/2	10		80	MHz
Skew CLK/2 with respect to CLK		Note 2	150	500	850	ps
Input clock to output connected to FBIN		Note 2	-500		500	ps
Output Clock Rise Time, 5 V		0.8 to 2.0 V, 15 pF load		0.3		ns
Output Clock Fall Time, 5 V		2.0 to 0.8 V, 15 pF load		0.4		ns
Output Clock Rise Time, 3.3 V		0.8 to 2.0 V, 15 pF load		0.45		ns
Output Clock Fall Time, 3.3 V		2.0 to 0.8 V, 15 pF load		0.55		ns
Input Clock Duty Cycle, 3.3 V		fin = 150 MHz	20		80	%
Output Clock Duty Cycle, 3.3 V		At VDD/2	45	49 to 51	55	%
Absolute Clock Period Jitter, CLK, Note 3		Deviation from Mean		±80		ps
One-Sigma Clock Period Jitter, CLK, Note 3				50		ps
Phase Noise, Relative to carrier		1 kHz offset		-105		dBc/Hz
Phase Noise, Relative to carrier		100 kHz offset		-115		dBc/Hz

Notes:

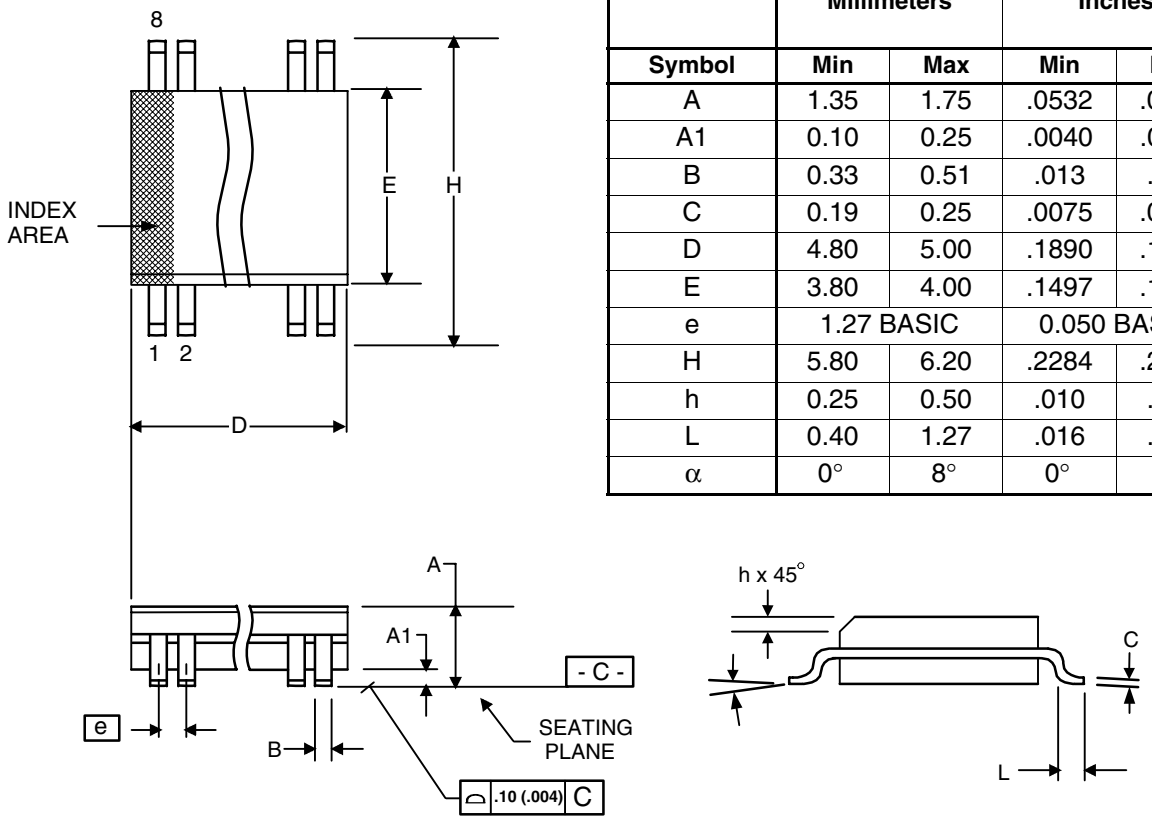
1. Sresses beyond these can permanently damage the device.
2. Assumes clocks with the same rise time, measured from rising edges at VDD/2. Measured with 33Ω termination resistors and 15 pF loads. Applies to both 3.3 V and 5 V operation.
3. CLK/2 has lower jitter (both absolute and one sigma, in ps) than CLK.

Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air				°C/W
	θ_{JA}	1 m/s air flow				°C/W
	θ_{JA}	3 m/s air flow				°C/W
Thermal Resistance Junction to Case	θ_{JC}					°C/W

Package Outline and Package Dimensions (8-pin SOIC, 150 Mil. Body)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches	
Symbol	**Min**	**Max**	**Min**	**Max**
A	1.35	1.75	.0532	.0688
A1	0.10	0.25	.0040	.0098
B	0.33	0.51	.013	.020
C	0.19	0.25	.0075	.0098
D	4.80	5.00	.1890	.1968
E	3.80	4.00	.1497	.1574
e	1.27 BASIC		0.050 BASIC	
H	5.80	6.20	.2284	.2440
h	0.25	0.50	.010	.020
L	0.40	1.27	.016	.050
α	0°	8°	0°	8°

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
571M*	ICS571M	Tubes	8-pin SOIC	0 to +70° C
571MT*		Tape and Reel	8-pin SOIC	0 to +70° C
571MLF	571MLF	Tubes	8-pin SOIC	0 to +70° C
571MLFT		Tape and Reel	8-pin SOIC	0 to +70° C

***NOTE: EOL for non-green parts to occur on 5/13/10 per PDN U-09-01**

Parts that are ordered with a "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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