
# PSMN2R2-40BS

## N-channel 40 V 2.2 mΩ standard level MOSFET in D2PAK

Rev. 1 — 20 March 2012 Product data sheet

## 1. Product profile

### 1.1 General description

Standard level N-channel MOSFET in SOT404 package qualified to 175 °C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

### 1.2 Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for standard level gate drive sources

### 1.3 Applications

- DC-to-DC convertors
- Load switching
- Motor control
- Server power supplies

### 1.4 Quick reference data

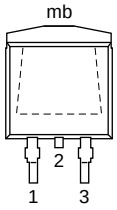
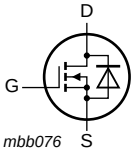
**Table 1. Quick reference data**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage | $T_j \geq 25$ °C; $T_j \leq 175$ °C | | - | - | 40 | V |
| $I_D$ | drain current | $T_{mb} = 25$ °C; $V_{GS} = 10$ V; see Figure 1 | [1] | - | - | 100 | A |
| $P_{tot}$ | total power dissipation | $T_{mb} = 25$ °C; see Figure 2 | | - | - | 306 | W |
| $T_j$ | junction temperature | | | -55 | - | 175 | °C |
| **Static characteristics** | | | | | | | |
| $R_{DSon}$ | drain-source on-state resistance | $V_{GS} = 10$ V; $I_D = 25$ A; $T_j = 100$ °C; see Figure 6 | | - | 2.73 | 3.2 | mΩ |
| | | $V_{GS} = 10$ V; $I_D = 25$ A; $T_j = 25$ °C; see Figure 6; see Figure 13 | | - | 1.88 | 2.2 | mΩ |
| **Dynamic characteristics** | | | | | | | |
| $Q_{GD}$ | gate-drain charge | $V_{GS} = 10$ V; $I_D = 25$ A; $V_{DS} = 20$ V; see Figure 14; see Figure 15 | | - | 25 | - | nC |
| $Q_{G(tot)}$ | total gate charge | | | - | 130 | - | nC |
| **Avalanche ruggedness** | | | | | | | |
| $E_{DS(AL)S}$ | non-repetitive drain-source avalanche energy | $V_{GS} = 10$ V; $T_{j(init)} = 25$ °C; $I_D = 100$ A; $V_{sup} \leq 40$ V; unclamped; $R_{GS} = 50$ Ω | | - | - | 1.24 | J |

[1] Continuous current is limited by package

## 2. Pinning information

**Table 2. Pinning information**

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|---|---|---|---|---|
| 1 | G | gate |  |  |
| 2 | D | drain[1] | | |
| 3 | S | source | | |
| mb | D | drain | | |



**SOT404 (D2PAK)**



[1] It is not possible to make connection to pin 2

## 3. Ordering information

**Table 3. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| PSMN2R2-40BS | D2PAK | plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped) | SOT404 |

## 4. Marking

**Table 4. Marking codes**

| Type number | Marking code |
|---|---|
| PSMN2R2-40BS | PSMN2R2-40BS |

## 5. Limiting values

**Table 5. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage | $T_j \geq 25$ °C; $T_j \leq 175$ °C | | - | 40 | V |
| $V_{DGR}$ | drain-gate voltage | $T_j \geq 25$ °C; $T_j \leq 175$ °C; $R_{GS} = 20$ kΩ | | - | 40 | V |
| $V_{GS}$ | gate-source voltage | | | -20 | 20 | V |
| $I_D$ | drain current | $V_{GS} = 10$ V; $T_{mb} = 100$ °C; see Figure 1 | [1] | - | 100 | A |
| | | $V_{GS} = 10$ V; $T_{mb} = 25$ °C; see Figure 1 | [1] | - | 100 | A |
| $I_{DM}$ | peak drain current | pulsed; $t_p \leq 10$ µs; $T_{mb} = 25$ °C; see Figure 3 | | - | 962 | A |
| $P_{tot}$ | total power dissipation | $T_{mb} = 25$ °C; see Figure 2 | | - | 306 | W |
| $T_{stg}$ | storage temperature | | | -55 | 175 | °C |
| $T_j$ | junction temperature | | | -55 | 175 | °C |
| $T_{sld(M)}$ | peak soldering temperature | | | - | 260 | °C |
| **Source-drain diode** | | | | | | |
| $I_S$ | source current | $T_{mb} = 25$ °C | [1] | - | 100 | A |
| $I_{SM}$ | peak source current | pulsed; $t_p \leq 10$ µs; $T_{mb} = 25$ °C | | - | 962 | A |
| **Avalanche ruggedness** | | | | | | |
| $E_{DS(AL)S}$ | non-repetitive drain-source avalanche energy | $V_{GS} = 10$ V; $T_{j(init)} = 25$ °C; $I_D = 100$ A; $V_{sup} \leq 40$ V; unclamped; $R_{GS} = 50$ Ω | | - | 1.24 | J |

[1] Continuous current is limited by package

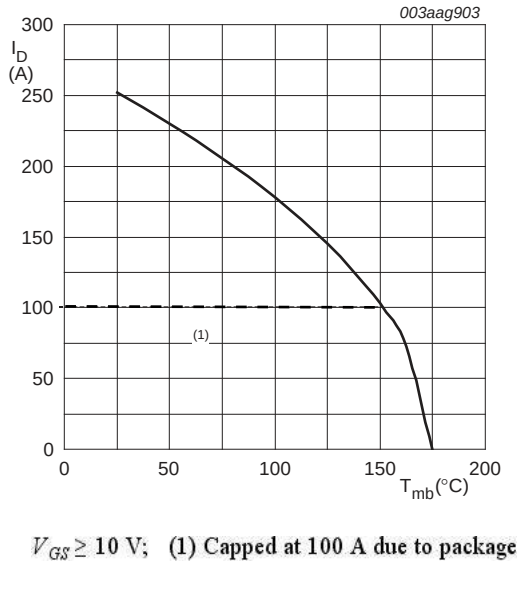



**Fig 1. Continuous drain current as a function of mounting base temperature.**

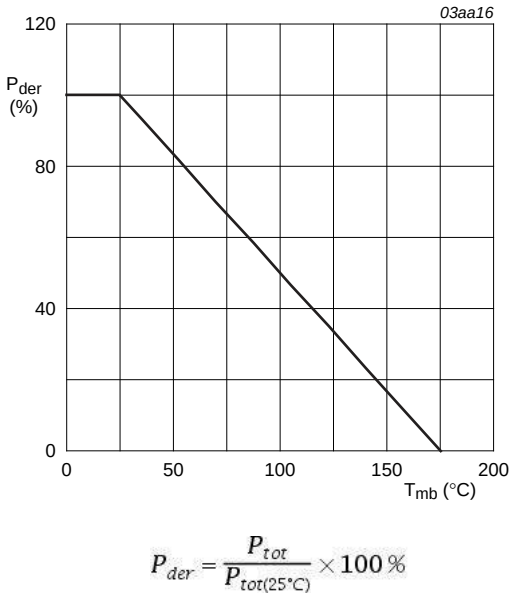
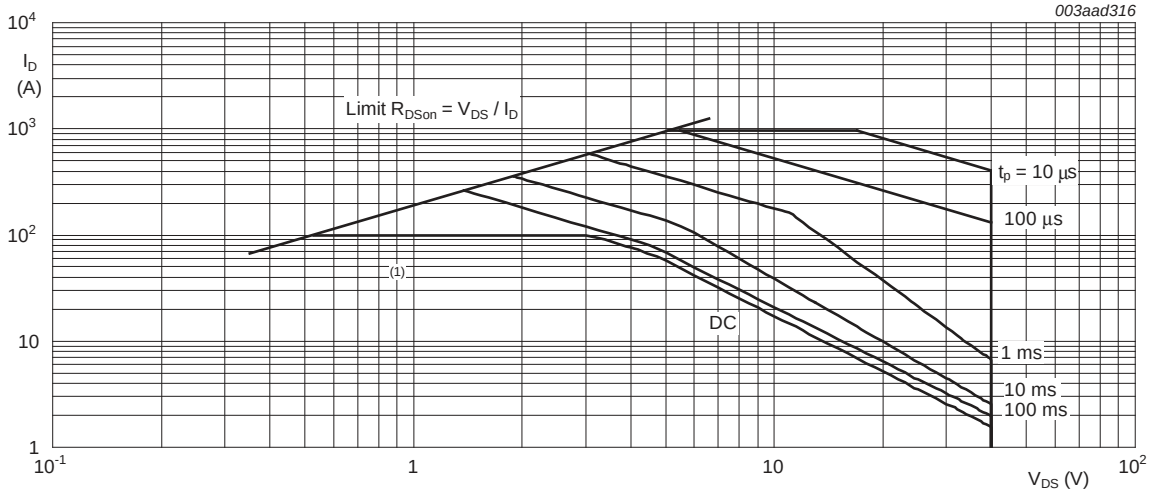



**Fig 2. Normalized total power dissipation as a function of mounting base temperature**




$T_{mb}$ = 25 °C; $I_{DM}$ is a single pulse; (1) Capped at 100 A due to package

**Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage**

# 6. Thermal characteristics

**Table 6. Thermal characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $R_{th(j\text{-}mb)}$ | thermal resistance from junction to mounting base | see Figure 4 | - | 0.25 | 0.5 | K/W |
| $R_{th(j\text{-}a)}$ | thermal resistance from junction to ambient | Minimum foot print; mounted in a printed circuit board | - | 50 | - | K/W |

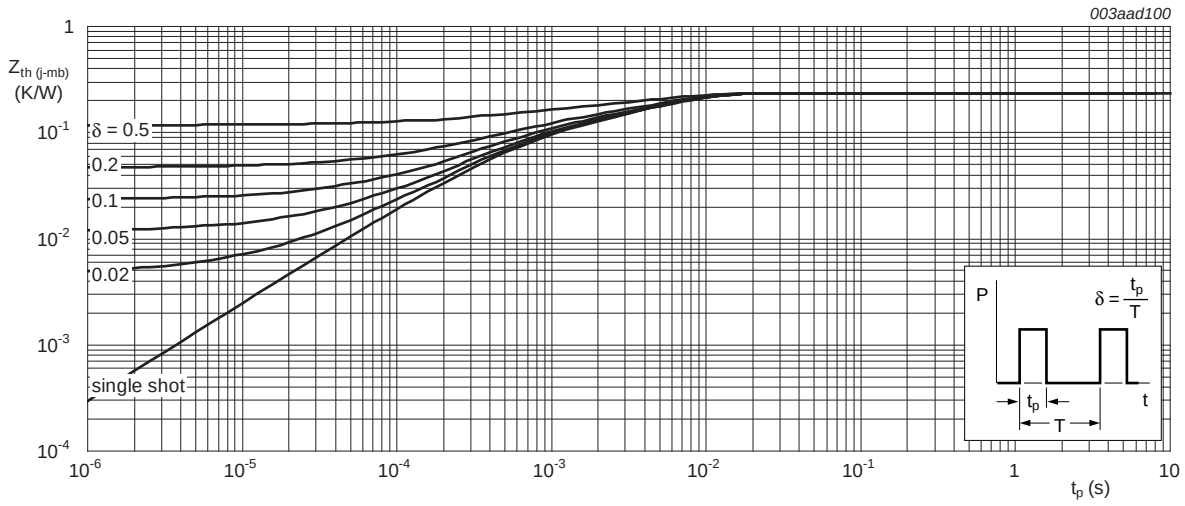



**Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration**

# 7. Characteristics

**Table 7. Characteristics**

*Tested to JEDEC standards where applicable.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Static characteristics** | | | | | | |
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $I_D$ = 250 µA; $V_{GS}$ = 0 V; $T_j$ = -55 °C | 36 | - | - | V |
| | | $I_D$ = 250 µA; $V_{GS}$ = 0 V; $T_j$ = 25 °C | 40 | - | - | V |
| $V_{GS(th)}$ | gate-source threshold voltage | $I_D$ = 1 mA; $V_{DS}$ = $V_{GS}$; $T_j$ = -55 °C; see Figure 11 | - | - | 4.6 | V |
| | | $I_D$ = 1 mA; $V_{DS}$ = $V_{GS}$; $T_j$ = 175 °C; see Figure 11 | 1 | - | - | V |
| | | $I_D$ = 1 mA; $V_{DS}$ = $V_{GS}$; $T_j$ = 25 °C; see Figure 12; see Figure 11 | 2 | 3 | 4 | V |
| $I_{DSS}$ | drain leakage current | $V_{DS}$ = 40 V; $V_{GS}$ = 0 V; $T_j$ = 25 °C | - | 0.02 | 10 | µA |
| | | $V_{DS}$ = 40 V; $V_{GS}$ = 0 V; $T_j$ = 125 °C | - | - | 200 | µA |
| $I_{GSS}$ | gate leakage current | $V_{GS}$ = 20 V; $V_{DS}$ = 0 V; $T_j$ = 25 °C | - | 10 | 100 | nA |
| | | $V_{GS}$ = -20 V; $V_{DS}$ = 0 V; $T_j$ = 25 °C | - | 10 | 100 | nA |
| $R_{DSon}$ | drain-source on-state resistance | $V_{GS}$ = 10 V; $I_D$ = 25 A; $T_j$ = 100 °C; see Figure 6 | - | 2.73 | 3.2 | mΩ |
| | | $V_{GS}$ = 10 V; $I_D$ = 25 A; $T_j$ = 175 °C; see Figure 13; see Figure 6 | - | 3.76 | 4.4 | mΩ |
| | | $V_{GS}$ = 10 V; $I_D$ = 25 A; $T_j$ = 25 °C; see Figure 6; see Figure 13 | - | 1.88 | 2.2 | mΩ |
| $R_G$ | internal gate resistance (AC) | f = 1 MHz | - | 1 | - | Ω |
| **Dynamic characteristics** | | | | | | |
| $Q_{G(tot)}$ | total gate charge | $I_D$ = 0 A; $V_{DS}$ = 0 V; $V_{GS}$ = 10 V | - | 110 | - | nC |
| | | $I_D$ = 25 A; $V_{DS}$ = 20 V; $V_{GS}$ = 10 V; see Figure 14; see Figure 15 | - | 130 | - | nC |
| $Q_{GS}$ | gate-source charge | | - | 42 | - | nC |
| $Q_{GS(th)}$ | pre-threshold gate-source charge | | - | 24 | - | nC |
| $Q_{GS(th-pl)}$ | post-threshold gate-source charge | | - | 18 | - | nC |
| $Q_{GD}$ | gate-drain charge | | - | 25 | - | nC |
| $V_{GS(pl)}$ | gate-source plateau voltage | $I_D$ = 25 A; $V_{DS}$ = 20 V; see Figure 14; see Figure 15 | - | 4.95 | - | V |
| $C_{iss}$ | input capacitance | $V_{DS}$ = 20 V; $V_{GS}$ = 0 V; f = 1 MHz; $T_j$ = 25 °C; see Figure 16 | - | 8423 | - | pF |
| $C_{oss}$ | output capacitance | | - | 1671 | - | pF |
| $C_{rss}$ | reverse transfer capacitance | | - | 814 | - | pF |
| $t_{d(on)}$ | turn-on delay time | $V_{DS}$ = 20 V; $R_L$ = 0.25 Ω; $V_{GS}$ = 10 V; $R_{G(ext)}$ = 1.5 Ω | - | 33.2 | - | ns |
| $t_r$ | rise time | | - | 40.4 | - | ns |
| $t_{d(off)}$ | turn-off delay time | | - | 66.6 | - | ns |
| $t_f$ | fall time | | - | 25.2 | - | ns |

**Table 7. Characteristics** *...continued*

*Tested to JEDEC standards where applicable.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Source-drain diode** | | | | | | |
| $V_{SD}$ | source-drain voltage | $I_S$ = 25 A; $V_{GS}$ = 0 V; $T_j$ = 25 °C; see Figure 17 | - | 0.85 | 1.2 | V |
| $t_{rr}$ | reverse recovery time | $I_S$ = 25 A; $dI_S/dt$ = -100 A/µs; $V_{GS}$ = 0 V; $V_{DS}$ = 20 V | - | 53.7 | - | ns |
| $Q_r$ | recovered charge | $I_S$ = 25 A; $dI_S/dt$ = -100 A/µs; $V_{GS}$ = 0 V; $V_{DS}$ = 20 V; $T_j$ = 25 °C | - | 80.75 | - | nC |

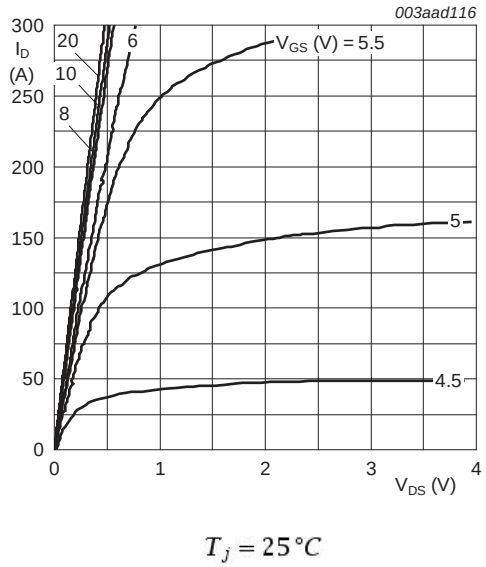



**Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values**

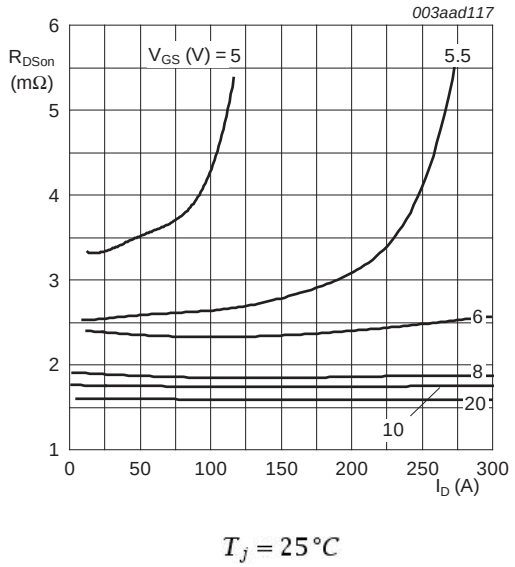
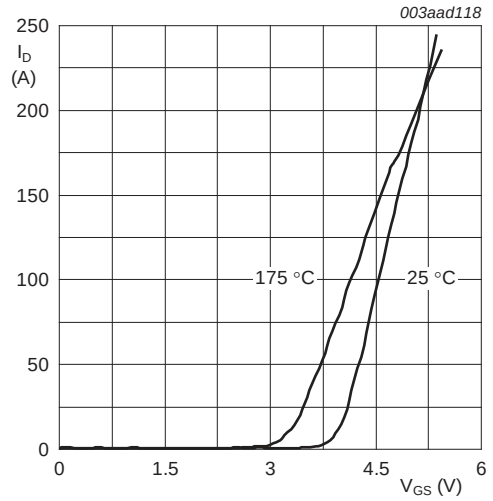
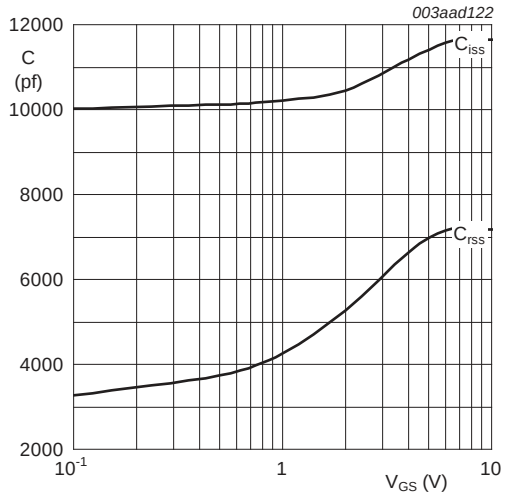



**Fig 6. Drain-source on-state resistance as a function of drain current; typical values**



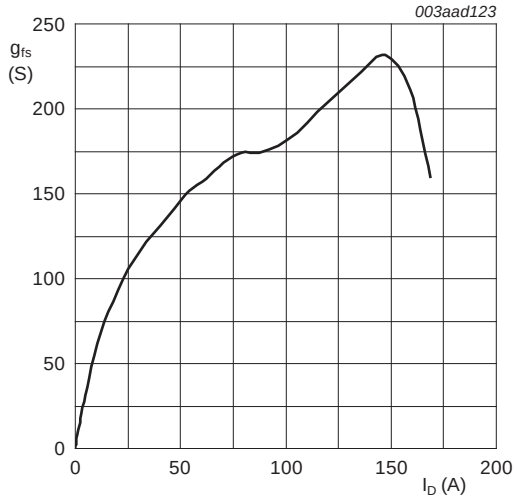

$V_{DS} > I_D \times R_{DSon}$

**Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values**



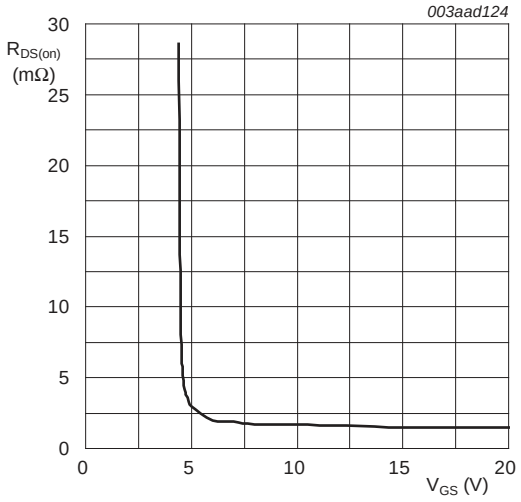

$V_{DS} = 0V; f = 1MHz$

**Fig 8. Input and reverse transfer capacitances as a function of gate-source voltage; typical values**



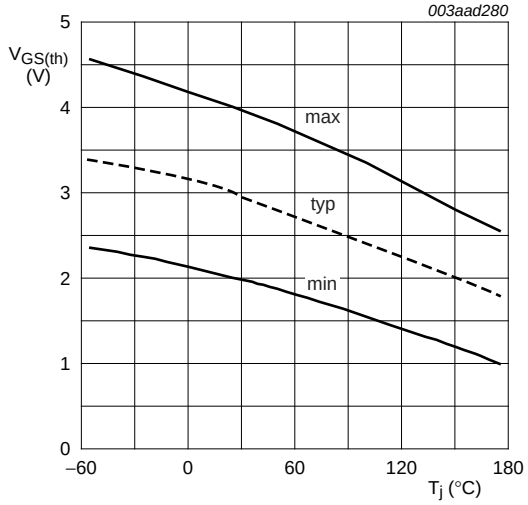

$T_j = 25°C; V_{DS} = 25V$

**Fig 9. Forward transconductance as a function of drain current; typical values**



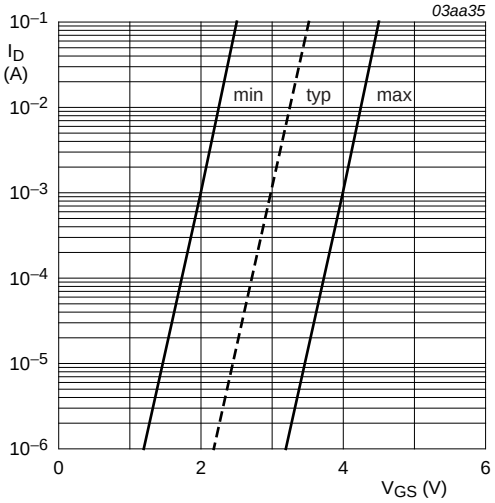

$T_j = 25\ °C; I_D = 25\ A$

**Fig 10. Drain-source on-state resistance as a function of gate-source voltage; typical values**



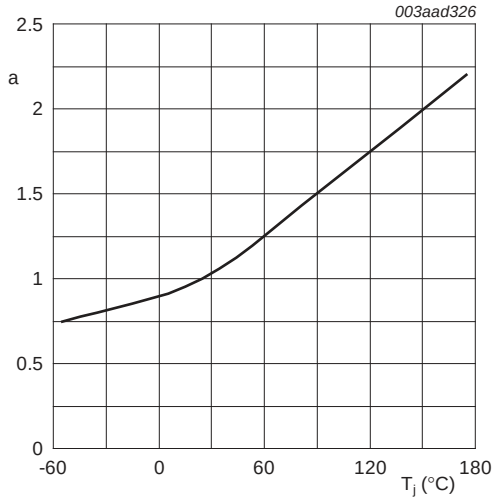

$I_D = 1\,\text{mA};\ V_{DS} = V_{GS}$

**Fig 11. Gate-source threshold voltage as a function of junction temperature**




$T_j = 25\,°C;\ V_{DS} = 5V$

**Fig 12. Sub-threshold drain current as a function of gate-source voltage**




$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

**Fig 13. Normalized drain-source on state resistance factor as a function of junction temperature**

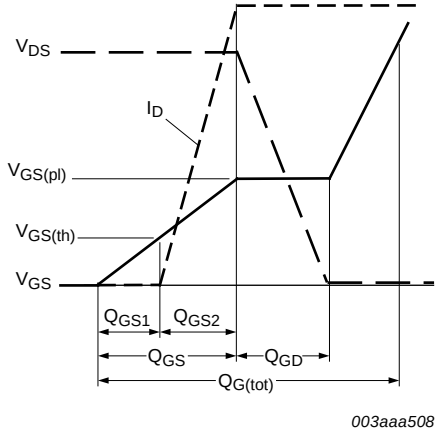
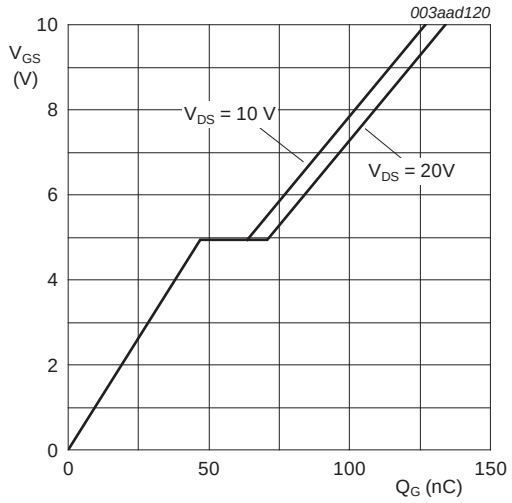
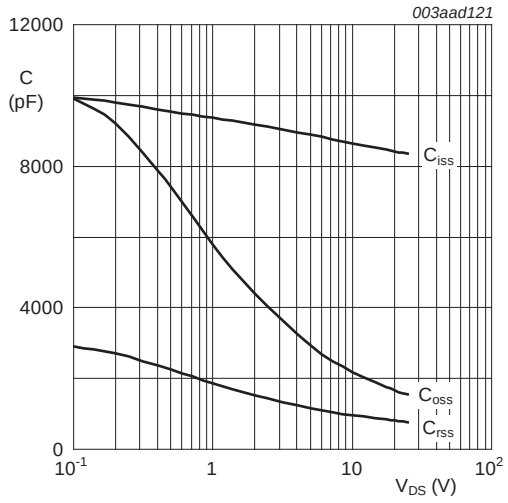



**Fig 14. Gate charge waveform definitions**



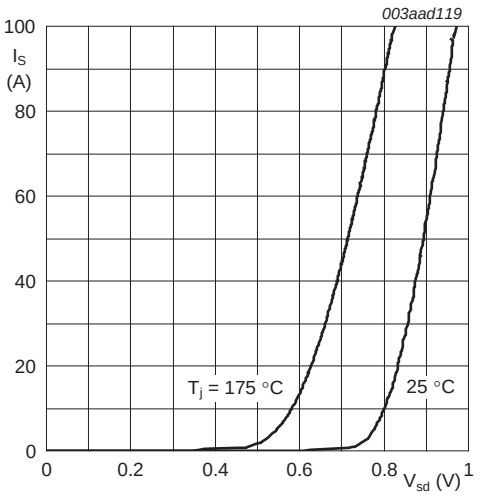

$T_j = 25\ °C;\ I_D = 25\ A$

**Fig 15. Gate-source voltage as a function of gate charge; typical values**




$V_{GS} = 0V; f = 1MHz$

**Fig 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**

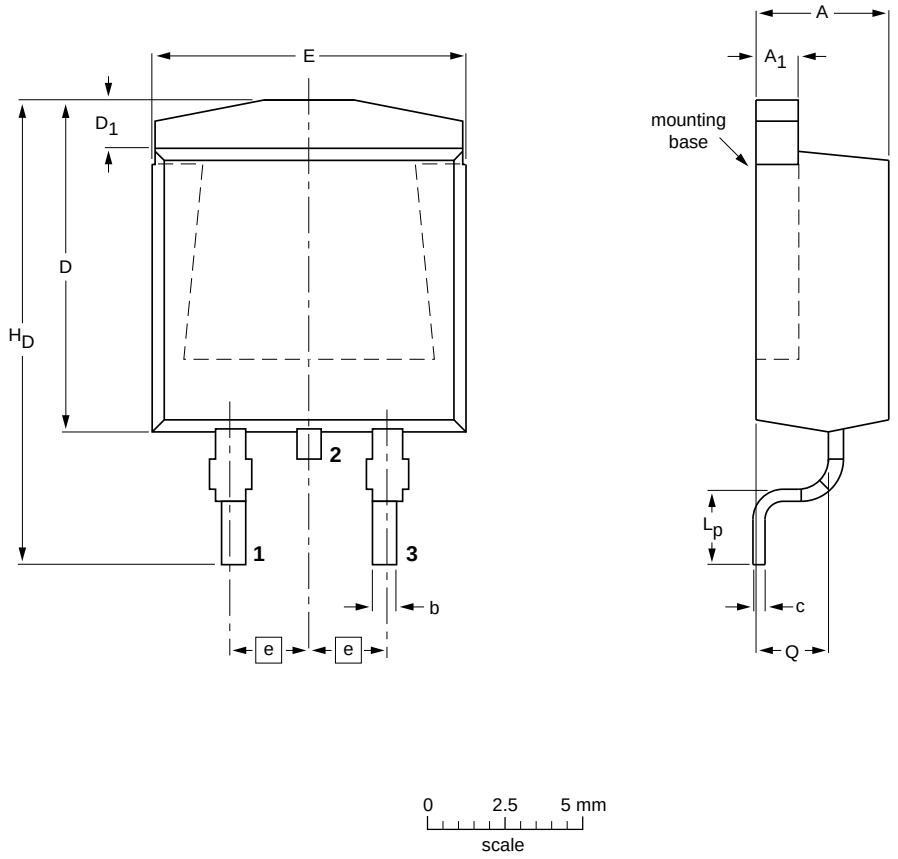



$V_{GS} = 0V$

**Fig 17. Source current as a function of source-drain voltage; typical values**

# 8. Package outline

**Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)** **SOT404**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A | $A_1$ | b | c | D max. | $D_1$ | E | e | $L_p$ | $H_D$ | Q |
|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 4.50<br>4.10 | 1.40<br>1.27 | 0.85<br>0.60 | 0.64<br>0.46 | 11 | 1.60<br>1.20 | 10.30<br>9.70 | 2.54 | 2.90<br>2.10 | 15.80<br>14.80 | 2.60<br>2.20 |

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT404 | | | | | | ~~05-02-11~~<br>06-03-16 |

**Fig 18. Package outline SOT404 (D2PAK)**

# 9. Revision history

**Table 8. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| PSMN2R2-40BS v.1 | 20120320 | Product data sheet | - | - |

# 10. Legal information

## 10.1 Data sheet status

| Document status[1] [2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

## 10.2 Definitions

**Preview** — The document is a preview version only. The document is still subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Draft** — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet** — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

**Product specification** — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

## 10.3 Disclaimers

**Limited warranty and liability** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use** — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Quick reference data** — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

**Limiting values** — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

**Terms and conditions of commercial sale** — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

**No offer to sell or license** — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

**Export control** — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

**Non-automotive qualified products** — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

**Translations** — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

## 10.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

**Adelante**,**Bitport**,**Bitsound**,**CoolFlux**,**CoReUse**,**DESFire**,**EZ-HV**,**FabKey**,**GreenChip**,**HiPerSmart**,**HITAG**,**I²C-bus** logo,**ICODE**,**I-CODE**,**ITEC**,**Labelution**,**MIFARE**,**MIFARE Plus**,**MIFARE Ultralight**,**MoReUse**,**QLPAK**,**Silicon Tuner**,**SiliconMAX**,**SmartXA**,**STARplug**,**TOPFET**,**TrenchMOS**,**TriMedia** and**UCODE** — are trademarks of NXP B.V.

**HD Radio** and**HD Radio** logo — are trademarks of iBiquity Digital Corporation.

# 11. Contact information

For more information, please visit:http://www.nxp.com

For sales office addresses, please send an email to:salesaddresses@nxp.com

## 12. Contents





For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

**Date of release: 20 March 2012**
**Document identifier: PSMN2R2-40BS**