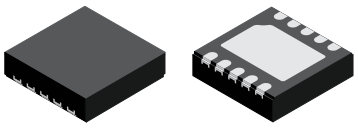
A89500

100 V Half-Bridge MOSFET Driver

FEATURES AND BENEFITS

- Half-bridge MOSFET driver
- AEC-Q100 qualified (K version)
- Suitable for 12 V, 24 V, and 48 V power networks
- Operates with up to 100 V bridge supply
- 8 to 15 V supply voltage
- Bootstrap gate drive for N-channel MOSFET bridge
- Cross-conduction protection
- Individual MOSFET control
- Low-power sleep mode
- Supply undervoltage lockout

PACKAGE:



Not to scale

10-lead DFN with wettable flank and exposed pad (suffix EJ)

DESCRIPTION

The A89500 is an N-channel power MOSFET driver capable of controlling MOSFETs connected in a half-bridge arrangement with up to 100 V bridge supply. It is specifically designed for applications with high-power inductive loads, such as brush DC motors, solenoids, and actuators and is compatible with 12 V, 24 V, and 48 V power networks.

Internal logic prevents the gate drive outputs from turning on at the same time, preventing cross-conduction. Each MOSFET is controlled by an independent logic-level input compatible with 3.3 V and 5 V logic.

The A89500 can be placed in a low-power sleep mode by a third discrete input. It requires a single 8 to 15 V supply to power the gate drivers.

The A89500 is supplied in a 10-lead DFN (suffix EJ) with wettable flank and exposed thermal pad. This package is lead (Pb) free, with 100% matte-tin leadframe plating.

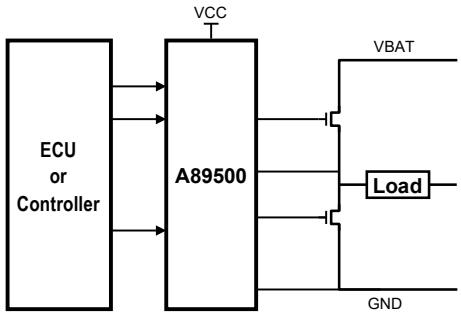


Figure 1: Typical Application

Table of Contents

SELECTION GUIDE

Part Number	Ambient Temperature Range (T_A)	Packing	Package
A89500GEJTR-T	–40°C to 105°C	1500 pieces per 7-inch reel	3 mm × 3 mm, 0.8 mm maximum height 10-lead DFN with exposed thermal pad and wettable flank
A89500KEJSR	–40°C to 150°C	6000 pieces per 13-inch reel	

ABSOLUTE MAXIMUM RATINGS [1]

Characteristic	Symbol	Notes	Rating	Unit
Supply Voltage	V_{CC}	VCC	–0.3 to 18	V
Logic Input Terminals	V_{IB}	HS, LS, RESETn	–0.3 to 6	V
Bootstrap Supply Terminal	V_C	C	–0.3 to V_{CC} + 100	V
High-Side Gate Drive Output Terminal	V_{GH}	GH	V_C – 16 to V_C + 0.3	V
		GH (transient)	V_C – 18 to V_C + 0.3	V
High-Side Source (Load) Terminal	V_S	S	V_C – 16 to V_C + 0.3	V
		S (transient)	V_C – 18 to V_C + 0.3	V
Low-Side Gate Drive Output Terminal	V_{GL}	GL	–0.3 to 18	V
Ambient Operating Temperature Range	T_A	Range G, limited by power dissipation	–40 to 105	°C
		Range K, limited by power dissipation	–40 to 150	°C
Maximum Continuous Junction Temperature	$T_{J(max)}$		165	°C
Transient Junction Temperature	T_{Jt}	Overtemperature event not exceeding 10 seconds; lifetime duration not exceeding 10 hours; guaranteed by design characterization.	180	°C
Storage Temperature Range	T_{stg}		–55 to 150	°C

[1] With respect to GND. Ratings apply when no other circuit operating constraints are present.

THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Symbol	Test Conditions [1]	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	4-layer PCB based on JEDEC standard	28	°C/W
		2-layer PCB with 3.8 in.^{2} copper each side	38	°C/W
	$R_{\theta JP}$		2	°C/W

[1] Additional thermal information available on the Allegro website.

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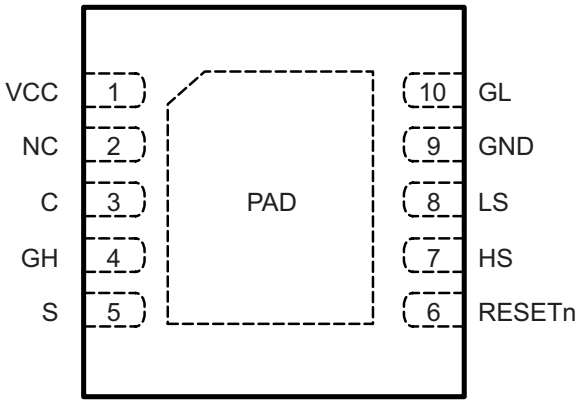
PINOUT DIAGRAM AND TERMINAL LIST



10-Lead DFN
(Suffix EJ)

Terminal List

Number	Name	Function
3	C	Bootstrap capacitor
4	GH	High-side gate drive output
10	GL	Low-side gate drive output
9	GND	Ground
7	HS	High-side control logic input
8	LS	Low-side control logic input
2	NC	No internal connection; connect to GND
6	RESETn	Standby mode control logic input
5	S	Load connection
1	VCC	Gate drive power supply input
–	PAD	Thermal pad; connect to GND

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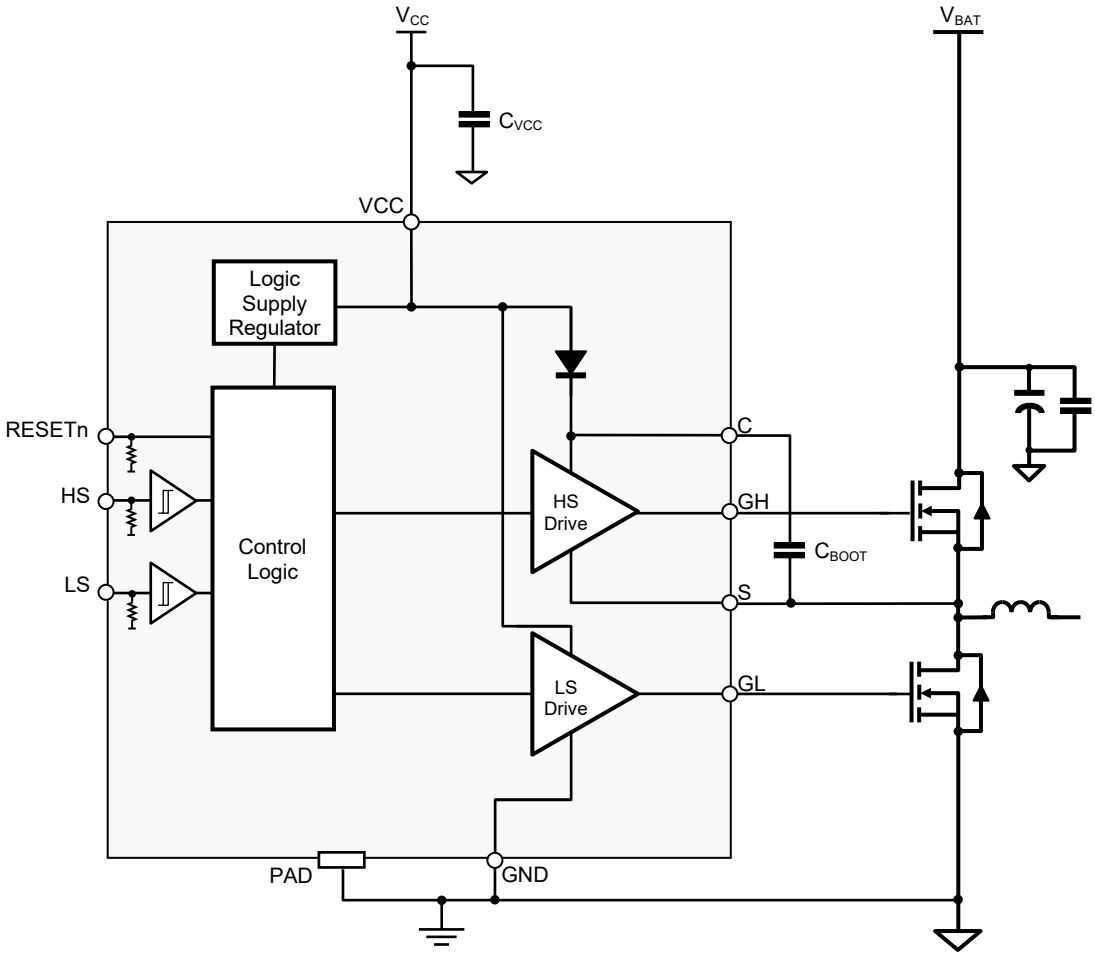
FUNCTIONAL BLOCK DIAGRAM



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ELECTRICAL CHARACTERISTICS: Valid at V_{CC} = 8 to 15 V; T_A = 25°C (G version) or T_J = –40°C to 150°C (K version), unless noted otherwise

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
SUPPLY AND REFERENCE						
VCC Functional Operating Range	V_{CC}	Operating, outputs active	8	–	15	V
		No unsafe states	0	–	15	V
VCC Quiescent Current	I_{CCQ}	RESETn = high, all gate drive outputs low	–	–	3	mA
	I_{CCS}	RESETn ≤ 300 mV, sleep mode	–	–	20	µA
VCC Undervoltage	V_{CCUV}	V_{CC} falling	6.3	6.65	7	V
VCC Undervoltage Hysteresis	$V_{CCUVHys}$		0.2	–	0.5	V
Internal Logic Supply Regulator Voltage [2]	V_{DL}		3	3.3	3.6	V
Bootstrap Diode Forward Voltage	V_{fBOOT}	I_D = 1 mA	0.7	1.3	1.7	V
		I_D = 100 mA	1.6	2.0	2.4	V
GATE OUTPUT DRIVE						
Turn-On Time, High-Side	$t_{r(HS)}$	C_{LOAD} = 33 nF, 2 to 8 V, $V_C – V_S$ = 12 V	–	105	231	ns
Turn-On Time, Low-Side	$t_{r(LS)}$	C_{LOAD} = 33 nF, 2 to 8 V, V_{CC} = 12 V	–	105	231	ns
Turn-Off Time, High-Side	$t_{f(HS)}$	C_{LOAD} = 33 nF, 8 to 2 V, $V_C – V_S$ = 12 V	–	46	133	ns
Turn-Off Time, Low-Side	$t_{f(LS)}$	C_{LOAD} = 33 nF, 8 to 2 V, V_{CC} = 12 V	–	46	133	ns
Pull-Up Peak Source Current, High-Side [1]	$I_{PUPK(HS)}$	$V_C – V_S$ = 12 V	–	–2.7	–1.5	A
Pull-Up Peak Source Current, Low-Side [1]	$I_{PUPK(LS)}$	V_{CC} = 12 V	–	–2.7	–1.5	A
Pull-Up On Resistance	$R_{DS(on)UP}$	T_J = 25°C, I_{GH} = –150 mA [1]	1.2	–	3.4	Ω
		T_J = 150°C, I_{GH} = –150 mA [1] (K version only)	2.0	–	5.1	Ω
Pull-Down Peak Sink Current [1]	I_{PDPK}	V_{CC} = 12 V	3.1	5.2	–	A
Pull-Down On Resistance	$R_{DS(on)DN}$	T_J = 25°C, I_{GL} = –150 mA [1]	0.4	–	1.0	Ω
		T_J = 150°C, I_{GL} = –150 mA [1] (K version only)	0.6	–	1.3	Ω
GH Output Voltage High	V_{GHH}	–1 mA < I_{GH} [1], 1 mA	V_C – 0.02	–	–	V
GH Output Voltage Low	V_{GHL}	–1 mA < I_{GH} [1], 1 mA	–	–	V_S + 0.02	V
GL Output Voltage High	V_{GLH}	–1 mA < I_{GL} [1], 1 mA	V_{CC} – 0.02	–	–	V
GL Output Voltage Low	V_{GLL}	–1 mA < I_{GL} [1], 1 mA	–	–	0.02	V
GH Passive Pull-Down	R_{GHPD}	VCC open circuit, $V_{GH} – V_S$ = 0.1 V	45	950	1700	kΩ
GL Passive Pull-Down	R_{GLPD}	VCC open circuit, V_{GL} = 0.1 V	45	950	1700	kΩ
GH Active Pull-Down	R_{GHPA}	$V_C – V_S$ > 3 V	5.9	10	37.6	kΩ
GL Active Pull-Down	R_{GLPA}	V_{CC} > 3 V	5.9	10	37.6	kΩ
Turn-Off Propagation Delay	$t_{P(off)}$	Input change to unloaded gate output change	17	–	32	ns
Turn-On Propagation Delay	$t_{P(on)}$	Input change to unloaded gate output change	17	–	32	ns
Propagation Delay Matching (On to Off)	Δt_{OO}		–	3	15	ns
LOGIC INPUTS						
Input Low Voltage	V_{IL}	HS, LS, RESETn	–	–	1.0	V
Input High Voltage	V_{IH}	HS, LS, RESETn	2.0	–	–	V
Input Hysteresis	V_{Ihys}	All logic inputs	200	300	600	mV
Input Pull-Down	R_{PD}	LS, HS, RESETn, 0 < V_{IN} < 6 V	–	50	–	kΩ

[1] For input and output current specifications, negative current is defined as coming out of (sourcing) the specified device terminal.
[2] VDL derived from VCC for internal use only. Not accessible on any device terminal.

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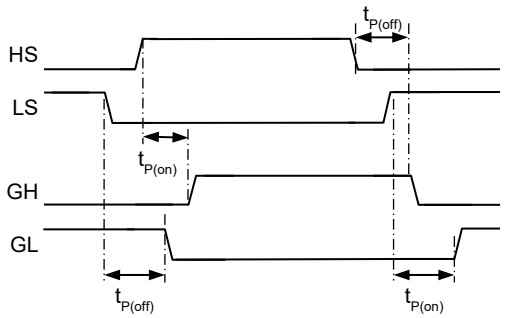

Figure 2: Gate Drive Timing – Control Inputs

Table 1: Control Logic – Logic Inputs

HS	LS	GH	GL	S	Comment
0	0	LO	LO	Z	Bridge disabled
0	1	LO	HI	LO	Bridge sinking
1	0	HI	LO	HI	Bridge sourcing
1	1	LO	LO	Z	Bridge disabled

HI = high-side FET active, LO = low-side FET active,
Z = high impedance, both FETs off,
RESETn = high

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FUNCTIONAL DESCRIPTION

The A89500 is a half-bridge MOSFET driver requiring a single supply of 8 to 15 V. The device high-side output stage is designed to operate at voltages up to 100 V, allowing the part to be used with 12 V, 24 V, and 48 V power networks.

The two high-current gate drives are capable of driving a wide range of N-channel power MOSFETs and are configured as a half-bridge driver with one high-side drive and one low-side drive.

Gate drive voltages are unregulated and are derived from the device V_{CC} supply.

A RESETn input allows the part to be put into a low-power sleep mode, and two logic-level inputs control the gate drive outputs. All logic inputs are compatible with 3.3 V and 5 V logic.

Input and Output Terminal Functions

VCC: The main power supply for the device. The main power supply should be connected to VCC through a reverse voltage protection circuit and should be decoupled with a ceramic capacitor, C_{VCC}, connected close to the supply and ground terminals.

GND: Analog, digital, and power ground. Connect to supply ground.

C: High-side connection for the bootstrap capacitor and positive supply for the high-side gate driver.

GH: High-side gate-drive output for an external N-channel MOSFET.

S: Source connection for the high-side MOSFET providing the negative supply connections for the floating high-side driver.

GL: Low-side gate-drive output for an external N-channel MOSFET.

HS: Logic input with pull-down to control the high-side gate drive.

LS: Logic input with pull-down to control the low-side gate drive.

RESETn: Disables part. Device disabled when taken low.

Power Supply

A single power supply voltage is required for the gate drivers and the internal logic. The supply, V_{CC}, should be connected to the VCC terminal through a reverse voltage protection circuit. A ceramic decoupling capacitor must be connected close to the VCC and GND terminals. Guidance on selecting a value of VCC capacitor is provided in the Application Information section below.

An internal regulator provides the supply to the internal logic. All logic is guaranteed to operate correctly to below the regulator undervoltage levels, ensuring that the A89500 will continue to operate safely until all logic is reset when a power-on-reset state is present.

The A89500 will operate within specified parameters with V_{CC} from 8 to 15 V.

Gate Drives

The A89500 is designed to drive external low on-resistance, power N-channel MOSFETs. It will supply the large transient currents necessary to quickly charge and discharge the external MOSFET gate capacitance in order to reduce dissipation in the external MOSFET during switching. The charge current for the low-side drive is provided directly by the VCC supply, and this must be capable of supporting the required pulsed current demands. The charge current for the high-side drives is provided by the bootstrap capacitor connected between the C and S terminals. MOSFET gate charge and discharge rates may be controlled by connecting an external gate resistor between the gate drive output and the gate terminal of the MOSFET. Guidance on estimating average operating VCC supply current is presented in the Application Information section below.

Bootstrap Supply

When the high-side drivers are active, the reference voltage for the driver will rise to close to the bridge supply voltage. The supply to the driver will then have to be above the bridge supply voltage to ensure that the driver remains active. This temporary high-side supply is provided by a bootstrap capacitor connected between the bootstrap supply terminal, C, and the high-side reference terminal, S.

The bootstrap capacitor is independently charged to approximately $V_{CC} - 1.2$ V when the associated reference S terminal is low. When the output swings high, the voltage on the bootstrap supply terminal rises with the output to provide the boosted gate voltage needed for the high-side N-channel power MOSFETs.

High-Side Gate Drive

A high-side gate-drive output for an external N-channel MOSFET is provided on the GH terminal. GH = 1 (or “high”) means that

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the upper half of the driver is turned on, and its drain will source current to the gate of the high-side MOSFET in the external load-driving bridge, turning it on. GH = 0 (or “low”) means that the lower half of the driver is turned on, and its drain will sink current from the external MOSFET’s gate circuit to the S terminal, turning it off.

The reference point for the high-side drive is the load connection, S. This terminal is also connected to the negative side of the bootstrap capacitor and is the negative supply reference connection for the floating high-side driver. The discharge current from the high-side MOSFET gate capacitance flows through this connection, which should have low-impedance traces to the MOSFET bridge.

Low-Side Gate Drive

The low-side gate drive output on GL is referenced to the GND terminal. This output is designed to drive an external N-channel power MOSFET. GL = 1 (or “high”) means that the upper half of the driver is turned on, and its drain will source current to the gate of the low-side MOSFET in the external power bridge, turning it on. GL = 0 (or “low”) means that the lower half of the driver is turned on, and its drain will sink current from the external MOSFET’s gate circuit to the GND terminal, turning it off.

Gate Drive Passive Pull-Down

Each gate drive output includes a discharge circuit to ensure that any external MOSFET connected to the gate drive output is held off when the power is removed. This discharge circuit appears as a resistor of nominally 950 kΩ between the gate drive and the source connections for each MOSFET. It is only active when the A89500 is not driving the output to ensure that any charge accumulated on the MOSFET gate has a discharge path even when the power is not connected.

Logic Control Inputs

Two logic-level digital inputs provide direct control for the gate drives, one for each drive. These logic inputs can be driven from 3.3 V or 5 V logic and all have a typical hysteresis of 300 mV to improve noise performance.

Input HS is active high and controls the high-side drive. Similarly input LS is active high and controls the low-side drive. The logical relationship between the inputs and the gate drive outputs is defined in Table 1.

Internal lockout logic ensures that the high-side output drive and low-side output drive cannot be active simultaneously When the control inputs request active high-side and low-side at the same time, then both high-side and low-side gate drives will be forced low.

Sleep Mode

RESETn is an active-low input that disables the A89500. In this state, quiescent current consumption is minimized, and the gate drive outputs are held off by the passive or active pull-downs, depending on the VCC pin connection.

Supply Undervoltage and Power-On Reset

When power is first applied to the A89500, the gate drive outputs are held in the disabled state until the voltage on the VCC pin exceeds the sum of the VCC Undervoltage threshold, V_{CCUV}, and the VCC Undervoltage Hysteresis, $V_{CCUVHys}$. At this point, the A89500 begins to operate as specified.

During operation, if the voltage on the VCC pin drops below the VCC Undervoltage threshold, V_{CCUV}, the gate drive outputs are immediately disabled.

Overtemperature

Maximum junction temperature must not exceed the limits specified in the Absolute Maximum Ratings table. The A89500 does not turn off automatically if the maximum junction temperature is exceeded and it is strongly recommended that suitable thermal management measures are incorporated at system level.

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APPLICATION INFORMATION

Dead Time Selection

The choice of power MOSFET and external series gate resistance determines the selection of the dead time. The dead time, t_{DEAD}, generated by the circuit or processor driving the logic inputs to the A89500 should be made long enough to ensure that one MOSFET has stopped conducting before the complementary MOSFET starts conducting. This should also account for the tolerance and variation of the MOSFET gate capacitance, the series gate resistance and the on-resistance of the driver in the A89500.

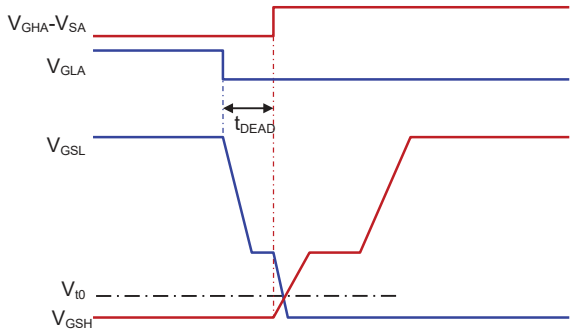

Figure 3: Minimum Dead Time

Figure 3 shows the typical switching characteristics of a pair of complementary MOSFETs. Ideally, one MOSFET should start to turn on just after the other has completely turned off. The point when a MOSFET starts to conduct is the threshold voltage, V_{t0}. The dead time should be long enough to ensure that the gate-source voltage of the MOSFET that is switching off is just below V_{t0} before the gate source voltage of the MOSFET that is switching on rises to V_{t0}. This will be the minimum theoretical dead time, but in practice the dead time will have to be longer than this to accommodate variations in MOSFET and driver parameters for process variations and over temperature.

Bootstrap Capacitor Selection

The A89500 requires a bootstrap capacitor, C. To simplify this description of the bootstrap capacitor selection criteria, generic naming is used here. So, for example, C_{BOOT}, Q_{BOOT}, and V_{BOOT} refer to the bootstrap capacitor, and Q_{GATE} refers to any of the two associated MOSFETs. C_{BOOT} must be correctly selected to ensure proper operation of the device: too large and time will be wasted charging the capacitor, resulting in a limit on the maximum duty cycle and PWM frequency; too small and there can be a large voltage drop at the time the charge is transferred from C_{BOOT} to the MOSFET gate.

To keep the voltage drop due to charge sharing small, the charge in the bootstrap capacitor, Q_{BOOT}, should be much larger than Q_{GATE}, the charge required by the gate:

$$Q_{BOOT} \gg Q_{GATE}$$

A factor of 20 is a reasonable value.

$$Q_{BOOT} = C_{BOOT} \times V_{BOOT} = Q_{GATE} \times 20$$

$$C_{BOOT} = \frac{Q_{GATE} \times 20}{V_{BOOT}}$$

where V_{BOOT} is the voltage across the bootstrap capacitor.

The voltage drop, ΔV, across the bootstrap capacitor as the MOSFET is being turned on can be approximated by:

$$\Delta V = \frac{Q_{GATE}}{C_{BOOT}}$$

So for a factor of 20, ΔV will be 5% of V_{BOOT}. C_{BOOT} must not exceed 10 µF.

Bootstrap Charging

It is necessary to ensure the high-side bootstrap capacitor is completely charged before a high-side PWM cycle is requested. The time required to charge the capacitor, t_{CHARGE}, in µs, is approximated by:

$$t_{CHARGE} = \frac{C_{BOOT} \times \Delta V}{100}$$

where C_{BOOT} is the value of the bootstrap capacitor in nF, and ΔV is the required voltage of the bootstrap capacitor.

At power up and when the drivers have been disabled for a long time, the bootstrap capacitor can be completely discharged. In this case, ΔV can be the full high-side drive voltage of approximately V_{CC} – 2 V. Otherwise, ΔV is the amount of voltage dropped during the charge transfer, which should be 400 mV or less. The capacitor is charged whenever the S terminal is pulled low and current flows from the capacitor connected to the VCC terminal through the internal bootstrap diode circuit to C_{BOOT}.

VCC Capacitor Selection

The VCC supply must provide the current for low-side gate drive circuit operation and charging the bootstrap capacitor.

When the low-side MOSFET is turned on, the gate drive circuit provides the high transient current to the gate that is necessary to turn the MOSFET on quickly. This current, which can have a peak value of several amperes, must be supplied by VCC.

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The turn-on current for the high-side MOSFET is similar in value, but is mainly supplied by the bootstrap capacitor, C_{BOOT}. However, the bootstrap capacitor must then be recharged from VCC. Unfortunately, the bootstrap recharge can occur a very short time after the low-side turn-on occurs.

To support these high transient currents, it is necessary to connect a suitable dedicated capacitor, C_{VCC}, between the VCC and GND terminals. A minimum value of 20 × C_{BOOT} is recommended, as a result of having to fully charge C_{BOOT} from a fully discharged state when switching commences.

As the maximum working voltage of C_{VCC} never exceeds V_{CC}, the capacitor voltage rating can be as low as 15 V. However, it is recommended that a capacitor rated to at least twice the maximum working voltage should be used to reduce any impact operating voltage may have on capacitance value. For best performance, C_{VCC} should be ceramic rather than electrolytic.

C_{VCC} should be mounted as close to the VCC and GND terminals as possible.

VCC Current Consumption

The average current drawn by the A89500 during operation, I_{CC}, can be estimated by summing the device quiescent current, I_{CCQ}, with the average current required to switch the connected MOSFETs. This may be expressed as:

$$I_{CC} = I_{CCQ} + (N \times f \times Q_{GATE})$$

where N is the number of MOSFETs being turned on per switching cycle (1 if the high-side MOSFET is permanently off and the low side MOSFET is switching, or 2 if both the high- and low-side MOSFETs are switching), f is the frequency at which the MOSFET(s) are being switched, and Q_{GATE} is the total gate charge specified for each connected MOSFET.

For example, if I_{CCQ} is 3 mA (per the Electrical Characteristic table), the number of MOSFETs N is equal to 2, the MOSFETs switching frequency f is 20 kHz, and the Q_{GATE} of the MOSFETs is 150 nC, then the average VCC Current Consumption I_{CC} is equal to 9 mA.

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INPUT / OUTPUT STRUCTURES

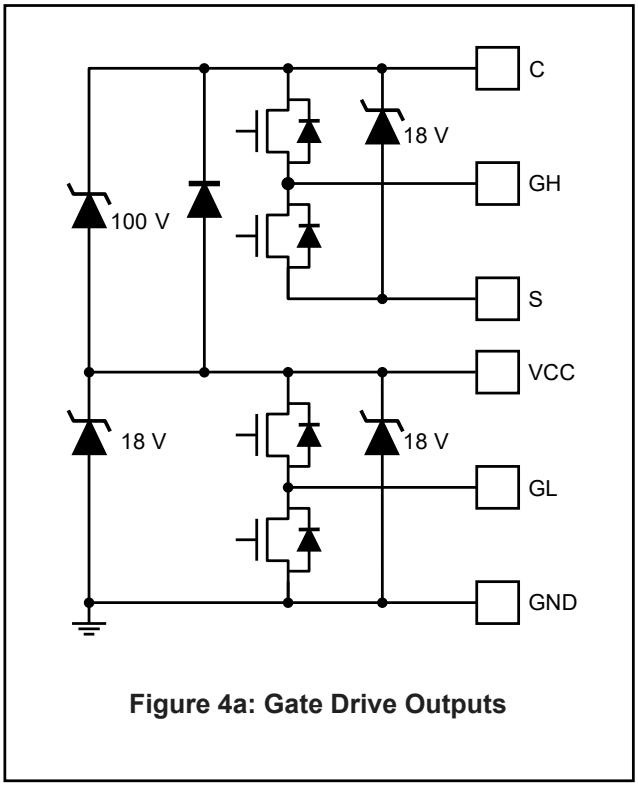

Figure 4a: Gate Drive Outputs

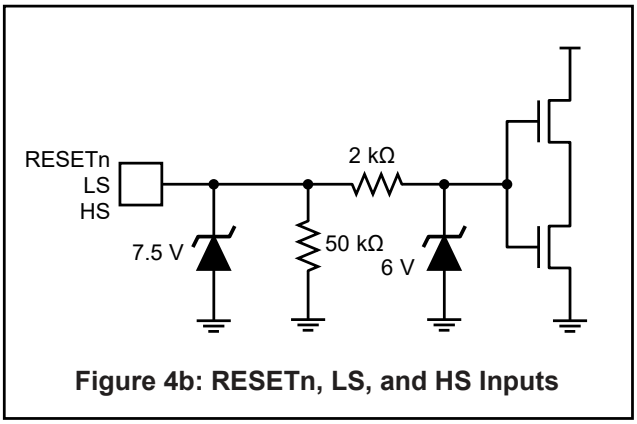

Figure 4b: RESETn, LS, and HS Inputs

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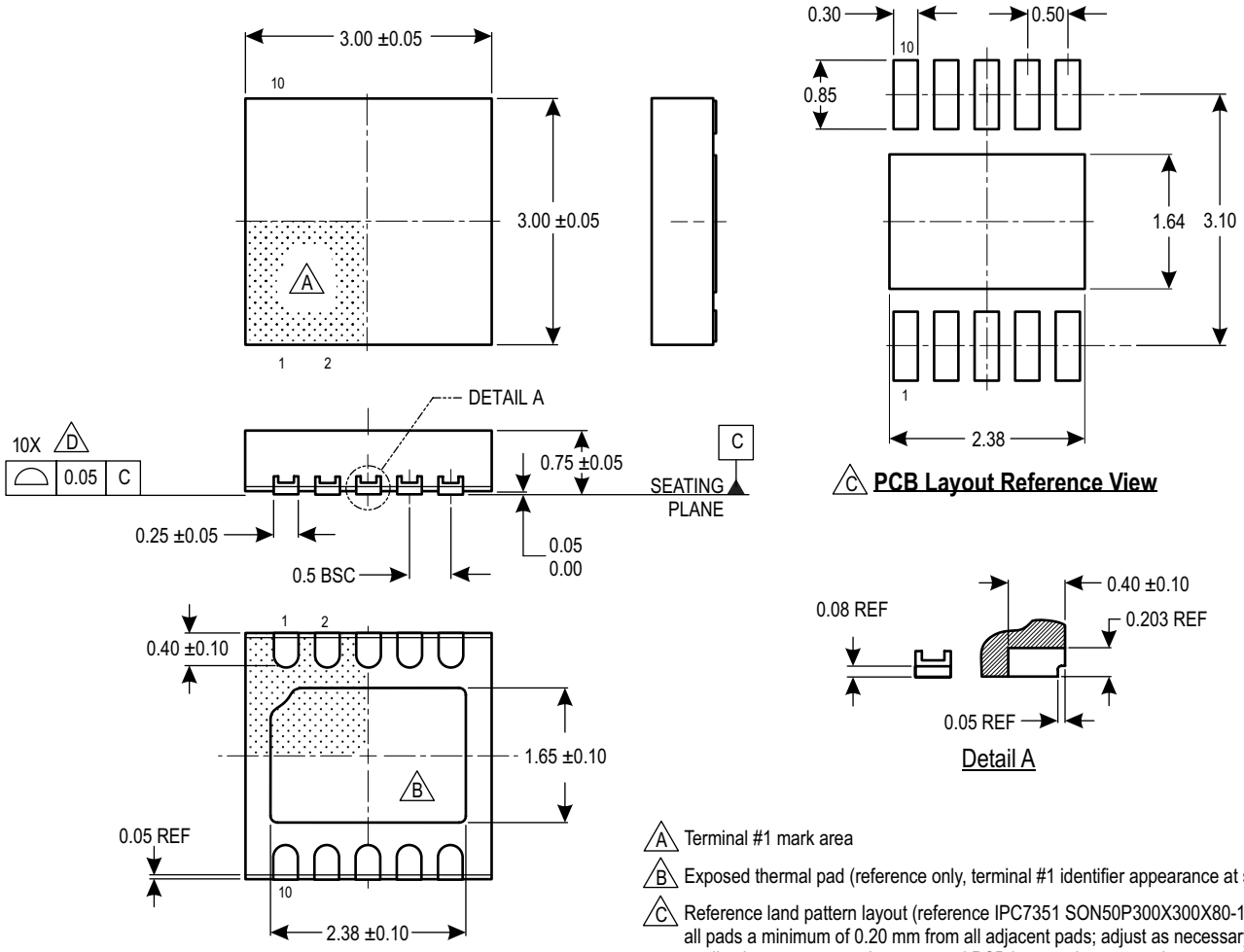
PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference JEDEC MO-229)
Dimensions in millimeters – NOT TO SCALE
Exact case and lead configuration at supplier discretion within limits shown



A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 SON50P300X300X80-11WEED3M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

Figure 5: EJ Package, 10-Lead DFN with Exposed Pad and Wettable Flank

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Revision History

Number	Date	Description
–	March 13, 2020	Initial release
1	March 23, 2020	Removed automotive version
2	June 10, 2020	Added automotive version

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