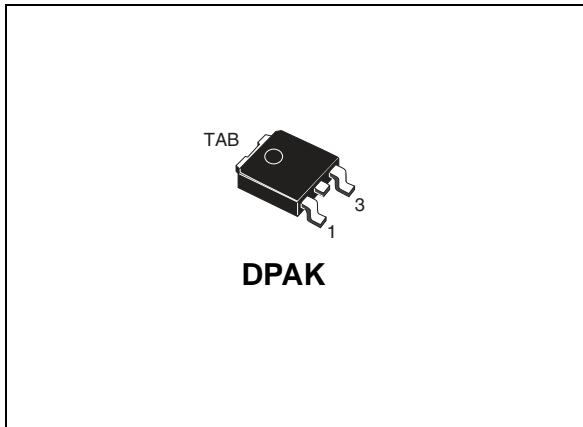


## Automotive-grade N-channel 100 V, 0.0085 $\Omega$ typ., 70 A STripFET™ F7 Power MOSFET in a DPAK package

Datasheet - production data



### Features

Order code	$V_{DS}$	$R_{DS(on)max}$	$I_D$	$P_{TOT}$
STD85N10F7AG	100 V	0.010 $\Omega$	70 A	85 W

- Designed for automotive applications and AEC-Q101 qualified
- Among the lowest  $R_{DS(on)}$  on the market
- Excellent figure of merit (FoM)
- Low  $C_{rSS}/C_{iSS}$  ratio for EMI immunity
- High avalanche ruggedness

### Applications

- Switching applications

### Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Figure 1. Internal schematic diagram

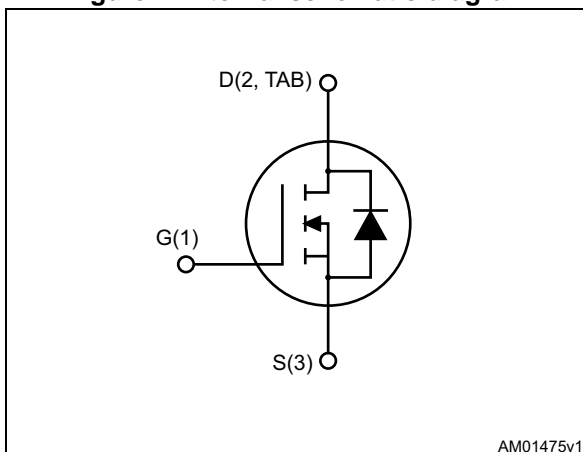


Table 1. Device summary

Order code	Marking	Package	Packing
STD85N10F7AG	85N10F7	DPAK	Tape and reel

# Contents

<b>1</b>	<b>Electrical ratings</b> .....	<b>3</b>
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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	100	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	70	A
	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	48	
$I_{DM}^{(1)}$	Drain current (pulsed)	280	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	85	W
$T_{stg}$	Storage temperature	- 55 to 175	$^\circ\text{C}$
$T_j$	Max. operating junction temperature		

1. Pulse width limited by safe operating area.

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-pcb}$	Thermal resistance junction-pcb max	50	$^\circ\text{C/W}$
$R_{thj-case}$	Thermal resistance junction-case max	1.76	

## 2 Electrical characteristics

( $T_C = 25\text{ °C}$  unless otherwise specified)

**Table 4. Static**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\ \mu\text{A}$ , $V_{GS} = 0$	100			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = 100\ \text{V}$			1	$\mu\text{A}$
		$V_{DS} = 100\ \text{V}$ , $T_C = 125\text{ °C}$			100	
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = 20\ \text{V}$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\ \mu\text{A}$	2.5	3.5	4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$I_D = 40\ \text{A}$ , $V_{GS} = 10\ \text{V}$		0.0085	0.010	$\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 50\ \text{V}$ , $f = 1\ \text{MHz}$ , $V_{GS} = 0$	-	3100	-	$\mu\text{F}$
$C_{oss}$	Output capacitance		-	700	-	
$C_{rss}$	Reverse transfer capacitance		-	45	-	
$Q_g$	Total gate charge	$V_{DD} = 50\ \text{V}$ , $I_D = 70\ \text{A}$ , $V_{GS} = 10\ \text{V}$ (see <a href="#">Figure 14</a> )	-	45	-	nC
$Q_{gs}$	Gate-source charge		-	18	-	
$Q_{gd}$	Gate-drain charge		-	13	-	

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 50\ \text{V}$ , $I_D = 40\ \text{A}$ , $R_G = 4.7\ \Omega$ , $V_{GS} = 10\ \text{V}$ (see <a href="#">Figure 15</a> and <a href="#">Figure 18</a> )	-	19	-	ns
$t_r$	Rise time		-	32	-	
$t_{d(off)}$	Turn-off delay time		-	36	-	
$t_f$	Fall time		-	13	-	

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		70	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		280	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 70\text{ A}$ , $V_{GS} = 0$	-		1.1	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 70\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$	-	70		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 80\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$ (see <a href="#">Figure 18</a> )	-	125		nC
$I_{RRM}$	Reverse recovery current		-	3.6		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

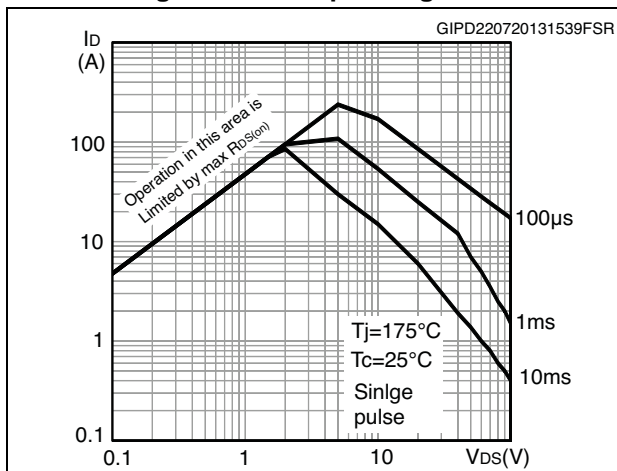


Figure 3. Thermal impedance

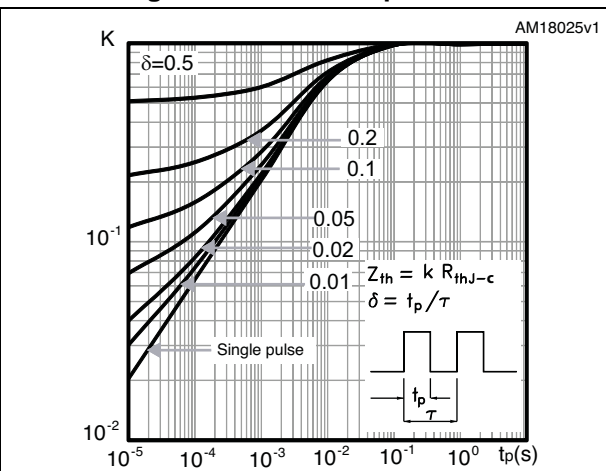


Figure 4. Output characteristics

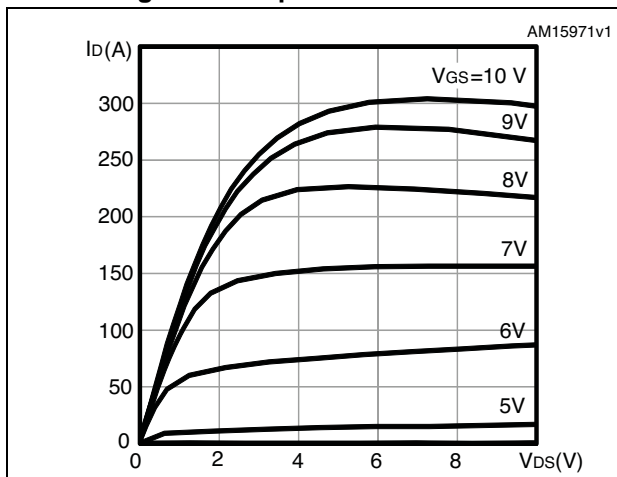


Figure 5. Transfer characteristics

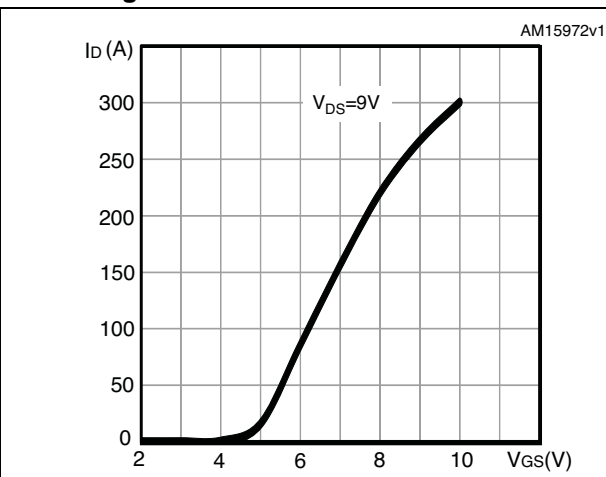


Figure 6. Static drain-source on-resistance

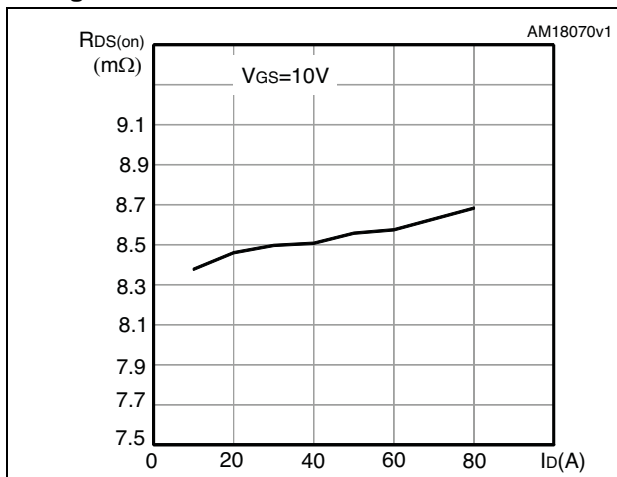


Figure 7. Gate charge vs gate-source voltage

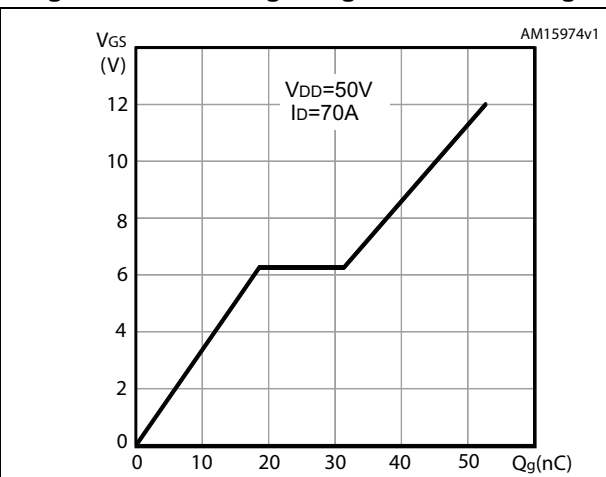


Figure 8. Capacitance variations

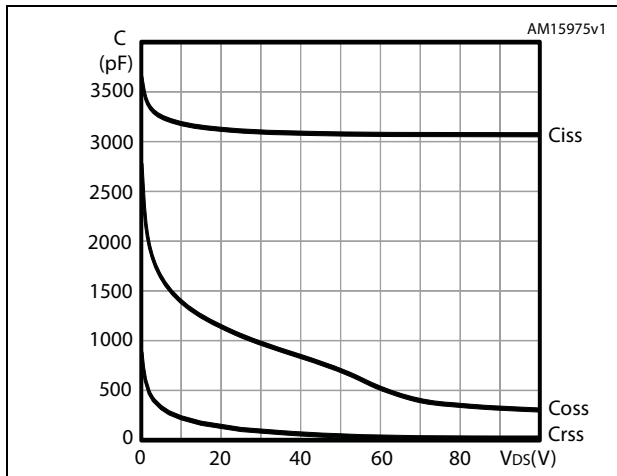


Figure 9. Normalized gate threshold voltage vs temperature

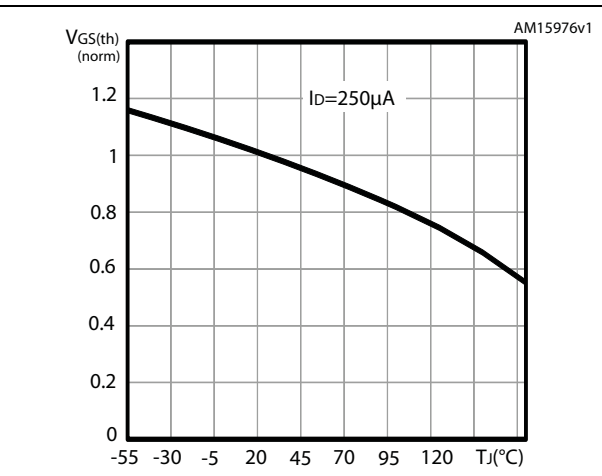


Figure 10. Normalized on-resistance vs temperature

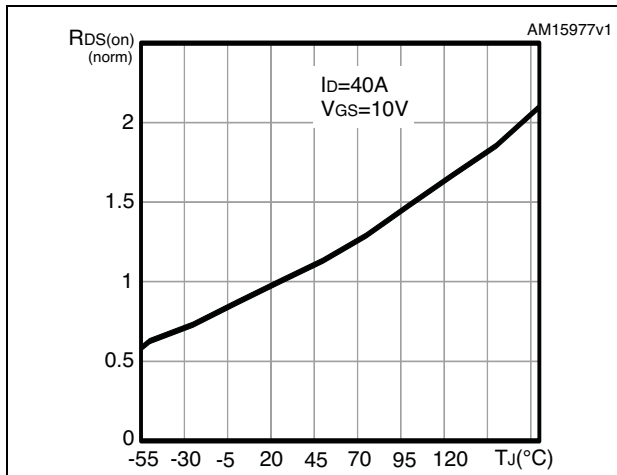


Figure 11. Source-drain diode forward characteristics

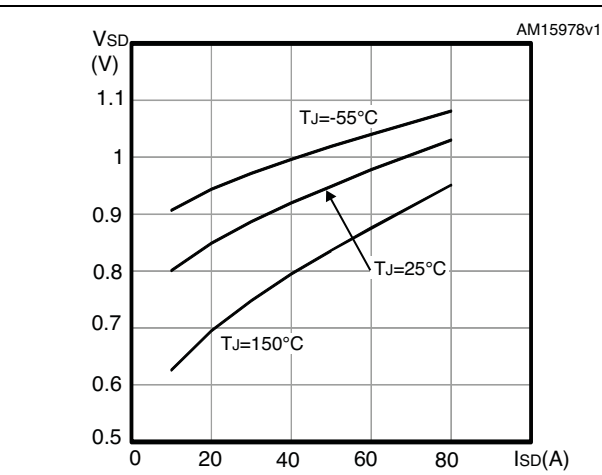
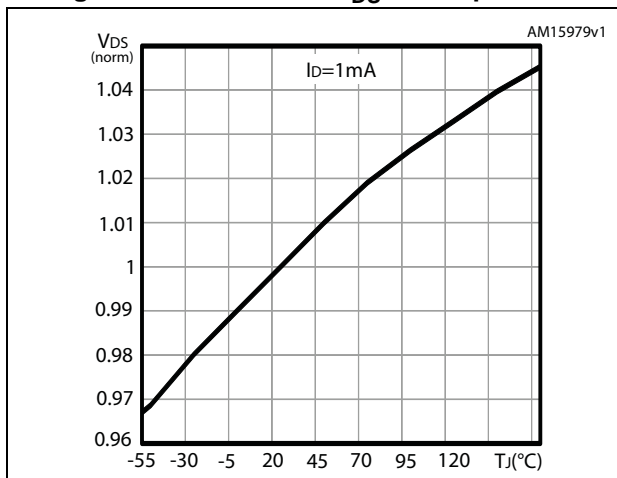


Figure 12. Normalized VDS vs temperature



### 3 Test circuits

Figure 13. Switching times test circuit for resistive load

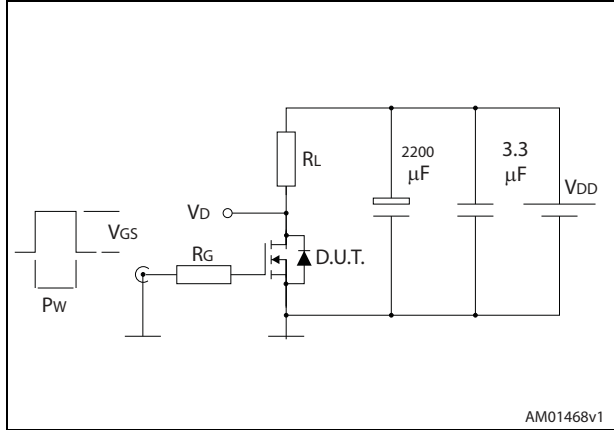


Figure 14. Gate charge test circuit

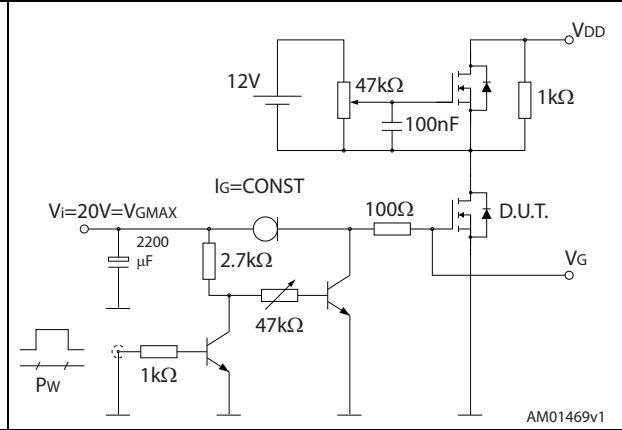


Figure 15. Test circuit for inductive load switching and diode recovery times

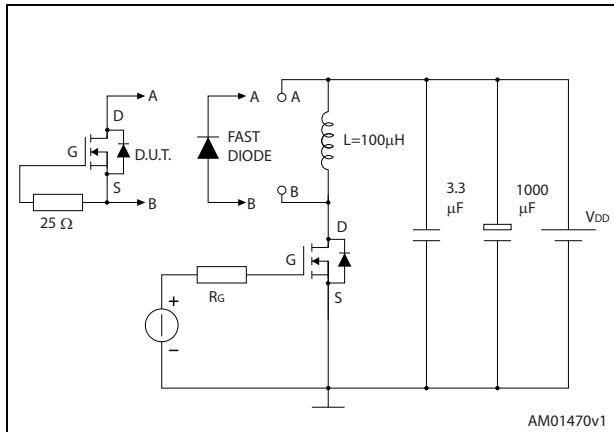


Figure 16. Unclamped inductive load test circuit

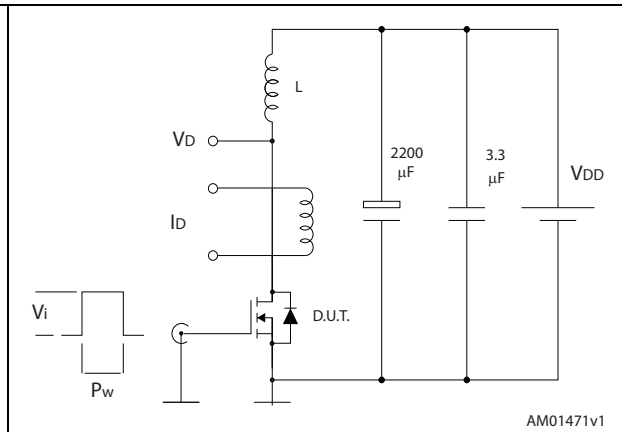


Figure 17. Unclamped inductive waveform

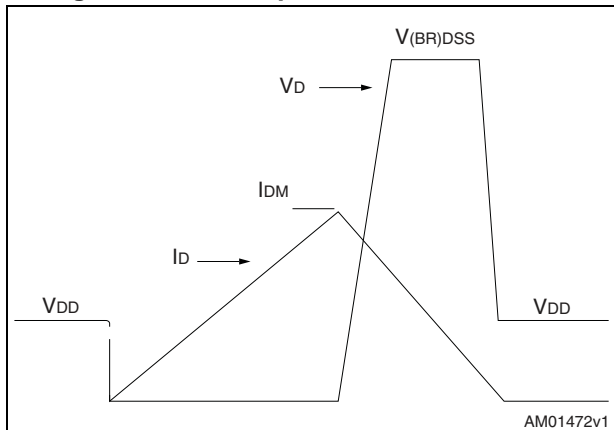
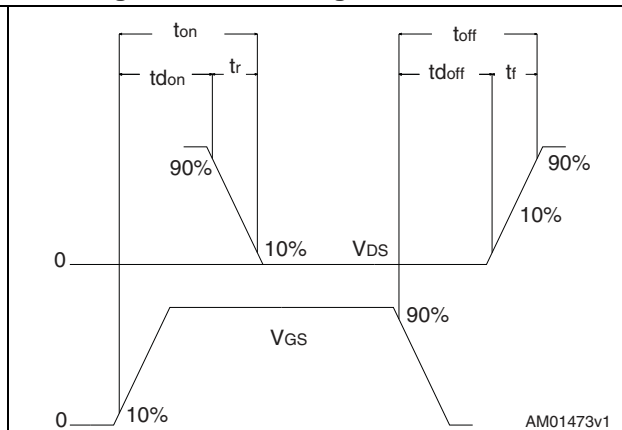


Figure 18. Switching time waveform





## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

### 4.1 DPAK (TO-252) type A2 package information

Figure 19. DPAK (TO-252) type A2 package outline

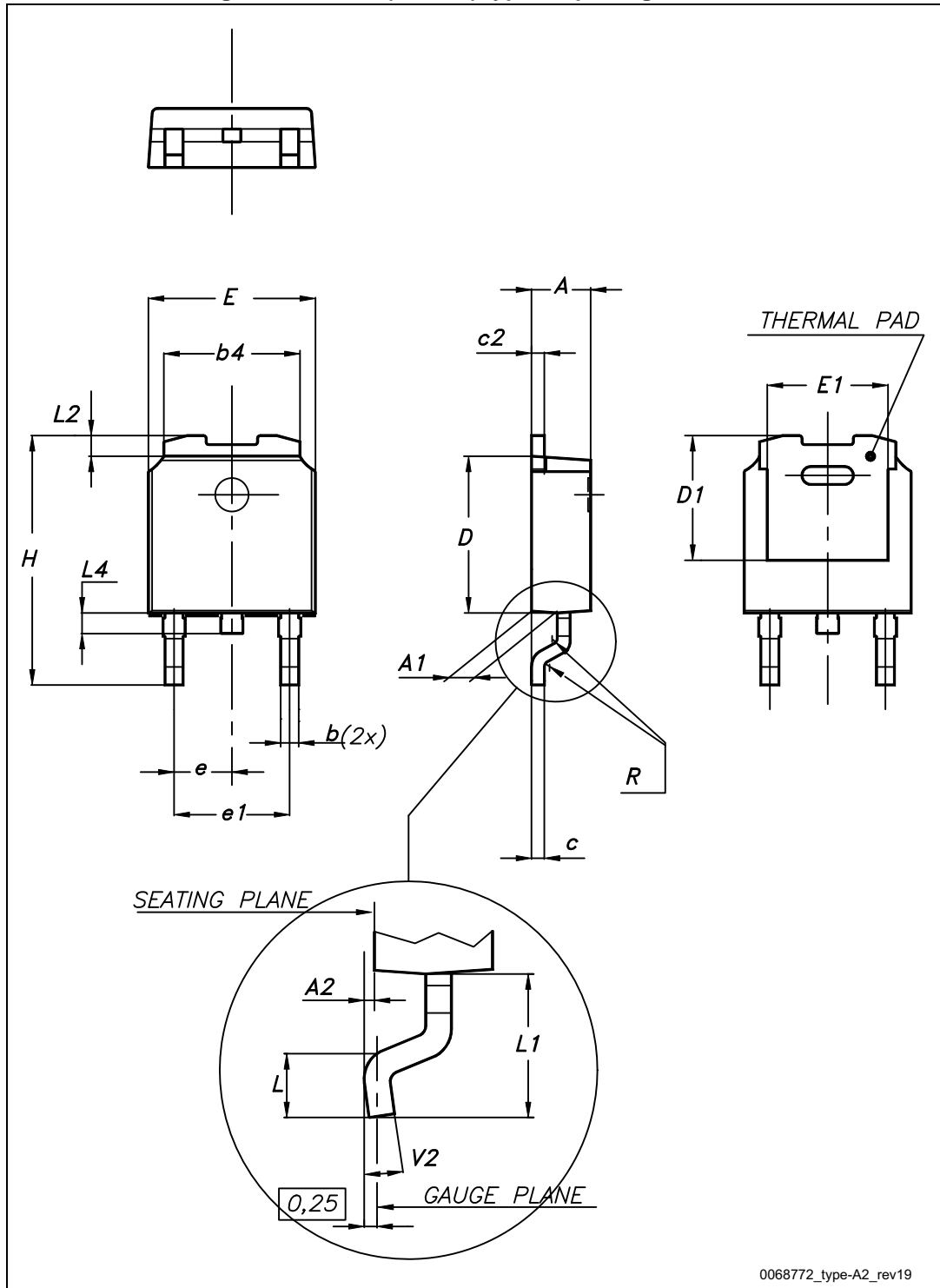
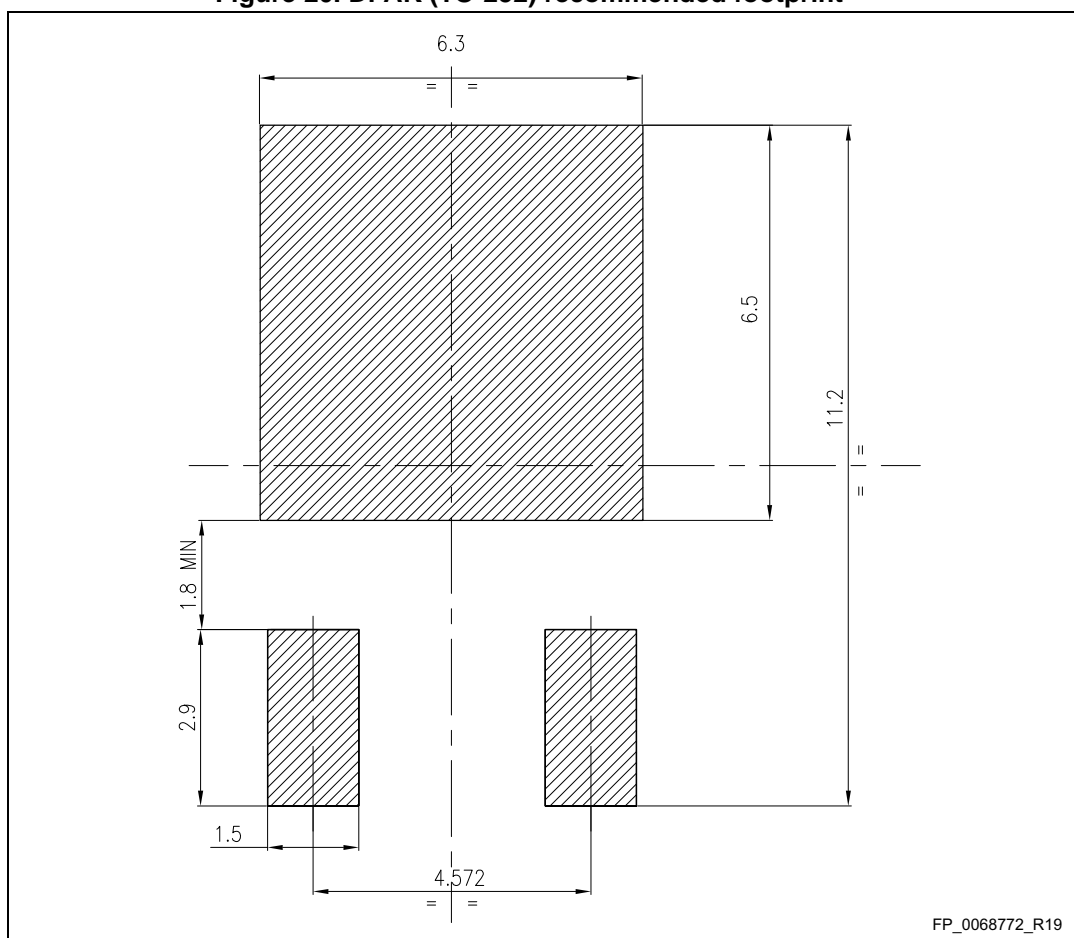


Table 8. DPAK (TO-252) type A2 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	5.10	5.20	5.30
e	2.16	2.28	2.40
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
L1	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 20. DPAK (TO-252) recommended footprint (a)



a. All dimensions are in millimeters

## 4.2 Packing information

Figure 21. Tape outline

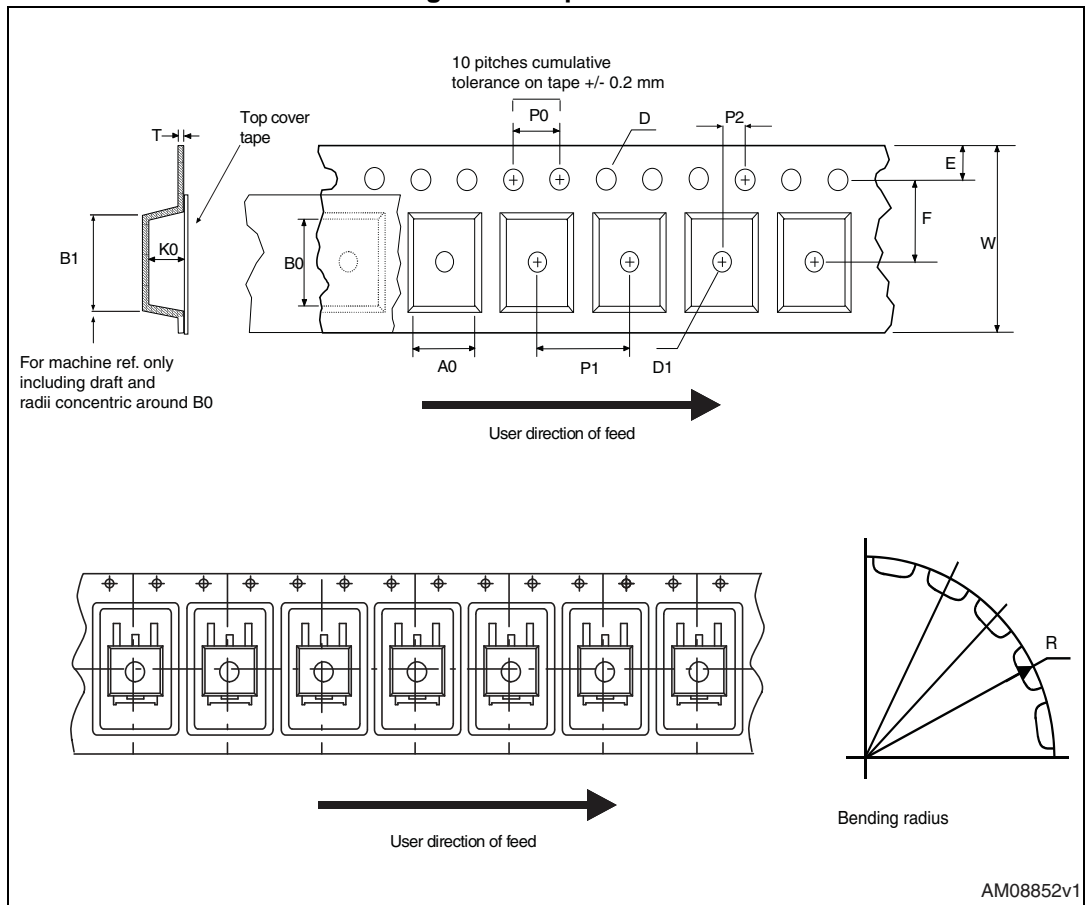


Figure 22. Reel outline

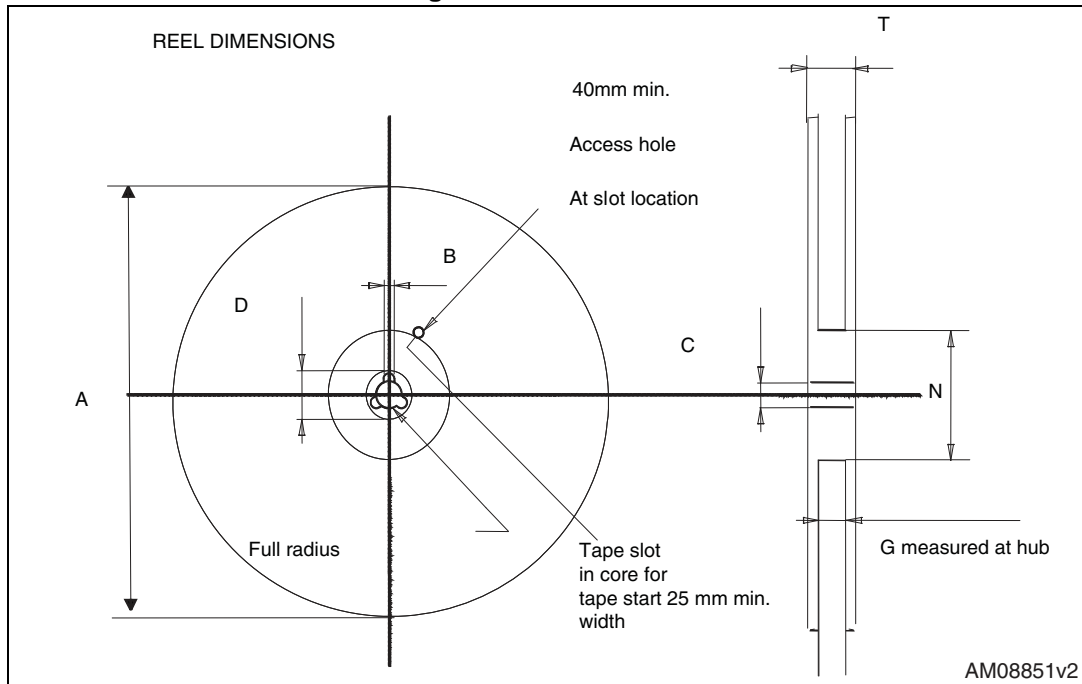


Table 9. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

## 5 Revision history

**Table 10. Document revision history**

Date	Revision	Changes
21-Oct-2014	1	First release.
26-May-2015	2	Text and formatting edits throughout document. Promoted document from "preliminary data" to "production data" Updated device package information.

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