TPS40200-Q1 Wide-Input-Range Nonsynchronous Voltage-Mode Controller

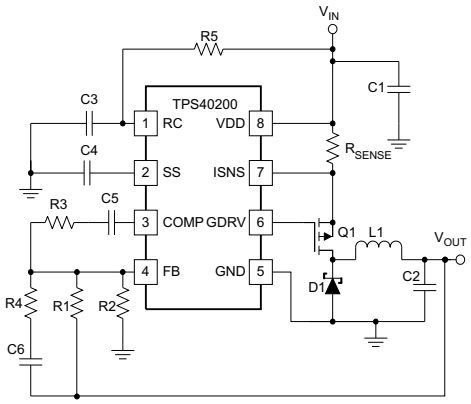
1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to 125°C
  - Device HBM ESD Classification Level 1B
  - Device CDM ESD Classification Level C6
- Input Voltage Range 4.5 V to 52 V
- Output Voltage (700 mV to 90% V_{IN})
- 200-mA Internal P-channel FET Driver
- Voltage Feed-Forward Compensation
- Undervoltage Lockout (UVLO)
- Programmable Fixed-Frequency (35-kHz to 500-kHz) Operation
- Programmable Short-Circuit Protection
- Hiccup Overcurrent Fault Recovery
- Programmable Closed-Loop Soft Start
- 700-mV 1% Reference Voltage
- External Synchronization
- Small 8-Pin SOIC (D) Package

2 Applications

- Automotive Controls
- Automotive Power Supplies
- Distributed Power Systems

Typical Application



3 Description

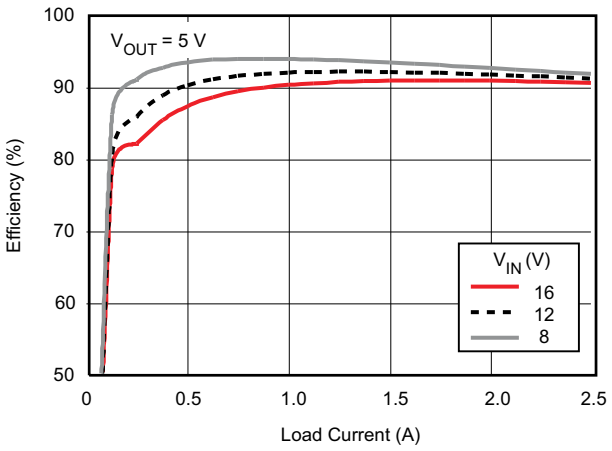
The TPS40200-Q1 is a flexible, nonsynchronous controller with a built-in 200-mA driver for P-channel FETs. The circuit operates with inputs up to 52 V, with a power-saving feature that turns off driver current once the external FET has been turned on fully. This feature extends the flexibility of the device, allowing it to operate with an input voltage up to 52 V without dissipating excessive power. The circuit operates with voltage-mode feedback and has feed-forward input-voltage compensation that responds instantly to input voltage change. The integral 700-mV reference is trimmed to 2%, providing the means to accurately control low voltages. The TPS40200-Q1 is available in an 8-pin SOIC package and supports many of the features of more complex controllers. Clock frequency, soft start, and overcurrent limit are each easily programmed by a single, external component. The device has undervoltage lockout (UVLO) and can be easily synchronized to other controllers or a system clock to satisfy sequencing and/or noise-reduction requirements.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS40200-Q1	SOIC (8)	3.91 mm × 4.90 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Efficiency of Application Circuit



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (July 2013) to Revision F **Page**

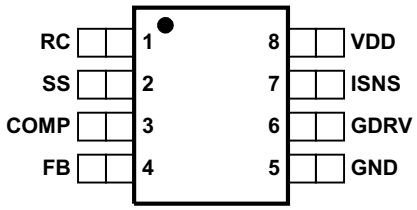
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Changed V_{IN} to V_{DD} throughout the document for consistency ... 3
- Added footnote for reference to *Minimum Controllable Pulse Width vs Frequency* section ... 5
- Changed TPS40200 to TPS40200-Q1 throughout document ... 10
- Added note for typical values of internal resistor and voltages ... 10
- Changed voltage to 8 V (typical) in *MOSFET Gate Drive* ... 11
- Changed *Programming the Operating Frequency* to *Selecting the Operating Frequency* ... 11
- Changed equation 4 ... 15
- Changed *Programming the Soft-Start Time* to *Calculating the Soft-Start Time* ... 16
- Changed equation 5 ... 16
- Deleted *Bill of Materials* tables ... 20
- Added designators Q2 and D2 to *Detailed Design Procedure* ... 21
- Added designator L1 to *Detailed Design Procedure* ... 23
- Added clarification for different values for capacitor C11 and C12 in schematic, which are for the EVM. Modified for use in applications per equations ... 23
- Changed R_{RC} to R3 in equation definition in *Switching Frequency* for consistency and clarity ... 24
- Changed R_{ILM} to 31 mΩ in *Calculating the Overcurrent Threshold Level* and added clarifiying information ... 24
- Added capacitor designator C6 in *Soft-Start Capacitor* ... 25

Changes from Revision D (July 2011) to Revision E **Page**

- Deleted T_A test condition and values from Feedback voltage parameter in *Electrical Characteristics* ... 5

5 Pin Configuration and Functions

D Package
8-Pin SOIC
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	RC	I	Switching frequency setting RC network. Connect a capacitor from RC pin to GND pin and a resistor from V_{IN} pin to RC pin. The device may be synchronized to an external clock by connecting an open-drain output to this pin and pulling it to GND. The pulse width for synchronization should not be excessive (see *Detailed Description*).
2	SS	I	Soft-start programming. Connect capacitor from SS to GND to program soft-start time. Pulling this pin below 150 mV causes the output switching to stop, placing the device in a shutdown state. The pin also functions as a restart timer for overcurrent events.
3	COMP	O	Error amplifier output. Connect control loop compensation network from COMP to FB.
4	FB	I	Error amplifier inverting input. Connect feedback resistor network center tap to this pin.
5	GND	—	Device ground
6	GDRV	O	Driver output for external P-channel MOSFET
7	ISNS	I	Current-sense comparator input. Connect a current sense resistor between ISNS and V_{DD} in order to set desired overcurrent threshold.
8	VDD	I	System input voltage. Connect local bypass capacitor from V_{DD} to GND.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input voltage	V_{DD}, ISNS	–0.3	52	V
	RC, FB	–0.3	5.5	
	SS	–0.3	9	
Output voltage	COMP	–0.3	9	V
	GDRV	V_{DD} – 10	V_{DD}	
Lead temperature 1,6 mm (1/16 in) from case for 10 s			260	°C
T_{stg} Storage temperature		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 (1)	±1000	V
		Charged-device model (CDM), per AEC Q100-011	±1500	
		Machine model (MM)	±100	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{DD}	Input voltage	4.5	52	V
T_A	Operating temperature	–40	125	°C

6.4 Thermal Information

over operating free-air temperature range (unless otherwise noted)

THERMAL METRIC(1)		TPS40200-Q1 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	115.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	64.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	56	°C/W
ψ_{JT}	Junction-to-top characterization parameter	17.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	55.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

–40°C < T_A < 125°C, V_{DD} = 12 V, f_{OSC} = 100 kHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOLTAGE REFERENCE						
V_{FB}	Feedback voltage	COMP = FB , 4.5 V < V_{DD} < 52 V, –40°C < T_A < 125°C	676	696	712	mV
GATE DRIVER						
I_{src}	Gate driver pullup current		125	300		mA
I_{snk}	Gate driver pulldown current		200	300		mA
V_{GATE}	Gate driver output voltage	V_{GATE} = (V_{DD} – V_{GDRV}), 12 V < V_{DD} < 52 V	5.6	8	10	V
QUIESCENT CURRENT						
I_{qq}	Device quiescent current	f_{OSC} = 300 kHz, Driver not switching, 4.5 V < V_{DD} < 52 V		1.5	3	mA
UNDERVOLTAGE LOCKOUT (UVLO)						
$V_{UVLO(on)}$	Turn-on threshold	–40°C < T_A < 125°C	3.8	4.25	4.55	V
$V_{UVLO(off)}$	Turn-off threshold			4.05		V
$V_{UVLO(HYST)}$	Hysteresis		110	200	275	mV
SOFT START						
$R_{SS(chg)}$	Internal soft-start pullup resistance		65	105	170	kΩ
$R_{SS(dchg)}$	Internal soft-start pulldown resistance		190	305	485	kΩ
V_{SSRST}	Soft-start reset threshold		100	150	200	mV
OVERCURRENT PROTECTION						
V_{ILIM}	Overcurrent threshold	4.5 V < V_{DD} < 52 V, –40°C < T_A < 125°C	50	100	140	mV
OC_{DF}	Overcurrent duty cycle (1)				2%	
$V_{ILIM(rst)}$	Overcurrent reset threshold		100	150	200	mV
OSCILLATOR						
f_{OSC}	Oscillator frequency range (1)		35		500	kHz
	Oscillator frequency	R_{RC} = 200 kΩ, C_{RC} = 470 pF	85	100	118	kHz
		R_{RC} = 68.1 kΩ, C_{RC} = 470 pF	210	300	345	
	Frequency line regulation	12 V < V_{DD} < 52 V	–9%		0%	
		4.5 V < V_{DD} < 12 V	–21%		0%	
V_{RMP}	Ramp amplitude	4.5 V < V_{DD} < 52 V		V_{DD} / 10		V
PULSE-WIDTH MODULATOR						
t_{MIN}	Minimum controllable pulse width (2)	V_{DD} = 12 V		200	540	ns
		V_{DD} = 30 V		100	200	
D_{MAX}	Maximum duty cycle	F_{osc} = 100 kHz, C_L = 470 pF	93%	95%		
		F_{osc} = 300 kHz, C_L = 470 pF	90%	93%		
K_{PWM}	Modulator and power-stage DC gain		8	10	12	V/V
ERROR AMPLIFIER						
I_{IB}	Input bias current			100	250	nA
AOL	Open loop gain (1)		60	80		dB
GBWP	Unity gain bandwidth (1)		1.5	3		MHz
$I_{COMP(src)}$	Output source current	V_{FB} = 0.6 V, COMP = 1 V	100	250		µA
$I_{COMP(snk)}$	Output sink current	V_{FB} = 1.2 V, COMP = 1 V	1	2.5		mA

(1) Specified by design
(2) See Figure 21 for typical t_{MIN} vs f_{OSC} at various input voltages.

6.6 Typical Characteristics

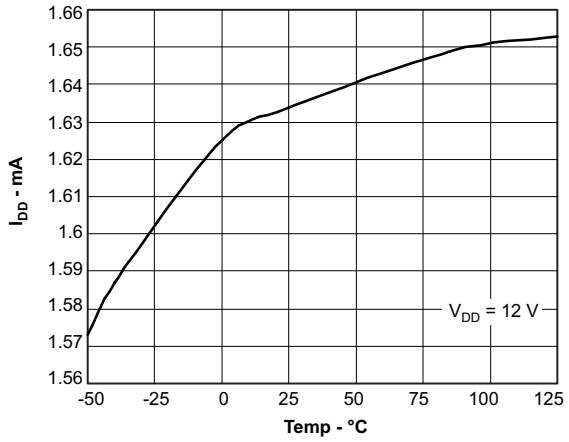


Figure 1. Quiescent Current vs Temperature

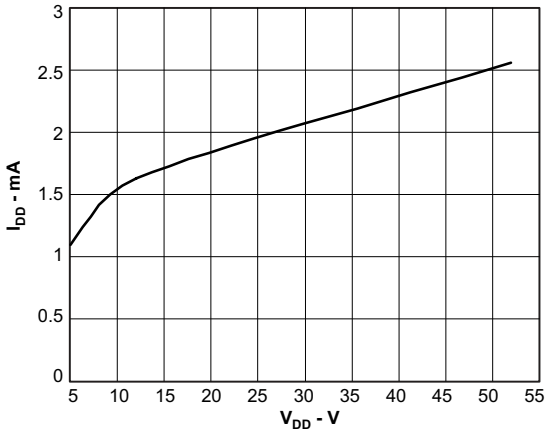


Figure 2. Quiescent Current vs V_{DD}

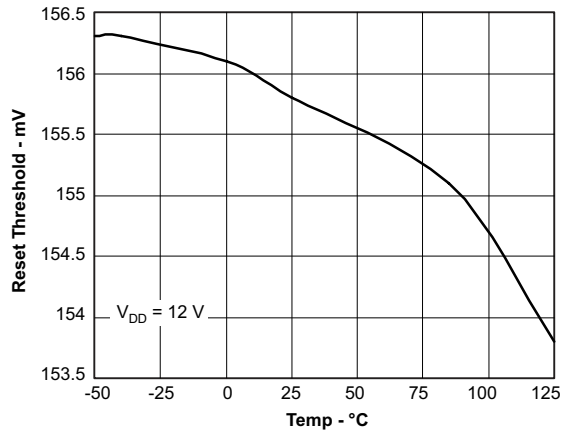


Figure 3. Soft-Start Threshold vs Temperature

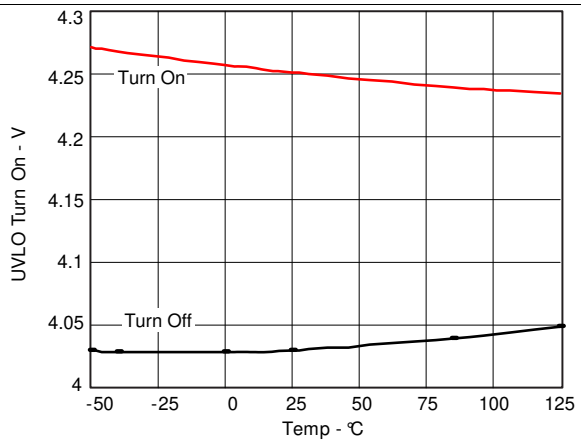


Figure 4. UVLO Turn On and Turn Off vs Temperature

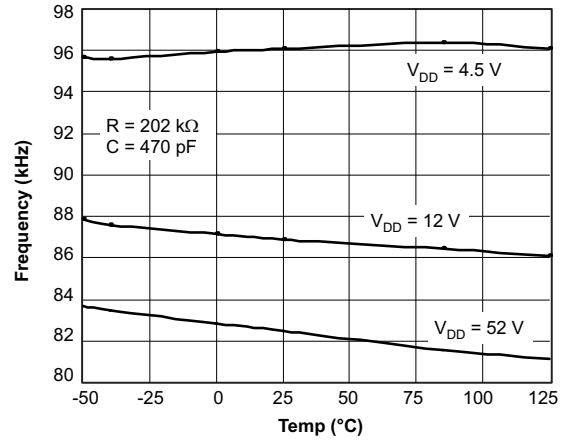


Figure 5. Oscillator Frequency vs Temperature

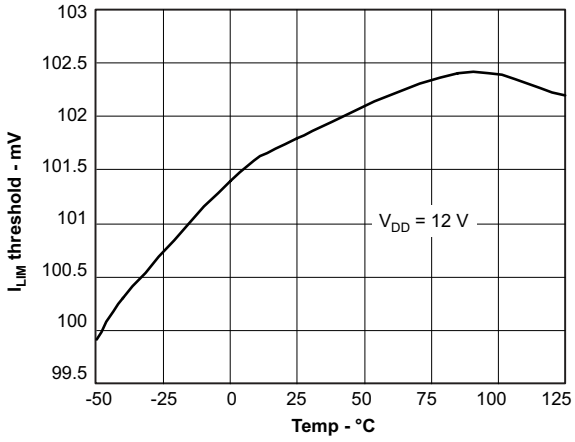


Figure 6. Current-Limit Threshold vs Temperature

Typical Characteristics (continued)

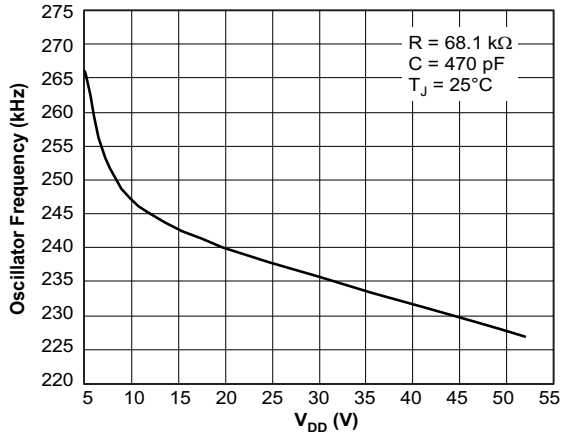


Figure 7. Oscillator Frequency vs V_{DD}

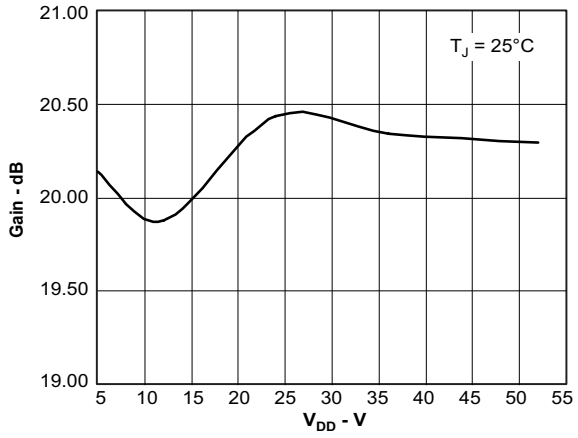


Figure 8. Power-Stage Gain vs V_{DD}

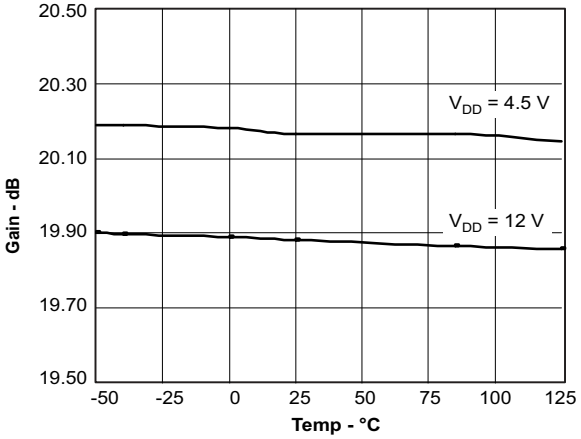


Figure 9. Power-Stage Gain vs Temperature

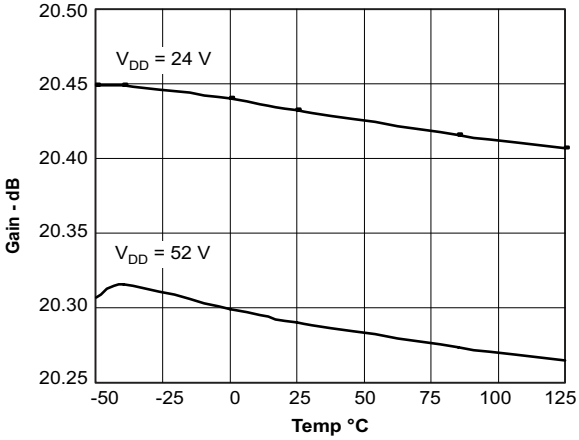


Figure 10. Power-Stage Gain vs Temperature

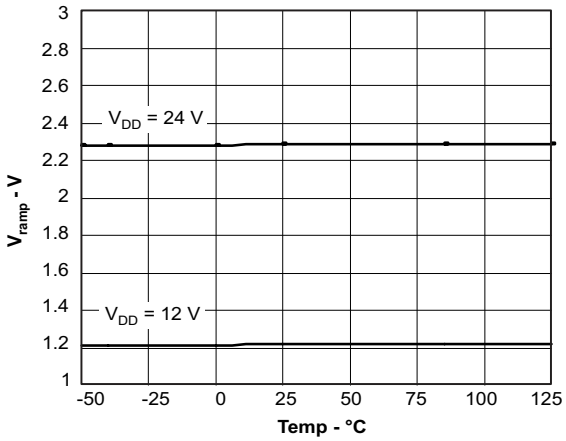


Figure 11. Modulator Ramp Amplitude vs Temperature

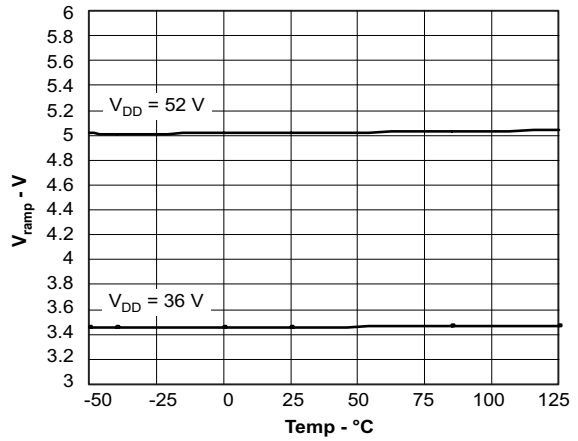


Figure 12. Modulator Ramp Amplitude vs Temperature

Typical Characteristics (continued)

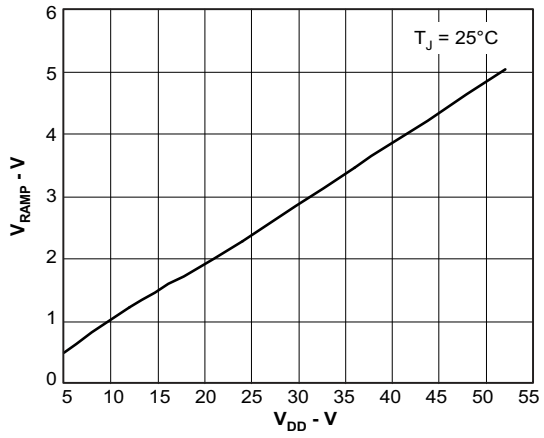


Figure 13. Modulator Ramp Amplitude vs V_{DD}

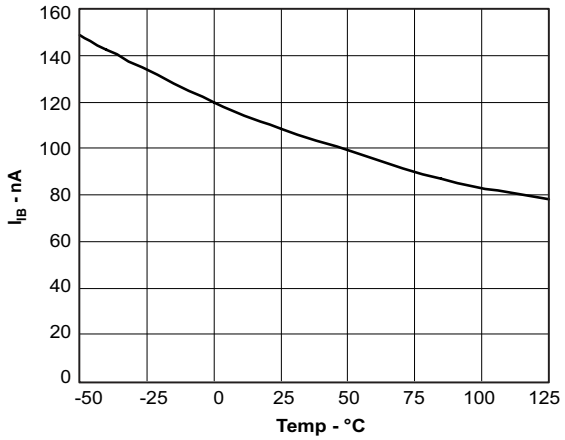


Figure 14. Feedback Amplifier Input Bias Current vs Temperature

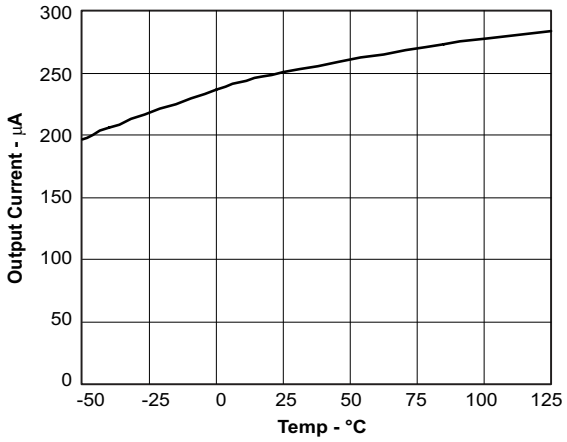


Figure 15. Comp Source Current vs Temperature

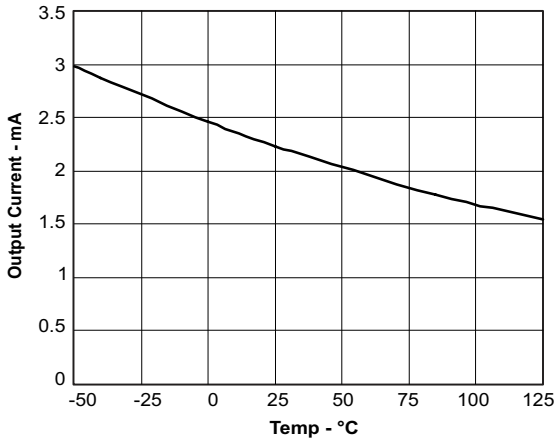


Figure 16. Comp Sink Current vs Temperature

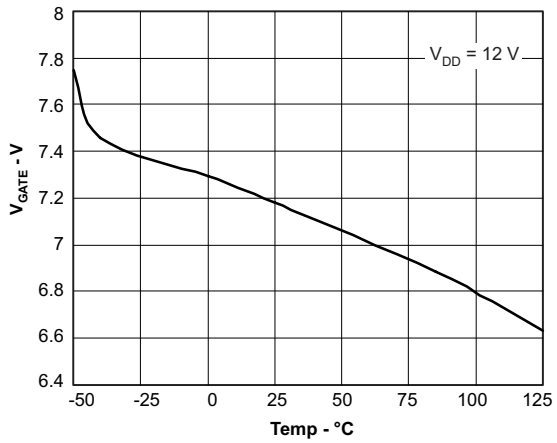


Figure 17. Gate Drive Voltage vs Temperature

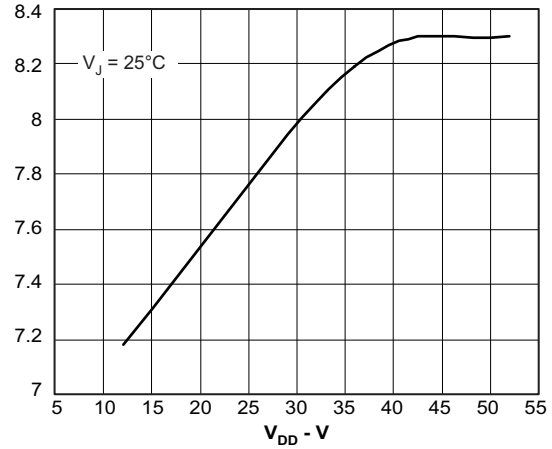


Figure 18. Gate Drive Voltage vs V_{IN}

Typical Characteristics (continued)

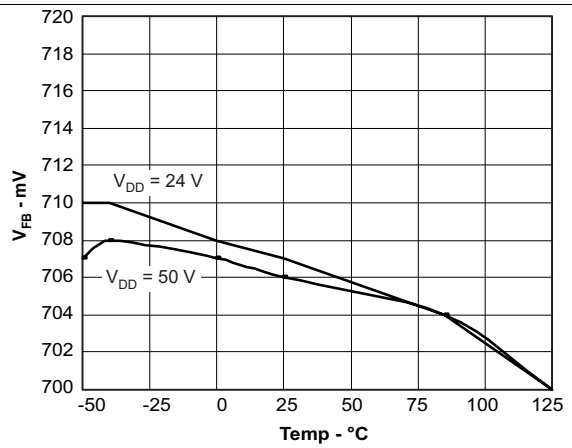


Figure 19. Reference Voltage vs Temperature

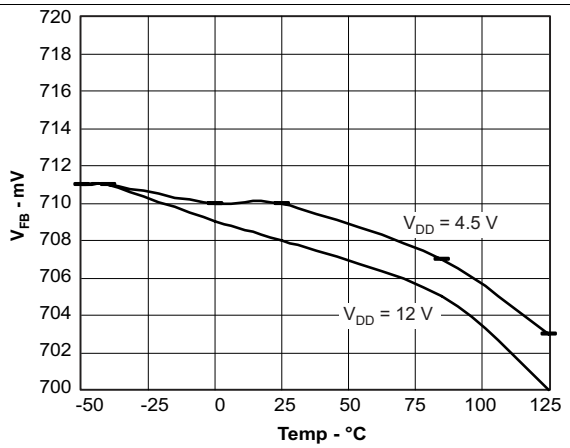


Figure 20. Reference Voltage vs Temperature

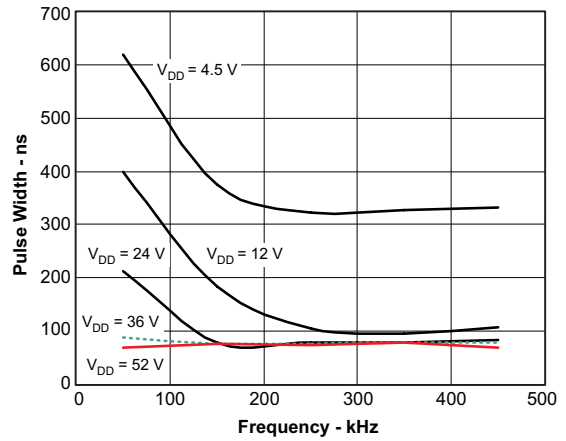


Figure 21. Minimum Controllable Pulse Width vs Frequency

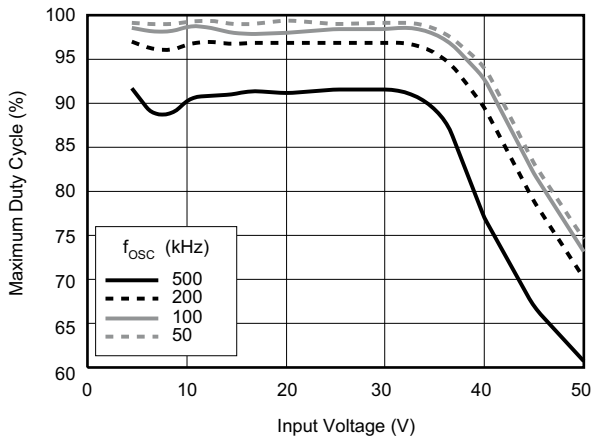


Figure 22. Maximum Duty Cycle vs Input Voltage

7 Detailed Description

7.1 Overview

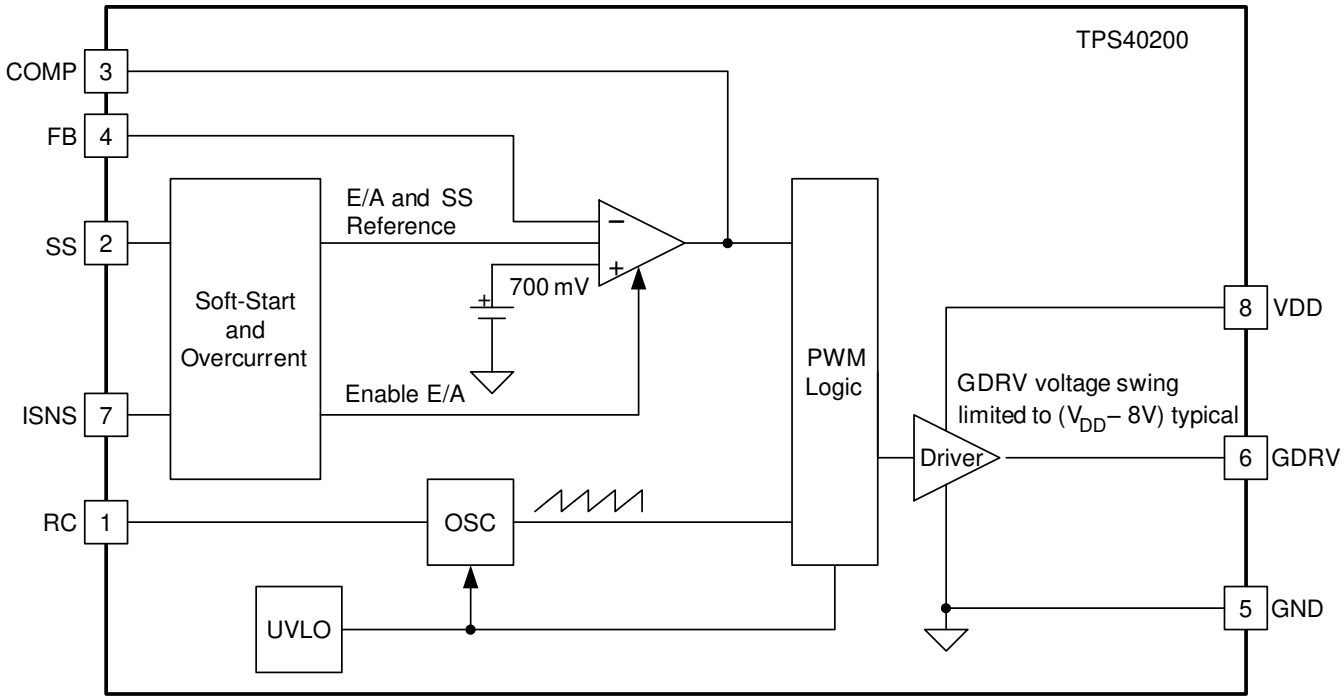
The TPS40200-Q1 is a nonsynchronous controller with a built-in 200-mA driver designed to drive high-speed P-channel FETs up to 500 kHz. Its small size combined with complete functionality makes the device both versatile and easy to use.

The controller uses a low-value current-sensing resistor in series with the input voltage and the source connection of the power FET to detect switching current. When the voltage drop across this resistor exceeds 100 mV, the device enters a hiccup fault mode at approximately 2% of the operating frequency.

The device uses voltage feedback to an error amplifier that is biased by a precision 700-mV reference. Feed-forward compensation from the input keeps the PWM gain constant over the full input voltage range, eliminating the need to change frequency compensation for different input voltages.

The device also incorporates a soft-start feature, where the output follows a slowly rising soft-start voltage, preventing output-voltage overshoot.

7.2 Functional Block Diagram



NOTE

In this block diagram and the following sections, the internal R resistor values and capacitor mV reference values are typical. Resistor and reference voltage values will vary based on process, temperature, and supply voltage of the device. Please see *Electrical Characteristics* for tolerances, where applicable.

7.3 Feature Description

7.3.1 MOSFET Gate Drive

The output-driver sinking current is approximately 200 mA and is designed to drive P-channel power FETs. When the driver pulls the gate charge of the FET, it is controlling to 8 V (typical), the drive current folds back to a low level so that high-power dissipation only occurs during the turn-on period of the FET. This feature is particularly valuable when turning on a FET at high input voltages, where leaving the gate drive current on would otherwise cause unacceptable power dissipation.

7.3.2 Undervoltage Lockout Protection

Undervoltage lockout (UVLO) protection ensures proper start-up of the device only when the input voltage has exceeded minimum operating voltage. UVLO protection incorporates hysteresis that eliminates hiccup starting in cases where input supply impedance is high.

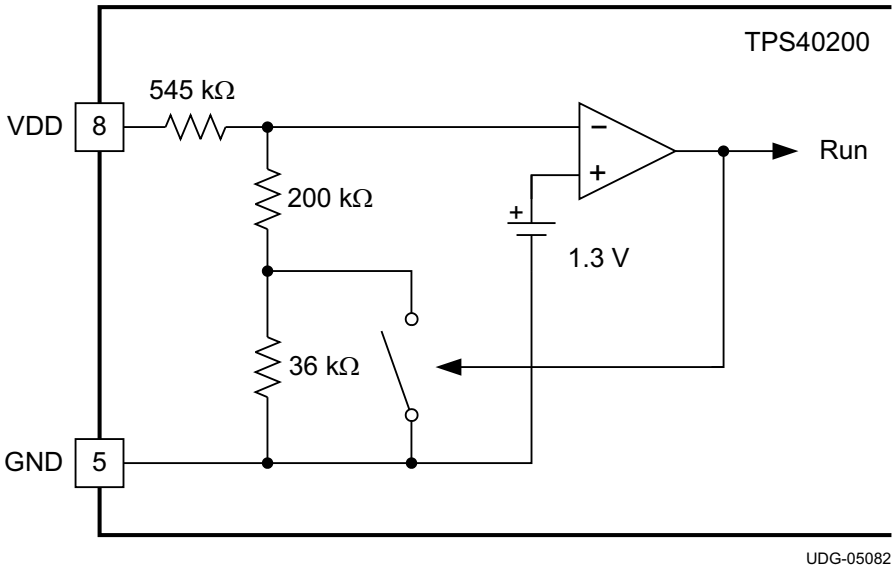


Figure 23. Undervoltage Lockout

Undervoltage protection ensures proper startup of the device only when the input voltage has exceeded minimum operating voltage. The UVLO level is measured at the V_{DD} pin with respect to GND. Start-up voltage is typically 4.3 V with approximately 200 mV of hysteresis. The device shuts off at a nominal 4.1 V. As shown in Figure 23, when the input V_{DD} voltage rises to 4.3 V, the 1.3-V comparator threshold voltage is exceeded a d a RUN signal occurs. Feedback from the output closes the switch and shunts the 200-kΩ resistor, so that an approximately 200-mV lower voltage, or 4.1 V, is required before the device shuts down.

7.3.3 Selecting the Operating Frequency

The operating frequency of the controller is determined by an external resistor R_{RC} that is connected from the RC pin to VDD and a capacitor attached from the RC pin to ground. This connection and the two oscillator comparators inside the device are shown in Figure 24. The oscillator frequency can be calculated using Equation 1.

$$f_{SW} = \frac{1}{R_{RC} \times C_{RC} \times 0.105} \quad (1)$$

where

- f_{SW} = clock frequency
- R_{RC} = timing resistor value in Ω
- C_{RC} = timing capacitor value in F

Feature Description (continued)

R_{RC} must be kept large enough that the current through it does not exceed 750 µA when the internal switch (shown in Figure 24) is discharging the timing capacitor. This condition may be expressed using Equation 2.

$$\frac{V_{IN}}{R_{RC}} \leq 750\ \mu A \tag{2}$$

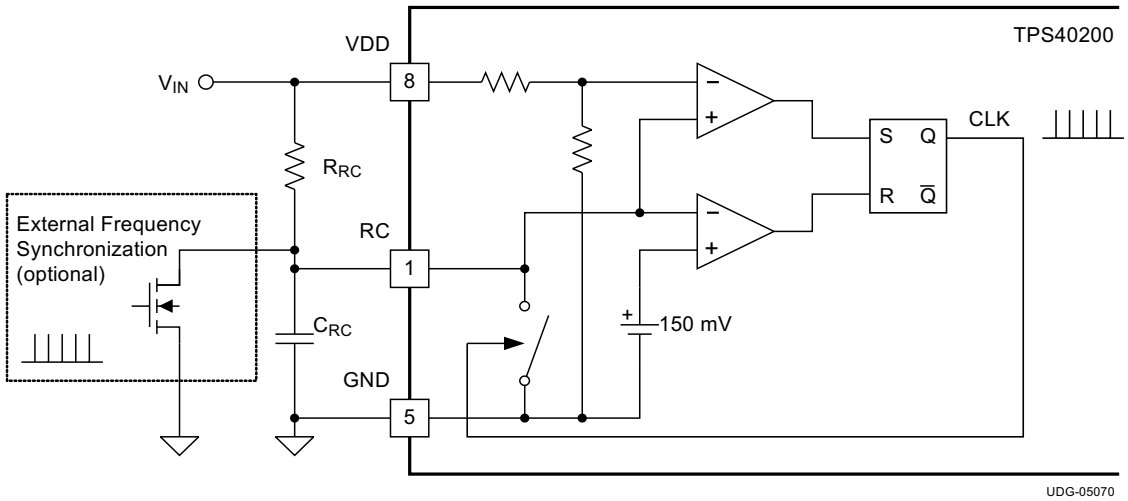


Figure 24. Oscillator Functional Diagram

7.3.4 Synchronizing the Oscillator

Figure 24 shows the functional diagram of the TPS40200-Q1 oscillator. When synchronizing the oscillator to an external clock, the RC pin must be pulled below 150 mV for 20 ns or more. The external clock frequency must also be higher than the free-running frequency of the converter. When synchronizing the controller, if the RC pin is held low for an excessive amount of time, erratic operation may occur. The maximum amount of time that the RC pin should be held low is the lesser of the following:

- 50% of a nominal output pulse, or
- 10% of the period of the synchronization frequency

Under circumstances where the input voltage is high and the duty cycle is less than 50%, a Schottky diode connected from the RC pin to an external clock may be used to synchronize the oscillator (see Figure 25). The cathode of the diode is connected to the RC pin. The trip point of the oscillator is set by an internal voltage divider to be 1/10 of the input voltage. The clock signal must have an amplitude higher than this trip point. When the clock goes low, it allows the reset current to restart the RC ramp , synchronizing the oscillator to the external clock. This provides a simple, single-component method for clock synchronization.

Feature Description (continued)

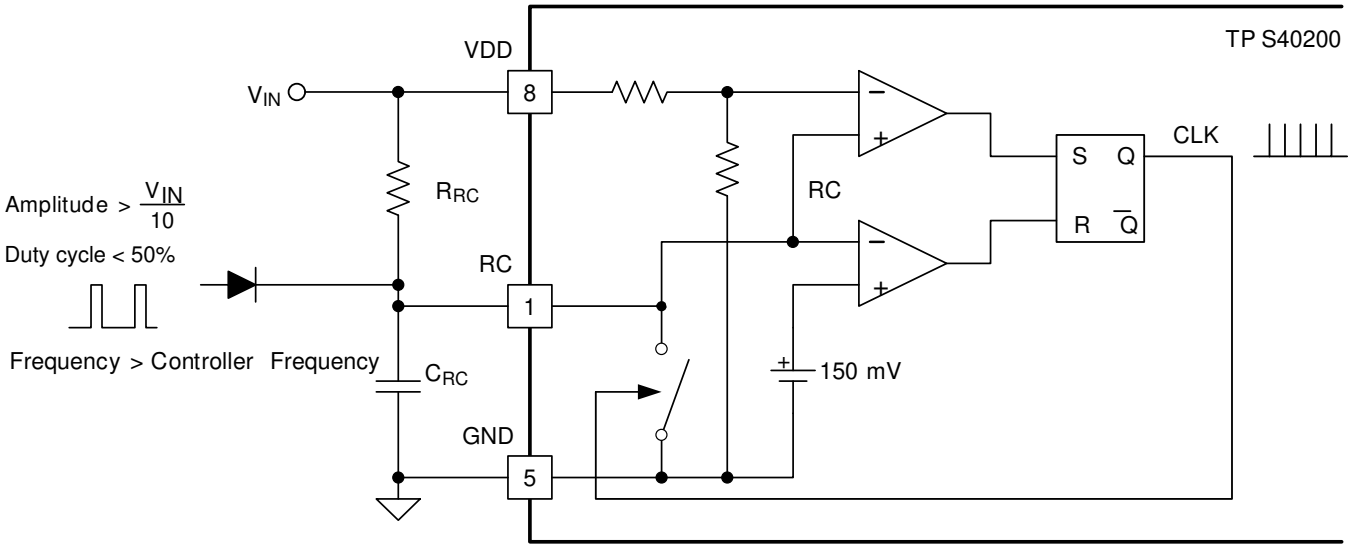


Figure 25. Diode-Connected Synchronization

7.3.5 Current-Limit Resistor Selection

As shown in Figure 28, a resistor in series with the power MOSFET sets the overcurrent protection level. Use a low-inductance resistor to avoid ringing signals and nuisance tripping. When the FET is on and the controller senses 100 mV or more drop from the V_{DD} pin to the ISNS pin, an overcurrent condition is declared. When this happens, the FET is turned off and, as shown in Figure 26, the soft-start capacitor is discharged. When the soft-start capacitor reaches a level below 150 mV, the converter clears the overcurrent condition flag and attempts to restart. If the condition that caused the overcurrent event to occur is still present on the output of the converter (see Figure 27), another overcurrent condition is declared and the process repeats indefinitely. Figure 27 shows the soft-start capacitor voltage during an extended output fault condition. The overall duty cycle of current conduction during a persistent fault is approximately 2%.

Feature Description (continued)

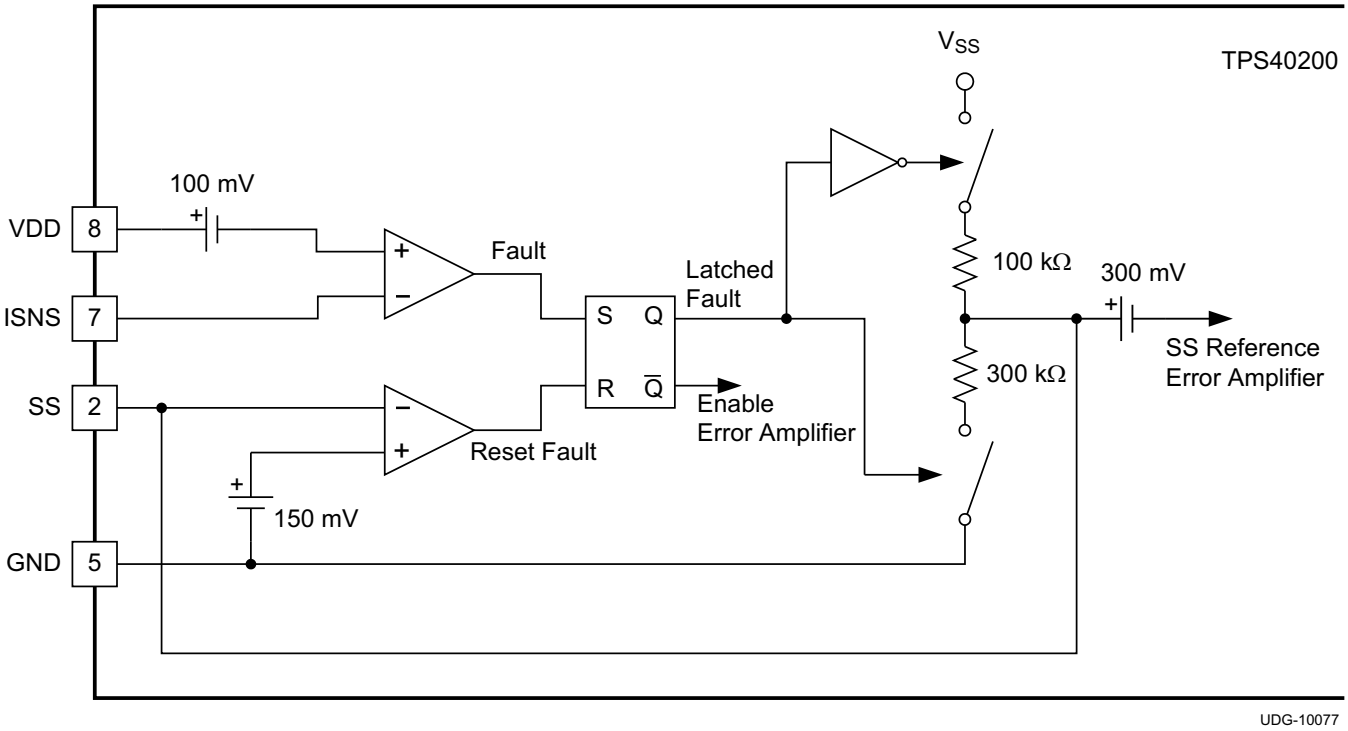


Figure 26. Current-Limit Reset

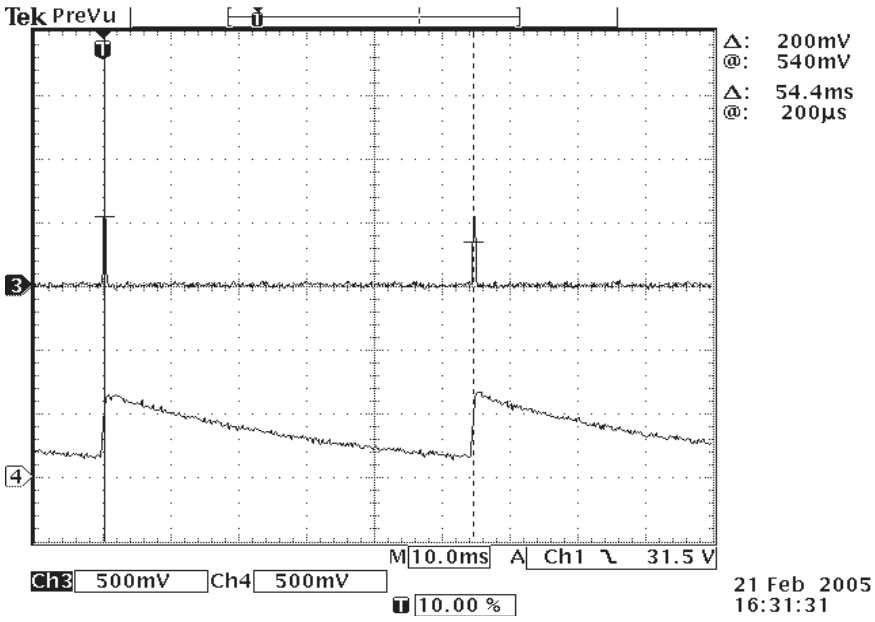


Figure 27. Typical Soft-Start Capacitor and V_{OUT} During Overcurrent

If necessary, a small RC filter can be added to the current sensing network to reduce nuisance tripping due to noise pickup. This filter can also be used to trim the overcurrent trip point to a higher level with the addition of a single resistor (see Figure 28). The nominal overcurrent trip point using the circuit of Figure 28 is described using Equation 3.

Feature Description (continued)

$$I_{OC} = \frac{V_{ILIM}}{R_{ILIM}} \times \frac{R_{F1} + R_{F2}}{R_{F2}}$$

where

- I_{OC} = overcurrent trip point, peak current in the inductor
- V_{ILIM} = overcurrent threshold voltage for the TPS40200-Q1, typically 100 mV
- R_{ILIM} = value of the current sense resistor in Ω
- R_{F1} and R_{F2} = values of the scaling resistors in Ω (3)

The value of the capacitor is determined by the nominal pulse width of the converter and the values of the scaling resistors R_{F1} and R_{F2}. It is best not to have the time constant of the filter longer than the nominal pulse width of the converter, otherwise a substantial increase in the overcurrent trip point occurs. Using this constraint, the capacitor value may be bounded using Equation 4.

$$C_F \leq \frac{\left(\frac{V_O}{V_{IN} \times f_{SW}}\right)}{\left[\frac{(R_{F1} \times R_{F2})}{(R_{F1} + R_{F2})}\right]}$$

where

- C_f = value of the current limit filter capacitor in F
- V_O = output voltage of the converter
- V_{IN} = input voltage to the converter
- f_{SW} = converter switching frequency
- R_{F1} and R_{F2} = values of the scaling resistors in Ω (4)

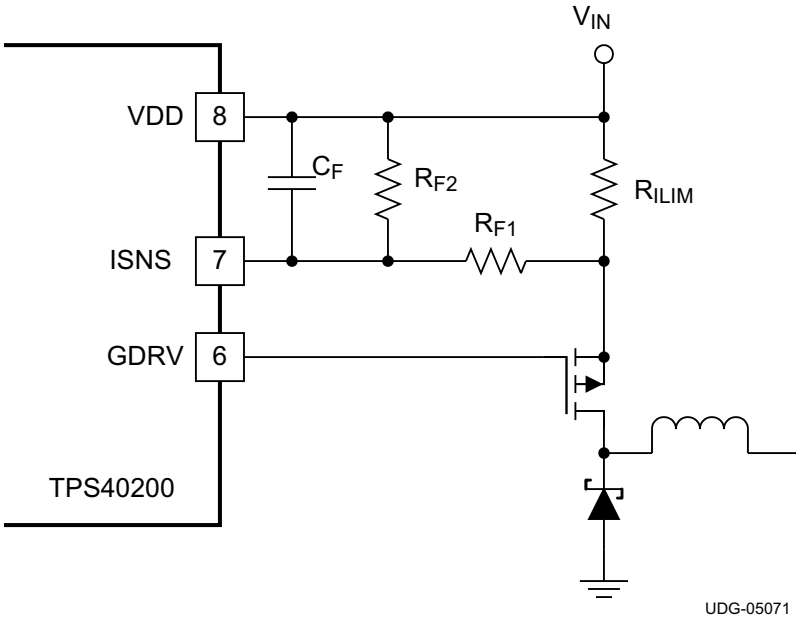


Figure 28. Current-Limit Adjustment

Feature Description (continued)

CAUTION

The current limit resistor, R_{ILM}, and its associated circuitry protect the device if the ISNS pin (pin 7) and the VDD pin (pin 8) are shorted or have other high-current load conditions. R_{ILM} and associated current-limiting circuitry may be eliminated if the supply input current is limited elsewhere in the application. However, by removing the current limit function, damage to the device or PCB during an overcurrent event may occur. The recommendation is to use the current limit.

7.3.6 Calculating the Soft-Start Time

An external capacitor (C_{SS}) connected from the SS pin to ground controls the TPS40200-Q1 soft-start interval. An internal charging resistor connected to V_{DD} produces a rising reference voltage that is connected through a 700-mV offset to the reference input of the TPS40200-Q1 error amplifier. When the soft-start capacitor voltage (V_{CSS}) is below 150 mV, there is no switching activity. When V_{CSS} rises above the 700-mV offset, the error amplifier starts to follow V_{SST} – 700 mV and uses this rising voltage as a reference. When V_{CSS} reaches 1.4 V, the internal reference takes over, and further increases have no effect. An advantage of initiating a slow start in this fashion is that the controller cannot overshoot, because its output follows a scaled version of the controller reference voltage. A conceptual drawing of the circuit that produces these results is shown in Figure 29. A consequence of the 700-mV offset is that the controller does not start switching until the V_{CSS} has charged up to 700 mV. The output remains at 0 V during the resulting delay. When V_{CCS} exceeds the 700-mV offset, the TPS40200-Q1 output follows the soft-start time constant. Once above 1.4 V, the 700-mV internal reference takes over, and normal operation begins.

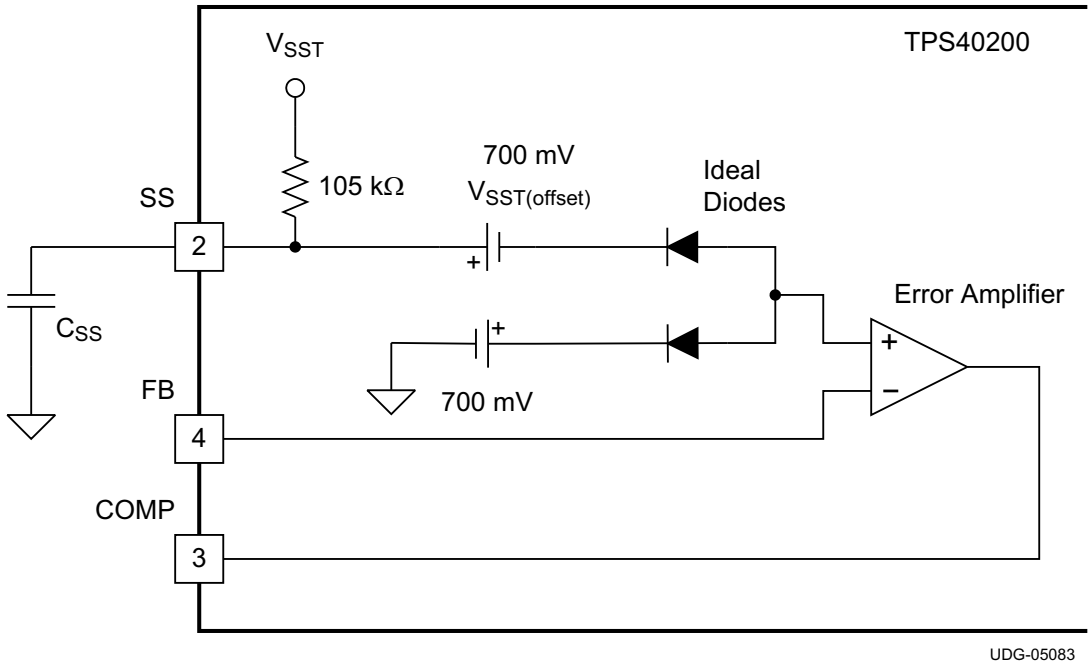


Figure 29. Soft-Start Circuit

The slow-start time should be longer (slower) than the time constant of the output LC filter. This time constraint may be expressed as:

$$t_S \geq 2\pi \times \sqrt{L_{OUT} \times C_{OUT}} \quad (5)$$

The calculation of the soft-start interval is simply the time it takes the RC network to exponentially charge from 0 V to 1.4 V. An internal 105-kΩ charging resistor is connected from the SS pin to V_{SST}. For applications where the voltage is above 8 V, an internal regulator clamps the maximum charging voltage to 8 V.

Feature Description (continued)

The result of this is a formula for the start up time, as given by Equation 6.

$$t_{SS} = R_c \times C_{SS} \times \ln\left(\frac{V_{SST}}{V_{SST} - 1.4}\right)$$

where

- t_{SS} = required soft-start time in seconds
- C_{SS} = soft-start capacitor value in F
- R_c = internal soft-start charging resistor (105 kΩ nominal)
- V_{SST} = input voltage up to a maximum of 8 V (6)

7.3.7 Voltage Setting and Modulator Gain

Since the input current to the error amplifier is negligible, the feedback impedance can be selected over a wide range. Knowing that the reference voltage is 708 mV, choose a convenient value for R1 and then calculate the value of R2 using Equation 7.

$$V_{OUT} = 0.708 \times \left(1 + \frac{R2}{R1}\right) \quad (7)$$

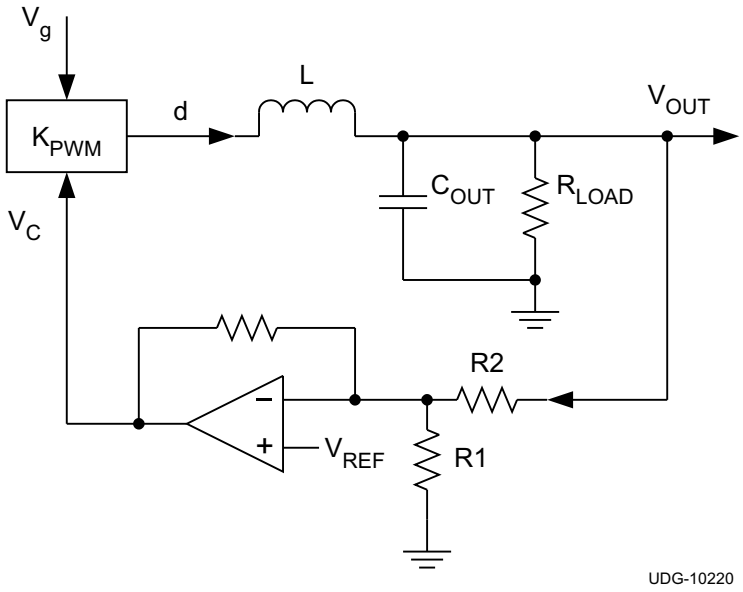


Figure 30. System Gain Elements

The error amplifier has a DC open-loop gain of at least 60 dB with a minimum of a 1.5-MHz gain bandwidth product, which gives the user flexibility with respect to the type of feedback compensation to use for the particular application. The gain selected by the user at the crossover frequency is set to provide an overall unity gain for the system. The crossover frequency should be selected so that the error amplifier open-loop gain is high with respect to the required closed-loop gain. This ensures that the amplifier response is determined by the passive feedback elements.

7.4 Device Functional Modes

7.4.1 Operation Near Minimum Input Voltage

The TPS40200-Q1 is designed to operate with input voltages above 4.5 V. The typical V_{DD} UVLO threshold is 4.25 V and the device may operate at input voltages down to the UVLO voltage. At input voltages below the actual UVLO voltage, the device will not switch. When V_{VDD} passes the UVLO threshold, the device will become active. Switching is enabled and the soft-start sequence is initiated. The TPS40200-Q1 will ramp up the output voltage at the rate determined by the external capacitor at the soft-start pin.

7.4.2 Operation With SS Pin

The SS pin has a 150-mV threshold, which can be used to disable the TPS40200-Q1. With SS forced below this threshold voltage, the device is disabled and switching is inhibited even if V_{VDD} is above its UVLO threshold. If the SS voltage is allowed to increase above the threshold while V_{VDD} is above its UVLO threshold, the device becomes active. Switching is enabled and the soft-start sequence is initiated. The TPS40200-Q1 will ramp up the output voltage at the rate determined by the external capacitor at the soft-start pin.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS40200-Q1 is a 4.5-V to 52-V buck controller with an integrated gate driver for a high-side p-channel MOSFET. This device is typically used to convert a higher DC voltage to a lower DC voltage with a maximum output current set by an external current sense resistor. In higher current applications, the maximum output current can also be limited by the thermal performance of the external MOSFET and rectifying diode switch. Use the following design procedure to select external components for the TPS40200-Q1. The design procedure illustrates the design of a typical buck regulator with the TPS40200-Q1.

8.2 Typical Applications

8.2.1 Buck Regulator, 8-V to 12-V Input, 3.3-V or 5-V Output at 2.5 A

The buck regulator design shown in Figure 31 shows the use of the TPS402000-Q1. It delivers 2.5 A at either 3.3 V or 5 V as selected by a single feedback resistor. It achieves approximately 90% efficiency at 3.3 V and 94% at 5 V. A discussion of design tradeoffs and methodology is included to serve as a guide to the successful design of forward converters using the TPS40200-Q1.

The efficiency from boards built from this design is shown in Figure 39 and Figure 40. Additional application information is available from Texas Instruments.

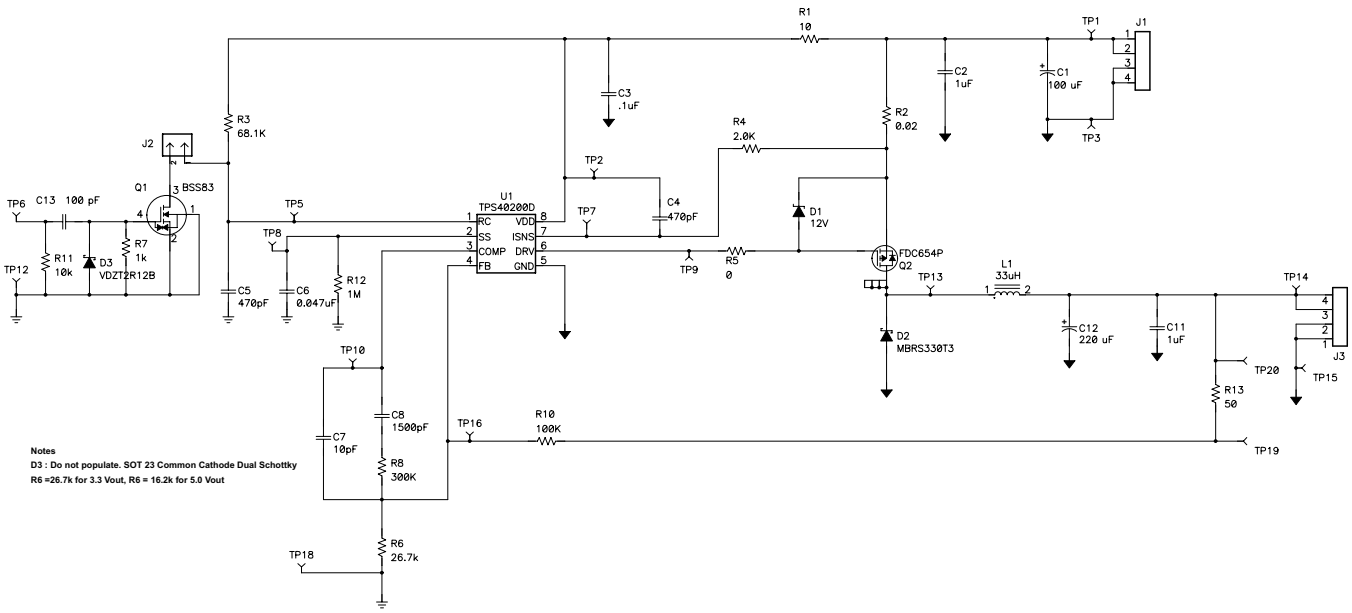


Figure 31. 8-V to 16-V V_{IN} Step-Down Buck Converter

Typical Applications (continued)

8.2.1.1 Design Requirements

Table 1 shows the design parameters for this example application.

Table 1. Design Parameters

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
V_{IN}	Input voltage		8	12	16	V
V_{OUT}	Output voltage	I_{OUT} at 2.5 A	3.2	3.3	3.4 (1)	V
	Line regulation	Approximately 0.2 % V_{OUT}	3.293	3.3	3.307	V
	Load regulation	Approximately 0.2% V_{OUT}	3.293	3.3	3.307	V
V_{OUT}	Output voltage	I_{OUT} at 2.5 A	4.85	5	5.15 (1)	V
	Line regulation	Approximately 0.2% V_{OUT}	4.99	5	5.01	V
	Load regulation	Approximately 0.2% V_{OUT}	4.99	5	5.01	V
V_{RIPPLE}	Output ripple voltage	At maximum output current		60		mV
V_{OVER}	Output overshoot	For 2.5-A load transient from 2.5 A to 0.25 A		100		mV
V_{UNDER}	Output undershoot	For 2.5-A load transient from 0.25 A to 2.5 A		60		mV
I_{OUT}	Output current		0.125		2.5	A
I_{SCP}	Short-circuit current trip point		3.75		5	A
	Efficiency	At nominal input voltage and maximum output current		90%		
F_S	Switching frequency			300		kHz

(1) Set-point accuracy is dependent on external resistor tolerance and the device reference voltage. Line and load regulation values are referenced to the nominal design output voltage.

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 FET Selection Criteria

1. The maximum input voltage for this application is 16 V. Switching the inductor causes overshoot voltages that can equal the input voltage. Because the $R_{DS(on)}$ of the FET rises with breakdown voltage, select a FET with the lowest breakdown voltage possible. In this case, a 30-V FET was selected.
2. Selecting the size of a power FET requires knowing both the switching losses and DC losses in the application. AC losses are all frequency dependent and directly related to device capacitances and device size. However, DC losses are inversely related to device size. The result is an optimum where the two types of losses are equal. Because device size is proportional to $R_{DS(on)}$, begin by selecting a device with an $R_{DS(on)}$ that results in a small loss of power relative to package thermal capability and overall efficiency objectives.
3. In this application, the efficiency target is 90% and the output power 8.25 W. This gives a total power-loss budget of 0.916 W. Total FET losses must be small relative to this number.

The DC conduction loss in the FET is given by Equation 8.

$$P_{DC} = I_{RMS}^{\ 2} \times R_{DS(on)} \tag{8}$$

The RMS current is given by Equation 9.

$$I_{rms} = \left[D \times \left(I_{OUT}^{\ 2} + \frac{\Delta I_{pp}^{\ 2}}{12} \right) \right]^{\frac{1}{2}}$$

where

- $\Delta I_{pp} = \Delta V \times D \times (t_s/L_l)$
- $\Delta V = V_{IN} - V_{OUT} - (DCR + R_{DS(on)}) \times I_{OUT}$
- $R_{DS(on)}$ = FET on-state resistance
- DCR = inductor DC resistance
- D = duty cycle
- t_S = reciprocal of the switching frequency

(9)

Using the values in this example, the DC power loss is 129 mW. The remaining FET losses are as follows:

- P_{SW} – The power dissipated while switching the FET on and off
- P_{GATE} – The power dissipated driving the FET gate capacitance
- P_{COSS} – The power switching the FET output capacitance

The total power dissipated by the FET is calculated using Equation 10.

$$P_{FET} = P_{SW} + P_{GATE} + P_{COSS} + P_{RDS(on)} \quad (10)$$

The P-channel FET, Q2, used in this application is a FDC654P with the following characteristics:

- $t_{RISE} = 13 \times 10^{-9}$
- $t_{FALL} = 6 \times 10^{-9}$
- $R_{DS(on)} = 0.1\ \Omega$
- $Q_{GD} = 1.2 \times 10^{-9}$
- $C_{OSS} = 83 \times 10^{-12}$
- $Q_G = 9$ nC
- $V_{GATE} = 1.9$ V
- $Q_{GS} = 1 \times 10^{-9}$

Using these device characteristics and the following formulas, P_{SW} is calculated using Equation 11:

$$P_{SW} = \frac{f_S}{2} \times \left(V_{IN} \times I_{pk} \times t_{CHON} \right) + \frac{f_S}{2} \left(V_{IN} \times I_{pk} \times t_{CHOFF} \right) = 10 \text{ mW}$$

where $t_{CHON} = \frac{Q_{GD} \times R_G}{V_{IN} - V_{TH}}$ and $t_{CHOFF} = \frac{Q_{GD} \times R_G}{V_{IN}}$ are the switching times for the power FET. (11)

$$P_{GATE} = Q_G \times V_{GATE} \times f_S = 22 \text{ mW} \quad (12)$$

$$P_{COSS} = \frac{C_{OSS} \times V_{IN\_MAX}{}^2 \times f_S}{2} = 2 \text{ mW} \quad (13)$$

The gate current is $I_G = Q_G \times f_S = 2.7$ mA.

The sum of the switching losses is 34 mW and is comparable to the 129-mW DC losses. At added expense, a slightly larger FET is better, because the DC loss drops and the AC losses increase, with both moving toward the optimum point of equal losses.

8.2.1.2.2 Rectifier Selection Criteria

- Rectifier breakdown voltage:

  The rectifier must withstand the maximum input voltage, which in this case is 16 V. To allow for switching transients that can approach the switching voltage, a 30-V rectifier was selected.
- Diode size:

  The importance of power losses from the Schottky rectifier (D2) is determined by the duty cycle. For a low duty-cycle application, the rectifier conducts most of the time and the current that flows through it times its forward drop can be the largest component of loss in the entire controller. In this application, the duty cycle ranges from 20% to 40%, which in the worst case means that the diode conducts 80% of the time. Where efficiency is of paramount importance, choose a diode with a minimum forward drop. In more cost-sensitive applications, size may be reduced to the point of the thermal limitations of the diode package.

  The device in this application is large relative to the current required by the application. In a more cost-sensitive application, a smaller diode in a less-expensive package will provide a less-efficient but appropriate solution.

  The device used, D2, has the following characteristics:
  - $V_f = 0.3$ V at 3 A
  - $C_t = 300$ pF (C_t = effective reverse voltage capacitance of the synchronous rectifier, D2)

The two components of the losses from the diode D2 are calculated using Equation 14.

$$P_{COND} = V_f \times \left(I_{OUT} + \frac{I_{RIPPLE}}{4}\right) \times (1 - D) = 653 \text{ mW} \quad (14)$$

where

- D = duty cycle
- I_{RIPPLE} = ripple current
- I_{OUT} = output current
- V_F = forward voltage
- P_{COND} = conduction power loss

The switching capacitance of this diode adds an AC loss, given by Equation 15.

$$P_{SW} = \frac{1}{2}\left[C \times (V_{IN} + V_f)^2 \times f\right] = 6.8 \text{ mW} \quad (15)$$

This additional loss raises the total loss to 660 mW.

At an output voltage of 3.3 V, the application runs at a nominal duty cycle of 27% with the diode conducting 72.5% of the time. As the output voltage is moved up to 5 V, the on time increases to 46% with the diode conducting only 54% of the time during each clock cycle. This change in duty cycle proportionately reduces the conduction power losses in the diode. This reduction may be expressed as Equation 16.

$$660 \times \left(\frac{0.54}{0.725}\right) = 491 \text{ mW} \quad (16)$$

for a savings in power of 660 – 491 = 169 mW.

To illustrate the relevance of this power savings, measure the full-load module efficiency for this application at 3.3 V and 5 V. The 5-V output efficiency is 92% versus 89% for the 3.3-V design. This difference in efficiency represents a 456-mW reduction in loss between the two conditions. This 169-mW power-loss reduction in the rectifier represents 37% of the difference.

8.2.1.2.3 Inductor Selection Criteria

The TPS40200-Q1 P-FET driver facilitates switching the power FET at a high frequency. In turn, this enables the use of smaller less-expensive inductors as illustrated in this 300-kHz application. Ferrite, with its good high-frequency properties, is the material of choice. Several manufacturers provide catalogs with inductor saturation currents, inductance values, and LSRs (internal resistance) for their various-sized ferrites.

In this application, the device must deliver a maximum current of 2.5 A. This requires that the saturation current of the output inductor is above 2.5 A plus one-half the ripple current caused during inductor switching. The value of the inductor determines this ripple current. A low value of inductance has a higher ripple current that contributes to ripple voltage across the resistance of the output capacitors. The advantages of a low inductance are a higher transient response, lower DCR, a higher saturation current, and a smaller less-expensive device. Too low an inductor, however, leads to higher peak currents, which ultimately are bounded by the overcurrent limit set to protect the output FET or by output ripple voltage. Fortunately, with low-ESR ceramic capacitors on the output, the resulting ripple voltage for relatively high ripple currents can be small.

For example, a single 1-µF 1206-sized 6.3-V ceramic capacitor has an internal resistance of 2 Ω at 1 MHz. For this 2.5-A application, a 10% ripple current of 0.25 A produces a 50-mV ripple voltage. This ripple voltage may be further reduced by additional parallel capacitors.

The other bound on inductance is the minimum current at which the controller enters discontinuous conduction. At this point, inductor current is zero. The minimum output current for this application is specified at 0.125 A. This average current is one-half the peak current that must develop during a minimum on time. The conditions for minimum on time are high line and low load.

L_{MIN} is calculated using Equation 17.

$$L_{MIN} = \frac{V_{IN} - V_{OUT}}{I_{PEAK}} \times t_{ON} = 32\ \mu H$$

where

- V_{IN} = 16 V
- V_{OUT} = 3.3 V
- I_{PEAK} = 0.25 A
- t_{ON} = 0.686 µs
- t_{ON} is given by $\frac{1}{300\ kHz} \times \frac{3.3\ V}{16\ V}$ (17)

The inductor used in the circuit, L1, is the closest standard value of 33 µH. This is the minimum inductance that can be used in the converter to deliver the minimum current while maintaining continuous conduction.

8.2.1.2.4 Output Capacitance

In order to satisfy the output voltage overshoot and undershoot specifications, there must be enough output capacitance to keep the output voltage within the specified voltage limits during load current steps.

In a situation where a full load of 2.5 A within the specified voltage limits is suddenly removed, the output capacitor must absorb energy stored in the output inductor. This condition may be described by realizing that the energy in the stored in the inductor must be suddenly absorbed by the output capacitance. This energy relationship is written using Equation 18.

$$\frac{1}{2} \times L_O I_O^2 \le \frac{1}{2} \times \left[C_O \left(V_{OS}^2 - V_O^2 \right) \right]$$

where

- V_{OS} = allowed overshoot voltage above the output voltage
- L_O = inductance
- I_O = output current
- C_O = output capacitance
- V_O = output voltage (18)

In this application, the worst-case load step is 2.25 A, and the allowed overshoot is 100 mV. With a 33-µH output inductor, this implies an output capacitance of 249 µF for a 3.3-V output and 165 µF for a 5-V output.

When the load increases from minimum to full load, the output capacitor must deliver current to the load. The worst case is for a minimum on time that occurs at 16 V_{IN}, 3.3 V_{OUT}, and minimum load. This corresponds to an off time of (1 – 0.2) times the period 3.3 µs and is the worst-case time before the inductor can start supplying current. This situation may be represented using Equation 19.

$$\Delta V_O < \Delta I_O \times \frac{t_{OFFMAX}}{C_O}$$

where

- ΔV_O = undershoot specification of 60 mV
- ΔI_O = load current step
- t_{OFFMAX} = maximum off time (19)

This condition produces a requirement of 100 µF for the output capacitance. The larger of these two requirements becomes the minimum value of output capacitance. In the schematic, an output capacitor of 220 µF (C12) in parallel with 1 µF (C11) is shown. This is from the EVM to balance both 3.3-V and 5-V output use cases. For fixed voltage output, modify the C11 and C12 values per the equations.

The ripple current develops a voltage across the ESR of the output capacitance, so another requirement on this component is that ESR be small relative to the ripple voltage specification.

8.2.1.2.5 Switching Frequency

The TPS40200-Q1 has a built-in 8-V, 200-mA, P-channel FET-driver output that facilitates using P-channel switching FETs. A clock frequency of 300 kHz was chosen as a switching frequency that represents a compromise between a high frequency that allows the use of smaller capacitors and inductors, and one that is not so high as to cause excessive transistor switching losses. As previously discussed, an optimum frequency can be selected by picking a value where the DC and switching losses are equal.

The frequency is set by using the design formula given in *FET Selection Criteria*.

$$R_{RC} \times C_{RC} = \frac{1}{0.105 \times f_{SW}} \quad (20)$$

where

- R_{RC} = timing resistor value in Ω or R3 = 68.1 kΩ
- C_{RC} = timing capacitor value in F or C5 = 470 pF
- f_{SW} = desired switching frequency in Hz, which in this case is 297 kHz

At a worst case of 16 V, the timing resistor draws about 250 µA, which is well below the 750-µA maximum that the circuit can pull down.

8.2.1.2.6 Calculating the Overcurrent Threshold Level

The current limit in the TSP40200-Q1 is triggered by a comparator with a 100-mV offset whose inputs are connected across a current-sense resistor between V_{DD} and the source of the high-side switching FET. When current in this resistor develops more than 100 mV, the comparator trips and terminates the output gate drive.

In this application, the current-limit resistor is set by the peak output stage current, which consists of the maximum load current plus one-half the ripple current. In this case, 2.5 + 0.125 = 2.625 A. To accommodate tolerances, a 25% margin is added, giving a 3.25-A peak current. Using the equation for I_{ILIM}, Figure 32 yields a value for R_{ILIM} of 31 mΩ. In the schematic, a 20-mΩ resistor, R2, was used for R_{ILIM}, which sets the current limit to 5 A. This schematic is from the EVM where evaluation at a higher current was allowed.

Current sensing in a switching environment requires attention to both circuit board traces and noise pickup. In the design shown, a small RC filter has been added to the circuit to prevent switching noise from tripping the current-sense comparator. The requirements of this filter are board dependent, but with the layout used in this application, no spurious overcurrent is observed.

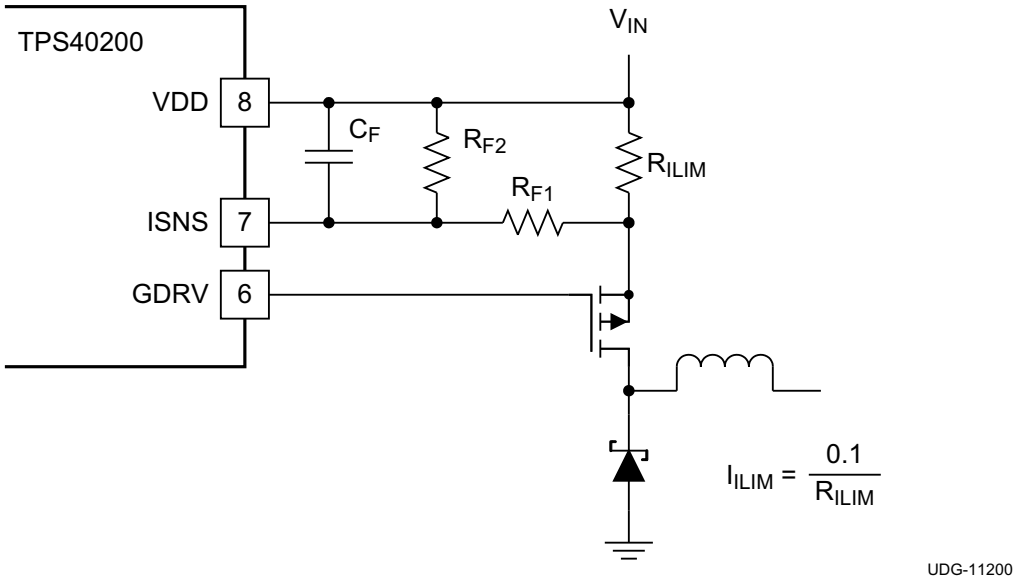


Figure 32. Overcurrent Trip Circuit for R_{F2} Open

8.2.1.2.7 Soft-Start Capacitor

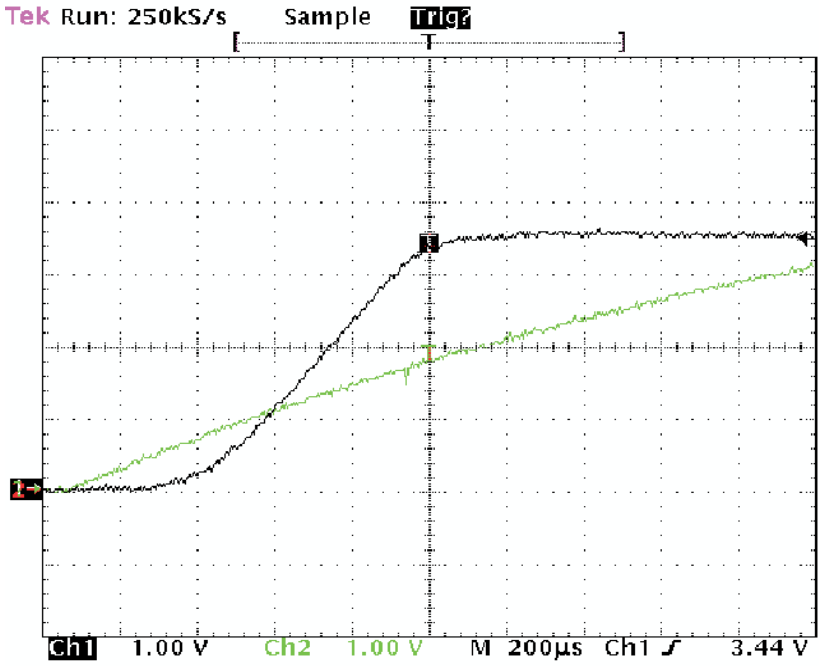
The soft-start interval is given (in pF) by Equation 21.

$$C_{SS} = \frac{t_{SS}}{R \times \ln\left(\frac{V_{SST}}{V_{SST} - 1.4}\right)} \times 10^3 \quad (21)$$

where

- R = internal 105-kΩ charging resistor
- V_{CC} = input voltage up to 8 V, where the charging voltage is internally clamped to 8 V maximum
- V_{OS} = 700 mV, and (because the input voltage is 12 V) V_{SST} = 8 V

The oscilloscope (Figure 33) shows the expected delay at the output (middle trace) until the soft-start node (bottom trace) reaches 700 mV. At this point, the output rises following the exponential rise of the soft-start capacitor voltage until the soft-start capacitor reaches 1.4 V and the internal 700-mV reference takes over. This total time is approximately 1 ms, which agrees with the calculated value of 0.95 ms when the soft-start capacitance is 0.047 µF, C6.



A. Channel 1 is the output voltage rising to 3.3 V.
B. Channel 2 is the soft-start pin.

Figure 33. Soft Start Showing Output Delay and Controlled Rise to Programmed Output Voltage

8.2.1.2.8 Frequency Compensation

The four elements that determine the system overall response are discussed in this section. The gain of the error amplifier (K_{EA}) is the first of these elements. Its output develops a control voltage that is the input to the PWM.

The TPS40200-Q1 has a unique modulator that scales the peak-to-peak amplitude of the PWM ramp to be 0.1 times the value of the input voltage. Because modulator gain is given by V_{IN} divided by V_{RAMP}, the modulator gain is 10 and is constant at 10 (20 dB) over the entire specified input-voltage range.

The last two elements that affect system gain are the transfer characteristic of the output LC filter and the feedback network from the output to the input to the error amplifier.

These four elements may be expressed using Equation 22 that represents the system transfer function as shown in Figure 34.

$$T_{V(S)} = K_{FB} \times K_{EA}(S) \times K_{PWM} \times X_{LC}(S) \quad (22)$$

where

- K_{FB} = output voltage setting divider
- K_{EA} = error amplifier feedback
- K_{PWM} = modulator gain
- X_{LC} = filter transfer function

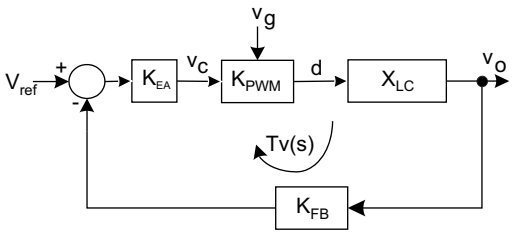


Figure 34. Control Loop

Figure 35 shows the feedback network used in this application. This is a Type II compensation network, which gives a combination of good transient response and phase boost for good stability. This type of compensation has a pole at the origin, causing a –20-dB/decade (–1) slope, followed by a zero that causes a region of flat gain, followed by a final pole that returns the gain slope to –1. The Bode plot in Figure 36 shows the effect of these poles and zeros.

The procedure for setting up the compensation network is as follows:

1. Determine the break frequency of the output capacitor.
2. Select a zero frequency well below this break frequency.
3. From the gain bandwidth of the error amplifier, select a crossover frequency at which the amplifier gain is large relative to expected closed-loop gain.
4. Select a second zero well above the crossover frequency that returns the gain slope to a –1 slope.
5. Calculate the required gain for the amplifier at crossover.

Be prepared to iterate this procedure to optimize the pole and zero locations as needed.

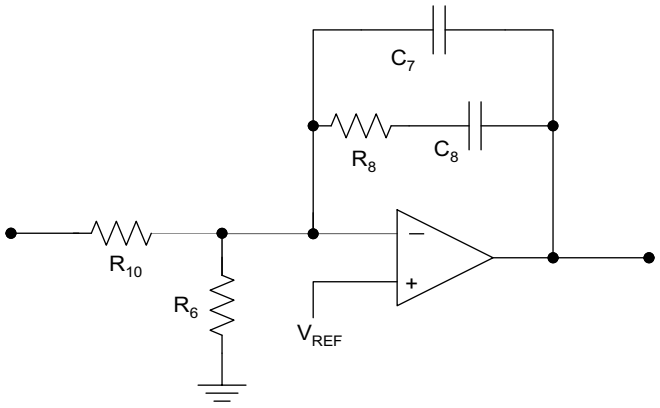


Figure 35. Error Amplifier Feedback Elements

The frequency response of this converter is largely determined by two poles that arise from the LC output filter and a higher-frequency zero caused by the ESR of the output capacitance. The poles from the output filter cause a 40-dB/decade rolloff with a phase shift approaching 180 degrees, followed by the output capacitor zero that reduces the roll off to –20 dB and gives a phase boost back toward 90 degrees. In other nomenclature, this is a –2 slope followed by a –1 slope. The two zeros in the compensation network act to cancel the double pole from the output filter. The two poles of the compensation network produce a region in which the error amplifier is flat and can be set to a gain such that the overall gain of the system is 0 dB. This region is set so that it brackets the system crossover frequency.

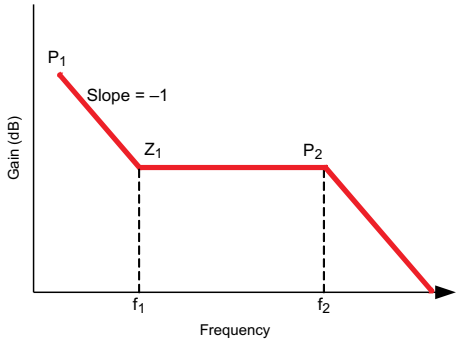


Figure 36. Error Amplifier Bode Plot

To properly compensate this system, it is necessary to know the frequencies of its poles and zeros.

8.2.1.2.8.1 Step 1

The break frequency of the output capacitor is given by Equation 23.

$$f_{ESR} = \frac{1}{2\pi \times R_{ESR} \times C_{OUT}}$$

where

- C_{OUT} = the output capacitor
- R_{ESR} = the ESR of the capacitors (23)

Because of the ESR of the output capacitor, this output filter has a single-pole response above the 1.8-kHz break frequency of the output capacitor and its ESR. This simplifies compensation since the system becomes essentially a single-pole system.

8.2.1.2.8.2 Step 2

The first zero is placed well below the 1.8-kHz break frequency of the output capacitor and its ESR. Phase boost from this zero is shown in Figure 38.

$$f_{Z1} = \frac{1}{2\pi \times R_8 \times C_8}$$

where

- R_8 = 300 kΩ
- C_8 = 1500 pF
- f_{Z1} = 354 Hz (24)

8.2.1.2.8.3 Step 3

From a minimum gain bandwidth product of 1.5 MHz, and knowing it has a 20-dB/decade rolloff, the open-loop gain of the error amplifier is 33 dB at 35 kHz. This approximate frequency is chosen for a crossover frequency to keep the amplifier gain contribution to the overall system gain small, as well as following the convention of placing the crossover frequency between 1/6 to 1/10 the 300-kHz switching frequency.

8.2.1.2.8.4 Step 4

The second pole is placed well above the 35-kHz crossover frequency.

$$f_{P2} = \frac{1}{2\pi \times C_7 \times C_8 \times R_8} \times (C_7 + C_8)$$

where

- R_8 = 300 kΩ
- C_7 = 10 pF
- C_8 = 1500 pF
- f_{P2} = 53 kHz (25)

8.2.1.2.8.5 Step 5

Use Equation 26 to calculate the gain elements in the system to determine the gain required by the error amplifier to make the overall gain 0 dB at 35 kHz.

$$T_{V(S)} = K_{FB} \times K_{EA}(S) \times K_{PWM} \times X_{LC}(S)$$

where

- K_{FB} is the output voltage setting divider
- K_{EA} is the error amplifier feedback
- K_{PWM} is the modulator gain
- X_{LC} is the filter transfer function (26)

With reference to Figure 37, the transfer characteristic $X_{LC}(S)$ of the output filter can be estimated by Equation 27.

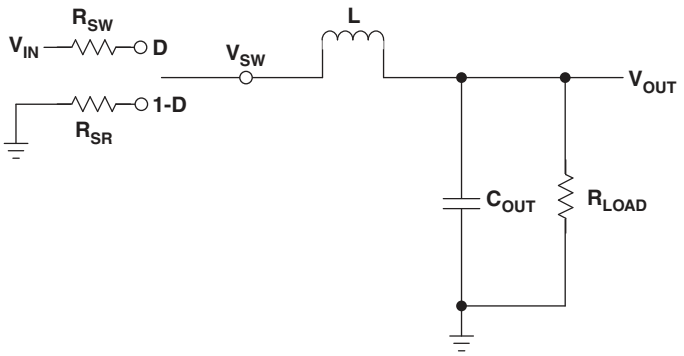


Figure 37. Output Filter Analysis

$$X_{LC}(S) = \frac{Z_{OUT}(S)}{Z_{OUT}(S) + Z_L(S) + R_{SW} \times D + R_{SR} \times (1 - D)}$$

where

- Z_{OUT} is the parallel combination of output capacitor(s) and the load
- R_{SW} is the $R_{DS(on)}$ of the switching FET plus the current-sense resistor
- R_{SR} is the resistance of the synchronous rectifier
- D is the duty cycle estimated as 3.3 / 12 = 0.27 (27)

To evaluate $X_{LC}(S)$ at 35 kHz, use Equation 28.

- $Z_{OUT}(S)$ at 35 kHz, which is dominated by the output capacitor's ESR; estimated to be 400 mΩ
- $Z_L(S)$ at 35 KHz is 7.25 Ω
- R_{SW} = 0.95 mΩ, including the R_{LIM} resistance
- R_{SR} = 100 mΩ

Using these numbers, $X_{LC}(S)$ = 0.04 or –27.9 dB.

The feedback network has a gain to the error amplifier given using Equation 28.

$$K_{fb} = \frac{R_{10}}{R_6}$$

where

- for 3.3 V_{OUT}, R6 = 26.7 kΩ (28)

Using the values in this application, K_{fb} = 11.4 dB.

The modulator has a gain of 10 that is flat to well beyond 35 kHz, so K_{PWM} = 20 dB.

To acheive 0-dB overall gain, the amplifier and feedback gain must be set to 7.9 dB (20 dB - 27.9 dB).

The amplifier gain, including the feedback gain, K_{fb}, can be approximated using Equation 29.

$$\frac{V_{OUT}}{V_{IN}}(S) = \frac{A_{VOL}}{1 + \frac{R_{10}}{R_8} + \frac{R_{10}}{Z_{FS}} \times (1 + A_{VOL})}$$

where

- Z_{FS} is the parallel combination of C_7 in parallel with the sum of R_8 and the impedance of C_8
- A_{VOL} is the open-loop gain of the error amplifier at 35 kHz, which is 44.6 or 33 dB (29)

Figure 38 shows the result of the compensation. The crossover frequency is 35 kHz, and the phase margin is 45°. The response of the system is dominated by the ESR of the output capacitor and is exploited to produce an essentially single-pole system with simple compensation.

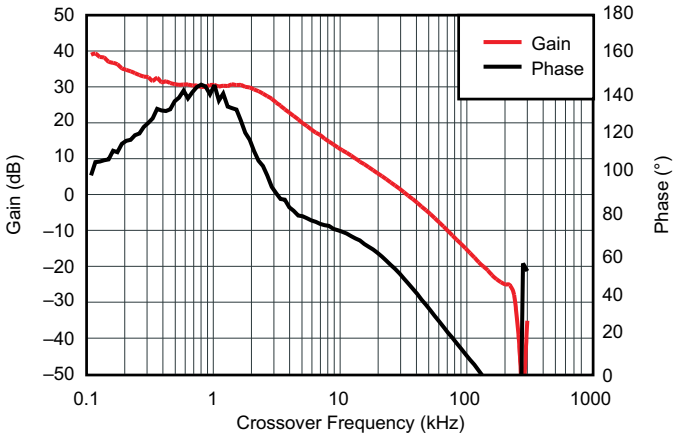


Figure 38. Overall System Gain and Phase Response

Figure 38 also shows the phase boost that gives the system a crossover phase margin of 47°.

8.2.1.3 Application Curves

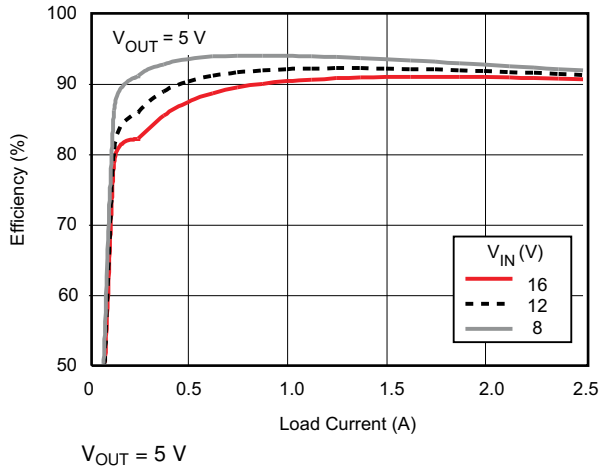


Figure 39. Full-Load Efficiency

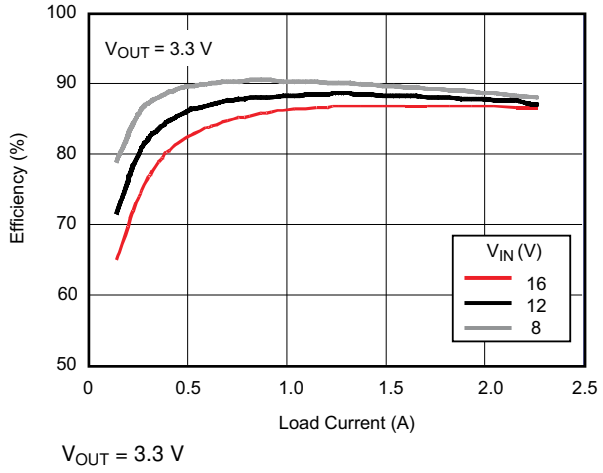


Figure 40. Full-Load Efficiency

8.2.2 Application 2: 18-V to 50-V Input, 16-V Output at 1 A

This is an example of using the TPS40200-Q1 in a higher voltage application. The output voltage is 16 V at 1 A with an 18-V to 50-V input. Module boards built to this schematic and a test report are available.

The efficiency and load regulation from boards built from this design are shown in Figure 42 and Figure 43. Further information and support material is available.

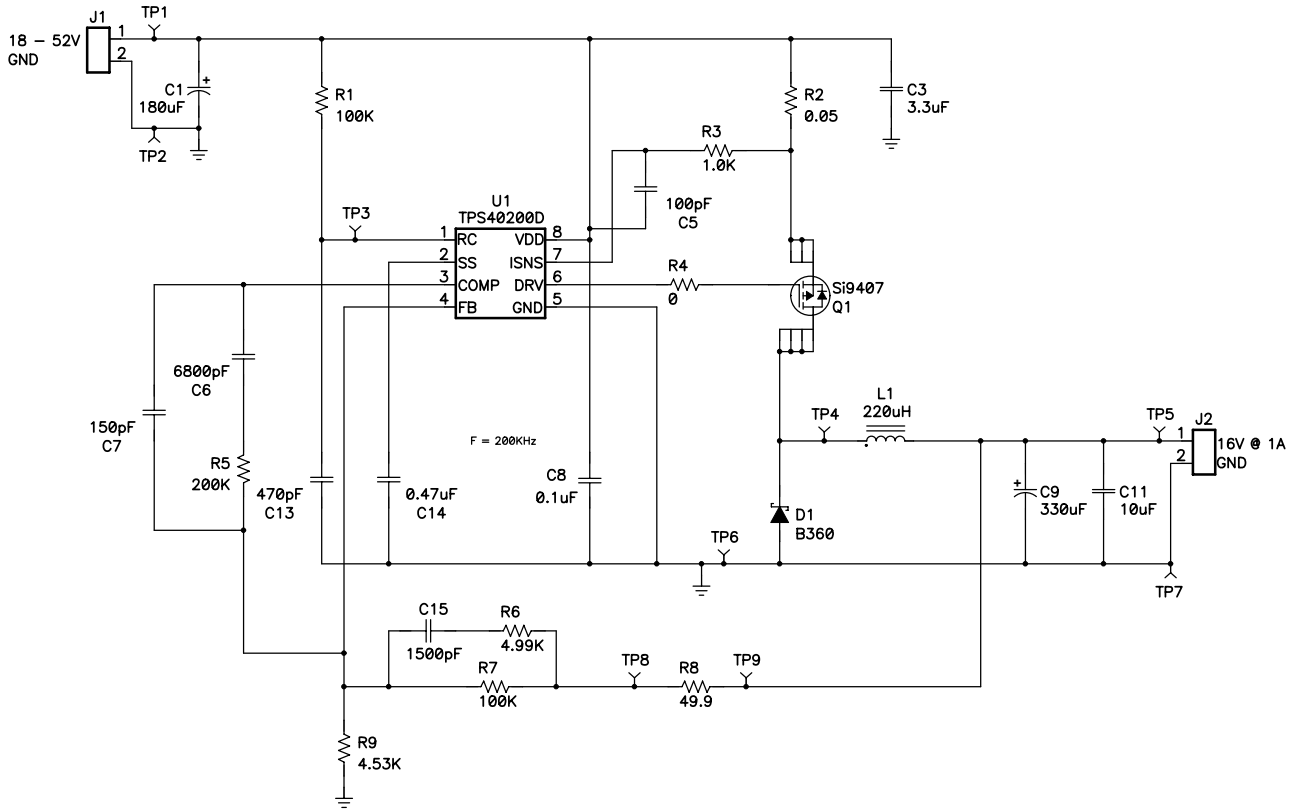


Figure 41. Buck Converter: V_{IN} = 18 V to 50 V, V_{OUT} = 16 V at 1 A

8.2.2.1 Design Requirements

Table 2 shows the design parameters for this example application.

Table 2. Design Parameters

PARAMETER		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	18		50	V
V_{OUT}	Output voltage		16		V
I_{OUT}	Output current			1	A
I_{SCP}	Short circuit current trip point		2		A
F_S	Switching frequency		200		kHz

8.2.2.2 Detailed Design Procedure

For the detailed design procedure, see the *Detailed Design Procedure* section for *Buck Regulator, 8-V to 12-V Input, 3.3-V or 5-V Output at 2.5 A*.

8.2.2.3 Application Curves

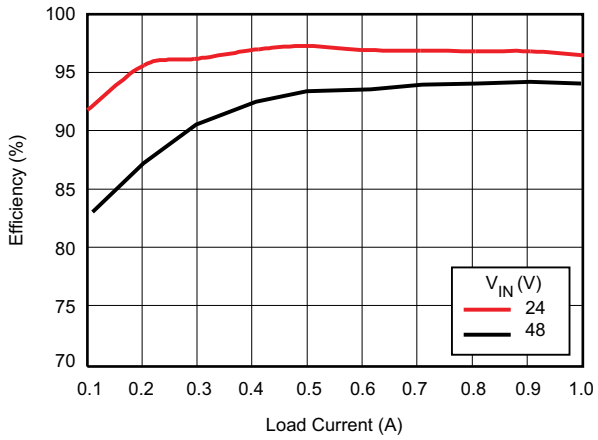


Figure 42. Efficiency vs Load

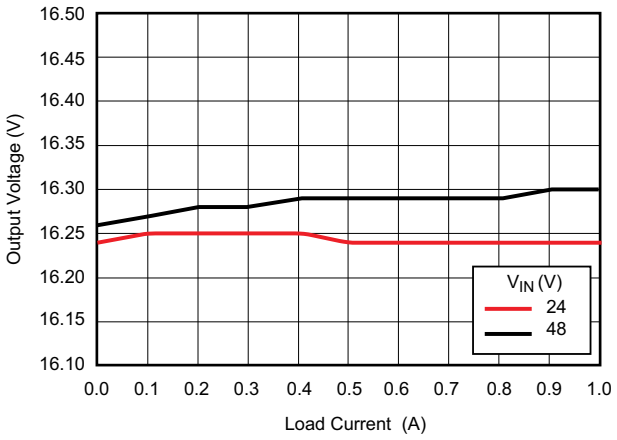


Figure 43. Load Regulation, Two Input Voltage Extremes

8.2.3 Application 3: Wide-Input-Voltage LED Constant-Current Driver

This application uses the TPS40200-Q1 as a buck controller that drives a string of LED diodes. The feedback point for this circuit is a sense resistor in series with this string. The low 0.7-V reference minimizes power wasted in this resistor and maintains the LED current at a value given by 0.7 V/R_{SENSE}. As the input voltage is varied, the duty cycle changes to maintain the LED current at a constant value, so that the light intensity does not change with large input-voltage variations.

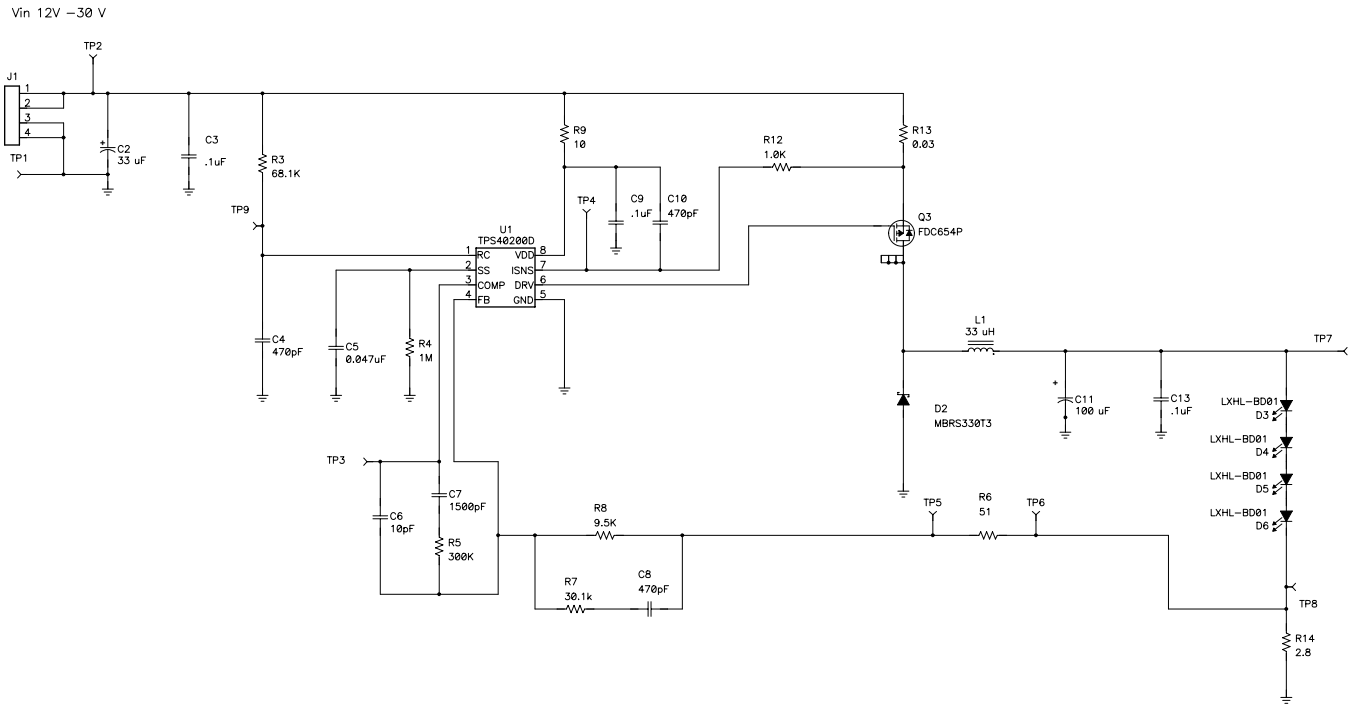


Figure 44. Wide-Input-Voltage Range LED Driver

8.2.3.1 Design Requirements

Table 3 shows the design parameters for this example application.

Table 3. Design Parameters

PARAMETER		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	12		30	V
I_{LED}	LED current		0.25		A
I_{SCP}	Short circuit current trip point		3.3		A
F_S	Switching frequency		300		kHz

8.2.3.2 Detailed Design Procedure

For the detailed design procedure, see the *Detailed Design Procedure* section for *Buck Regulator, 8-V to 12-V Input, 3.3-V or 5-V Output at 2.5 A*.

8.2.3.3 Application Curve

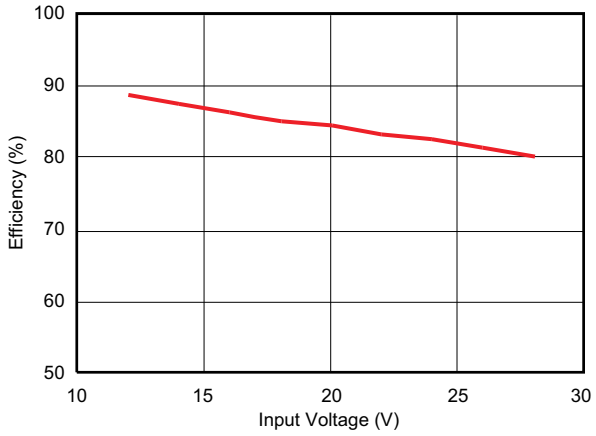


Figure 45. Efficiency vs Input Voltage

9 Power Supply Recommendations

The TPS40200-Q1 is designed to operate from an input voltage supply range between 4.5 V and 52 V. This input supply should be well regulated. If the input supply is located more than a few inches from the buck power stage controlled by the TPS40200-Q1, additional bulk capacitance may be required in addition to the ceramic-bypass capacitors. An electrolytic capacitor with a value of 100 µF is a typical choice.

10 Layout

10.1 Layout Guidelines

- Keep AC current loops as short as possible. For the maximum effectiveness from C3, place it near the V_{DD} pin of the controller and design the input AC loop consisting of C1-R_{SENSE}-Q1-D1 to be as short as possible. Excessive high-frequency noise on VDD during switching degrades overall regulation as the load increases.
- The output loop A (D1-L1-C2) should also be kept as small as possible. Otherwise, the output noise performance of the application will be degraded.
- TI recommends that traces carrying large AC currents not be connected through a ground plane. Instead, use PCB traces on the top layer to conduct the AC current, and use the ground plane as a noise shield. Split the ground plane as necessary to keep noise away from the TPS40200-Q1 and noise-sensitive areas, such as feedback resistors R6 and R10.
- Keep the SW node as physically small as possible to minimize parasitic capacitance and to minimize radiated emissions.
- For good output-voltage regulation, Kelvin connections should be brought from the load to R6 and R10.
- The trace from the R6-R10 junction to the TPS40200-Q1 should be short and kept away from any noise source, such as the SW node.
- The gate drive trace should be as close to the power FET gate as possible.

The TPS40200-Q1 is encapsulated in a standard plastic SOIC-8 package.

10.2 Layout Example

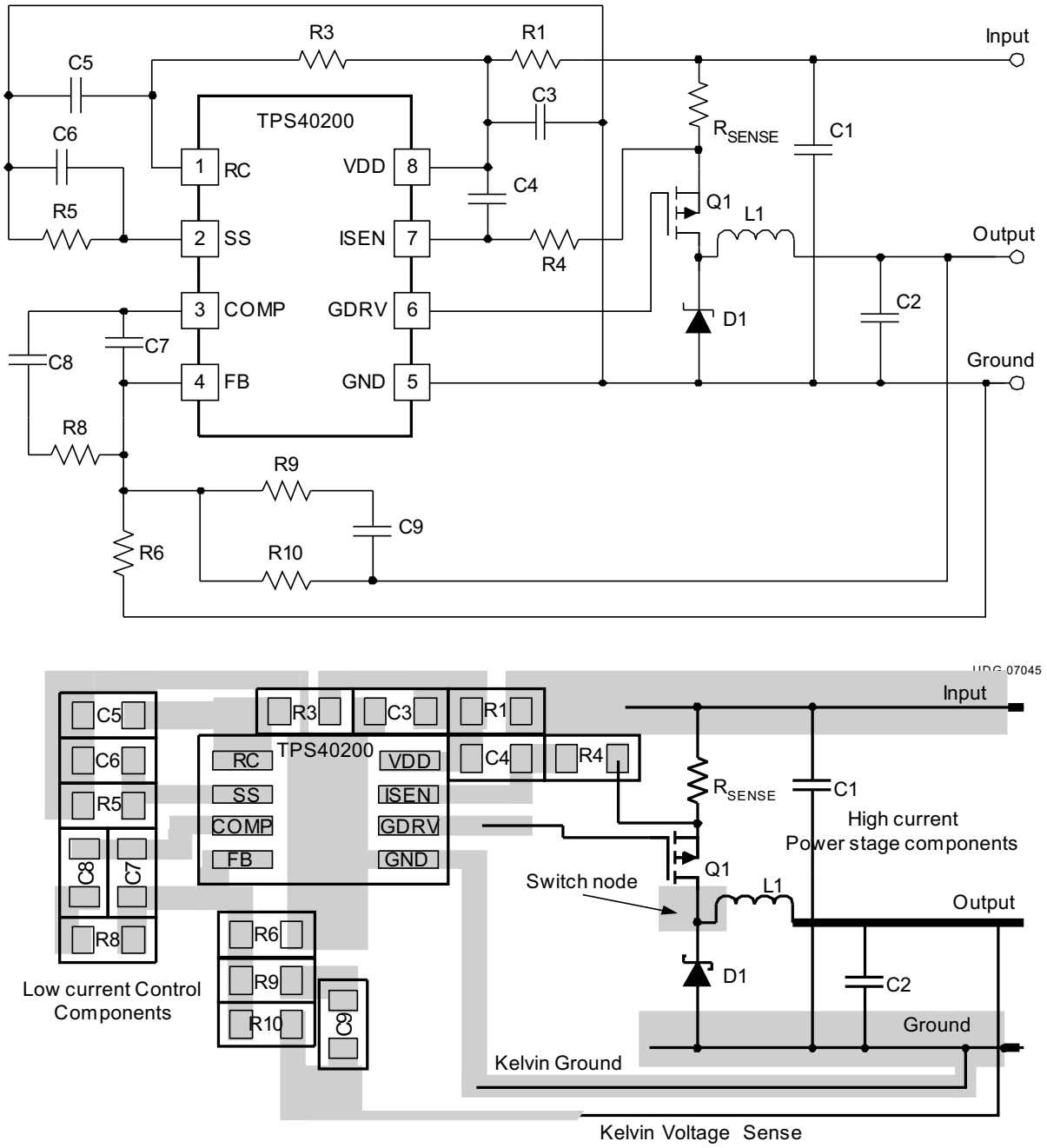


Figure 46. PCB Layout Recommendations

11 Device and Documentation Support

11.1 Device Support

11.1.1 Related Products

- TPS4007/9 Low-Input Synchronous Buck Controller
- TL5001 Wide-Input-Range Controller

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- *Under the Hood of Low-Voltage DC/DC Converters*, SEM1500 Topic 5, 2002 Seminar Series (SLUP206)
- *Understanding Buck Power Stages in Switch-Mode Power Supplies* (SLVA057)
- *Automotive Infotainment Guide* (SSAY002)
- *Designing Stable Control Loops*, SEM 1400, 2001 Seminar Series (http://power.ti.com)

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS40200QDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	40200Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

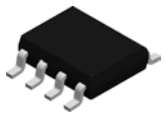
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPS40200-Q1 :

- Catalog: TPS40200
- Enhanced Product: TPS40200-EP

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

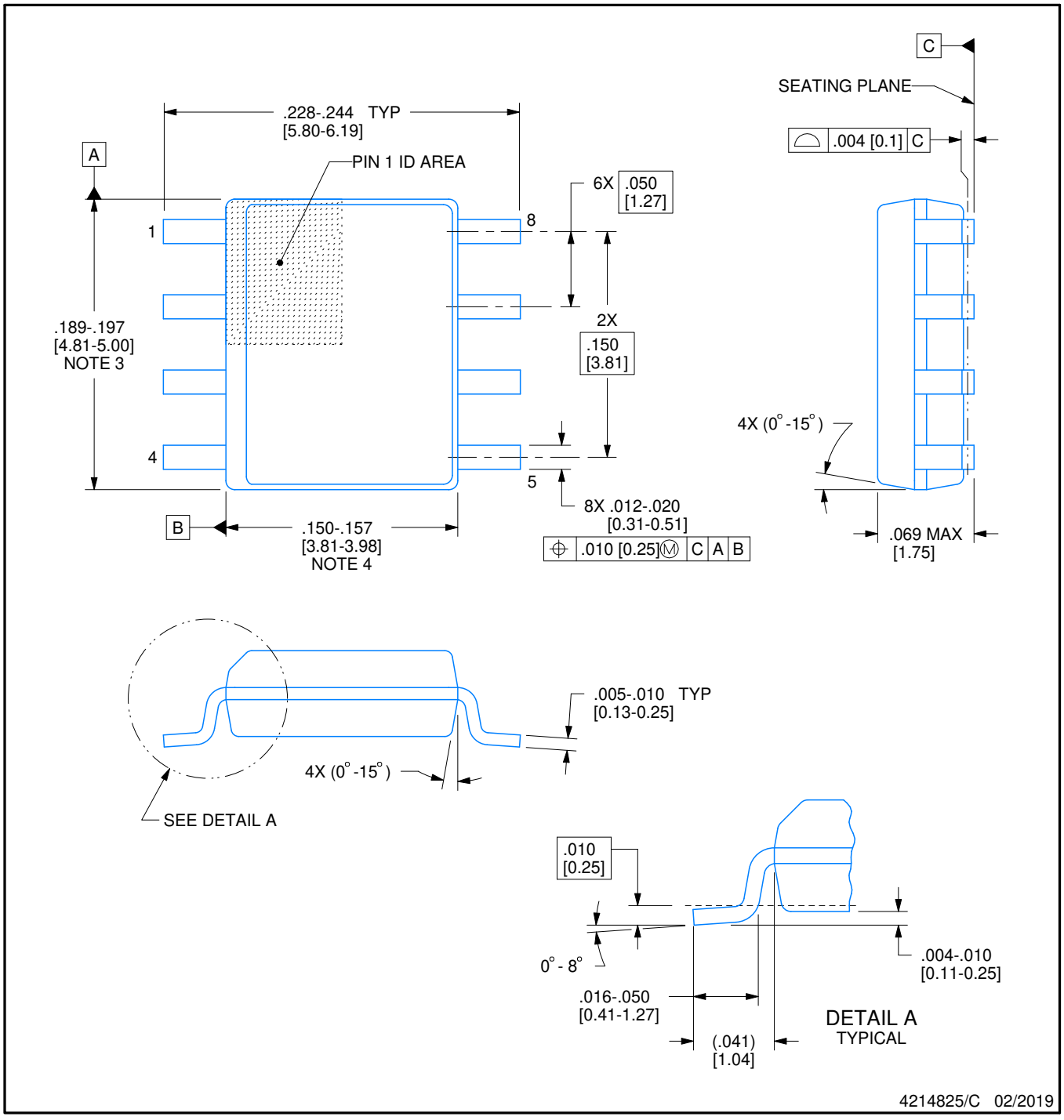


PACKAGE OUTLINE

D0008A

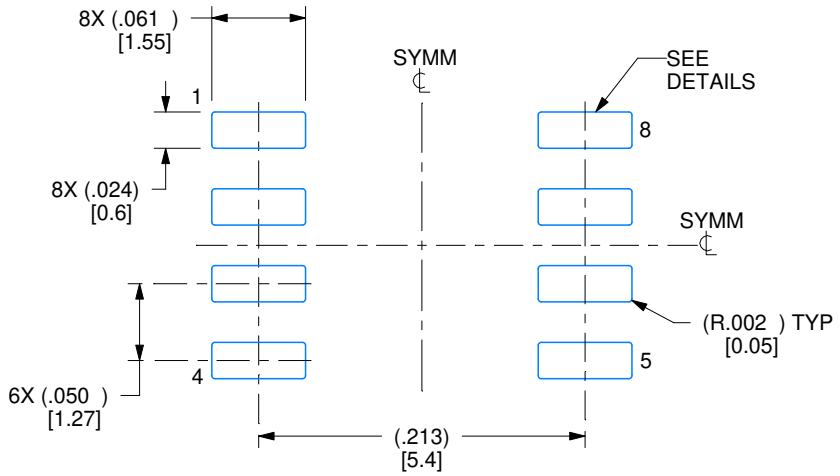
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

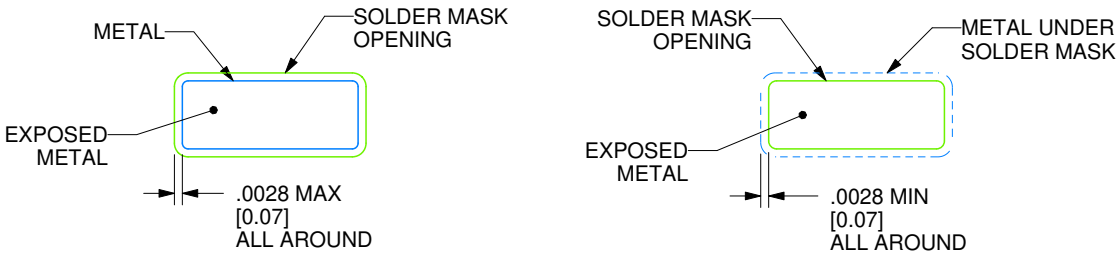


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

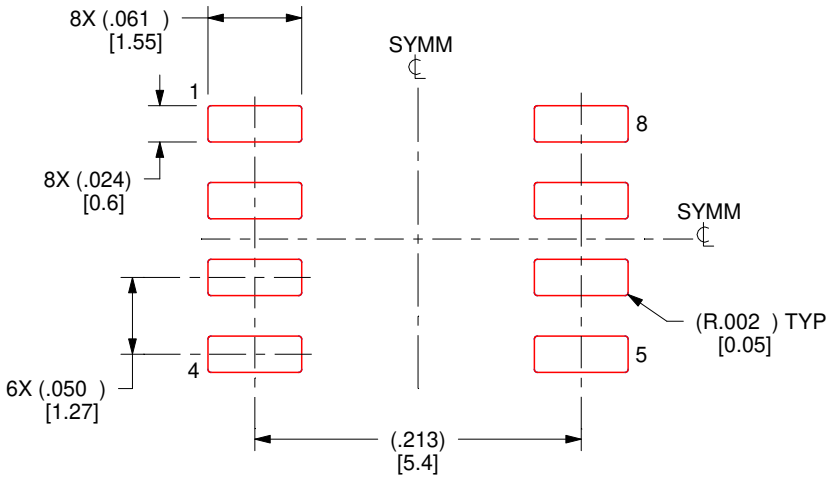
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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