Datasheet

# 3.0V to 20V, 6A 1ch Synchronous Buck Converter Integrated FET

## BD95500MUV

### General Description

BD95500MUV is a switching regulator with current capability of 6A and the ability to achieve low output voltages of 0.7V to 5.0V from a wide input voltage range of 3V to 20V. Built-in NMOS power transistors and implementation of Simple Light Load Mode technology (SLLM$^{TM}$) make this device highly-efficient. SLLM$^{TM}$ improves efficiency when the device is used is used with light load, providing high efficiency over a wider range of loads. The device also uses H$^3$Reg$^{TM}$, a ROHM proprietary control method, to achieve ultra-fast transient response against load changes. BD95500MUV is especially designed for various applications and is integrated with protection features such as soft-start, variable frequency, short circuit protection with timer latch, over voltage protection, and power good function.

### Features

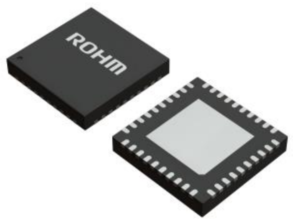
- H$^3$Reg$^{TM}$ DC/DC Converter Controller
- Selectable Simple Light Load Mode (SLLM$^{TM}$), and Forced Continuous Mode
- Built-in Thermal Shut Down (TSD), Under Voltage Lockout (UVLO), Adjustable Over-Current Protection (OCP), Over Voltage Protection (OVP), Short Circuit Protection (SCP)
- Soft Start Function to Minimize Rush Current during Startup
- Adjustable Switching Frequency (f=200KHz to600KHz)
- Built-in Output Discharge Function
- Tracking Function
- Integrated Boot Strap Diode
- Power Good Function

### Key Specifications

| | |
|---|---|
| Input Voltage Range: | 3.0V to 20V |
| Output Voltage Range: | 0.7V to 5.0V |
| Output Current: | 6.0A(Max) |
| High Side ON Resistance: | 50mΩ(Typ) |
| Low Side ON Resistance: | 50mΩ(Typ) |
| Standby Current: | 0μA (Typ) |
| Operating Temperature Range: | -10°C to +100°C |

### Package

W (Typ) x D (Typ) x H (Max)




**VQFN040V6060**
**6.00mm x 6.00mm x 1.00mm**

### Applications

Mobile PC, Desktop PC, LCD-TV, Digital Components, etc.

### Typical Application Circuit

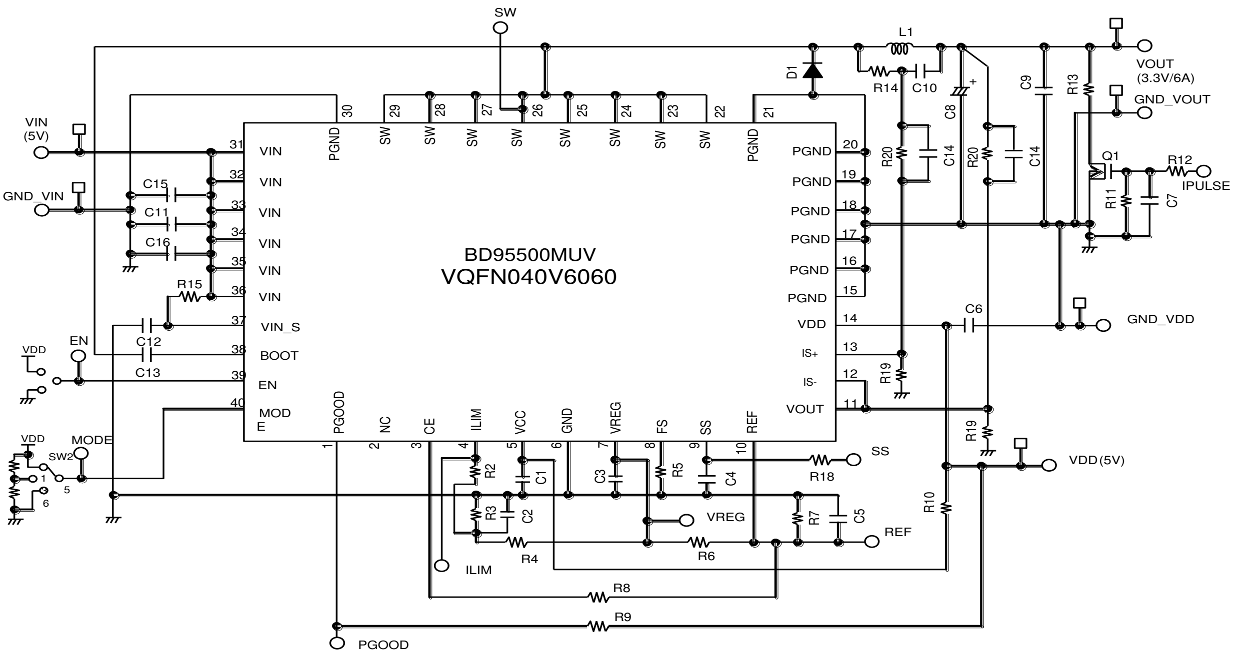



Figure 1. Typical Application Circuit

○Product structure：Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

## Pin Configuration

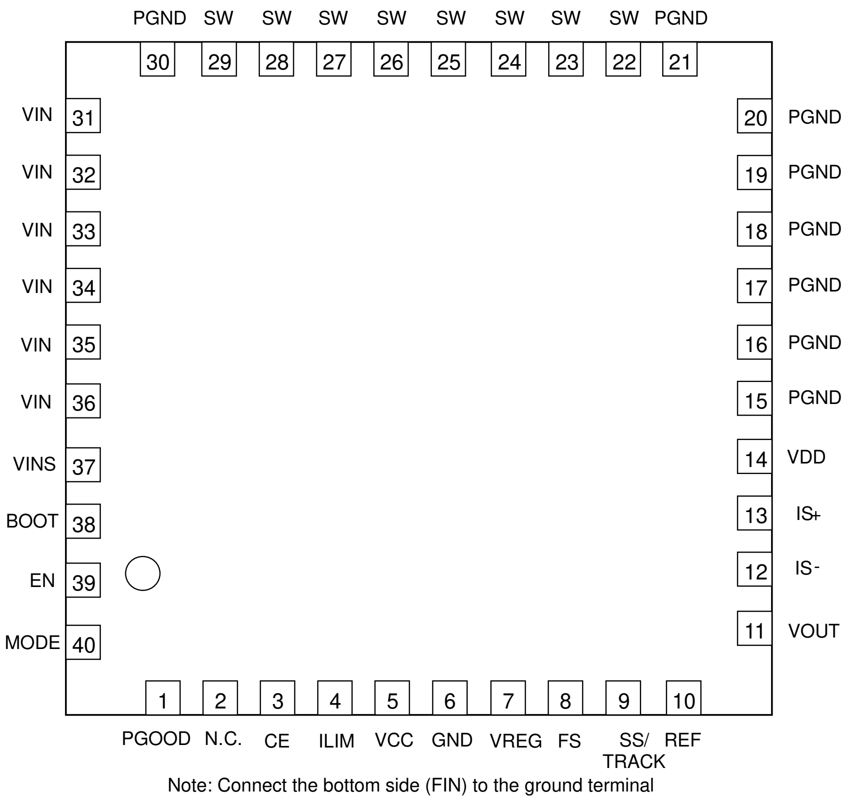



Figure 2. Pin Configuration

## Pin Description

(Function Table)

| Pin No. | Pin Name | Pin Function |
|---|---|---|
| 1 | PGOOD | Power good output (±10% window) |
| 2 | N.C. | No connection |
| 3 | CE | Ceramic capacitor reactive pin |
| 4 | ILIM | Current limit setting |
| 5 | VCC | Power supply input (control block) |
| 6 | GND | Sense ground |
| 7 | VREG | IC reference voltage (2.5V/500µA) |
| 8 | FS | Switching frequency adjustment (30kΩ to 100kΩ) |
| 9 | SS/TRACK | Soft start setting (w/ capacitor)/Tracking voltage input |
| 10 | REF | VOUT setting |
| 11 | VOUT | Output voltage sense |
| 12 | IS- | Current sense (-) |
| 13 | IS+ | Current sense (+) |
| 14 | VDD | FET driver power supply (5V input) |
| 15 to 21 | PGND | Power ground |
| 22 to 29 | SW | High side FET source |
| 30 | PGND | Power ground |
| 31 to 36 | VIN | Battery voltage input (3.3V to 20V input) |
| 37 | VINS | Battery voltage sense |
| 38 | BOOT | HG driver power supply |
| 39 | EN | Enable input (IC is ON when high) |
| 40 | MODE | Control mode selection<br>Low: Continuous Mode<br>High: SLLM™ |
| bottom | FIN | Substrate connection |

## Block Diagram

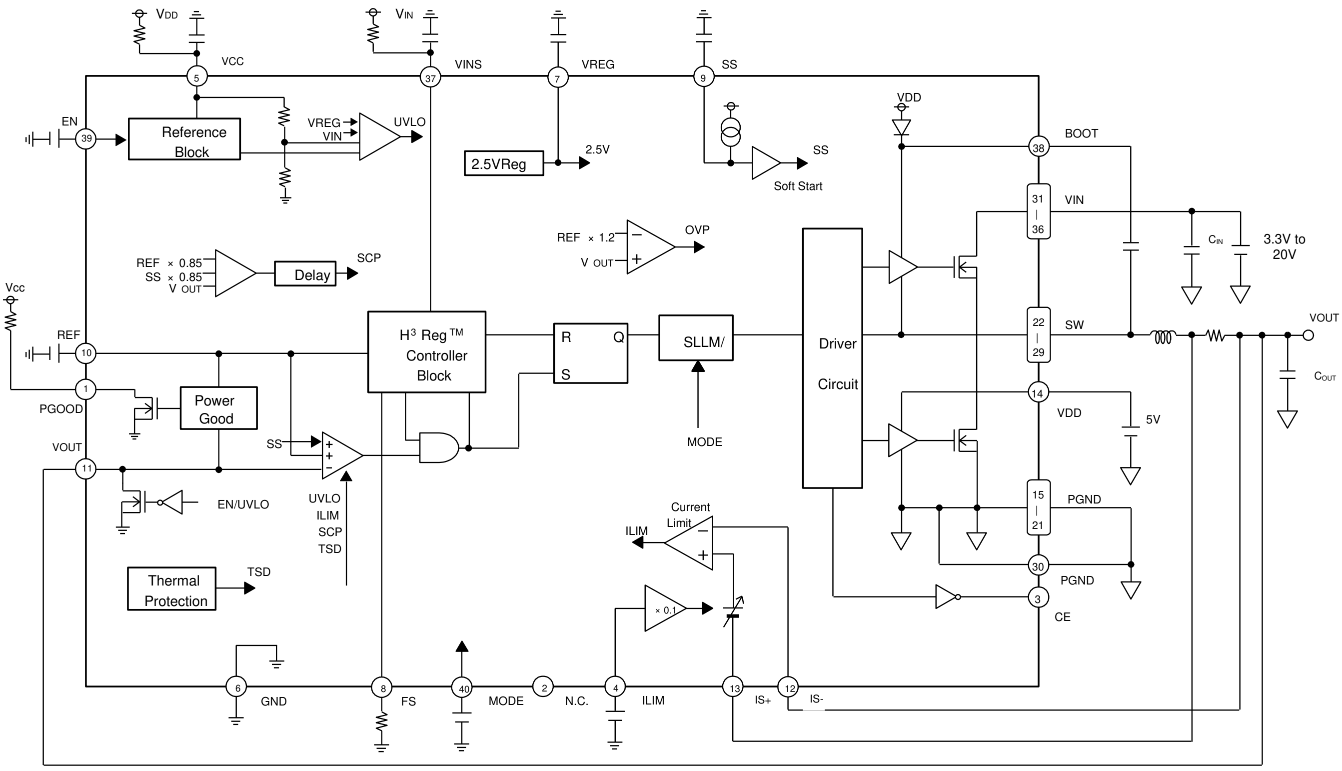



Figure 3. Block Diagram

## Description of Blocks

1. VCC (Pin 5)
   This is the power supply pin for the IC's internal circuits, except for the FET driver. The input supply voltage ranges from 4.5V to 5.5V. It is recommended that a 10Ω/0.1µF RC filter be connected to this pin and VDD.

2. EN (Pin 39)
   Enables or disables the switching regulator. When the voltage on this pin reaches 2.3V or higher, the internal switching regulator is turned ON. At voltages less than 0.8V, the regulator is turned OFF.

3. VDD (Pin 14)
   This is the power supply pin that drives the LOW side FET and the Boot-strap diode. It is recommended that a 1µF to 10µF bypass capacitor be connected to compensate for rush current during the FET ON/OFF transition.

4. VREG (Pin 7)
   This is the reference voltage output pin. The voltage at this pin is 2.5V, with 500µA of current ability. It is recommended to put a 0.22µF to 1µF capacitor (X5R or X7R) between VREG and GND (Pin 6). When REF is not adjusted from the external voltage supply, the REF voltage can be adjusted using the external resistor divider of VREG.

5. REF (Pin 10)
   This is the output voltage adjustment pin. The output voltage (0.7V to 2.0V) is determined by a resistor divider network from VREG pin. It is also very convenient for synchronizing the external voltage supply. Variations in the voltage level on this pin affect the output voltage (REF≈VOUT).

6. ILIM (Pin 4)
   BD95500MUV detects the voltage between IS+ pin and IS- pin and limits the output current (OCP). Voltage equivalent to 1/10 of the voltage at ILIM is the voltage drop of the external current sense resistor. A very low current sense resistor or inductor DCR can also be used for this platform.

7. SS/TRACK (Pin 9)
   This is the adjustment pin to set the soft start time. SS voltage is low during standby status. When EN is ON, the soft start time can be determined by the SS charge current and capacitor between SS-GND. Until SS reaches REF voltage, the output voltage is equivalent to SS voltage. And also this pin enables the tracking function. The output voltage keeps track of a power supply rail by connecting 10kΩ-resistor between the power supply rail and SS/TRACK pin.

## Description of Blocks - continued

8. VINS (Pin 37)
   The duty cycle, which controls the output voltage, is determined by the input voltage. In other words, the output voltage is affected by the input voltage. Therefore, when the voltage at VINS fluctuates, the output voltage also becomes unstable. Since the VINS line is also the input voltage of the switching regulator, stability depends on the impedance of the voltage supply. It is recommended to connect a bypass capacitor or RC filter that is suitable for the actual application.

9. FS (Pin 8)
   This pin adjusts the switching frequency with the use of a resistor. It is recommended that a resistor be connected across FS and GND (pin 6).The frequency range is from 200 kHz to 600 kHz.

10. IS+ (Pin 13), IS- (Pin 12)
    These pins are connected to both sides of the current sense resistors to detect output current. The voltage drop between IS+ and IS- is compared with the voltage equivalent to 1/10 of the voltage at ILIM. When this voltage drop hits the specified voltage level, the output voltage is turned OFF. Since the maximum input voltage to these pins is 2.7V, set the output voltage by the resistor divider network in case the output voltage is 2.7V or more.

11. BOOT (Pin 38)
    This is the voltage supply which drives the high side FET and a diode for the built-in Boot-strap function. The maximum absolute ratings are 30V (from GND) and 7V (from SW). The BOOT voltage swings between ($V_{IN}$+$V_{CC}$) and $V_{CC}$ during active operation.

12. PGOOD (Pin 1)
    This pin is the output pin for Power Good. It is an open drain pin and is recommended to be connected to a power supply through a pull-up resistor (about 100kΩ).

13. CE (Pin 3)
    This pin is for the ceramic capacitor. It is used to utilize low ESR capacitor for output capacitor.

14. MODE (Pin 40)
    This is the pin that can change the control mode. Low: continuous mode, High: SLLM™.

15. VOUT (Pin 11)
    This is the monitor pin for the output voltage. This IC forces the voltage at this pin to be almost equal to VOUT (REF≈VOUT). When output voltage required is 2V or more, output voltage can be set by the resistor divider network.

16. SW (Pin 22-29)
    This is a connection pin for the inductor. The voltage at this pin swings between VIN and GND. The trace from the output to the inductor should be as short and wide as possible.

17. VIN (Pin 31-36)
    This is the input power supply pin. The recommended input voltage is 3.3V to 20V. This pin should be bypassed directly to ground by a power capacitor.

18. PGND (Pin 15-21, 30)
    This is the power ground pin. The wiring pattern to this pin should be as short and wide as possible. Connect to the reverse side of IC when connecting to GND (6 pin).

## Absolute Maximum Ratings (Ta=25°C)

| Parameter | Symbol | Rating | Unit |
|---|---|---|---|
| Input Voltage 1 | $V_{CC}$ | 7 (Note 1) | V |
| Input Voltage 2 | $V_{DD}$ | 7 (Note 1) | V |
| Input Voltage 3 | $V_{IN}$ | 24 (Note 1) | V |
| BOOT Voltage | $V_{BOOT}$ | 30 | V |
| BOOT-SW Voltage | $V_{BOOT-SW}$ | 7 | V |
| LG Voltage | $V_{LG}$ | $V_{DD}$ | V |
| REF Voltage | $V_{REF}$ | $V_{CC}$ | V |
| Output Voltage | $V_{OUT}/V_{IS+}/V_{IS-}$ | $V_{CC}$ | V |
| ILIM/SS/FS/MODE Voltage | $V_{ILIM}/V_{SS}/V_{FS}/V_{MODE}$ | $V_{CC}$ | V |
| VREG Voltage | $V_{REG}$ | $V_{CC}$ | V |
| EN Input Voltage | $V_{EN}$ | 7 | V |
| Output Current (Average) | $I_{SW}$ | 6 | A |
| Power Dissipation 1 | Pd1 | 0.54 (Note 2) | W |
| Power Dissipation 2 | Pd2 | 1.00 (Note 3) | W |
| Power Dissipation 3 | Pd3 | 3.77 (Note 4) | W |
| Power Dissipation 4 | Pd4 | 4.66 (Note 5) | W |
| Operating Temperature Range | Topr | -10 to +100 | °C |
| Storage Temperature Range | Tstg | -55 to +150 | °C |
| Junction Temperature | Tjmax | +150 | °C |

(Note 1) Not to exceed Pd, ASO, and Tjmax=150°C.
(Note 2) Reduce by 4.3mW/°C for Ta over 25°C (not mounted on heat radiation board )
(Note 3) Reduce by 8.0mW/°C for Ta over 25°C (when mounted on a 1 layer 70.0mm x 70mm x 1.6mm Glass-epoxy. (Copper foil area : 0mm$^2$))
(Note 4) Reduce by 30.1mW/°C for Ta over 25°C (when mounted on a 4 layer 70.0mm x 70mm x 1.6mm Glass-epoxy PCB. (1st and 4th layer copper foil area : 20.2mm$^2$, 2nd and 3rd layer copper foil area : 5505mm$^2$))
(Note 5) Reduce by 37.3mW/°C for Ta over 25°C (when mounted on a 4 layer 70.0mm x 70mm x 1.6mm Glass-epoxy. (All copper foil area : 5505mm$^2$))
**Caution:** Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

## Recommended Operating Conditions (Ta=25°C)

| Parameter | Symbol | Rating | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| Input Voltage 1 | $V_{CC}$ | 4.5 | 5.5 | V |
| Input Voltage 2 | $V_{DD}$ | 4.5 | 5.5 | V |
| Input Voltage 3 | $V_{IN}$ | 3.0 | 20 | V |
| BOOT Voltage | $V_{BOOT}$ | 4.5 | 25 | V |
| SW Voltage | $V_{SW}$ | -0.7 | +20 | V |
| BOOT-SW Voltage | $V_{BOOT-SW}$ | 4.5 | 5.5 | V |
| MODE Input Voltage | $V_{MODE}$ | 0 | 5.5 | V |
| EN Input Voltage | $V_{EN}$ | 0 | 5.5 | V |
| Output Adjustable Voltage | $V_{REF}$ | 0.7 | 2.0 | V |
| IS Input Voltage | $V_{IS+}/V_{IS-}$ | 0.7 | 2.7 | V |
| Minimum ON Time | $t_{ON\_MIN}$ | - | 200 | nsec |

## Electrical Characteristics

(Unless otherwise noted, Ta=25°C, $V_{CC}$=5V, $V_{DD}$=5V, $V_{EN}$ / $V_{MODE}$=5V, $V_{IN}$=12V, $V_{REF}$=1.8V, $R_{FS}$=68kΩ)

| Parameter | Symbol | Limit Min | Limit Typ | Limit Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| [Whole Device] | | | | | | |
| VCC Bias Current | $I_{CC}$ | - | 1200 | 2000 | μA | |
| VIN Bias Current | $I_{IN}$ | - | 100 | 200 | μA | |
| VCC Standby Current | $I_{CCSTB}$ | - | 0 | 10 | μA | $V_{EN}$＝0V |
| VIN Standby Current | $I_{INSTB}$ | - | 0 | 10 | μA | $V_{EN}$＝0V |
| EN Low Voltage | $V_{ENLOW}$ | GND | - | 0.8 | V | |
| EN High Voltage | $V_{ENHIGH}$ | 2.3 | - | 5.5 | V | |
| EN Bias Current | $I_{EN}$ | - | 7 | 10 | μA | |
| VREG Voltage | $V_{REG}$ | 2.475 | 2.500 | 2.525 | V | $I_{VREG}$=0 to 500μA, Ta=-10°C to +100°C |
| [Under Voltage Locked Out ] | | | | | | |
| VCC Threshold Voltage | $V_{CC\_UVLO}$ | 4.1 | 4.3 | 4.5 | V | $V_{CC}$:Sweep Up |
| VCC Hysteresis Voltage | $dV_{CC\_UVLO}$ | 100 | 160 | 220 | mV | $V_{CC}$:Sweep Down |
| VIN Threshold Voltage | $V_{IN\_UVLO}$ | 2.4 | 2.6 | 2.8 | V | $V_{IN}$:Sweep Up |
| VIN Hysteresis | $dV_{IN\_UVLO}$ | 100 | 160 | 220 | mV | $V_{IN}$:Sweep Down |
| VREG Threshold Voltage | $V_{REG\_UVLO}$ | 2.0 | 2.2 | 2.4 | V | $V_{REG}$:Sweep Up |
| VREG Hysteresis Voltage | $dV_{REG\_UVLO}$ | 100 | 160 | 220 | mV | $V_{REG}$:Sweep Down |
| [$H^3Reg^{TM}$ Control Block] | | | | | | |
| ON Time | $t_{ON}$ | 400 | 500 | 600 | nsec | |
| Maximum ON Time | $t_{ONMAX}$ | - | 3 | 6.0 | μsec | |
| Minimum OFF Time | $t_{OFFMIN}$ | - | 450 | 550 | nsec | |
| [FET Block] | | | | | | |
| High Side ON Resistance | $R_{HGHON}$ | - | 50 | 80 | mΩ | |
| Low Side ON Resistance | $R_{HGLON}$ | - | 50 | 80 | mΩ | |
| [SCP Block] | | | | | | |
| SCP Start up Voltage | $V_{SCP}$ | REF x 0.60 | REF x 0.70 | REF x 0.80 | V | |
| Delay Time | $t_{SCP}$ | - | 1.0 | 2.0 | ms | |
| [OVP Block] | | | | | | |
| OVP Detect Voltage | $V_{OVP}$ | REF x 1.16 | REF x 1.2 | REF x 1.24 | V | |
| [Soft Start Block] | | | | | | |
| Charge Current | $I_{SS}$ | 2 | 4 | 6 | μA | |
| Discharge Current | $I_{DIS}$ | 0.5 | 1.0 | 2.0 | μA | |
| Standby Voltage | $V_{SS\_STB}$ | - | - | 50 | mV | |
| [Over-Current Protection Block] | | | | | | |
| Current Limit Threshold 1 | $V_{ILIM1}$ | 40 | 50 | 60 | mV | $V_{ILIM}$=0.5V , Ta=-10°C to +100°C |
| Current Limit Threshold 2 | $V_{ILIM2}$ | 160 | 200 | 240 | mV | $V_{ILIM}$=2.0V |
| [VOUT Setting] | | | | | | |
| VOUT Offset Voltage 1 | $V_{OUTOFF1}$ | REF-10m | REF | REF+10m | V | Ta=-10°C to +100°C |
| VOUT Bias Current | $I_{VOUT}$ | -100 | 0 | +100 | nA | |
| REF Bias Current | $I_{REF}$ | -100 | 0 | +100 | nA | |
| IS+ Input Current | $I_{IS+}$ | -1 | 0 | +1 | μA | $V_{IS+}$=1.8V |
| IS- Input Current | $I_{IS-}$ | -1 | 0 | +1 | μA | $V_{IS-}$=1.8V |
| [MODE Block] | | | | | | |
| SLLM Threshold | $V_{THSLLM}$ | $V_{CC}$-0.5 | - | $V_{CC}$ | V | |
| Forced Continuous Mode | $V_{THCONT}$ | GND | - | 0.5 | V | |
| Input Impedance | $R_{MODE}$ | - | 400 | - | kΩ | |
| [Power Good Block] | | | | | | |
| VOUT Power Good Low Voltage | $V_{OUTPL}$ | REF x 0.85 | REF x 0.90 | REF x 0.95 | V | |
| VOUT Power Good High Voltage | $V_{OUTPH}$ | REF x 1.05 | REF x 1.10 | REF x 1.15 | V | |

**Typical Performance Curves**

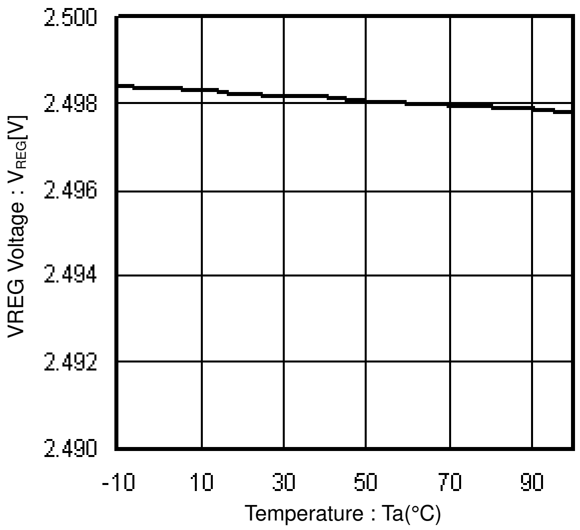



Figure 4. VREG Voltage vs Temperature

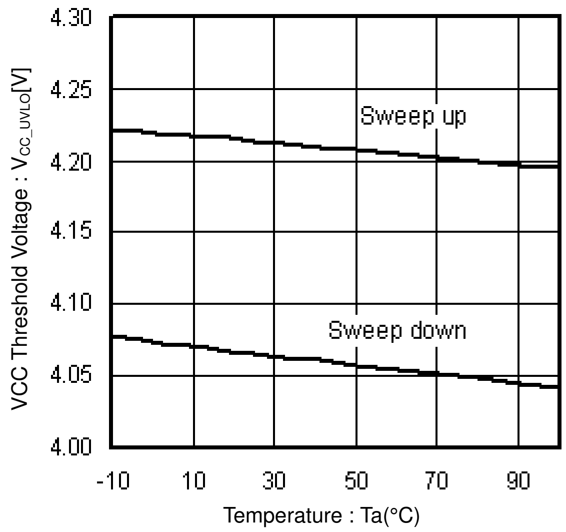



Figure 5. VCC Threshold Voltage vs Temperature

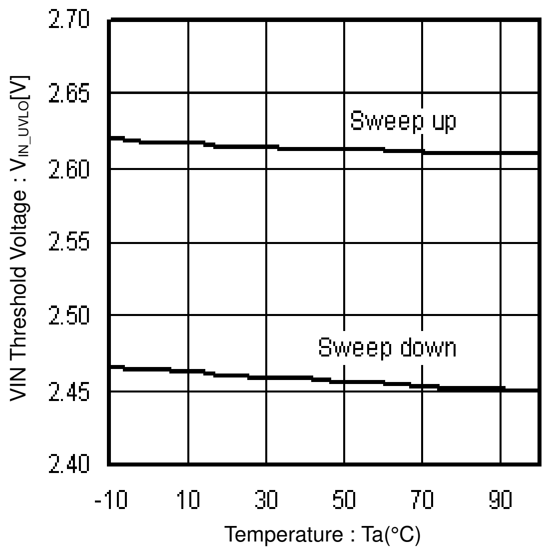



Figure 6. VIN Threshold Voltage vs Temperature

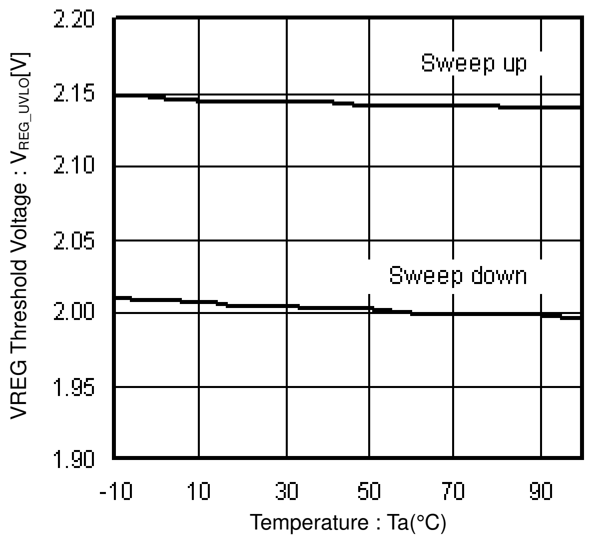



Figure 7. VREG Threshold Voltage vs Temperature

**Typical Performance Curves – continued**

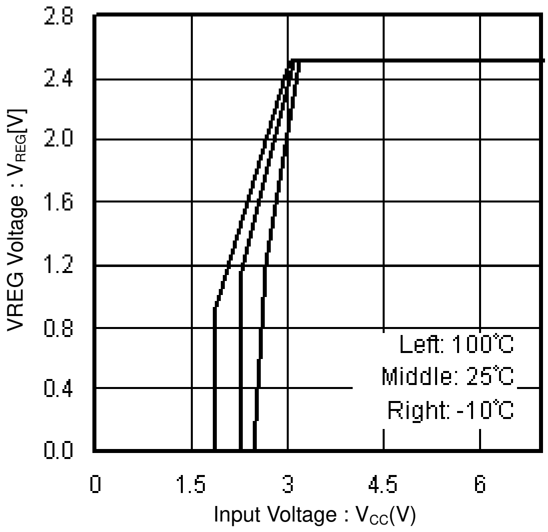



Figure 8. VREG Voltage vs Input Voltage

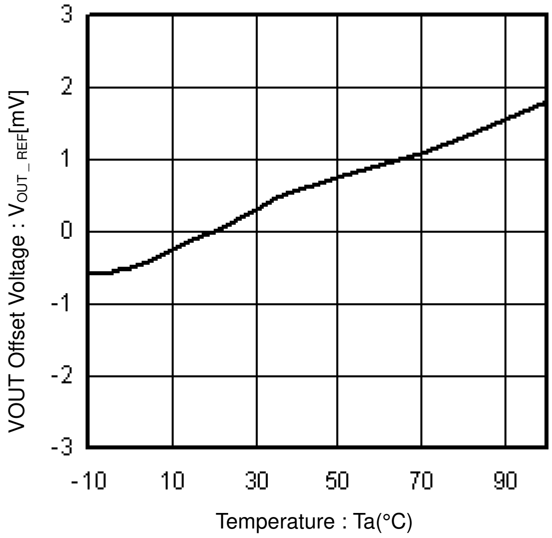



Figure 9. VOUT Offset Voltage vs Temperature

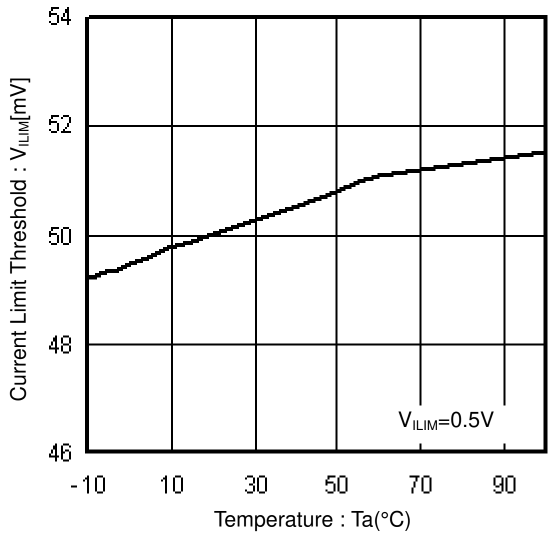



Figure 10. Current Limit Threshold vs Temperature

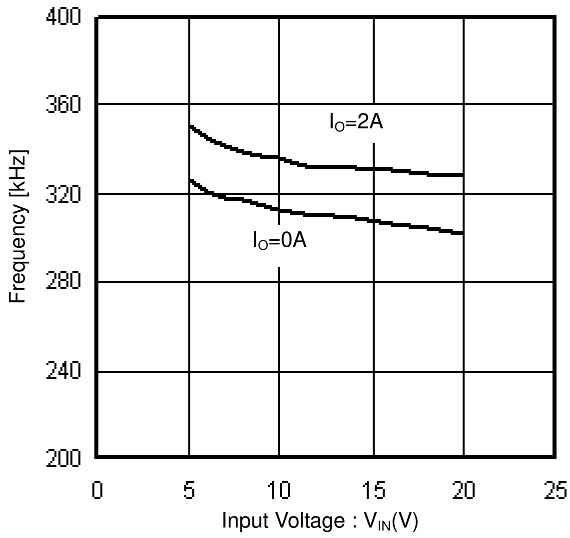



Figure 11. Frequency vs Input Voltage

**Typical Performance Curves – continued**

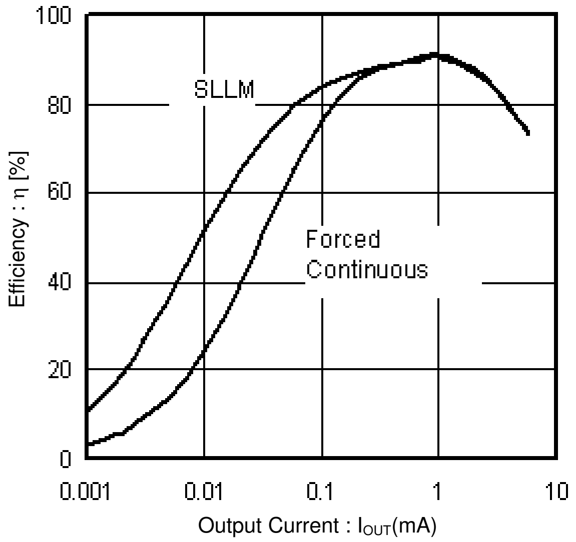



Figure 12. Efficiency vs Output Current
($V_{IN}$=7V, $V_{OUT}$=1.5V)

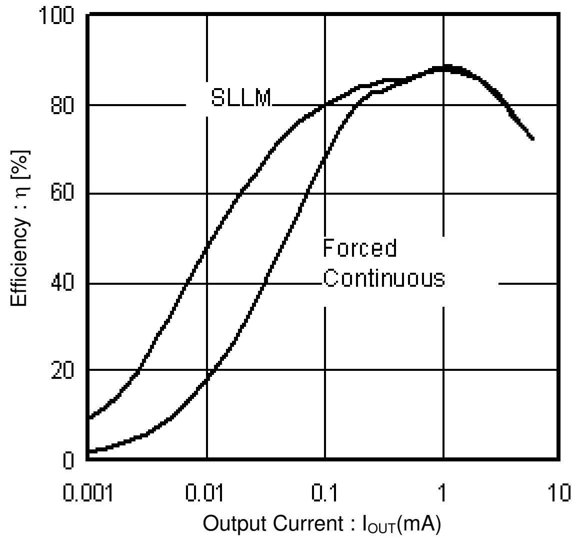



Figure 13. Efficiency vs Output Current
($V_{IN}$=12V, $V_{OUT}$=1.5V)

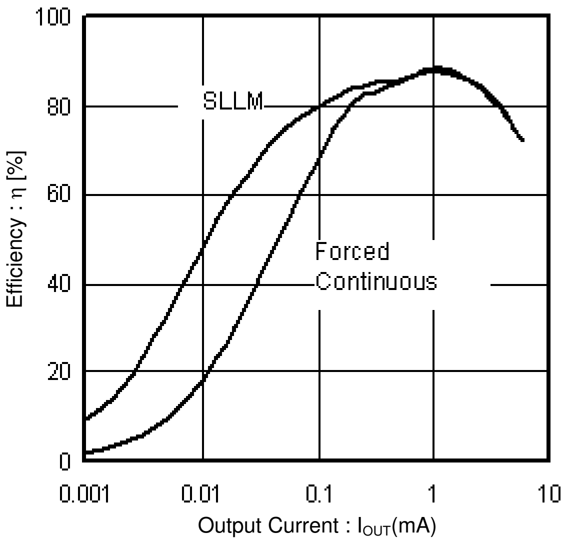



Figure 14. Efficiency vs Output Current
($V_{IN}$=19V, $V_{OUT}$=1.5V)

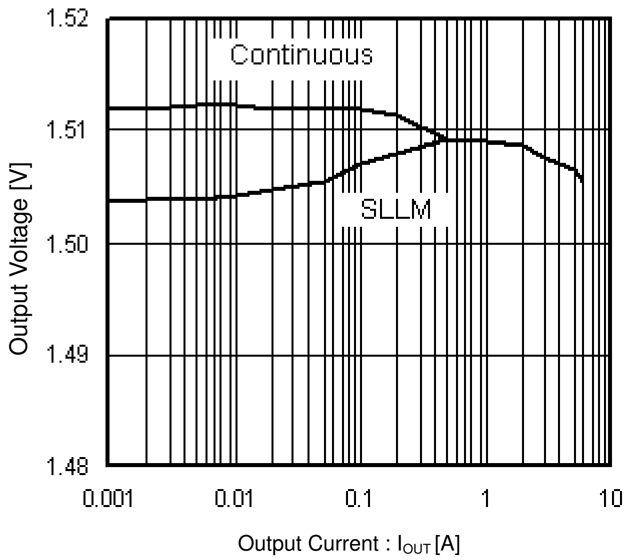



Figure 15. Output Voltage vs
Output Current

**Typical Performance Curves – continued**

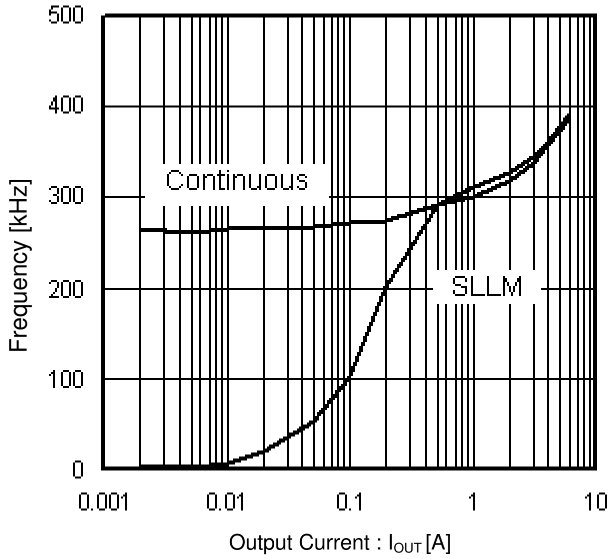



Figure 16. Frequency vs Output Current

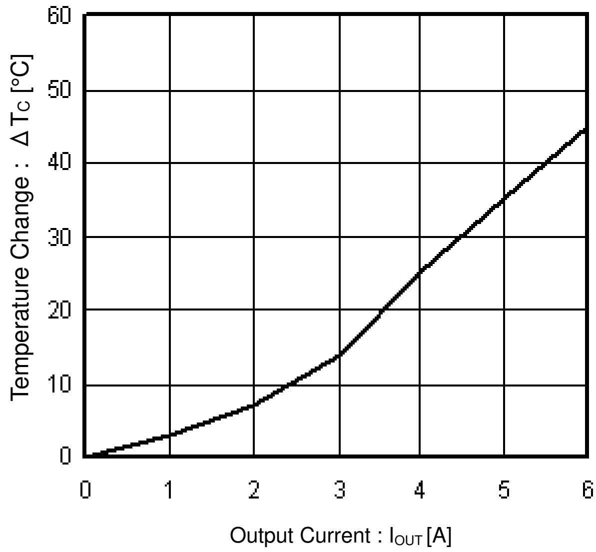



Figure 17. Temperature Change vs Output Current

**Typical Waveforms**

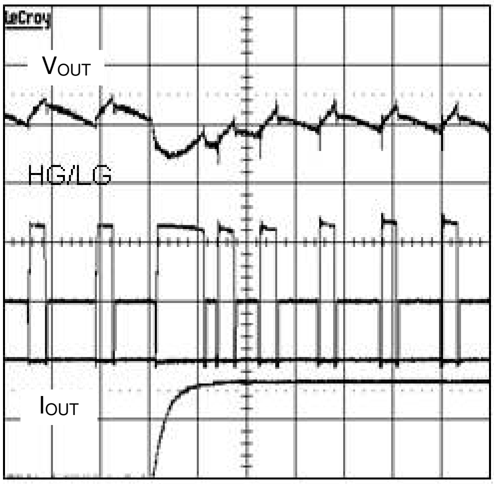



Figure 18. Transient Response
($V_{IN}$=7V)

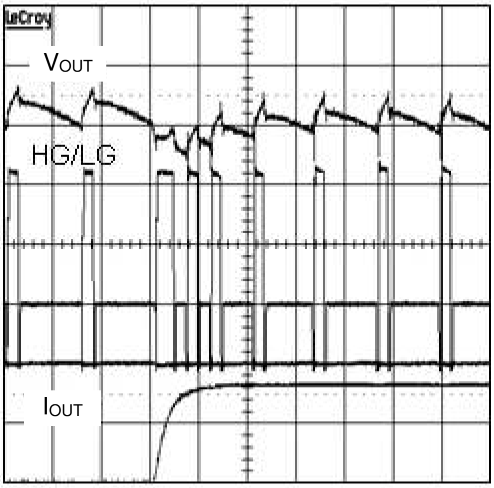



Figure 19. Transient Response
($V_{IN}$=12V)

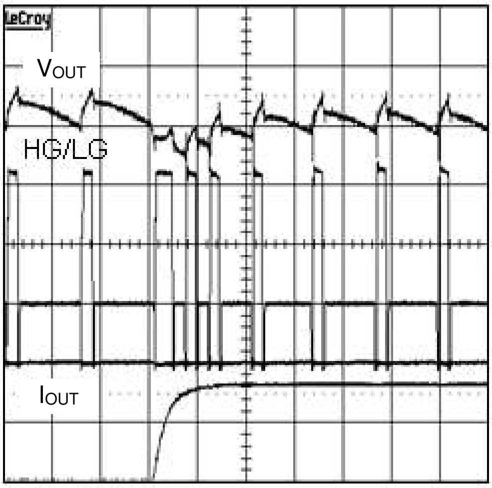



Figure 20. Transient Response
($V_{IN}$=19V)

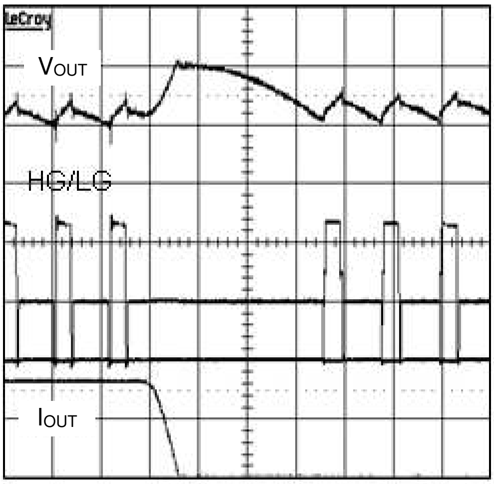



Figure 21. Transient Response
($V_{IN}$=7V)

**Typical Waveforms – continued**

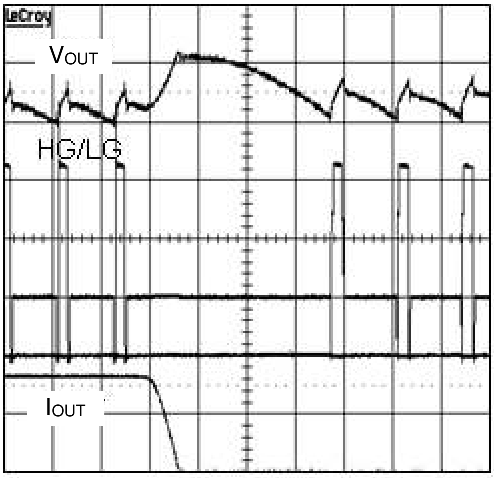



Figure 22. Transient Response
($V_{IN}$=12V)

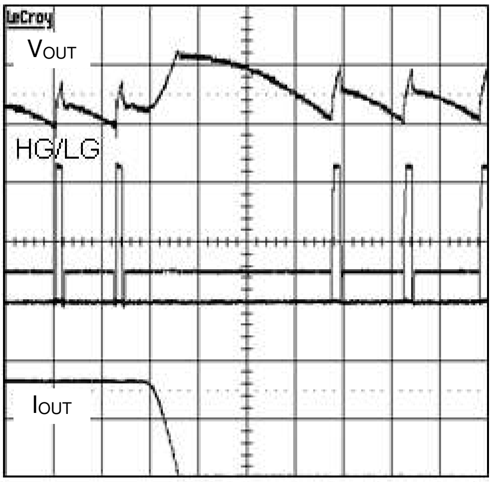



Figure 23. Transient Response
($V_{IN}$=19V)

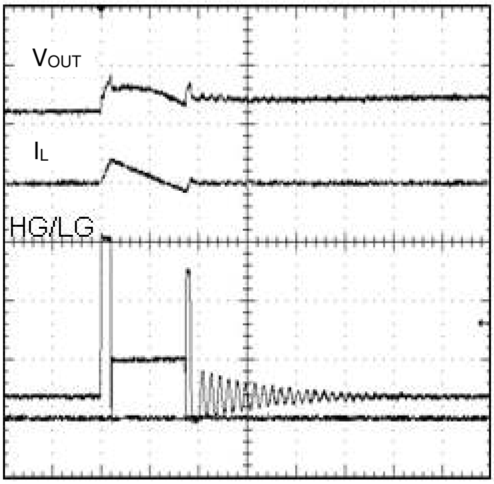



Figure 24. SLLM Mode
($I_{OUT}$=0A)

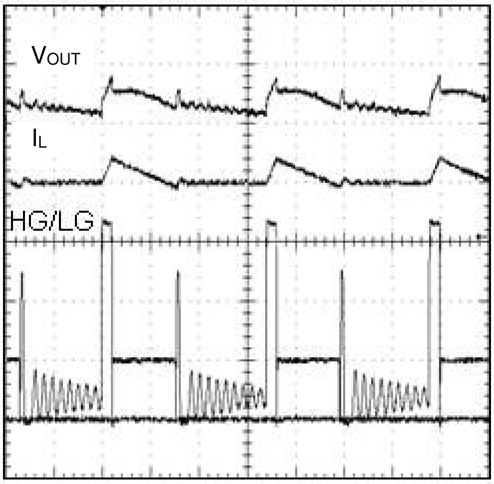



Figure 25. SLLM Mode
($I_{OUT}$=0.4A)

**Typical Waveforms – continued**

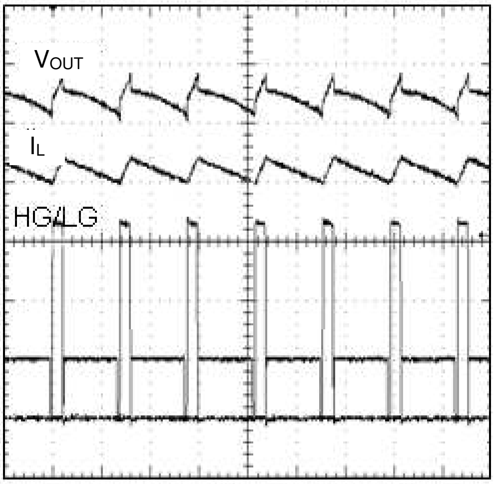



Figure 26. SLLM Mode
($I_{OUT}$=1A)

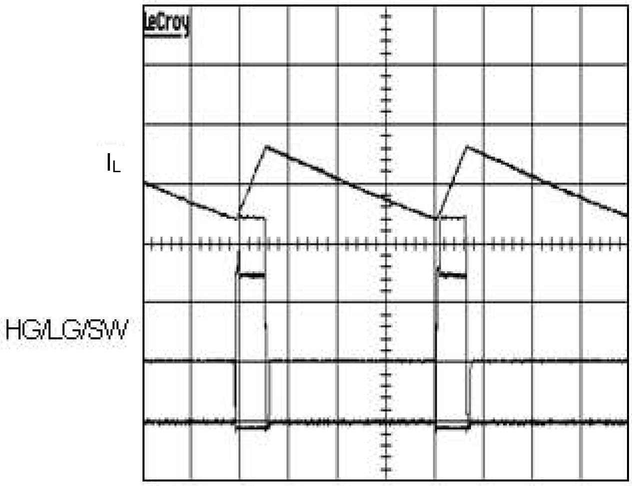



Figure 27. Continuous Mode
($I_O$=0A)

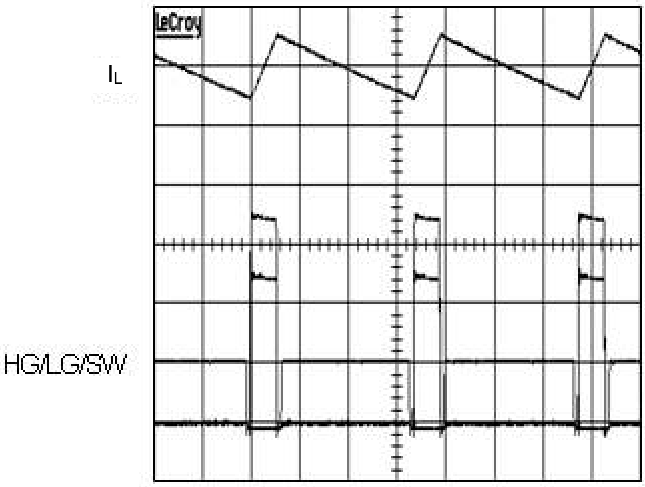



Figure 28. Continuous Mode
($I_O$=4A)

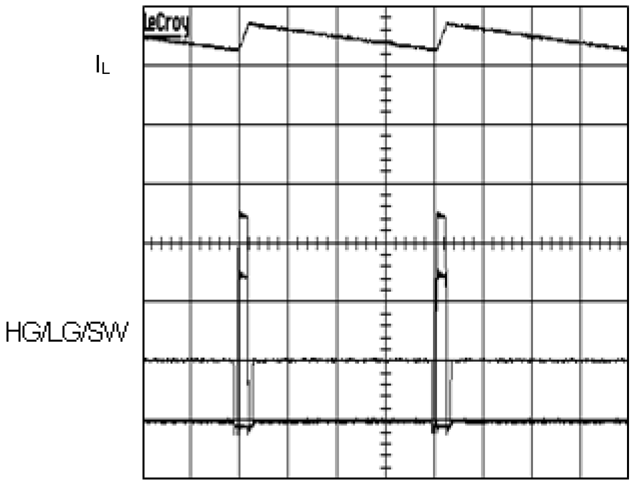



Figure 29. OCP Status
($I_O$=5A)

**Typical Waveforms – continued**

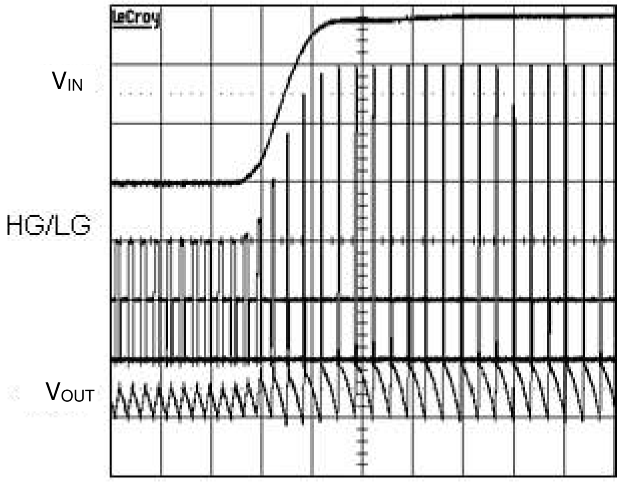



Figure 30. VIN Change
(5V to 19V)

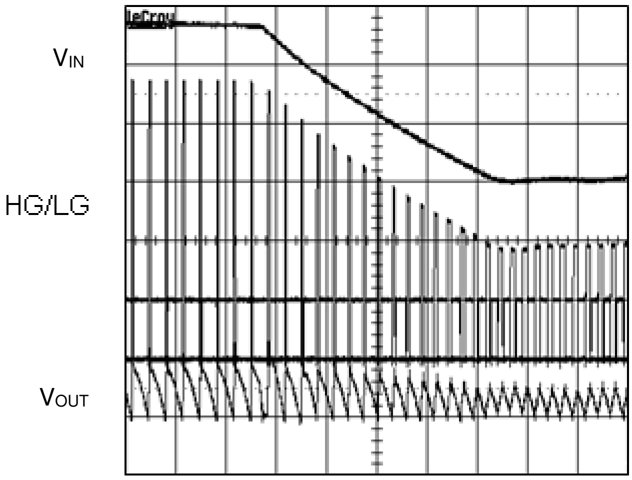



Figure 31. VIN Change
(19V to 5V)

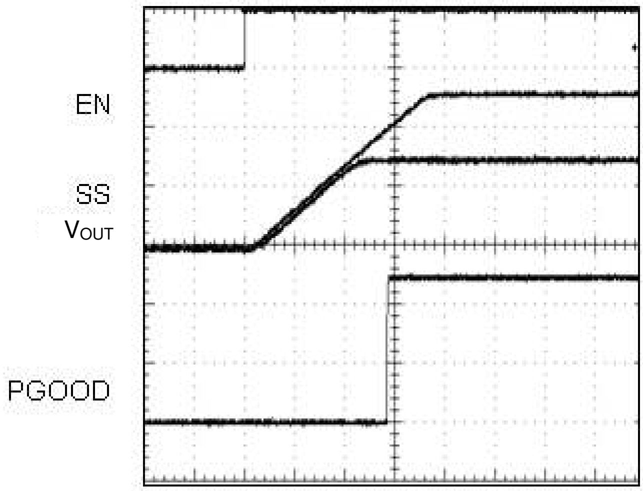


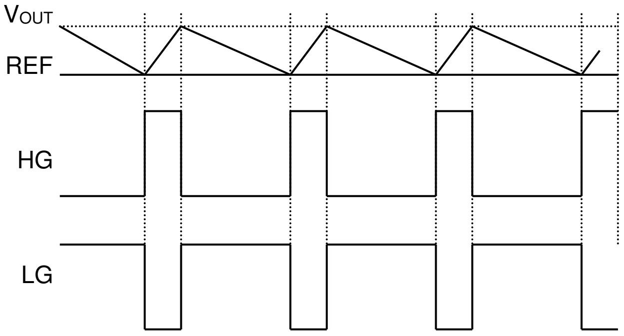

Figure 32. EN Wake Up

## Application Information

**1. Explanation of Operation**

The BD95500MUV is a switching regulator that incorporates ROHM's proprietary H³Reg™ CONTROLLA control system. When $V_{OUT}$ drops suddenly due to changes in load, the system quickly restores the output voltage by extending the $t_{ON}$ time interval. This improves the regulator's transient response. When light-load mode is activated, the IC employs the Simple Light Load Mode (SLLM™) controller, further improving system efficiency.

H³Reg™ control
(Normal Operation)

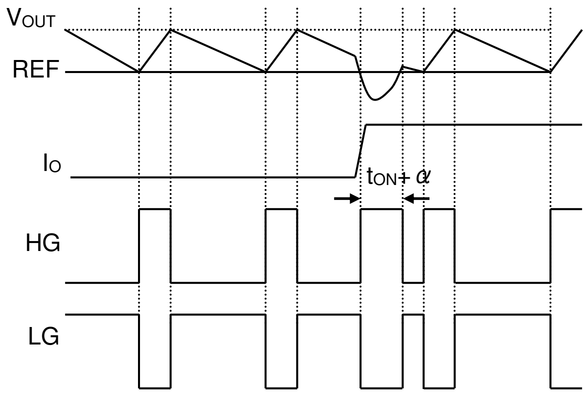



When $V_{OUT}$ falls to a threshold voltage (REF), the H³Reg™ CONTROLLA system is activated.

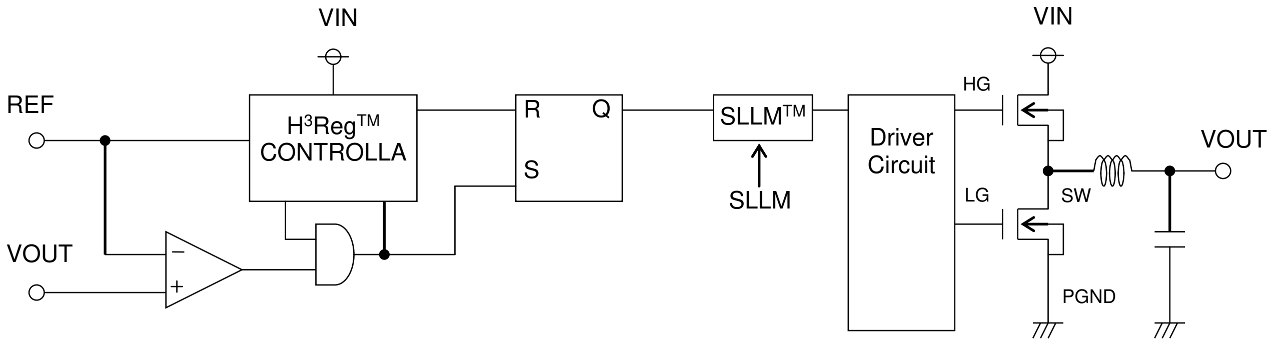
$$t_{ON} = \frac{REF}{V_{IN}} \times \frac{1}{f} [\mathrm{sec}] \quad \cdot\cdot\cdot (1)$$

High Gate output is determined by the above equation.

(Rapid Changes in Load)

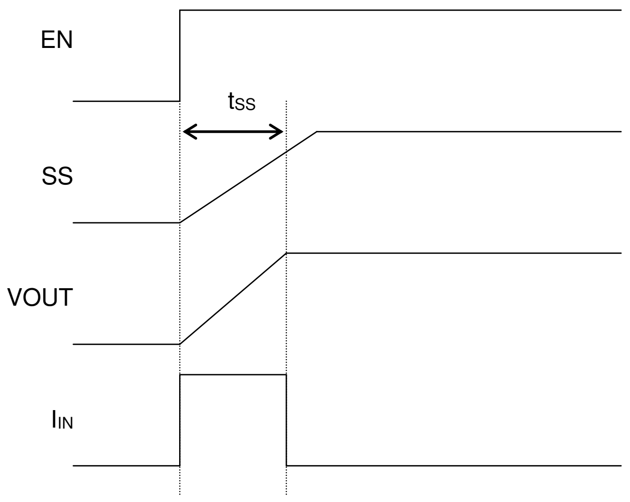



When $V_{OUT}$ drops due to a sudden change in load and $V_{OUT}$ remains below REF after the preprogrammed $t_{ON}$ time interval has elapsed, the system quickly restores $V_{OUT}$ by extending the $t_{ON}$ time, thereby improving transient response.



**2. Timing Chart**

(1) Soft Start Function




Soft start function is enabled when EN pin is set to HIGH. Current control circuitry takes effect at startup, yielding a moderate "ramping start" in output voltage. Soft start timing and incoming current are given by equation (2) and (3) below:

Soft Start Time

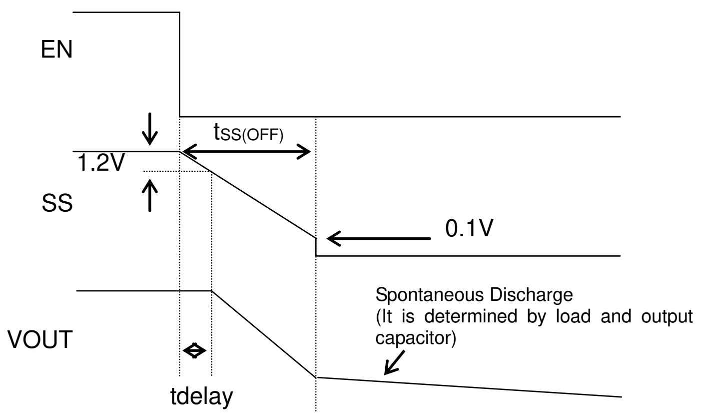
$$t_{SS} = \frac{REF \times C_{SS}}{4\mu A(typ)} \quad [\mathrm{sec}] \quad \cdots (2)$$

Rush Current

$$I_{IN}(ON) = \frac{C_O \times V_{OUT}}{t_{SS}} \quad [A] \quad \cdots (3)$$

Where:
$C_{SS}$ is the Soft start capacitor
$C_O$ is the Output capacitor

(2) Soft Stop Function




Soft stop is enabled when EN pin is set to LOW. Current circuitry control takes effect at startup, yielding a gradually falling output voltage. Soft stop time and rush current are given by equation (4) below.

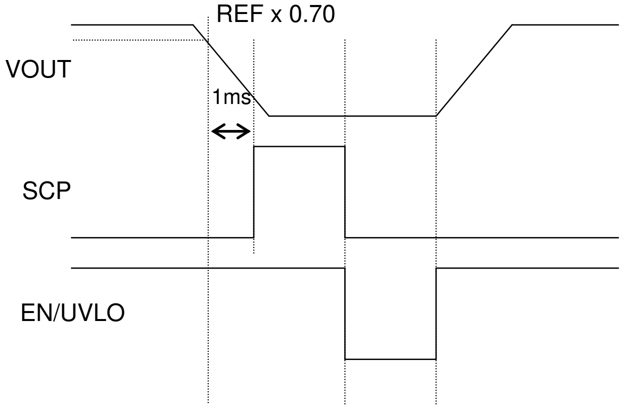
Soft Stop Time

$$t_{SS(OFF)} = \frac{(REF + 2V_{BE}) \times C_{SS}}{1\mu A(typ)} \quad [\mathrm{sec}] \quad \cdots (4)$$

$$\Delta V_{SS} = 1.2 \quad [V] \quad (typ)$$

$$tdelay = \frac{C_{SS}}{1\mu A(typ)} \quad [\mathrm{sec}] \quad \cdots (5)$$

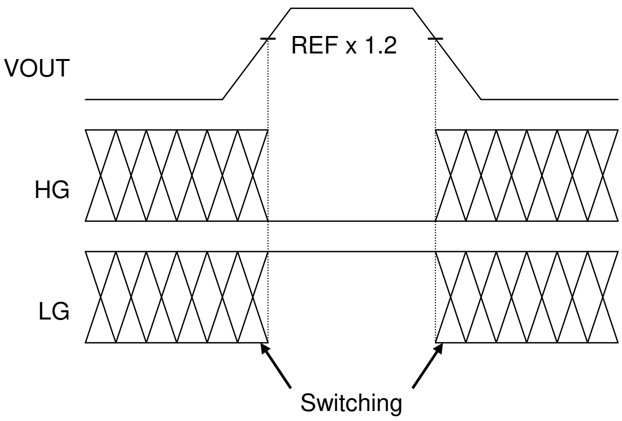
(3) Timer Latch Type Short Circuit Protection




When output voltage (IS-) falls to REF x 0.7 or less, the SCP comparator inside the IC is enabled. If the High state continues for 1ms or more (programmed time inside IC), the IC goes OFF. It can be restored either by reconnecting the EN pin or disabling UVLO.

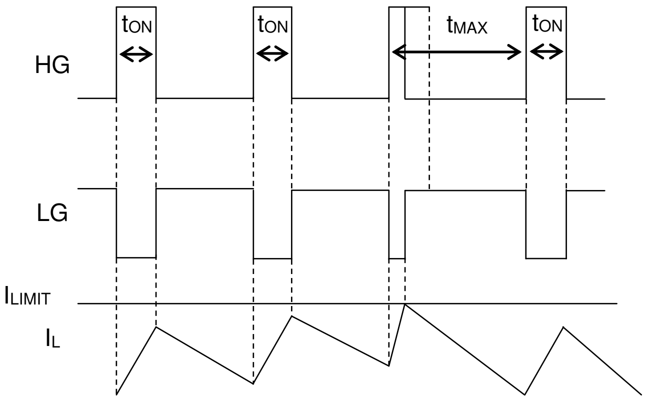
**Timing Chart – continued**

(4) Output Over Voltage Protection



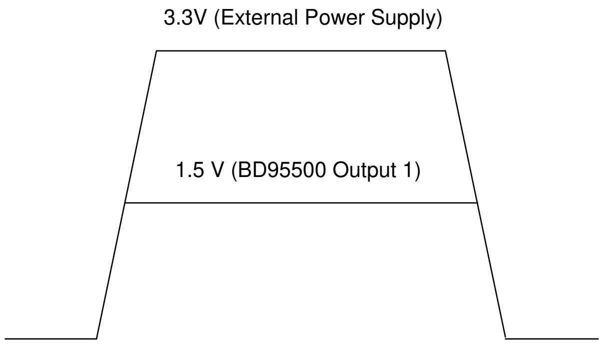

When the output reaches or exceeds REF x 1.2, the output over voltage protection is triggered, turning the low-side FET completely ON to reduce the output (LG=High, HG=Low). When the output falls, it returns to the standard operation.

(5) Over-Current Protection Circuit




During normal operation, the High Gate becomes HIGH during the ON time $t_{ON}$ (P.15) when VOUT becomes less than REF. However, when the inductor current $I_L$ exceeds OCP setting current ($I_{LIMIT}$), HG becomes LOW. After the max ON time $t_{MAX}$, HG becomes HIGH again if the output voltage is lower than the specific voltage level and $I_L$ is lower than $I_{LIMIT}$ level.

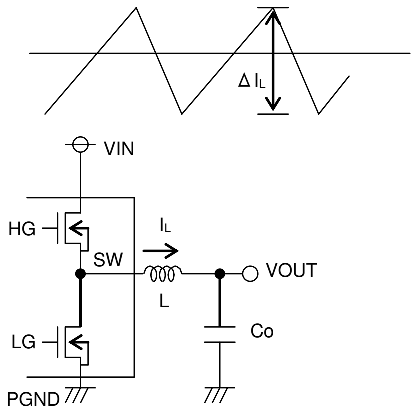
(6) Synchronous Operation with External Power Supply




These power supply sequences are realized to connect SS pin to other power supply output through the resistance (10kΩ).

### 3. External Component Selection

(1) Inductor (L) Selection



Output Ripple Current

The inductor's value directly influences the output ripple current. As indicated by equation (4) below, the greater the inductance or switching frequency, the lower the ripple current:

$$\Delta I_L = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{L \times V_{IN} \times f} \quad [A] \quad \cdots (4)$$

The proper output ripple current setting is about 30% of the maximum output current.

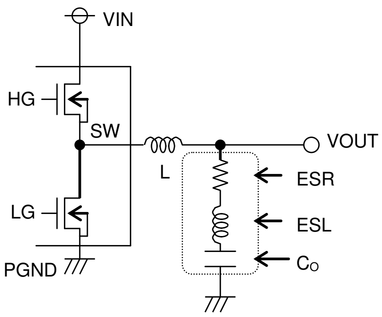
$$\Delta I_L = 0.3 \times I_{OUTMAX} \quad [A] \quad \cdots (5)$$

$$L = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{L \times V_{IN} \times f} \quad [H] \quad \cdots (6)$$

where:
$\Delta I_L$ is the output ripple current
$f$ is the switch frequency

(a) Passing a current larger than the inductor's rated current will cause magnetic saturation in the inductor and decreases system efficiency. In selecting the inductor, be sure to allow enough margin to assure that the peak current does not exceed the inductor's rated current value.
(b) To minimize possible inductor damage and maximize efficiency, choose an inductor with a low DCR and ACR.

(2) Output Capacitor ($C_O$) Selection



Output Capacitor

When determining the proper output capacitor, be sure to consider the equivalent series resistance (ESR) and equivalent series inductance (ESL) required to set the output ripple voltage to 20mV or more.
When selecting the limit of the inductor, be sure to allow enough margin for the output voltage.
Output ripple voltage is determined by equation (7) below.

$$\Delta V_{OUT} = \Delta I_L \times ESR + ESL \times \Delta I_L / t_{ON} \quad \cdots (7)$$

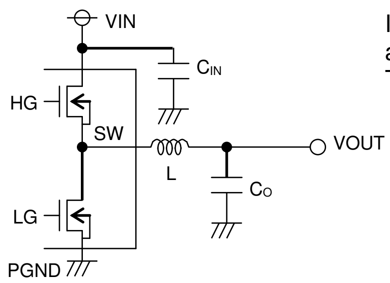
Where:
$\Delta I_L$ is the output ripple current
$ESR$ is the $C_O$ equivalent series resistance
$ESL$ is the equivalent series inductance

Please give consideration to the conditions of equation (8) below for output capacity, bear in mind that the output rise time must be established within the soft start time frame.

$$C_O \le \frac{t_{SS} \times (Limit - I_{OUT})}{V_{OUT}} \quad \cdots (8)$$

where:
$t_{SS}$ is the Soft start time (See formula (2) in P16)
Limit is the over-current detection (See formula (10)(11) in P19)
Note: Improper capacitor may cause startup malfunctions

(3) Input Capacitor ($C_{IN}$) Selection



Input Capacitor

In order to prevent extreme over-current conditions, the input capacitor must have a low enough ESR to fully support a large ripple in the output.
The formula for ripple current $I_{RMS}$ is given by equation (9) below.

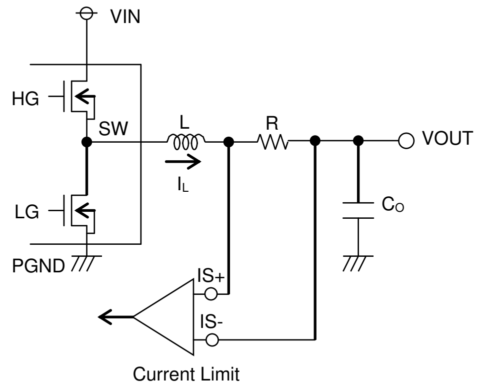
$$I_{RMS} = I_{OUT} \times \frac{\sqrt{V_{IN}(V_{IN} - V_{OUT})}}{V_{IN}} \quad [A] \quad \cdots (9)$$

$$\text{Where } V_{IN} = 2 \times V_{OUT}, I_{RMS} = \frac{I_{OUT}}{2}$$

A low-ESR capacitor is recommended to reduce ESR loss and maximize efficiency.

**External Component Selection – continued**

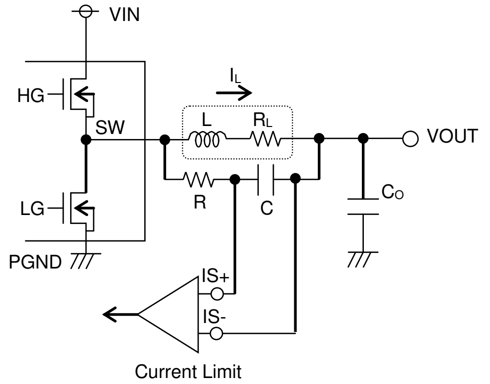
(4) Setting Detection Resistance




The over-current protection function detects the peak value of the output ripple current.
This parameter (setting value) is determined by equation (10) below.

$$I_{LIMIT} = \frac{V_{ILIM} \times 0.1}{R} \quad [A] \quad \cdot\cdot\cdot (10)$$

where:
$V_{ILIM}$ is the ILIM voltage
$R$ is the detection resistance

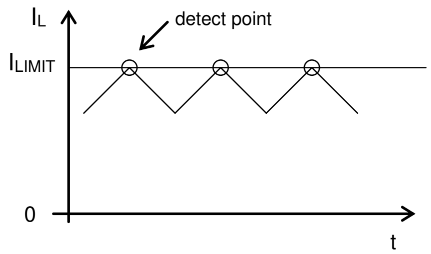



When the over-current protection is detected by the DCR of coil L, this parameter (setting value) is determined by equation (11) below.

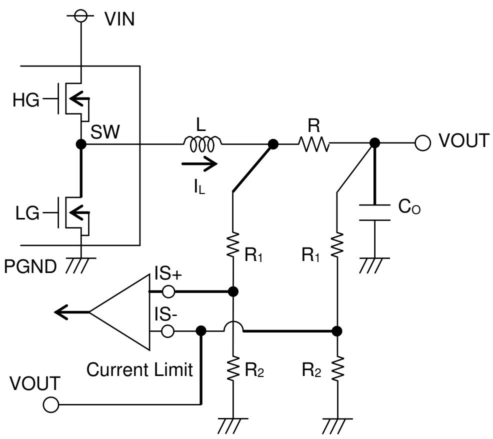
$$I_{LIMIT} = V_{ILIM} \times 0.1 \times \frac{R \times C}{L} \quad [A] \quad \cdot\cdot\cdot (11)$$

$$(R_L = \frac{L}{R \times C})$$

where:
$V_{ILIM}$ is the ILIM voltage
$R_L$ is the DCR value of coil




As soon as the voltage drop between IS+ and IS-, which is generated by the inductor current, reaches a specific threshold, the gate voltage of the high side MOSFET becomes low.
Since the peak voltage of the inductor ripple current is detected, this operation can sense high current ripple operation caused by inductance saturated rated current and lead to high reliable systems.



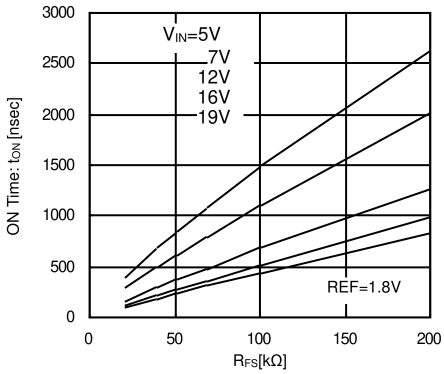

When the output voltage is 2.7V or more, use the setup like in the left figure for setting output voltage for IS+ and IS-.
According to the setting value above, $I_{LIMIT}$ setting current is proportion to the resistor divider ratio.

$$I_{LIMIT} = \frac{R_1 + R_2}{R_1} \times \frac{V_{ILIM} \times 0.1}{R} \quad [A] \quad \cdot\cdot\cdot (12)$$

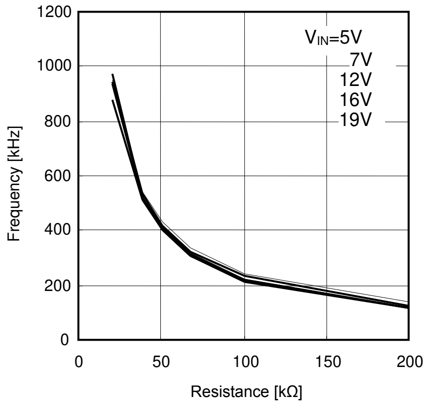
where:
$V_{ILIM}$ is the ILIM voltage
R is the detection resistance

**External Component Selection – continued**

(5) Frequency Adjustment




Exchange to Frequency Characteristic

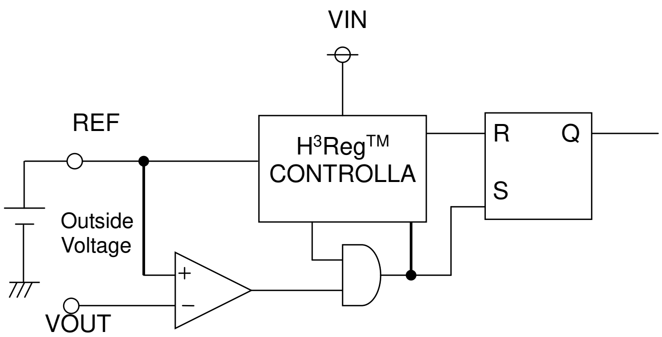



The On Time ($t_{ON}$) at steady state is determined by the resistor value connected to FS pin.
But actually SW rising time and falling time are the effects of the influence of the external MOSFET gate capacitance and switching time. This leads to an increase in $t_{ON}$ and slight lowering of the total frequency.
When $t_{ON}$, input voltage and $V_{REF}$ voltage are known, the switching frequency can be determined by the following equation:

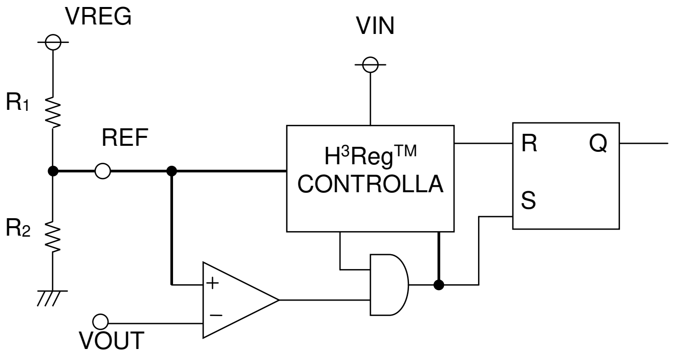
$$f = \frac{V_{REF}}{V_{IN} \times t_{ON}} \quad \cdot\cdot\cdot (13)$$

Additionally, when output current is around 0A in continuous mode, this “dead time” also has an effect on $t_{ON}$, further lowering the switching frequency. Confirm the switching frequency by measuring the current through the coil (at the point where current does not flow backwards) during normal operation.

(6) Setting Standard Voltage (REF)




It is possible to set the reference voltage (REF) with external power supply voltage.



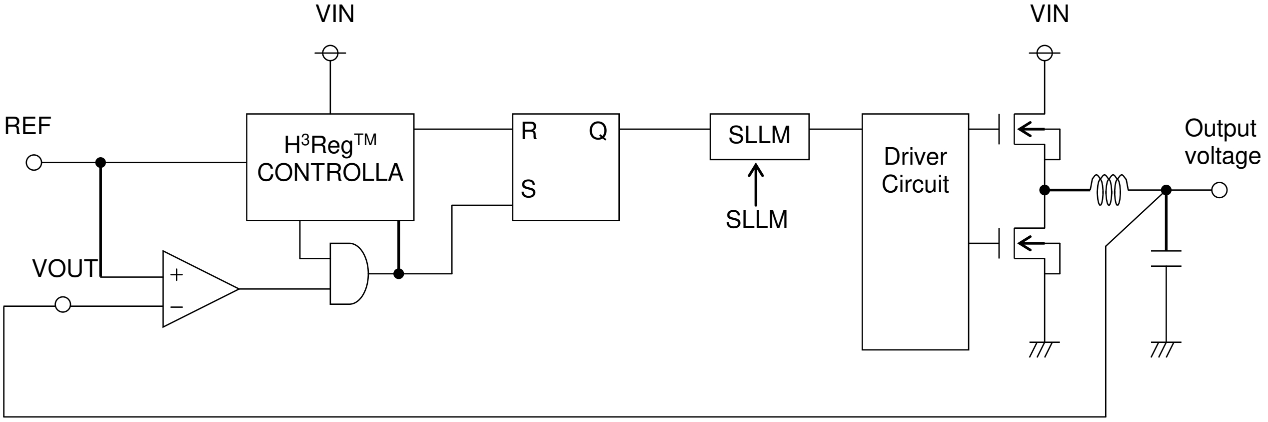

It is possible to set the reference voltage (REF) by the resistance division value from $V_{REG}$ in case it is not set with an external power supply.

$$REF = \frac{R_2}{R_1 + R_2} \times V_{REG} \quad [V] \quad \cdot\cdot\cdot (14)$$

**External Component Selection – continued**

(7) Setting Output Voltage

This IC is operated wherein the output voltage is almost equal to REF voltage (REF≈VOUT).
It is also operated that the output voltage is feed back to FB pin in case the output voltage is 0.7V to 2.0V.



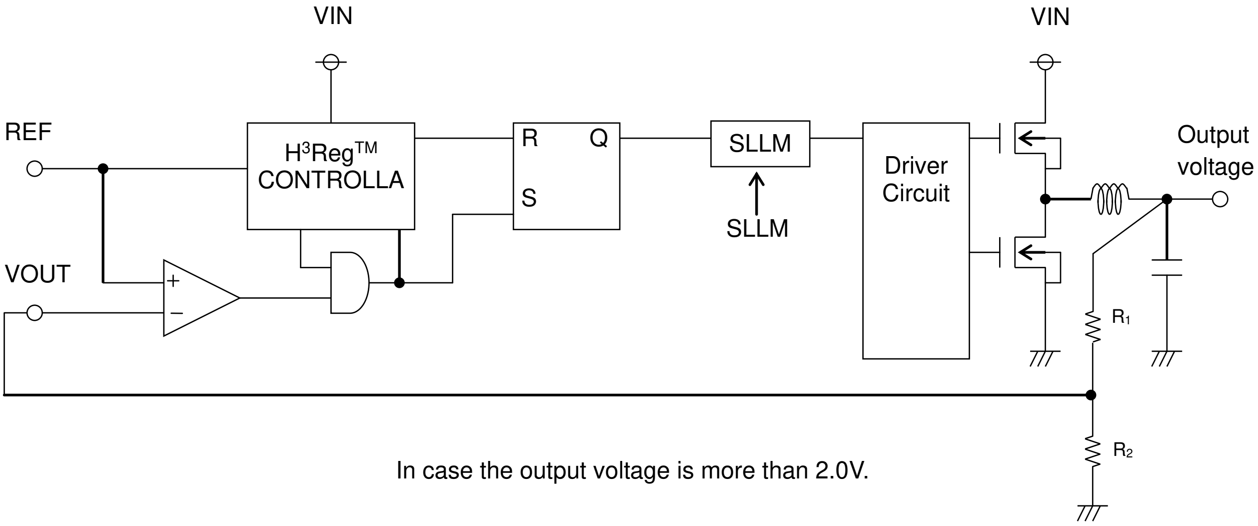

In case the output voltage range is 0.7V to 2.0V.

Additionally, in case the output voltage is more than 2.0V, the output voltage is feed back to VOUT pin through a resistor divider network.

$$OutputVoltage \approx \frac{R_1 + R_2}{R_2} \times REF \quad [V] \qquad \cdots (15)$$

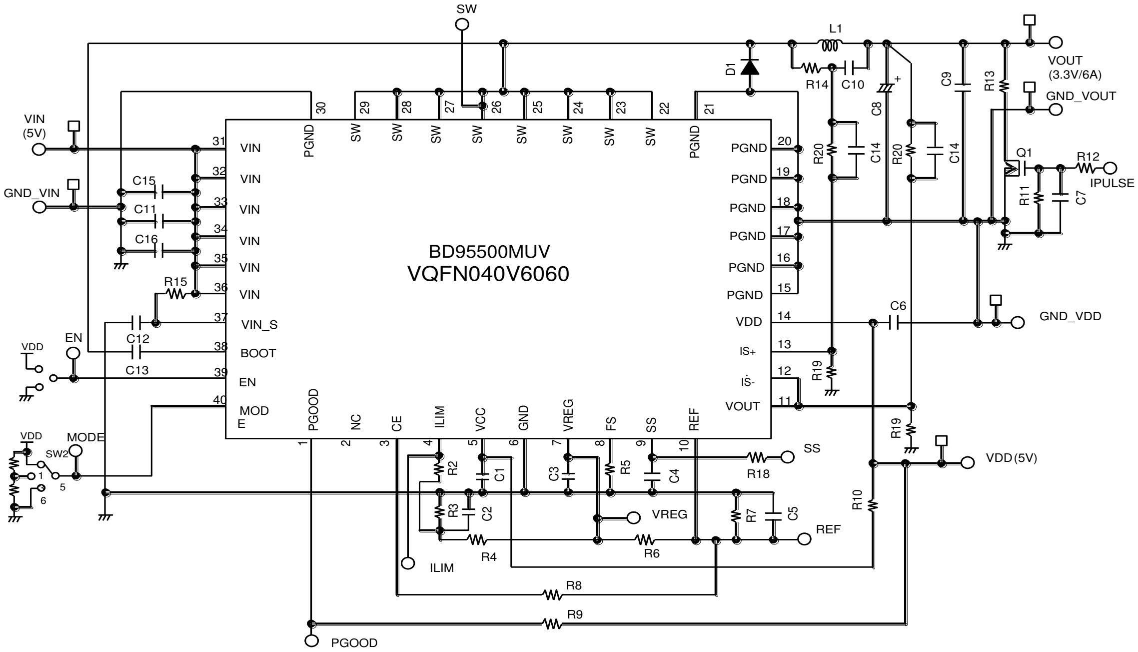
And then the frequency is also in proportion to the divided ratio.

$$f = \frac{R_2}{R_1 + R_2} \times \frac{REF}{V_{IN} + t_{ON}} \qquad \cdots (16)$$




In case the output voltage is more than 2.0V.

## 4. Evaluation Board Circuit (Frequency=300kHz Continuous/SLLM Circuit Example)

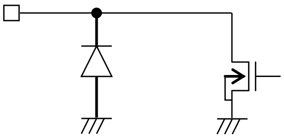



## 5. Evaluation Board Parts List

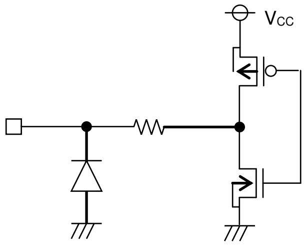
| Part No | Value | Company | Part name | Part No | Value | Company | Part name |
|---|---|---|---|---|---|---|---|
| U1 | - | ROHM | BD95500MUV | R17 | 100kΩ | ROHM | MCR03 Series |
| D1 | - | ROHM | RB051L-40 | R18 | 1kΩ | ROHM | MCR03 Series |
| L1 | 4.3µH | Sumida | CDEP105NP-4R3MC-88 | R19 | 10kΩ | ROHM | MCR03 Series |
| Q1 | - | - | - | R20 | 12kΩ | ROHM | MCR03 Series |
| R1 | 0Ω | ROHM | MCR03 Series | C1 | 0.1µF | MURATA | GRM18 Series |
| R2 | 0Ω | ROHM | MCR03 Series | C2 | 100pF | MURATA | GRM18 Series |
| R3 | 100kΩ | ROHM | MCR03 Series | C3 | 0.47µF | MURATA | GRM18 Series |
| R4 | 150kΩ | ROHM | MCR03 Series | C4 | 1000pF | MURATA | GRM18 Series |
| R5 | 68kΩ | ROHM | MCR03 Series | C5 | 1000pF | MURATA | GRM18 Series |
| R6 | 100kΩ | ROHM | MCR03 Series | C6 | 10µF | MURATA | GRM21 Series |
| R7 | 150kΩ | ROHM | MCR03 Series | C7 | - | MURATA | GRM18 Series |
| R8 | - | ROHM | MCR03 Series | C8 | 220µF | SANYO or something | functional high polymer |
| R9 | 100kΩ | ROHM | MCR03 Series | C9 | 10µF | MURATA | GRM21 Series |
| R10 | 10Ω | ROHM | MCR03 Series | C10 | 0.1µF | MURATA | GRM18 Series |
| R11 | - | ROHM | MCR03 Series | C11 | 10µF | KYOSERA or something | CM316B106M25A |
| R12 | 10Ω | ROHM | MCR03 Series | C12 | 0.1µF | MURATA | GRM18 Series |
| R13 | | ROHM | MCR03 Series | C13 | 0.1µF | MURATA | GRM18 Series |
| R14 | 1kΩ | ROHM | MCR03 Series | C14 | 100pF | MURATA | GRM18 Series |
| R15 | 1kΩ | ROHM | MCR03 Series | C15 | 10µF | KYOSERA or something | CM316B106M25A |
| R16 | 100kΩ | ROHM | MCR03 Series | C16 | 0.1µF | MURATA | GRM18 Series |

## I/O Equivalent Circuit

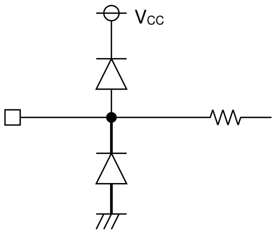
Pin 1 (PGOOD)



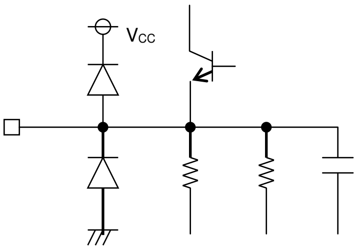
Pin 3 (CE)



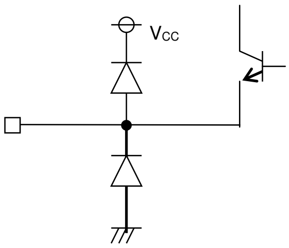

Pin 4 (ILIM)



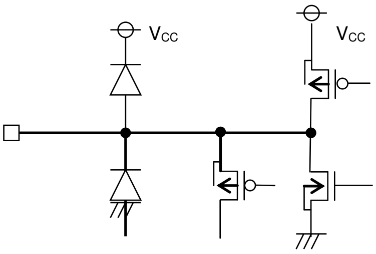

Pin 7 (VREG)



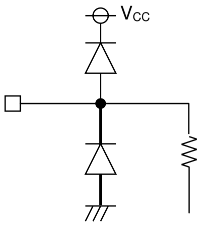

Pin 8 (FS)



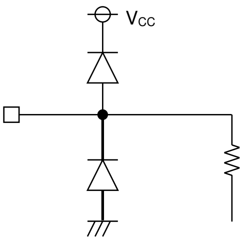

Pin 9 (SS/TRACK)



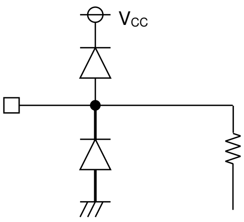

Pin 10 (REF)



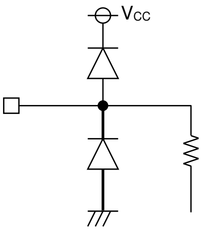

Pin 11 (VOUT)



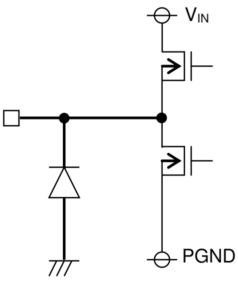

Pin 12 (IS-)



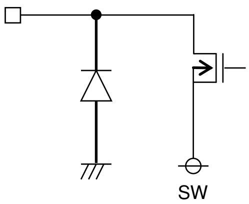

Pin 13 (IS+)



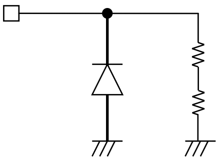

Pin 22-29 (SW)



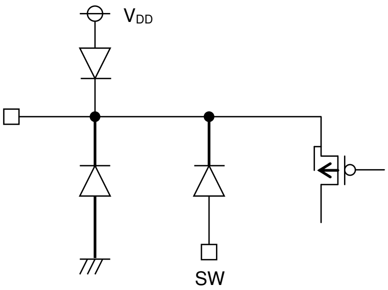

Pin 31-36 (VIN)



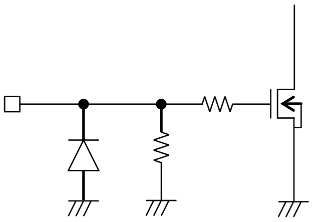

Pin 37 (VINS)



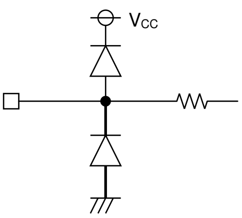
Pin 38 (BOOT)




Pin 39 (EN)

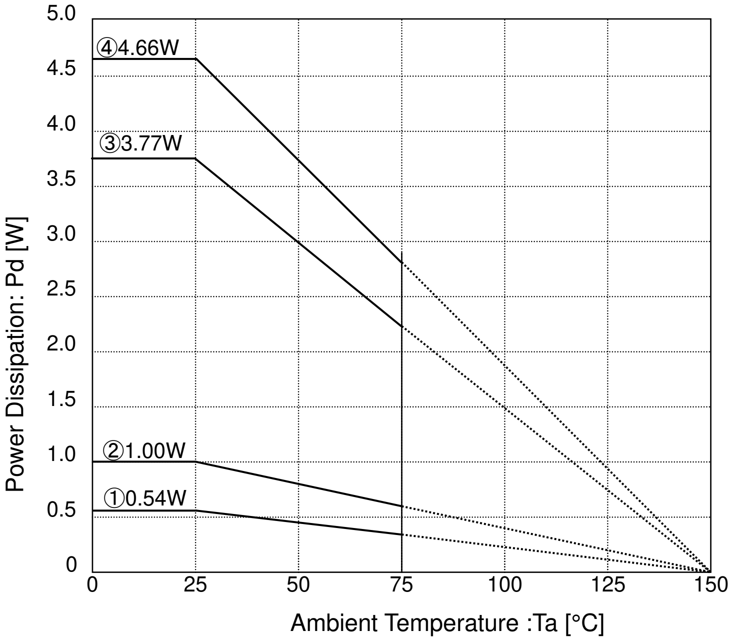


Pin 40(MODE)



**Power Dissipation**

VQFN040V6060




①IC Only
θj-a=231.5°C/W

②IC mounted on 1-layer board (with 20.2 $mm^2$ copper thermal pad)
θj-a=125.0°C/W

③IC mounted on 4-layer board (with 20.2 $mm^2$ pad on top layer,5505 $mm^2$ pad on layers 2,3)
θj-a=33.2°C/W

④IC mounted on 4-layer board (with 5505$mm^2$ pad on all layers)
θj-a=26.8°C/W

## Operational Notes

1. **Reverse Connection of Power Supply**
Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

## Operational Notes – continued

11. **Unused Input Pins**
Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

12. **Regarding the Input Pin of the IC**
This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

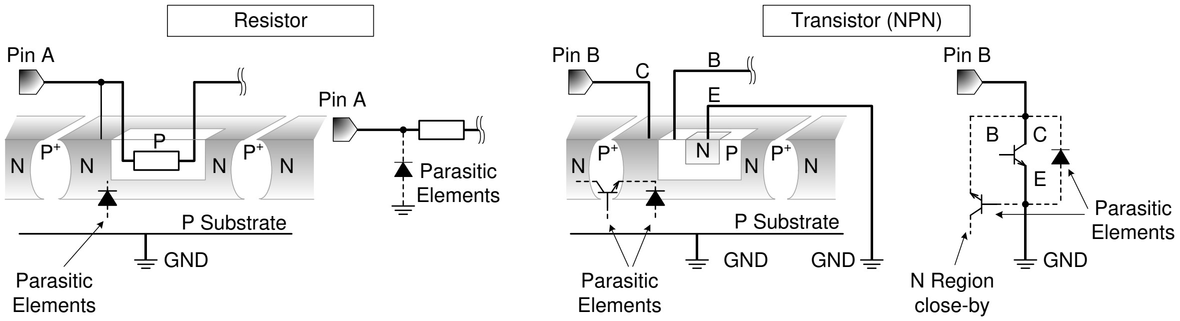



Figure 33. Example of monolithic IC structure

13. **Area of Safe Operation (ASO)**
Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

14. **Thermal Shutdown Circuit(TSD)**
This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

| | TSD ON Temp. [°C] (typ) | Hysteresis Temp. [°C] (typ) |
|---|---|---|
| BD95500MUV | 175 | 15 |

15. **Ground wiring traces**
When using both small-signal and large-current GND traces, the two ground traces should be routed separately but connected to a single ground potential within the application in order to avoid variations in the small-signal ground caused by large currents. Also ensure that the GND traces of external components do not cause variations on GND voltage.

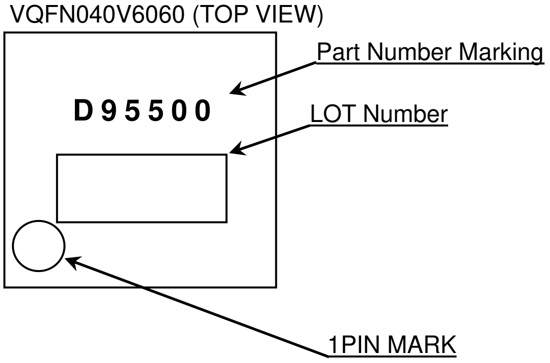
## Ordering Information

B D 9 5 5 0 0 M U V - E 2

- Part Number
- Package
  MUV: VQFN040V6060
- Packaging and forming specification
  E2: Embossed tape and reel

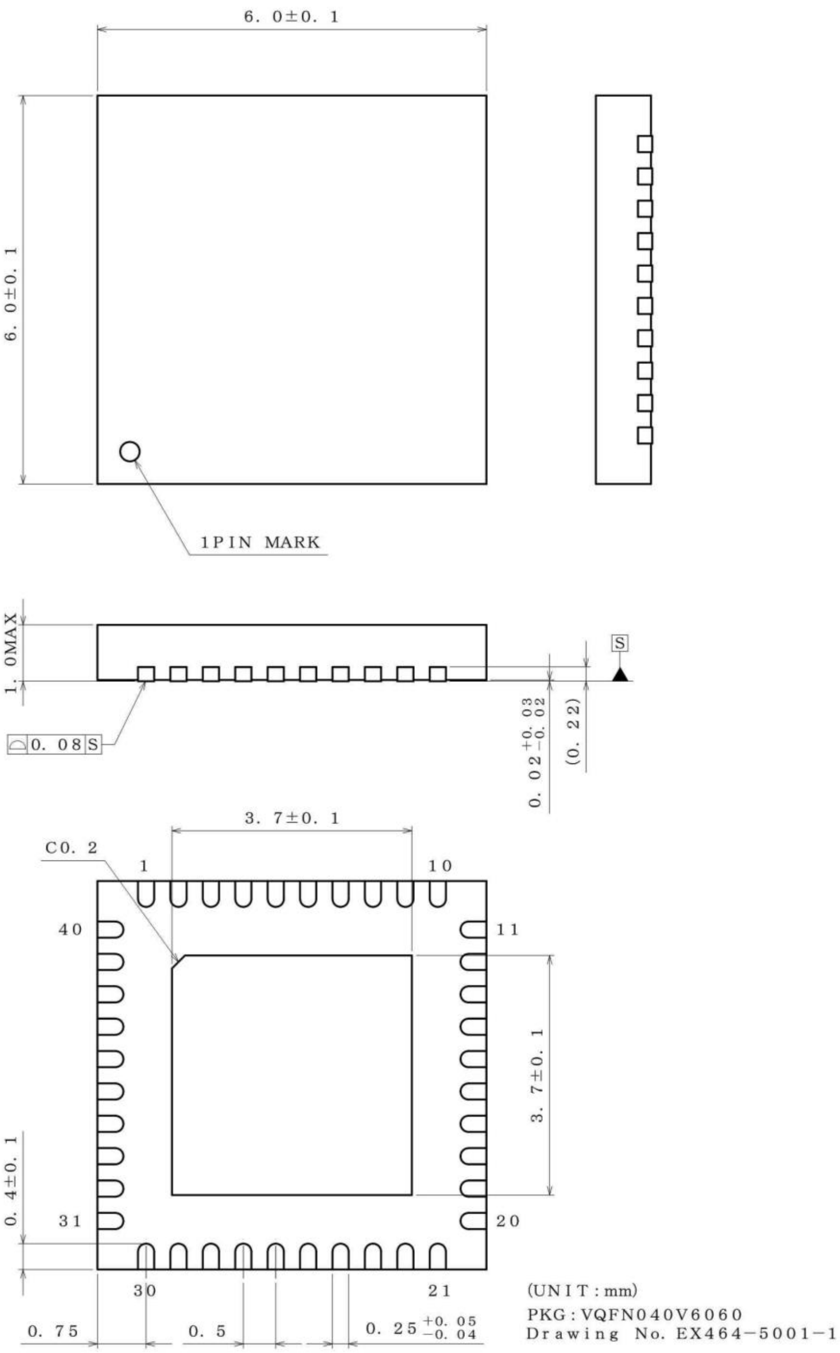
## Marking Diagram

VQFN040V6060 (TOP VIEW)



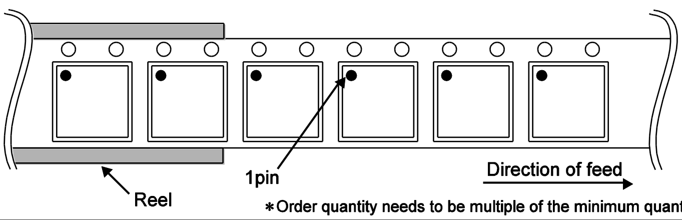
## Physical Dimension Tape and Reel information

| Package Name | VQFN040V6060 |
|---|---|




<Tape and Reel information>

| | |
|---|---|
| Tape | Embossed carrier tape |
| Quantity | 2000pcs |
| Direction of feed | E2<br>( The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand ) |




∗Order quantity needs to be multiple of the minimum quantity.

## Revision History

| Date | Revision | Changes |
|---|---|---|
| 27.Nov.2014 | 001 | New Release |

# Notice

## Precaution on using ROHM Products

1. Our Products are designed and manufactured for application in ordinary electronic equipments (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

| JAPAN | USA | EU | CHINA |
|---|---|---|---|
| CLASSⅢ | CLASSⅢ | CLASSⅡb | CLASSⅢ |
| CLASSⅣ | | CLASSⅢ | |

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are designed and manufactured for use under standard conditions and not under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including $Cl_2$, $H_2S$, $NH_3$, $SO_2$, and $NO_2$
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

## Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

## Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

## Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

## Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

## Precaution for Product Label

QR code printed on ROHM Products label is for ROHM's internal use only.

## Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

## Precaution for Foreign Exchange and Foreign Trade act

Since our Products might fall under controlled goods prescribed by the applicable foreign exchange and foreign trade act, please consult with ROHM representative in case of export.

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