TEXAS INSTRUMENTS

REF2125

SBAS798 – SEPTEMBER 2017

REF2125 Low-Drift, Low-Power, Small-Footprint, Series Voltage Reference With Clean Start

1 Features

- Initial Accuracy: ±0.05% (maximum)
- Temperature Coefficient : 6 ppm/°C (maximum)
- Operating Temperature Range: −40°C to +125°C
- Output Current: ±10 mA
- Low Quiescent Current: 95 μA (maximum)
- Wide Input Voltage: 12 V
- Output 1/f Noise (0.1 Hz to 10 Hz): 5 μV_{PP}/V
- Excellent Long-Term Stability 30 ppm/1000 hrs
- Small Footprint 5-Pin SOT-23 Package

2 Applications

- Precision Data Acquisition Systems
- Power Monitoring
- PLC Analog I/O Modules
- Industrial Instrumentation
- Field Transmitters
- Test Equipment
- 4 - 20mA Loop sensors
- LCR Meters

3 Description

The REF2125 device is a low temperature drift (6 ppm/°C), low-power, high-precision CMOS voltage reference, featuring ±0.05% initial accuracy, low operating current with power consumption less than 95 μA. This device also offers very low output noise of 5 μV_{p-p} /V, which enables its ability to maintain high signal integrity with high-resolution data converters and noise critical systems.

Stability and system reliability are further improved by the low output-voltage hysteresis of the device and low long-term output voltage drift. Furthermore, the small size and low operating current of the devices (95 μA) make them ideal for portable and battery-powered applications.

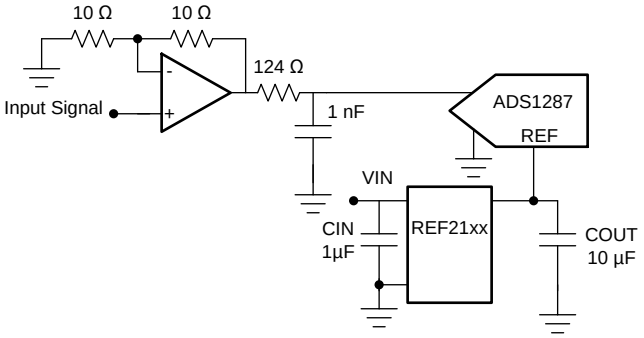
REF2125 is specified for the wide temperature range of −40°C to +125°C. Contact the TI sales representative for additional voltage options.

Device Information[1]

PART NAME	PACKAGE	BODY SIZE (NOM)
REF2125	SOT-23 (5)	2.90 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



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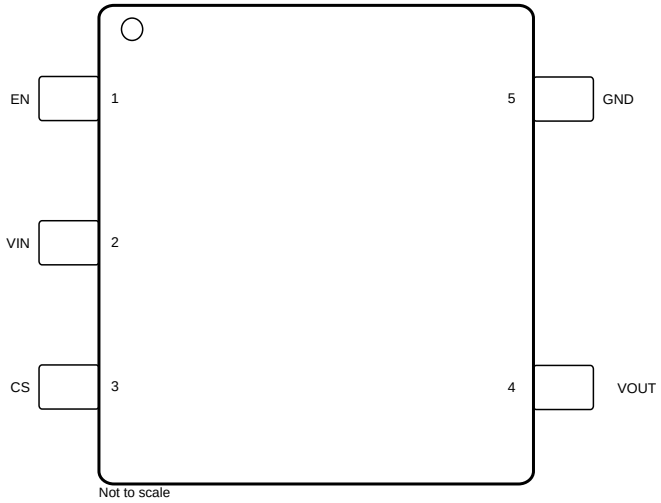
4 Revision History

DATE	REVISION	NOTES
September 2017	*	Initial release

5 Pin Configuration and Functions

DBV Package
5-Pin SOT-23
Top View



Not to scale

Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	EN	Input	Enable connection. Enables or disables the device.
2	VIN	Power	Input supply voltage connection.
3	CS	Input	Clean start pin. Connect to a resistor or capacitor to enable the clean start feature.
4	VOUT	Output	Reference voltage output.
5	GND	Ground	Ground connection.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	IN	V_{REF} + 0.05	13	V
	EN	–0.3	IN + 0.3	
Output voltage	V_{REF}	–0.3	5.5	V
Output short circuit current			20	mA
Temperature	Operating, T_A	–55	150	°C
	Storage T_{stg}	–65	170	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
IN	Supply input voltage (I_L = 0 mA, T_A = 25°C)	V_{REF} + V_{DO} (1)		12	V
EN	Enable voltage	0		IN	V
I_L	Output current	–10		10	mA
T_A	Operating temperature	–40	25	125	°C

(1) Dropout voltage.

6.4 Thermal Information

THERMAL METRIC(1)		REF2125 DBV (SOT-23) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	185	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	156	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	29.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	33.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	29.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

At T_A = 25°C unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ACCURACY AND DRIFT							
	Output voltage accuracy	–40°C ≤ T_A ≤ 125°C		–0.05%		0.05%	
	Output voltage temperature coefficient(1)				2.5	6	ppm/°C
LINE AND LOAD REGULATION							
$\Delta V_{(O\Delta VIN)}$	Line regulation	V_{IN} = 2.55 V to 12 V , T_A = 25°C			2		ppm/V
		V_{IN} = V_{REF} + V_{DO}(2) to 12 V, −40°C ≤ T_A ≤ 125°C				15	
$\Delta V_{(O\Delta IL)}$	Load regulation	I_L = 0 mA to 10 mA, V_{IN} = 3 V, T_A = 25°C	Sourcing		20		ppm/mA
		I_L = 0 mA to 10 mA, V_{IN} = 3 V, −40°C ≤ T_A ≤ 125°C	Sourcing			30	
		I_L = 0 mA to –10 mA, V_{IN} = V_{REF}+ V_{DO}(2), T_A = 25°C	Sinking		40		
		I_L = 0 mA to –10 mA, V_{IN} = V_{REF}+ V_{DO}(2), −40°C ≤ T_A ≤ 125°C	Sinking			70	
I_{SC}	Short-circuit current(3)	V_{REF} = 0, C_{CS} = No connect, T_A = 25°C			18		mA
		R_{CS} = 500kΩ, T_A = 25°C			7		mA
		C_{CS} = GND, T_A = 25°C			0.5		mA
NOISE							
e_n p-p	Output voltage noise(4)	f = 0.1 Hz to 10 Hz			5		µV p-p/V
		f = 10 Hz to 10 kHz			24		µV rms
e_n	Output voltage noise density	f = 1 kHz			0.25		ppm/√Hz
HYSTERESIS AND LONG TERM STABILITY							
	Long-term stability(5)	1000 hours			30		ppm
	Output voltage hysteresis(6)	T_A = 25°C to −40°C to 125°C to 25°C, Cycle 1			30		ppm
		T_A = 25°C to −40°C to 125°C to 25°C, Cycle 2			10		
TURNON							
t_{ON}	Turnon time	0.1% of output voltage settling, C_L = 10 µF, REF2125			2.5		ms
CAPACITIVE LOAD							
C_L	Stable output capacitor value	−40°C ≤ T_A ≤ 125°C		0.1		10	µF
OUTPUT VOLTAGE							
V_{REF}	Output voltage	REF2125			2.5		V

(1) Temperature drift is specified according to the box method. See *Feature Description* for more details.
(2) Dropout voltage under test condition is 100mV.
(3) In clean start section it is referred as I_{PEAK}.
(4) The peak-to-peak noise measurement procedure is explained in more detail in *Noise Performance*.
(5) Long-term stability measurement procedure is explained in more in detail in *Long-Term Stability*.
(6) The thermal hysteresis measurement procedure is explained in more detail in *Thermal Hysteresis*.

Electrical Characteristics (continued)

At T_A = 25°C unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER SUPPLY							
V_{IN}	Input voltage			V_{REF} + V_{DO}		12	V
I_L	Output current capacity	V_{IN} = V_{REF} + V_{DO} (2) to 12 V	Sourcing	10			mA
		V_{IN} = V_{REF} + V_{DO} (2) to 12 V	Sinking	–10			
I_Q	Quiescent current	−40°C ≤ T_A ≤ 125°C	Active mode		72	95	µA
		−40°C ≤ T_A ≤ 125°C	Shutdown mode		2.5	3	
V_{DO}	Dropout voltage	I_L = 0 mA, T_A= 25°C			50		mV
		I_L = 0 mA, −40°C ≤ T_A ≤ +125°C				100	
		I_L = 10 mA, −40°C ≤ T_A ≤ +125°C				500	
V_{EN}	ENABLE pin voltage	Voltage reference in active mode (EN = 1)		1.6			V
		Voltage reference in shutdown mode (EN = 0)				0.5	
I_{EN}	ENABLE pin leakage current	ENABLE = V_{IN}, −40°C ≤ T_A ≤ 125°C			1	2	µA

6.6 Typical Characteristics

at T_A = 25°C, V_{IN} = V_{EN} = 12 V, I_L = 0 mA , C_L = 10 µF, C_{IN} = 0.1 µF (unless otherwise noted)

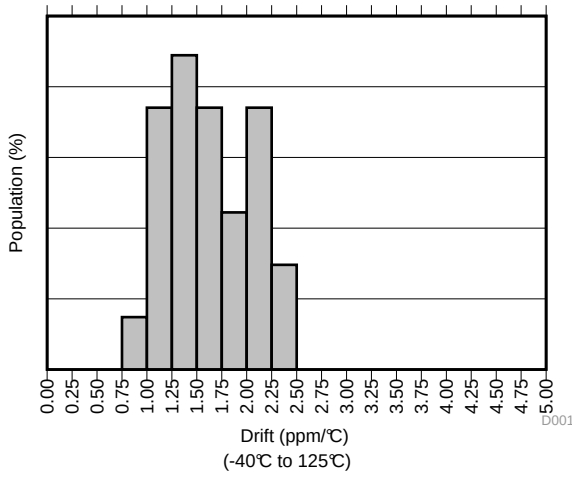


Figure 1. Temperature Drift

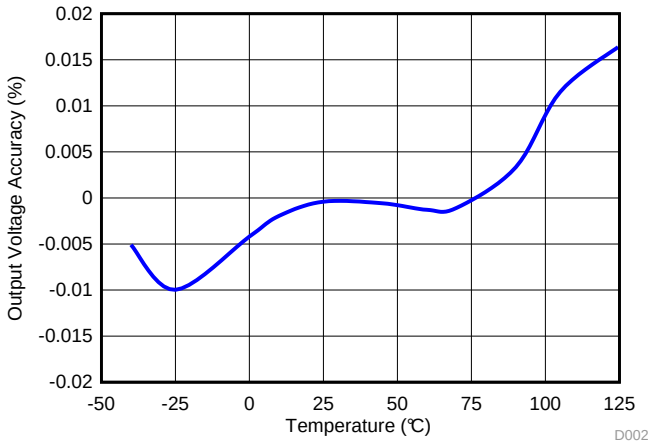


Figure 2. Output Voltage Accuracy vs Temperature

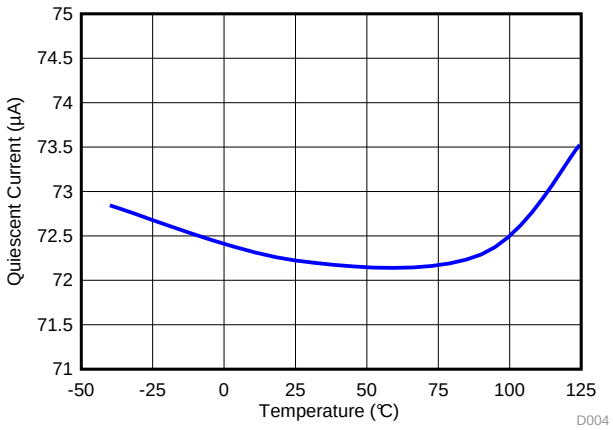


Figure 3. Quiescent Current vs Temperature

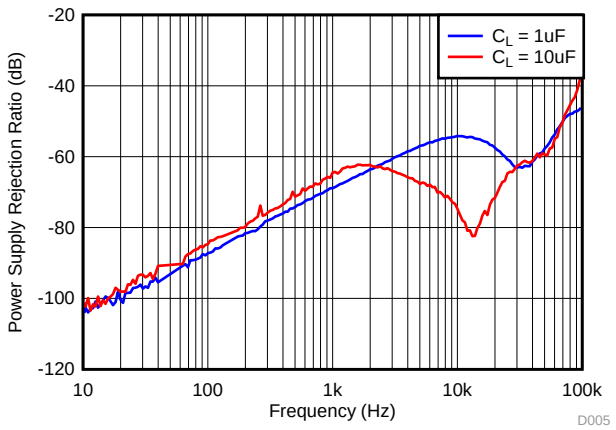


Figure 4. Power-Supply Rejection Ratio vs Frequency

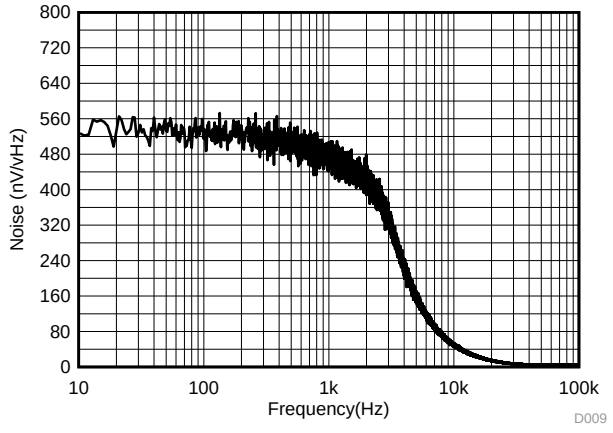


Figure 5. Noise Performance 10 Hz to 10 kHz

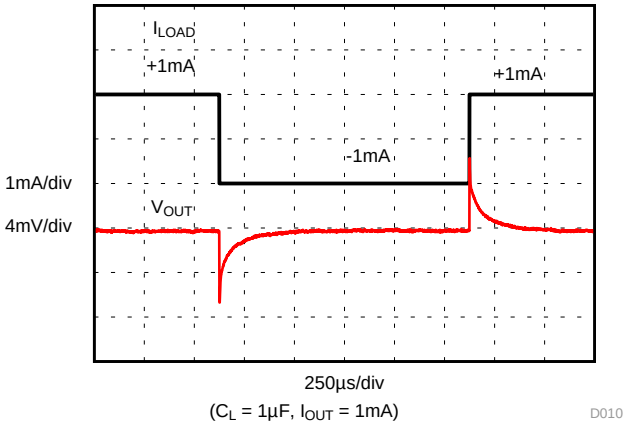


Figure 6. Load Transient

Typical Characteristics (continued)

at T_A = 25°C, V_{IN} = V_{EN} = 12 V, I_L = 0 mA , C_L = 10 µF, C_{IN} = 0.1 µF (unless otherwise noted)

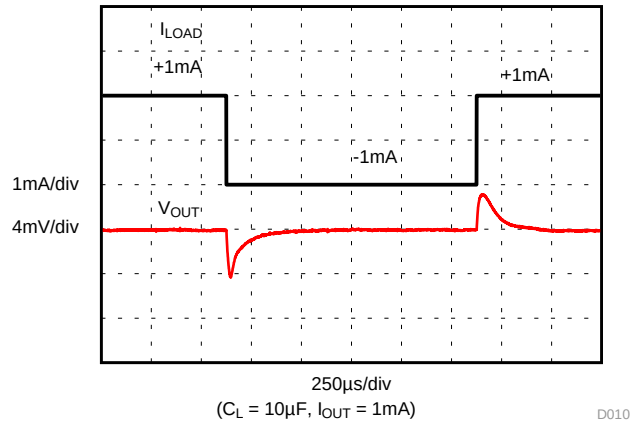


Figure 7. Load Transient

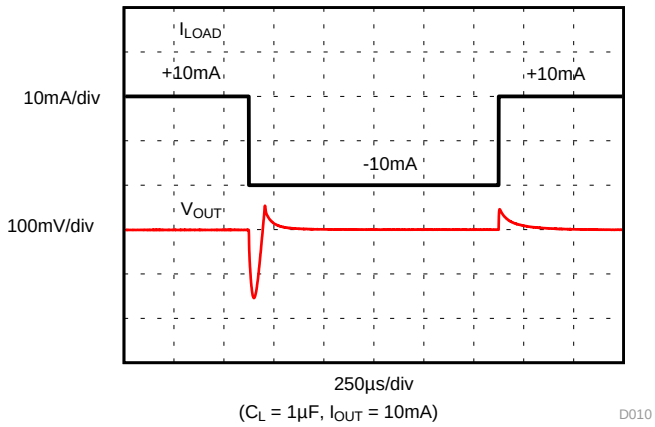


Figure 8. Load Transient

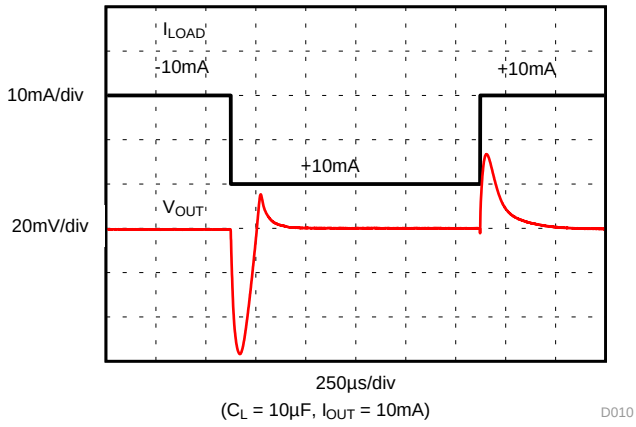


Figure 9. Load Transient

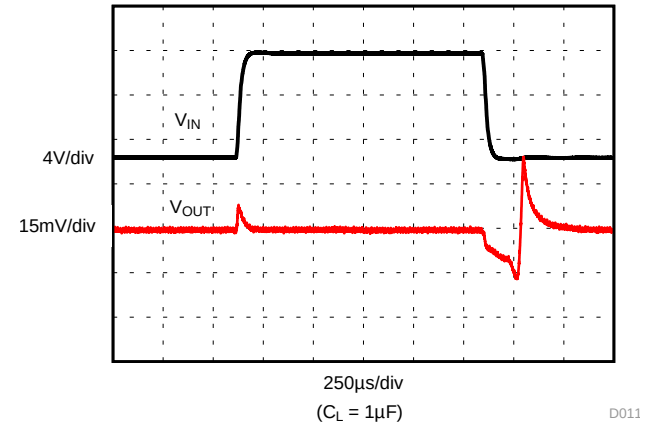


Figure 10. Line Transient

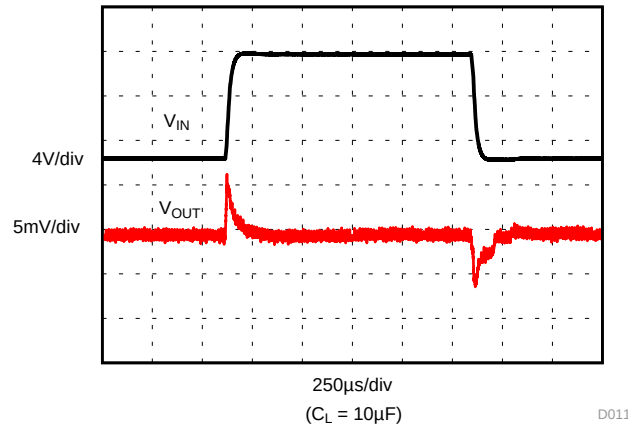


Figure 11. Line Transient

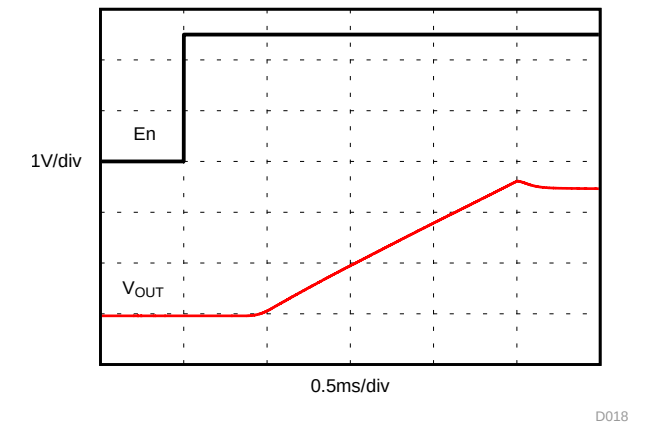


Figure 12. Start-Up

Typical Characteristics (continued)

at T_A = 25°C, V_{IN} = V_{EN} = 12 V, I_L = 0 mA , C_L = 10 µF, C_{IN} = 0.1 µF (unless otherwise noted)

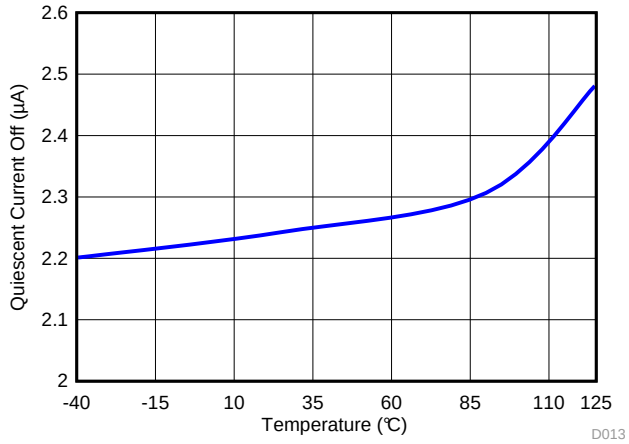


Figure 13. Quiescent Current Shutdown Mode

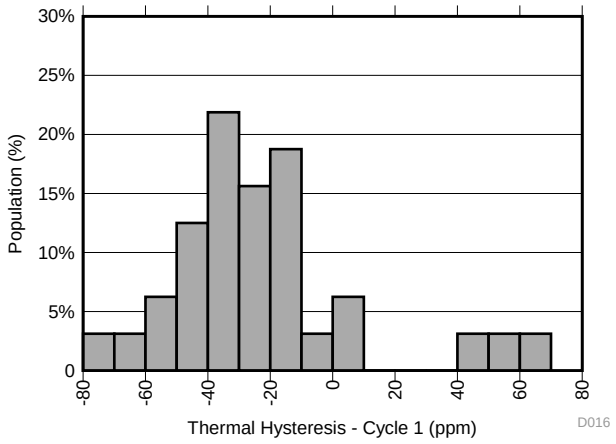


Figure 14. Thermal Hysteresis Distribution (Cycle 1)

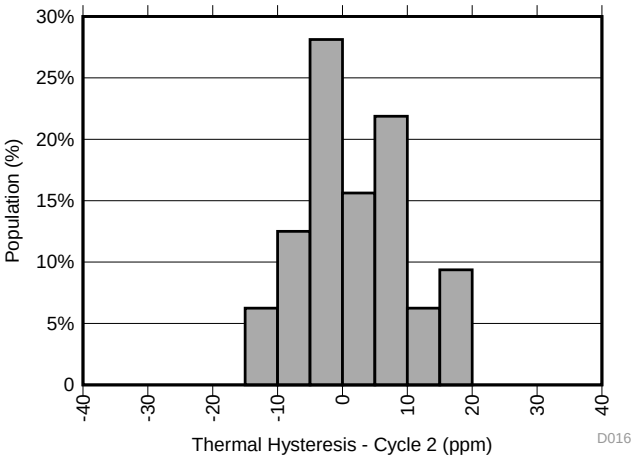
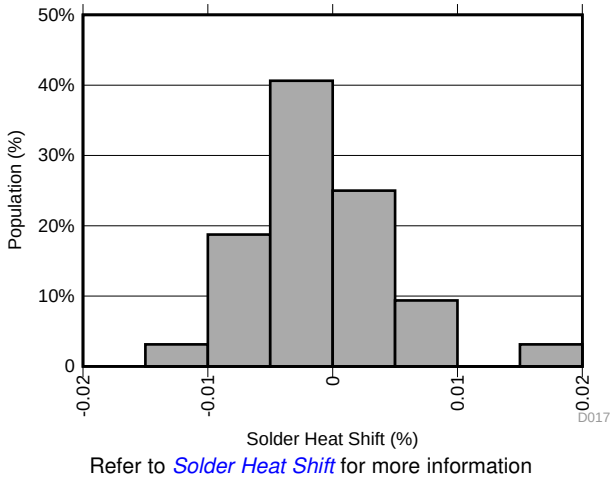


Figure 15. Thermal Hysteresis Distribution (Cycle 2)



Refer to *Solder Heat Shift* for more information

Figure 16. Solder Heat Shift Distribution

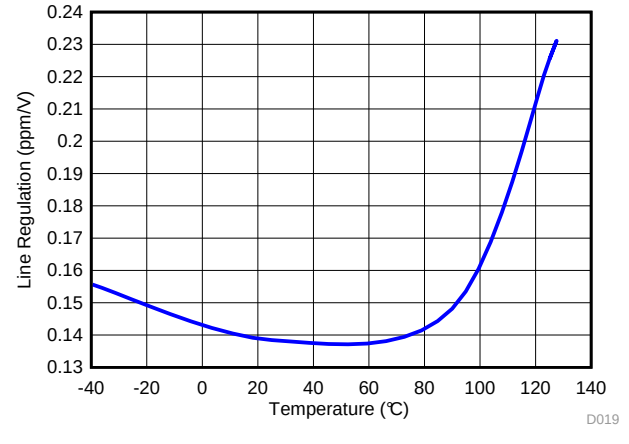


Figure 17. Line Regulation

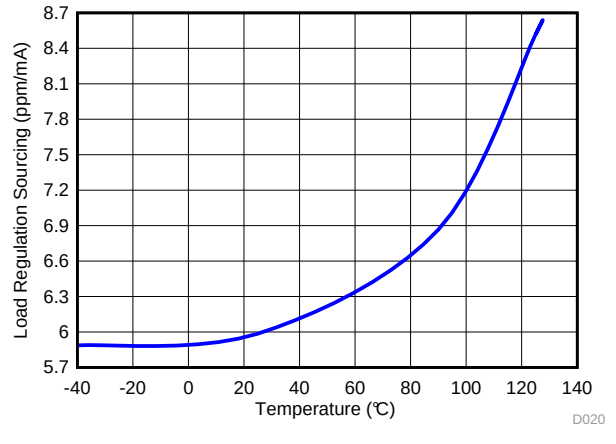


Figure 18. Load Regulation Sourcing

Typical Characteristics (continued)

at T_A = 25°C, V_{IN} = V_{EN} = 12 V, I_L = 0 mA , C_L = 10 µF, C_{IN} = 0.1 µF (unless otherwise noted)

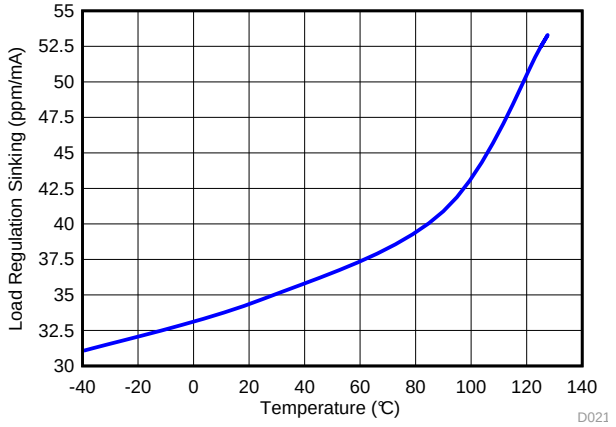


Figure 19. Load Regulation Sinking

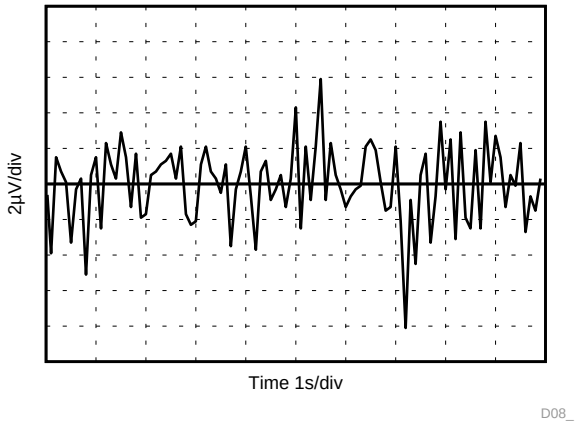


Figure 20. 0.1-Hz to 10-Hz Noise (V_{REF})

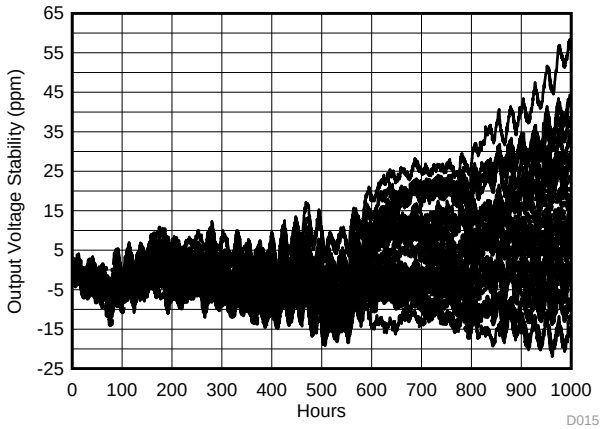


Figure 21. Long Term Stability - 1000 hours (V_{REF})

7 Parameter Measurement Information

7.1 Solder Heat Shift

The materials used in the manufacture of the REF2125 have differing coefficients of thermal expansion, resulting in stress on the device die when the part is heated. Mechanical and thermal stress on the device die can cause the output voltages to shift, degrading the initial accuracy specifications of the product. Reflow soldering is a common cause of this error.

In order to illustrate this effect, a total of 32 devices were soldered on four printed circuit boards [16 devices on each printed circuit board (PCB)] using lead-free solder paste and the paste manufacturer suggested reflow profile. The reflow profile is as shown in Figure 22. The printed circuit board is comprised of FR4 material. The board thickness is 1.65 mm and the area is 114 mm × 152 mm.

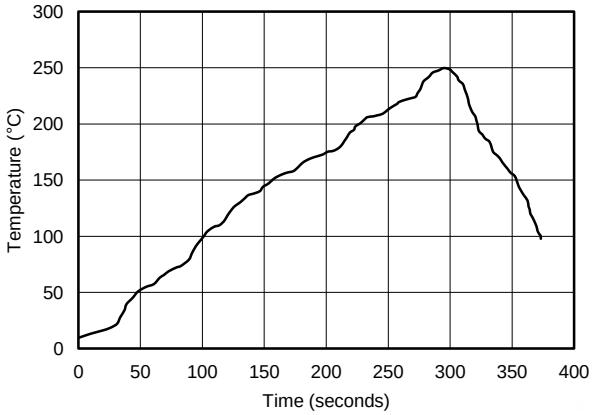


Figure 22. Reflow Profile

The reference and bias output voltages are measured before and after the reflow process; the typical shift is displayed in Figure 23. Although all tested units exhibit very low shifts (< 0.01%), higher shifts are also possible depending on the size, thickness, and material of the printed circuit board. An important note is that the histograms display the typical shift for exposure to a single reflow profile. Exposure to multiple reflows, as is common on PCBs with surface-mount components on both sides, causes additional shifts in the output bias voltage. If the PCB is exposed to multiple reflows, solder the device in the second pass to minimize its exposure to thermal stress.

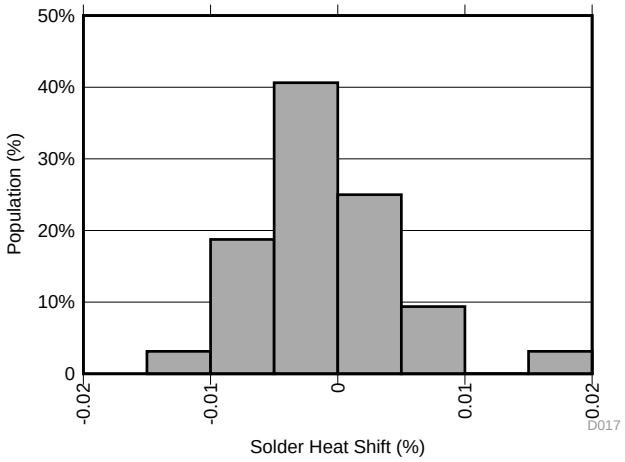


Figure 23. Solder Heat Shift Distribution, V_{REF} (%)

7.2 Long-Term Stability

One of the key parameters of the REF2125 reference is long-term stability. Typical characteristic expressed as: curves shows the typical drift value for the REF2125 is 30 ppm from 0 to 1000 hours. This parameter is characterized by measuring 32 units at regular intervals for a period of 1000 hours. It is important to understand that long-term stability is not ensured by design and that the output from the device may shift beyond the typical 30 ppm specification at any time. For systems that require highly stable output voltages over long periods of time, the designer should consider burning in the devices prior to use to minimize the amount of output drift exhibited by the reference over time

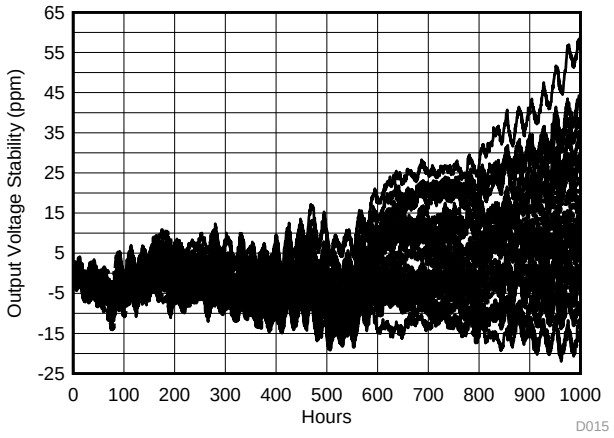


Figure 24. Long Term Stability - 1000 hours (V_{REF})

7.3 Thermal Hysteresis

Thermal hysteresis is measured with the REF2125 soldered to a PCB, similar to a real-world application. Thermal hysteresis for the device is defined as the change in output voltage after operating the device at 25°C, cycling the device through the specified temperature range, and returning to 25°C. Hysteresis can be expressed by Equation 1:

$$V_{HYST} = \left(\frac{| V_{PRE} - V_{POST} |}{V_{NOM}} \right) \times 10^6 \text{ (ppm)} \quad (1)$$

where

- V_{HYST} = thermal hysteresis (in units of ppm)
- V_{NOM} = the specified output voltage
- V_{PRE} = output voltage measured at 25°C pre-temperature cycling
- V_{POST} = output voltage measured after the device has cycled from 25°C through the specified temperature range of –40°C to +125°C and returns to 25°C.

Typical thermal hysteresis distribution is as shown in Figure 25.

Thermal Hysteresis (continued)

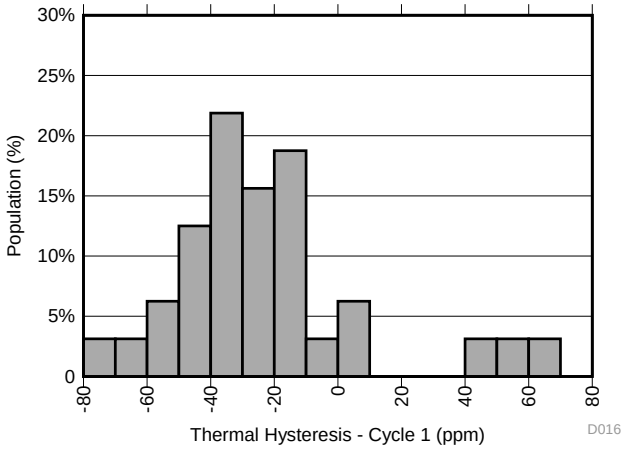


Figure 25. Thermal Hysteresis Distribution (V_{REF})

7.4 Power Dissipation

The REF2125 voltage reference is capable of source and sink up to 10 mA of load current across the rated input voltage range. However, when used in applications subject to high ambient temperatures, the input voltage and load current must be carefully monitored to ensure that the device does not exceeded its maximum power dissipation rating. The maximum power dissipation of the device can be calculated with Equation 2:

$$T_J = T_A + P_D \times R_{\theta JA} \quad (2)$$

where

- P_D is the device power dissipation
- T_J is the device junction temperature
- T_A is the ambient temperature
- $R_{\theta JA}$ is the package (junction-to-air) thermal resistance

Because of this relationship, acceptable load current in high temperature conditions may be less than the maximum current-sourcing capability of the device. In no case should the part be operated outside of its maximum power rating because doing so can result in premature failure or permanent damage to the device.

7.5 Noise Performance

Typical 0.1-Hz to 10-Hz voltage noise can be seen in Figure 26 . Device noise increases with output voltage and operating temperature. Additional filtering can be used to improve output noise levels, although care must be taken to ensure the output impedance does not degrade ac performance. Peak-to-peak noise measurement setup is shown in Figure 26.

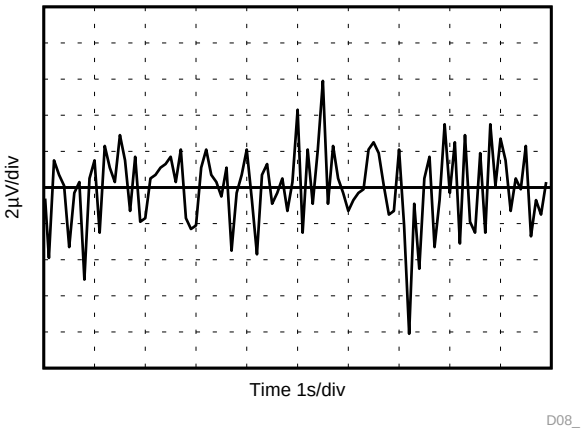


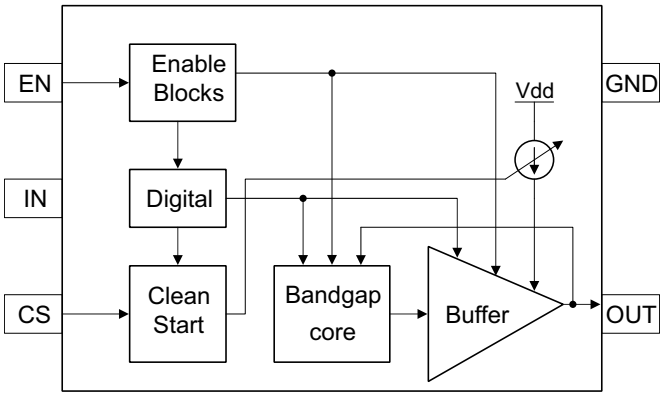
Figure 26. 0.1-Hz to 10-Hz Noise (V_{REF})

8 Detailed Description

8.1 Overview

The REF2125 is part of a family of low-noise, precision bandgap voltage references that are specifically designed for excellent initial voltage accuracy and drift. The *Functional Block Diagram* is a simplified block diagram of the REF2125 showing basic band-gap topology.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Supply Voltage

The REF2125 family of references features an extremely low dropout voltage. The REF2125 can be operated with a supply of only 1 mV above the output voltage in an unloaded condition. For loaded conditions, a typical dropout voltage versus load is shown on the front page. The REF2125 features a low quiescent current that is extremely stable over changes in both temperature and supply. The typical room temperature quiescent current is 72 μA, and the maximum quiescent current over temperature is just 95 μA. Supply voltages below the specified levels can cause the REF2125 to momentarily draw currents greater than the typical quiescent current. Use a power supply with a fast rising edge and low output impedance to easily prevent this issue.

8.3.2 Low Temperature Drift

The REF2125 is designed for minimal drift error, which is defined as the change in output voltage over temperature. The drift is calculated using the box method, as described by Equation 3:

$$\text{Drift} = \left(\frac{V_{REF(MAX)} - V_{REF(MIN)}}{V_{REF} \times \text{Temperature Range}} \right) \times 10^6 \quad (3)$$

8.3.3 Load Current

The REF2125 family is specified to deliver a current load of ±10 mA per output. The V_{REF} output of the device are protected from short circuits by limiting the output short-circuit current to 18 mA. The device temperature increases according to Equation 4:

$$T_J = T_A + P_D \times R_{\theta JA} \quad (4)$$

where

- T_J = junction temperature (°C),
- T_A = ambient temperature (°C),
- P_D = power dissipated (W), and
- $R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

The REF2125 maximum junction temperature must not exceed the absolute maximum rating of 150°C.

Feature Description (continued)

8.3.4 Clean Start Feature

In many applications (for example, loop powered applications), the supply at VIN has inductive impedance. This can cause the supply to dip during start-up because of the large output capacitor connected to the voltage reference and the inductive supply. The REF2125 family has an internal clean start block to control the peak of the inrush current during start-up. This feature is illustrated in *Functional Block Diagram*. The peak of inrush current can be calculated as Equation 5:

$$I_{PEAK} \approx 466\mu A + 13.54\mu A \times R_{CS} \quad (5)$$

where

- I_{PEAK} = Peak of inrush current (µA), has a range of [0.5 mA, 19 mA],
- R_{cs} = External resistor connected to the CS pin

During power up, I_{PEAK} is split between the device current and output current. The output current (I_{OUT}) is split between output capacitor and load current (I_{LOAD}). The device current can be estimated to be $I_Q+I_{OUT}/183$, where I_Q is quiescent current at no load. Hence for a given I_{LOAD} it is important to choose R_{cs} such that I_{PEAK} is larger than I_{LOAD}. Above equations capture typical characteristics and hence it is suggested to include ±25% margins while budgeting for inrush current and also while choosing R_{cs} for a given I_{LOAD}. This inrush current continues to stay at the limiting value (I_{PEAK}) till output reaches close to V_{REF} (2.5 V).

When a C_{cs} is also connected in parallel to R_{cs}, The inrush current limit shall rise exponentially to the steady state value (I_{PEAK}) as calculated using above equations, with a time constant of $R_{cs} \times C_{cs}$. Hence the initial (and maximum) rate of rise of inrush current shall be $I_{PEAK} /(R_{cs} \times C_{cs})$. Because the inrush current rate is limited, the loop powered supply dip is controlled.

8.4 Device Functional Modes

8.4.1 EN Pin

When the ENABLE pin of the REF2125 is pulled high, the device is in active mode. The device must be in active mode for normal operation. The REF2125 can be placed in a low-power mode by pulling the ENABLE pin low. When in shutdown mode, the output of the device becomes high impedance and the quiescent current of the device reduces to 2 µA in shutdown mode. The EN pin must not be pulled higher than VIN supply voltage. See the *Thermal Information* for logic high and logic low voltage levels.

8.4.2 Negative Reference Voltage

For applications requiring a negative and positive reference voltage, the REF2125 and OPA735 can be used to provide a dual-supply reference from a 5-V supply. Figure 27 shows the REF2125 used to provide a 2.5-V supply reference voltage. The low drift performance of the REF2125 complements the low offset voltage and zero drift of the OPA735 to provide an accurate solution for split-supply applications. Take care to match the temperature coefficients of R1 and R2.

Device Functional Modes (continued)

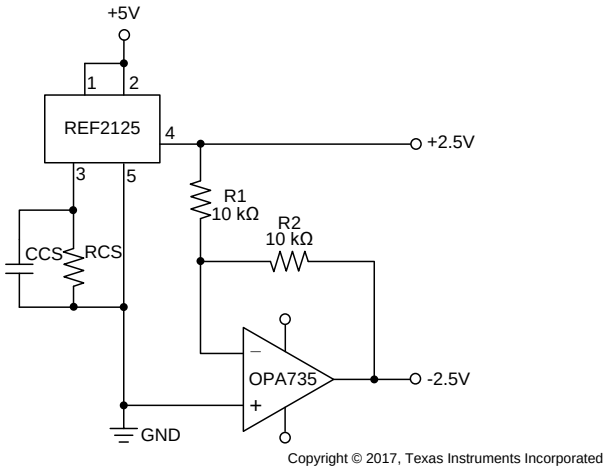


Figure 27. REF2125 and OPA735 Create Positive and Negative Reference Voltages

9 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

As this device has many applications and setups, there are many situations that this datasheet can not characterize in detail. Basic applications includes positive/negative voltage reference and data acquisition systems. For more information see application sections in the REF32xx data sheet.

9.2 Typical Application: Basic Voltage Reference Connection

The circuit shown in Figure 28 shows the basic configuration for the REF2125 references. Connect bypass capacitors according to the guidelines in *Input and Output Capacitors*.

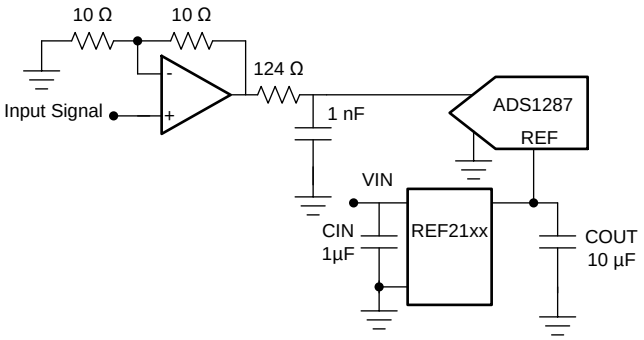


Figure 28. Basic Reference Connection

9.2.1 Design Requirements

A detailed design procedure is described based on a design example. For this design example, use the parameters listed in Table 1 as the input parameters.

Table 1. Design Example Parameters

DESIGN PARAMETER	VALUE
Input voltage V_{IN}	5 V
Output voltage V_{OUT}	2.5 V
REF2125 input capacitor	1 µF
REF2125 output capacitor	10 µF

9.2.2 Detailed Design Procedure

9.2.2.1 Input and Output Capacitors

A 1-µF to 10-µF electrolytic or ceramic capacitor can be connected to the input to improve transient response in applications where the supply voltage may fluctuate. Connect an additional 0.1-µF ceramic capacitor in parallel to reduce high frequency supply noise.

A ceramic capacitor of at least 0.1 µF must be connected to the output to improve stability and help filter out high frequency noise. An additional 1-µF to 10-µF electrolytic or ceramic capacitor can be added in parallel to improve transient performance in response to sudden changes in load current; however, keep in mind that doing so increases the turnon time of the device.

Best performance and stability is attained with low-ESR, low-inductance ceramic chip-type output capacitors (X5R, X7R, or similar). If using an electrolytic capacitor on the output, place a 0.1-μF ceramic capacitor in parallel to reduce overall ESR on the output.

9.2.2.2 V_{IN} Slew Rate Considerations

In applications with slow-rising input voltage signals, the reference exhibits overshoot or other transient anomalies that appear on the output. These phenomena also appear during shutdown as the internal circuitry loses power.

To avoid such conditions, ensure that the input voltage wave-form has both a rising and falling slew rate close to 6 V/ms.

9.2.2.3 Shutdown/Enable Feature

The REF2125 references can be switched to a low power shut-down mode when a voltage of 0.5 V or lower is input to the ENABLE pin. Likewise, the reference becomes operational for ENABLE voltages of 1.6 V or higher. During shutdown, the supply current drops to less than 2 μA, useful in applications that are sensitive to power consumption.

If using the shutdown feature, ensure that the ENABLE pin voltage does not fall between 0.5 V and 1.6 V because this causes a large increase in the supply current of the device and may keep the reference from starting up correctly. If not using the shutdown feature, however, the ENABLE pin can simply be tied to the IN pin, and the reference remains operational continuously.

9.2.3 Application Curves

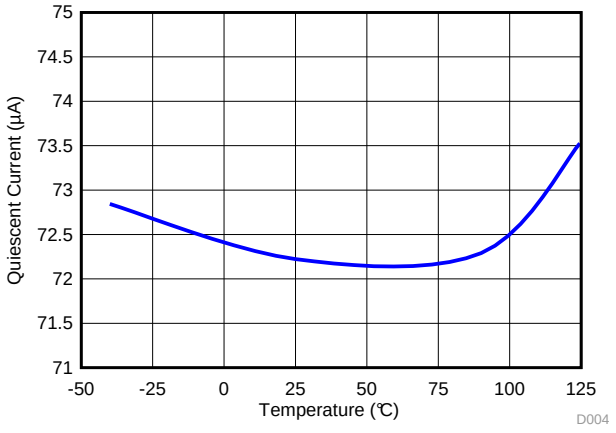


Figure 29. Quiescent Current vs Temperature

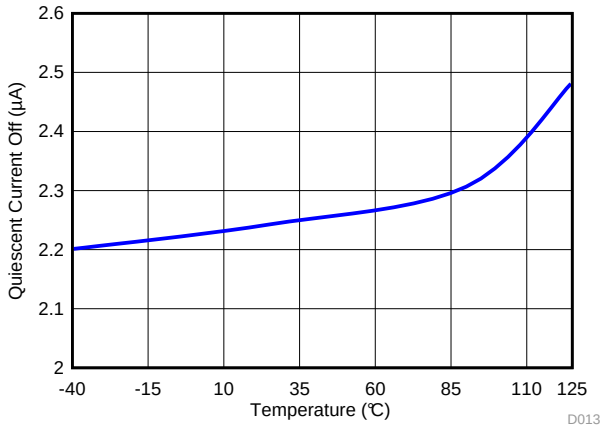


Figure 30. Quiescent Current Shutdown Mode

10 Power-Supply Recommendations

The REF2125 family of references feature an extremely low-dropout voltage. These references can be operated with a supply of only 50 mV above the output voltage. TI recommends a supply bypass capacitor ranging between 0.1 μF to 10 μF.

11 Layout

11.1 Layout Guidelines

Figure 31 illustrates an example of a PCB layout for a data acquisition system using the REF2125. Some key considerations are:

- Connect low-ESR, 0.1-μF ceramic bypass capacitors at V_{IN}, V_{REF} of the REF2125.
- Decouple other active devices in the system per the device specifications.
- Using a solid ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup.
- Place the external components as close to the device as possible. This configuration prevents parasitic errors (such as the Seebeck effect) from occurring.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when absolutely necessary.

11.2 Layout Example

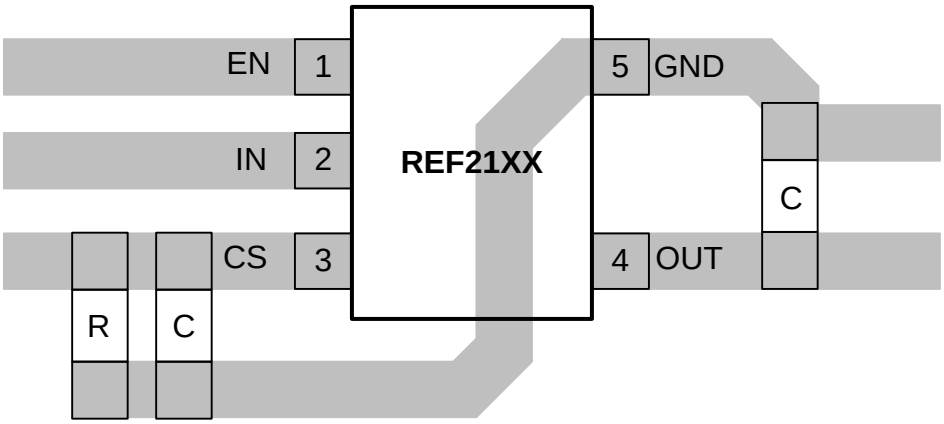


Figure 31. Layout Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- *INA21x Voltage Output, Low- or High-Side Measurement, Bidirectional, Zero-Drift Series, Current-Shunt Monitors*
- *Low-Drift Bidirectional Single-Supply Low-Side Current Sensing Reference Design*

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
REF2125IDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	19DD	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

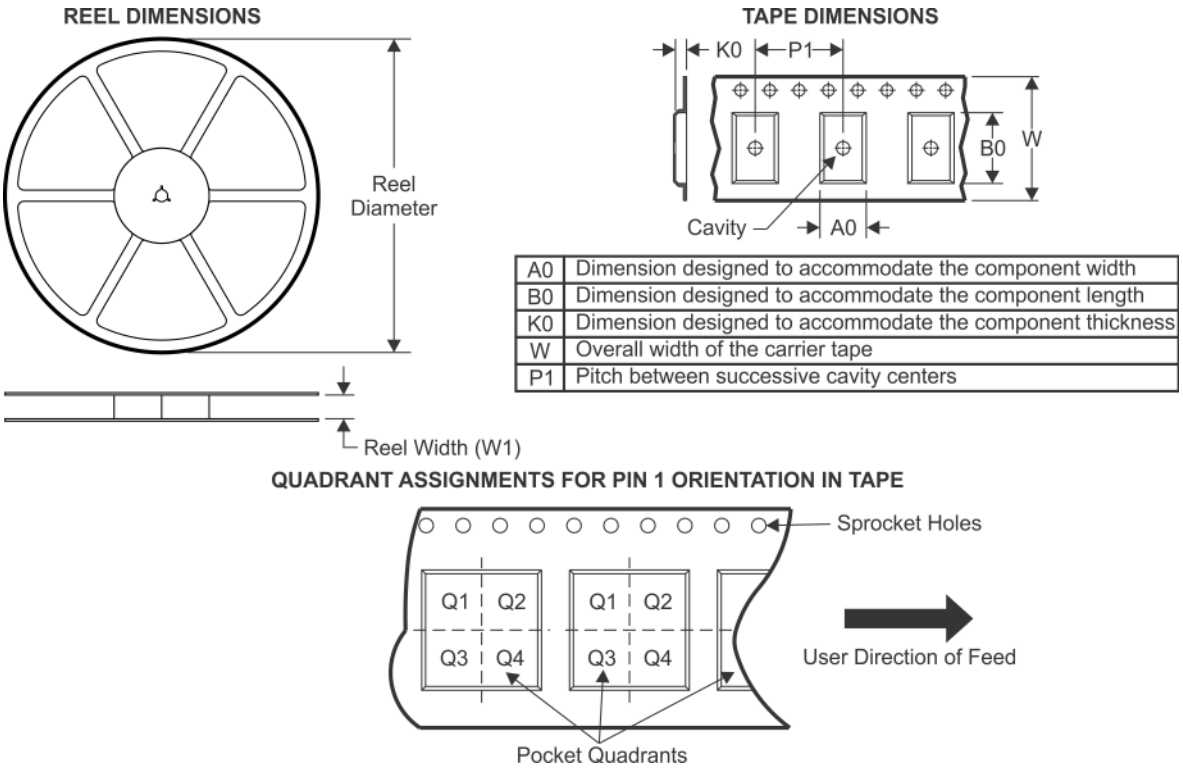
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

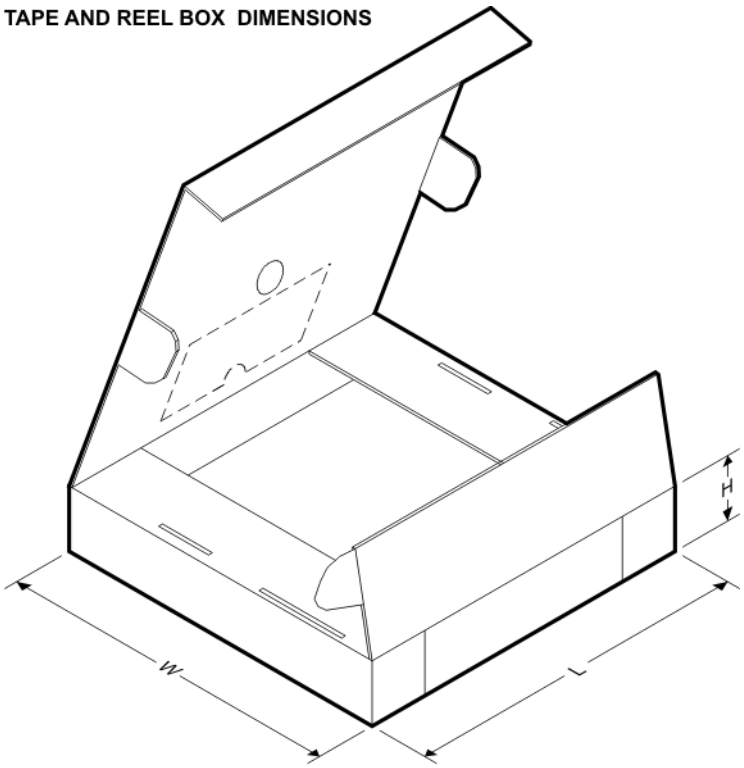


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
REF2125IDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

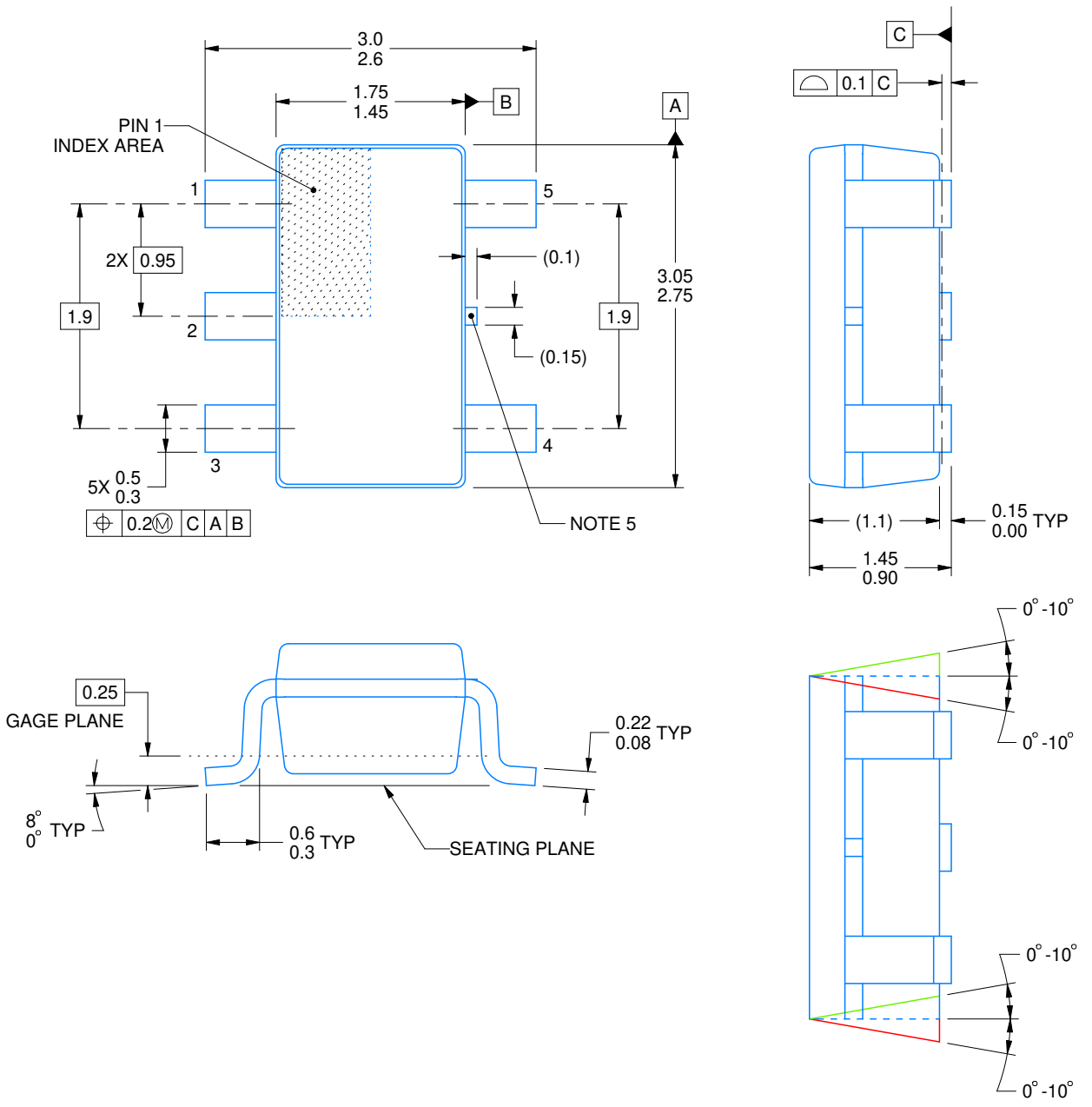
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
REF2125IDBVR	SOT-23	DBV	5	3000	445.0	220.0	345.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



ALTERNATIVE PACKAGE SINGULATION VIEW

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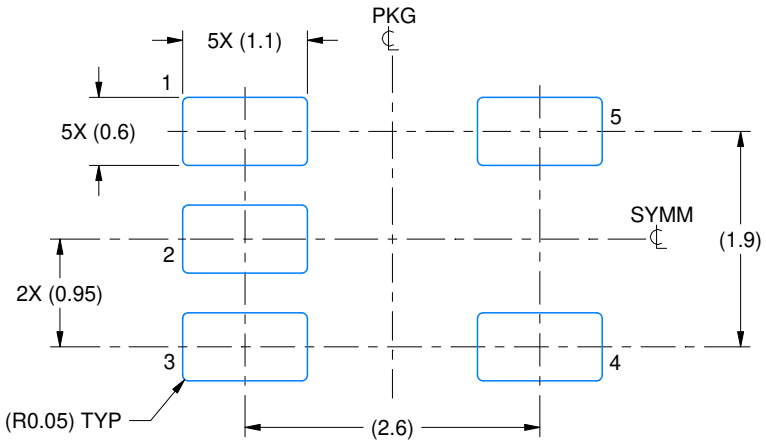
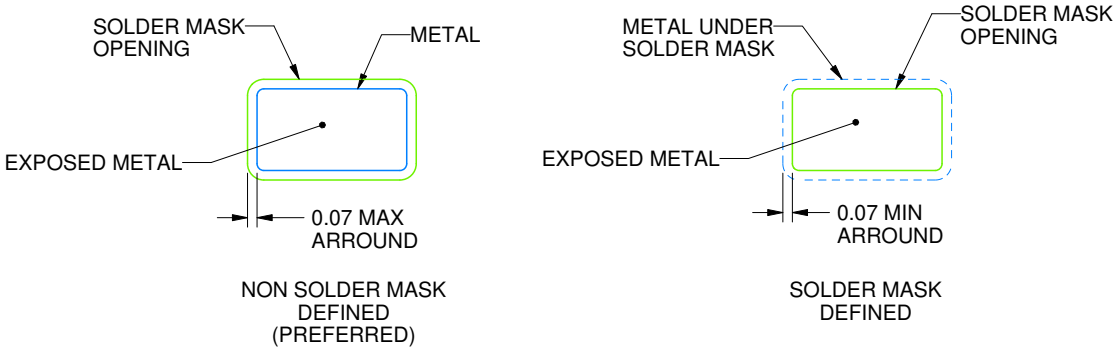
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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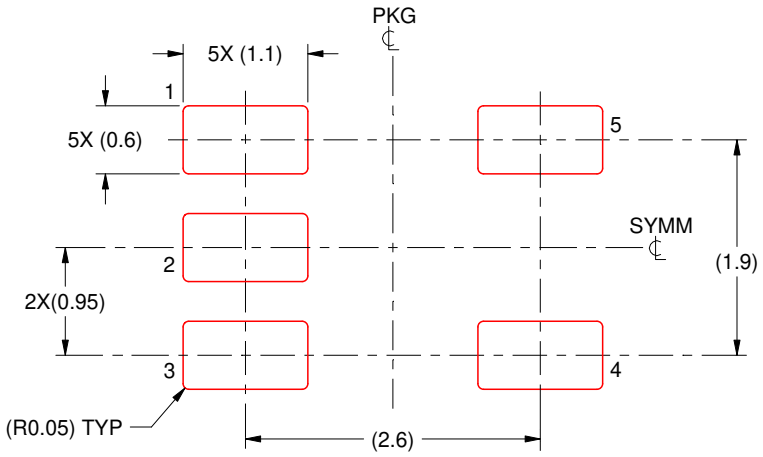
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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