ICM7224
4½-Digit LCD Display Counter

GENERAL DESCRIPTION

The ICM7224 device is a high-performance CMOS 4½-digit counter, including decoder, output latch, display driver, count inhibit, leading zero blanking, and reset circuitry.

The counter section provides direct static counting, guaranteed from DC to 15 MHz, using a 5V ±10% supply over the operating temperature range. At normal ambient temperatures, the devices will typically count up to 25 MHz. The COUNT input is provided with a Schmitt trigger to allow operation in noisy environments and correct counting with slowly changing inputs. The COUNT INHIBIT, STORE and RESET inputs allow a direct interface with the ICM7207/A to implement a low cost, low power frequency counter with a minimum component count.

These devices also incorporate several features intended to simplify cascading four-digit blocks. The CARRY output allows the counter to be cascaded, while the Leading Zero Blanking INput and OUTput allows correct Leading Zero Blanking between four-decade blocks. The BackPlane driver of the LCD devices may be disabled, allowing the segments to be slaved to another backplane signal, necessary when using an eight or twelve digit, single backplane display.

These devices provide maximum count of 19999. The display drivers are not of the multiplexed type and each display segment has its own individual drive pin, providing high quality display outputs. The ICM7224 drives LCD displays.

The ICM7224 is packaged in a standard 40-pin dual-in-line plastic or CERDIP package, or in dice.

FEATURES

- **High Frequency Counting — Guaranteed 15MHz, Typically 25MHz at 5V**
- **Low Power Operation — Typically Less Than 100μW Quiescent**
- **$\overline{\text{STORE}}$ and $\overline{\text{RESET}}$ Inputs Permit Operation as Frequency or Period Counter**
- **True $\overline{\text{COUNT INHIBIT}}$ Disables First Counter Stage**
- **$\overline{\text{CARRY}}$ Output for Cascading Four-Digit Blocks**
- **Schmitt-Trigger On The COUNT Input Allows Operation in Noisy Environments or With Slowly Changing Inputs**
- **Leading Zero Blanking INput and OUTput for Correct Leading Zero Blanking With Cascaded Devices**
- **LCD Devices Provide Complete Onboard Oscillator and Divider Chain to Generate Backplane Frequency, or Backplane Driver May Be Disabled Allowing Segments to be Slaved to A Master Backplane Signal**

ORDERING INFORMATION

Part Number	Temperature Range	Package
ICM7224IPL	-25°C to +85°C	40 Pin Plastic DIP
ICM7224IJL	-25°C to +85°C	40 Pin CERDIP
ICL7224RIPL*	-25°C to +85°C	40 Pin Plastic DIP

* "R" indicates device with reversed leads configuration.

ICM7224 Direct Drive LCD

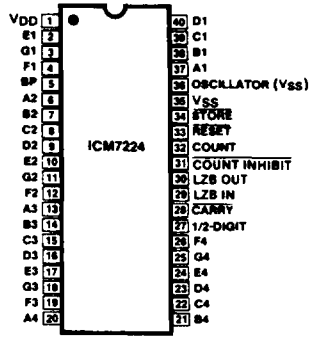

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Figure 1: Pin Configuration

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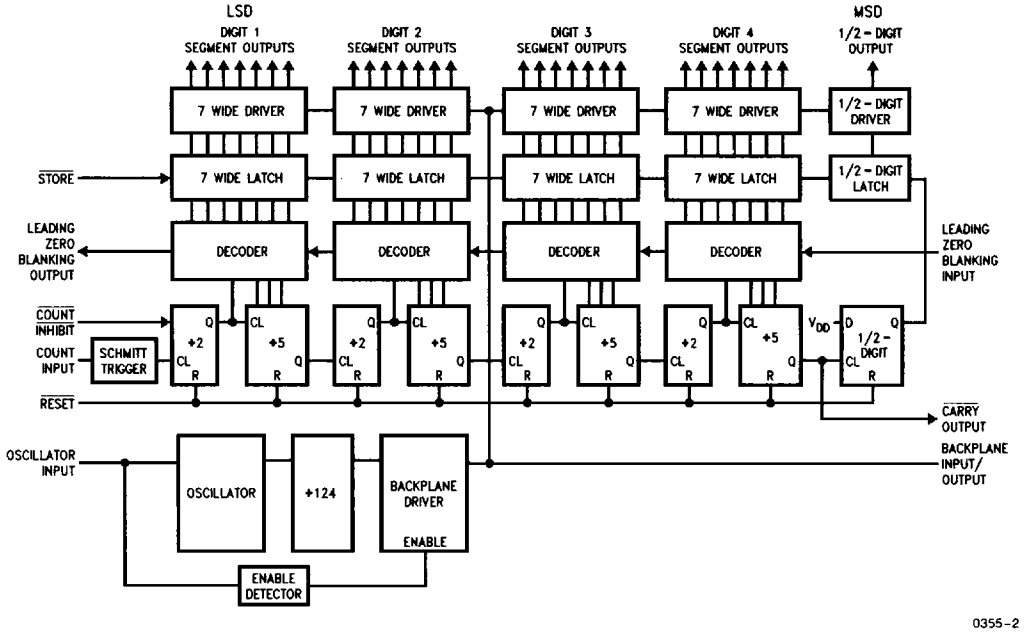
NOTE: All typical values have been characterized but are not tested.

ICM7224/ICM7225

ICM7224, LCD Display



ICM7225, LED Display

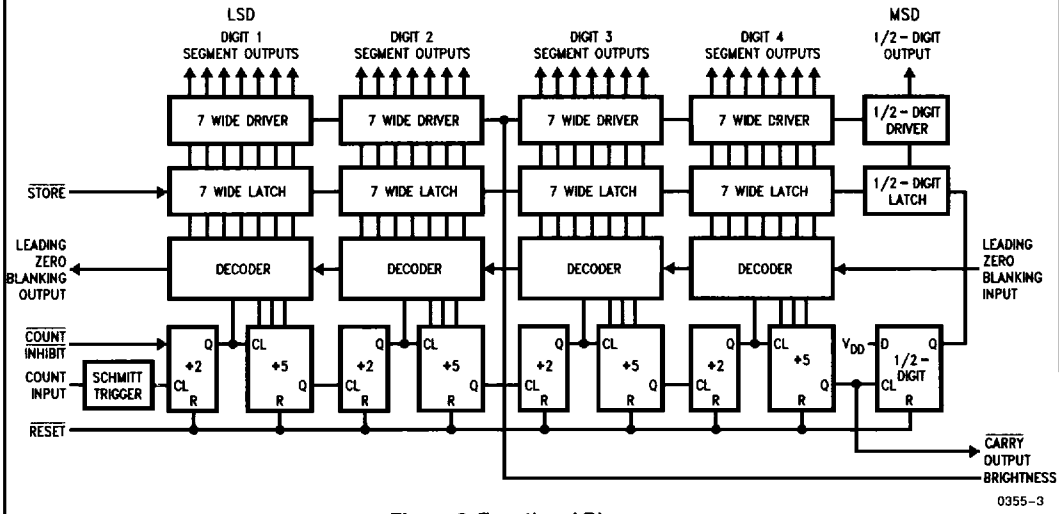


Figure 2: Functional Diagrams

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($V_{DD}-V_{SS}$) 6.5V
Input Voltage (Any Terminal) (Note 2) ..... ($V_{DD}+0.3V$) to ($V_{SS}-0.3V$)
Power Dissipation (Note 1) ..... 0.5W @ 70°C
Operating Temperature Range ..... −25°C to +85°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... 300°C

NOTE 1: This limit refers to that of the package and will not be obtained during normal operation.

2: Due to the SCR structure inherent in the CMOS process, connecting any terminal to voltages greater than V_{DD} or less than V_{SS} may cause destructive device latchup. For this reason, it is recommended that no inputs from sources operating on a different power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the ICM7224/ICM7225 be turned on first.

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

ELECTRICAL CHARACTERISTICS ($V_{DD}=5V$, $V_{SS}=0V$, $T_A=25°C$, unless otherwise indicated)

ICM7224 CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD}	Operating current	Test circuit, Display blank		10	50	μA
V_{SUPPLY}	Operating supply voltage range ($V_{DD}-V_{SS}$)		3		6	V
I_{OSCI}	OSCILLATOR *input current*	Pin 36		±2	±10	μA
t_R, t_F	Segment rise/fall time	$C_{load}=200pF$		0.5		μs
t_R, t_F	BackPlane rise/fall time	$C_{load}=5000pF$		1.5		
f_{OSC}	Oscillator frequency	Pin 36 Floating		19		kHz
f_{BP}	Backplane frequency	Pin 36 Floating		150		Hz

ICM7225 CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{STBY}	Operating current display off	Pin 5 (BRighTness) at V_{SS} Pins 29, 31-34 at V_{DD}		10	50	μA
V_{SUPP}	Operating supply voltage range ($V_{DD}-V_{SS}$)		4		6	V
I_{DD}	Operating current	Pin 5 at V_{DD}, Display 18888		200		mA
I_{SLK}	Segment leakage current	Segment Off		±0.01	±1	μA
I_{SEG}	Segment on current	Segment On, Vout = +3V	5	8		mA
I_H	Half-digit on current	Half-digit on, Vout = +3V	10	16		

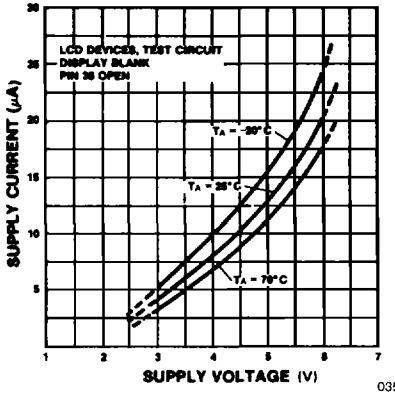
FAMILY CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_P	Input Pullup Currents	Pins 29, 31, 33, 34 Vin = $V_{DD}-3V$		10		μA
V_{IH}	Input High Voltage	Pins 29, 31, 33, 34	3			V
V_{IL}	Input Low Voltage	Pins 29, 31, 33, 34			1	
V_{CT}	$\overline{COUNT}$ Input Threshold			2		
V_{CH}	$\overline{COUNT}$ Input Hysteresis			0.5		
I_{OH}	Output High Current	$\overline{CARRY}$ Pin 28 Leading Zero Blanking OUT Pin 30 Vout = $V_{DD}-3V$	−350	−500		μA
I_{OL}	Output Low Current	$\overline{CARRY}$ Pin 28 Leading Zero Blanking OUT Pin 30 Vout = +3V	350	500		
f_{COUNT}	Count Frequency	$4.5V<V_{DD}<6V$	0		15	MHz
t_S,t_R	$\overline{STORE}$, $\overline{RESET}$ Minimum Pulse Width		3			μs

NOTE: All typical values have been characterized but are not tested.

TYPICAL PERFORMANCE CHARACTERISTICS

7224 OPERATING SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



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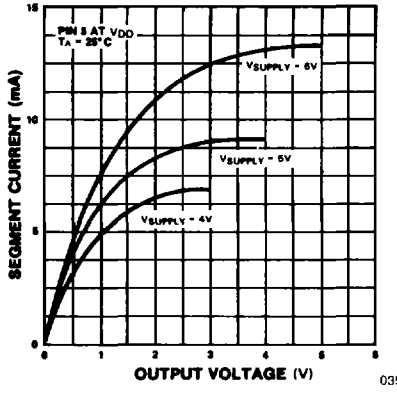
7225 LED SEGMENT CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



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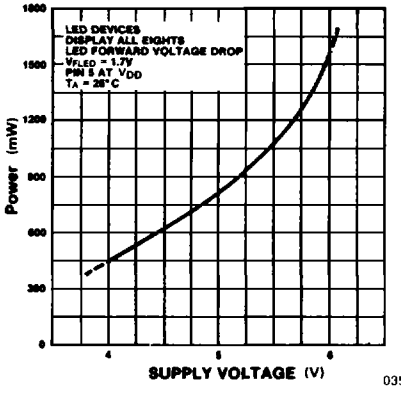
7225 OPERATING POWER (LED DISPLAY) AS A FUNCTION OF SUPPLY VOLTAGE



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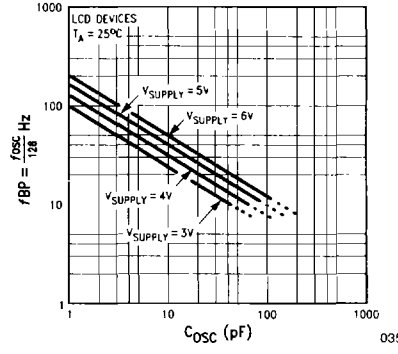
7224 BACKPLANE FREQUENCY AS A FUNCTION OF OSCILLATOR CAPACITOR C_{OSC}



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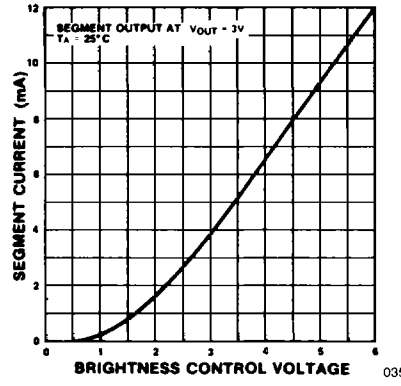
7225 LED SEGMENT CURRENT AS A FUNCTION OF BRIGHTNESS CONTROL VOLTAGE



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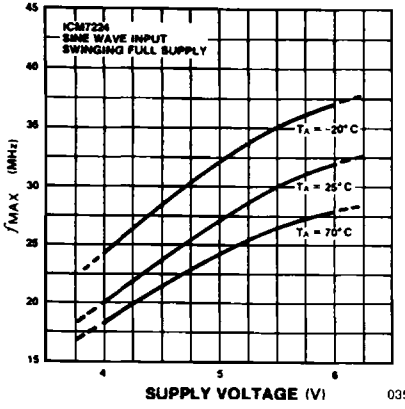
MAXIMUM COUNT FREQUENCY (TYPICAL) AS A FUNCTION OF SUPPLY VOLTAGE



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NOTE: All typical values have been characterized but are not tested

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

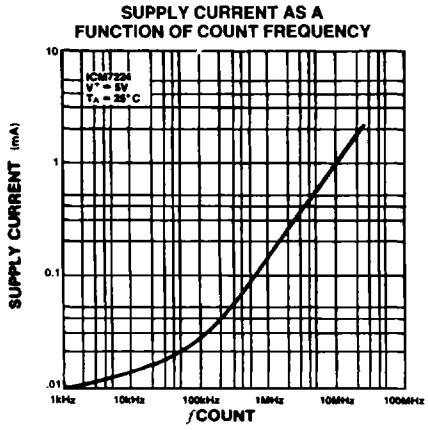

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TABLE I: Control Input Definitions

INPUT	TERMINAL	VOLTAGE	FUNCTION
Leading Zero Blanking INput	29	V_{DD} or Floating V_{SS}	Leading Zero Blanking Enabled Leading Zeroes Displayed
$\overline{\text{COUNT INHIBIT}}$	31	V_{DD} or Floating V_{SS}	Counter Enabled Counter Disabled
$\overline{\text{RESET}}$	33	V_{DD} or Floating V_{SS}	Inactive Counter Reset to 0000
$\overline{\text{STORE}}$	34	V_{DD} or Floating V_{SS}	Output Latches not Updated Output Latches Updated

CONTROL INPUT DEFINITIONS

In Table I, V_{DD} and V_{SS} are considered to be normal operating input logic levels. Actual input low and high levels are specified in the Operating Characteristics. For lowest power consumption, input signals should swing over the full supply.

DETAILED DESCRIPTION

LCD Device

The LCD device provides outputs suitable for driving conventional 4½-digit by seven segment LCD displays. They include 29 individual segment drivers, a backplane driver, and a self-contained oscillator and divider chain to generate the backplane frequency (See Figure 4).

The segment and backplane drivers each consist of a CMOS inverter, with the n- and p-channel devices ratioed to provide identical on resistances, and thus equal rise and fall times. This eliminates any D.C. component which could arise from differing rise and fall times, and ensures maximum display life.

The backplane output can be disabled by connecting the OSCILLATOR input (pin 36) to V_{SS}. This synchronizes the 29 segment outputs directly with a signal input at the BP terminal (pin 5) and allows cascading of several slave devices to the backplane output of one master device. The backplane may also be derived from an external source. This allows the use of displays with characters in multiples of four and a single backplane. A slave device will represent a load of approximately 200pF (comparable to one additional segment). The limitation on the number of devices that can be slaved to one master device backplane driver is the additional load represented by the larger backplane of displays of more than four digits, and the effect of that load on the backplane rise and fall times. A good rule of thumb to observe in order to minimize power consumption, is to keep the rise and fall times less than about 5 microseconds. The backplane driver of one device should handle the backplane to a display of 16 one-half-inch characters without the rise and fall times exceeding 5μs (ie, 3 slave devices and the display backplane driven by a fourth master device). It is recommended that if more than four devices are to be slaved together, that the backplane signal be derived externally and all the ICM7224 devices be slaved to it.

This external backplane signal should be capable of driving very large capacitive loads with short (1-2μs) rise and fall times. The maximum frequency for a backplane signal should be about 150Hz, although this may be too fast for optimum display response at lower display temperatures, depending on the display used.

The onboard oscillator is designed to free run at approximately 19kHz, at microampere power levels. The oscillator frequency is divided by 128 to provide the backplane frequency, which will be approximately 150Hz with the oscilla-

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NOTE: All typical values have been characterized but are not tested.

tor free-running. The oscillator frequency may be reduced by connecting an external capacitor between the OSCillator terminal (pin 36) and V_{DD}; see the plot of oscillator/backplane frequency in "Typical Characteristics" for detailed information.

The oscillator may also be overdriven if desired, although care must be taken to insure that the backplane driver is not disabled during the negative portion of the overdriving signal (which could cause a D.C. component to the display). This can be done by driving the OSCILLATOR input between the positive supply and a level out of the range where the backplane disable is sensed, about one fifth of the supply voltage above the negative supply. Another technique for overdriving the oscillator (with a signal swinging the full supply) is to skew the duty cycle of the overdriving signal such that the negative portion has a duration shorter than about one microsecond. The backplane disable sensing circuit will not respond to signals of this duration.

LED Device

The LED device provides outputs suitable for directly driving 4½-digit by seven segment common-anode LED displays. They include 28 individual segment drivers and one half-digit driver, each consisting of a low-leakage current-controlled open-drain n-channel transistor.

The drain current of these transistors can be controlled by varying the voltage at the BRighTness input (pin 5). The voltage at this pin is transferred to the gates of the output devices for "on" segments, and thus directly modulates the transistor's "on" resistance. A brightness control can be easily implemented with a single potentiometer controlling the voltage at pin 5, connected as in Figure 3. The potentiometer should be a high value (100kΩ to 1MΩ) to minimize power consumption, which can be significant when the display is off.

The BRighTness input may also be operated digitally as a display enable; when at V_{DD}, the display is fully on, and at V_{SS}, fully off. The display brightness may also be controlled by varying the duty cycle of a signal swinging between the two supplies at the BRighTness input.

Note that the LED devices have two connections for V_{SS}; both should be connected. The double connection is necessary to minimize effects of bond wire resistance with the large total display currents possible.

When operating the LED devices at higher temperatures and/or higher supply voltages, the device power dissipation may need to be reduced to prevent excessive chip temperatures. The maximum power dissipation is 1 watt at 25°C, derated linearly above 35°C to 500mW at 70°C (15mW/°C above 35°C). Power dissipation for the device is given by:

$$P = (V_{DD} - V_{FLED}) \times (I_{SEG}) \times (n_{SEG})$$

where V_{FLED} is the LED forward voltage drop, I_{SEG} is segment current, and n_{SEG} is the number of "ON" segments. It is recommended that if the device is to be operated at elevated temperatures the segment current be limited by use of the BRighTness input to keep power dissipation within the limits described above.

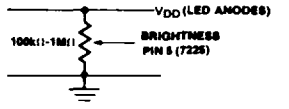

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Figure 3: Brightness Control

COUNTER SECTION

The devices in the ICM7224/ICM7225 family implement a four-digit ripple carry resettable counter, including a Schmitt trigger on the COUNT input and a $\overline{\text{CARRY}}$ output. Also included is an extra D-type flip-flop, clocked by the $\overline{\text{CARRY}}$ signal which controls the half-digit segment driver. This output driver can be used as either a true half-digit or as an overflow indicator. The counter will increment on the negative-going edge of the signal at the COUNT input, while the $\overline{\text{CARRY}}$ output provides a negative-going edge following the count which increments the counter from 9999 to 10000. Once the half-digit flip-flop has been clocked, it can only be reset (with the rest of the counter) by a negative level at the $\overline{\text{RESET}}$ terminal, pin 33. However, the four decades will continue to count in a normal fashion after the half-digit is set, and subsequent $\overline{\text{CARRY}}$ outputs will not be affected.

A negative level at the $\overline{\text{COUNT INHIBIT}}$ input disables the first divide-by-two in the counter chain without affecting its clock. This provides a true inhibit, not sensitive to the state of the COUNT input, which prevents false counts that can result from using a normal logic gate to prevent counting.

Each decade of the counter directly drives a four-to-seven segment decoder which develops the required output data. The output data is latched at the driver. When the $\overline{\text{STORE}}$ pin is low, these latches are updated, and when it is high or floating, the latches hold their contents.

The decoders also include zero detect and blanking logic to provide leading zero blanking. When the Leading Zero Blanking INput is floating or at a positive level, this circuitry is enabled and the device will blank leading zeroes. When it is low, or the half-digit is set, leading zero blanking is inhibited, and zeroes in the four digits will be displayed. The Leading Zero Blanking OUTput is provided to allow cascaded devices to blank leading zeroes correctly. This output will assume a positive level only when all four digits are blanked; this can only occur when the Leading Zero Blanking INput is at a positive level and the half-digit is not set.

For example, in an eight-decade counter with overflow using two ICM7224/ICM7225 devices, the Leading Zero Blanking OUTput of the high order digit would be connected to the Leading Zero Blanking INput of the low order digit device. This will assure correct leading zero blanking for all eight digits.

NOTE: All typical values have been characterized but are not tested

The $\overline{\text{STORE}}$, $\overline{\text{RESET}}$, $\overline{\text{COUNT INHIBIT}}$, and Leading Zero Blanking INputs are provided with pullup devices, so that they may be left open when a positive level is desired. The $\overline{\text{CARRY}}$ and Leading Zero Blanking OUTputs are suitable for interfacing to CMOS logic in general, and are specifically designed to allow cascading of ICM7224 to ICM7225 devices in four-digit blocks.

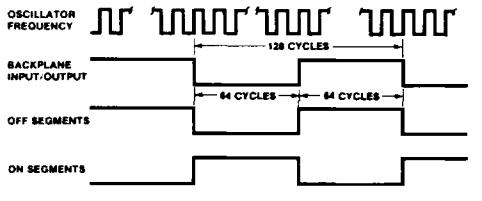

Figure 4: ICM7224 Display Waveforms

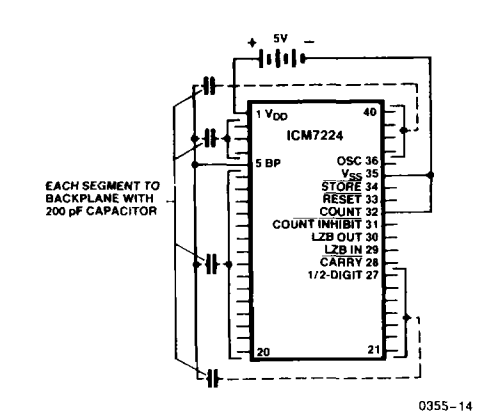

Figure 5: Test Circuit

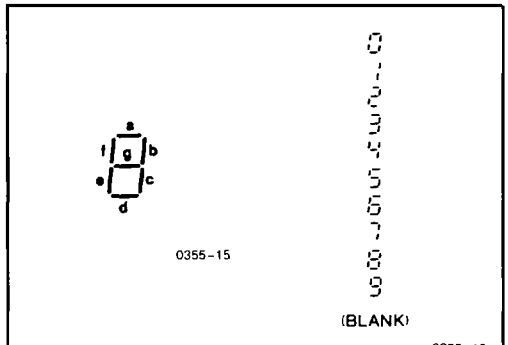

Figure 6: Segment Assignment and Display Font

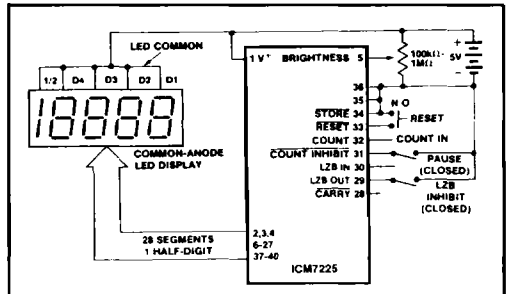

Figure 7: Typical Application (Unit Counter)

APPLICATIONS

Figures 7 and 8 show two typical applications for ICM7224/25 devices.

In Figure 7 an ICM7225, LED display and a few passive components form a unit counter. The device counts and totals the input pulses. Since the $\overline{\text{STORE}}$ input is tied to V_{SS} the display simultaneously updates the counts. The circuit has switches for pause operation, leading zero blanking control, and a pushbutton for resetting the counter.

Figure 8 shows an 8-digit precision frequency counter. The circuit uses two ICM7224s cascaded to provide an 8-digit display. Backplane output of the second device is disabled and is driven by the first device. The ½ digit output of the second device is used for overflow indication. The input signal is fed to the first device and the COUNT input of the second is driven by the $\overline{\text{CARRY}}$ output of the first. Notice that leading zero blanking is controlled on the second device and the LZB OUT of the second one is tied to LZB IN of the first one. An ICM7207A device is used as a timebase generator and frequency counter controller. It generates count window, store and reset signals which are directly compatible with ICM7224 inputs (notice the need for *an inverter at* $\overline{\text{COUNT INHIBIT}}$ *input*). *The ICM7207A provides* two count window signals (1s and 0.1s gating) for displaying frequencies in Hz or tens of Hz (× 10 Hz).

NOTE. All typical values have been characterized but are not tested.

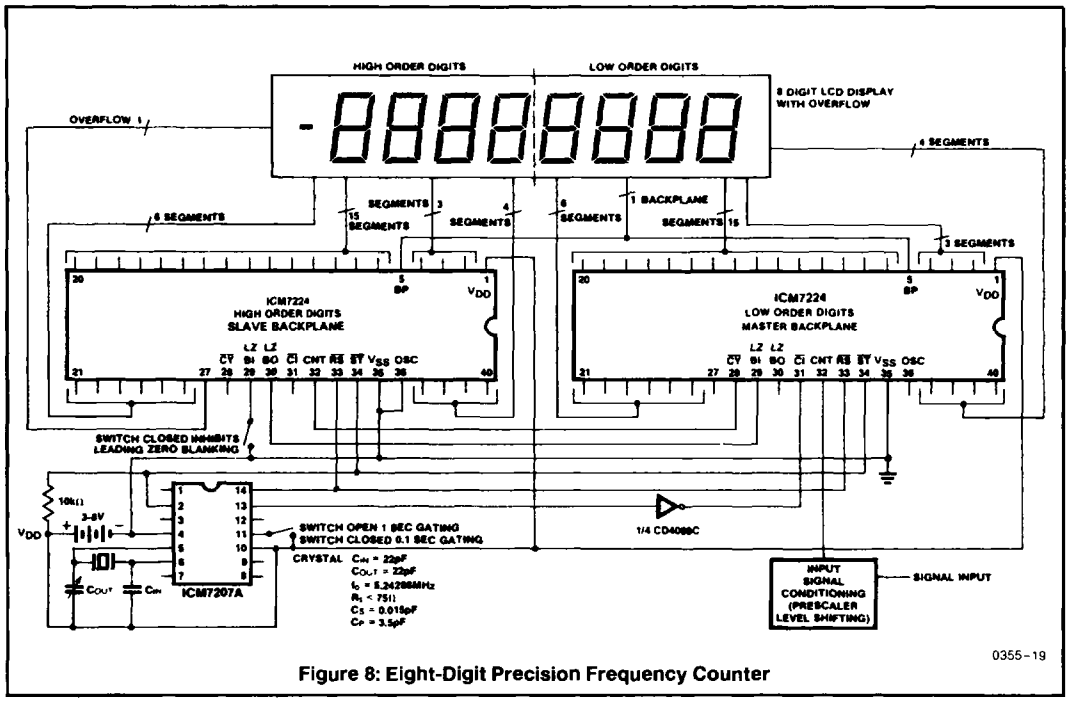

Figure 8: Eight-Digit Precision Frequency Counter

NOTE: All typical values have been characterized but are not tested.