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April 1st, 2010 Renesas Electronics Corporation

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MOS FIELD EFFECT TRANSISTOR 2SJ599

SWITCHING P-CHANNEL POWER MOS FET

DESCRIPTION

The 2SJ599 is P-channel MOS Field Effect Transistor designed for solenoid, motor and lamp driver.

FEATURES

• Low on-state resistance:

 $R_{DS(on)1} = 75 \text{ m}\Omega$ MAX. (Vgs = -10 V, ID = -10 A)

 $R_{DS(on)2} = 111 \text{ m}\Omega \text{ MAX.} \text{ (Vgs} = -4.0 \text{ V, ID} = -10 \text{ A)}$

Low input capacitance:

Ciss = 1300 pF TYP. (VDS = -10 V, VGS = 0 V)

- · Built-in gate protection diode
- TO-251/TO-252 package

ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

Drain to Source Voltage (Vgs = 0 V)	Voss	-60	V
Gate to Source Voltage (VDS = 0 V)	VGSS	∓20	V
Drain Current (DC) (Tc = 25°C)	$I_{D(DC)}$	∓20	Α
Drain Current (pulse) Note1	I _{D(pulse)}	∓50	Α
Total Power Dissipation (Tc = 25°C)	PT	35	W
Total Power Dissipation (T _A = 25°C)	PT	1.0	W
Channel Temperature	T_ch	150	°C
Storage Temperature	T_{stg}	-55 to +150	°C
Single Avalanche Current Note2	las	-20	Α
Single Avalanche Energy Note2	Eas	40	mJ

Notes 1. PW \leq 10 μ s, Duty Cycle \leq 1%

2. Starting T_{ch} = 25°C, V_{DD} = -30 V, R_G = 25 Ω , V_{GS} = -20 \rightarrow 0 V

ORDERING INFORMATION

<u> </u>					
PART NUMBER	PACKAGE				
2SJ599	TO-251 (MP-3)				
2SJ599-Z	TO-252 (MP-3Z)				

(TO-251)



(TO-252)



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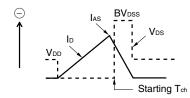
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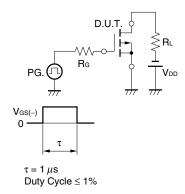
ELECTRICAL CHARACTERISTICS (TA = 25°C)

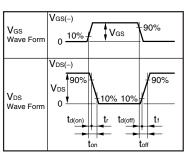
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	IDSS	V _{DS} = -60 V, V _{GS} = 0 V			-10	μА
Gate Leakage Current	lgss	$V_{GS} = \mp 20 \text{ V}, V_{DS} = 0 \text{ V}$			∓10	μΑ
Gate Cut-off Voltage	V _{GS(off)}	$V_{DS} = -10 \text{ V}, I_{D} = -1 \text{ mA}$	-1.5	-2.0	-2.5	V
Forward Transfer Admittance	y fs	$V_{DS} = -10 \text{ V}, I_{D} = -10 \text{ A}$	8	16		S
Drain to Source On-state Resistance	RDS(on)1	Vgs = -10 V, ID = -10 A		60	75	mΩ
	RDS(on)2	Vgs = -4.0 V, ID = -10 A		78	111	mΩ
Input Capacitance	Ciss	V _{DS} = -10 V		1300		pF
Output Capacitance	Coss	V _G S = 0 V		240		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		100		pF
Turn-on Delay Time	td(on)	ID = -10 A		8		ns
Rise Time	tr	Vgs = -10 V		9		ns
Turn-off Delay Time	td(off)	V _{DD} = -30 V		52		ns
Fall Time	tf	$R_G = 0 \Omega$		16		ns
Total Gate Charge	Q _G	ID = -20 A		26		nC
Gate to Source Charge	Qgs	V _{DD} = -48 V		5		nC
Gate to Drain Charge	Q _{GD}	V _{GS} = -10 V		7		nC
Body Diode Forward Voltage	V _{F(S-D)}	IF = 20 A, VGS = 0 V		1.0		V
Reverse Recovery Time	trr	IF = 20 A, VGS = 0 V		51		ns
Reverse Recovery Charge	Qrr	$di/dt = 100 A/\mu s$		102		nC

TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

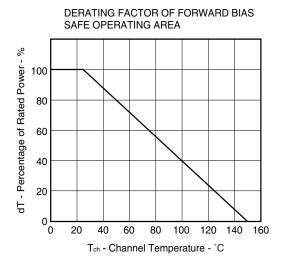


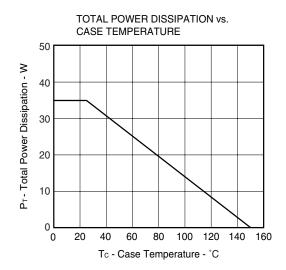


TEST CIRCUIT 3 GATE CHARGE

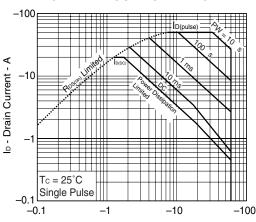
$$\begin{array}{c|c} D.U.T. \\ \hline \\ I_G = -2 \text{ mA} \\ \hline \\ PG. \\ \hline \\ \end{array}$$

TYPICAL CHARACTERISTICS (TA = 25°C)



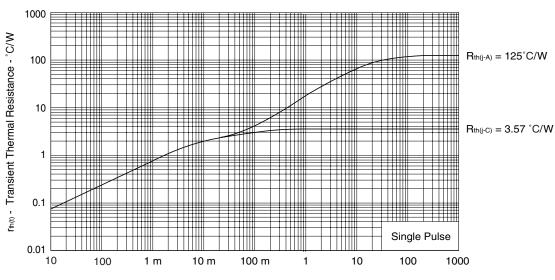


FORWARD BIAS SAFE OPERATING AREA



VDS - Drain to Source Voltage - V

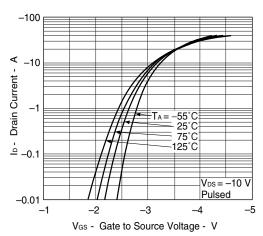
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



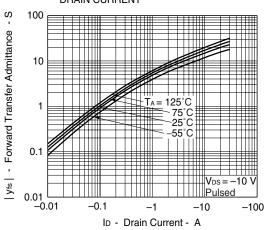
PW - Pulse Width - s

DDS 3

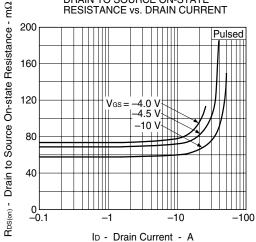
FORWARD TRANSFER CHARACTERISTICS



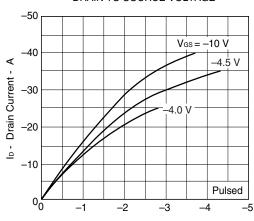
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT 200

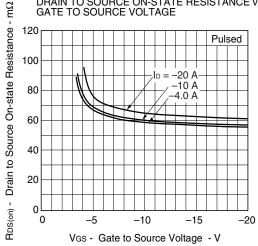


DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE

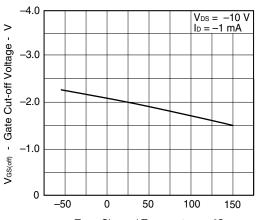


V_{DS} - Drain to Source Voltage - V

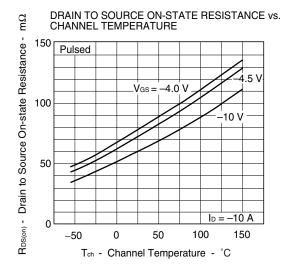
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

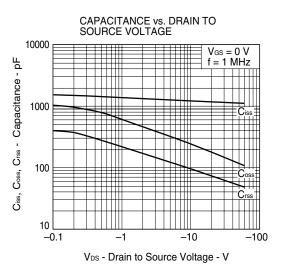


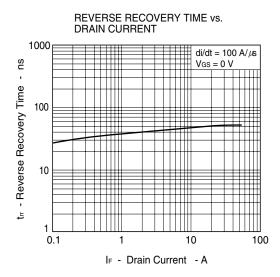
GATE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE

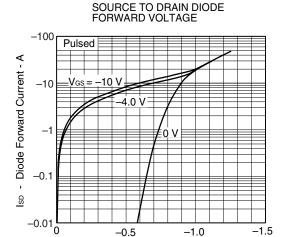


 T_{ch} - Channel Temperature - $^{\circ}C$

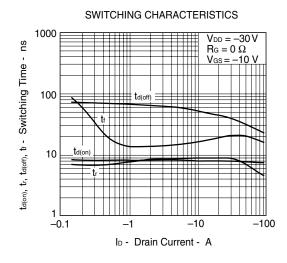


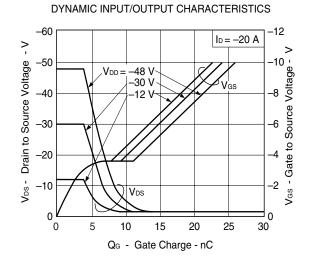


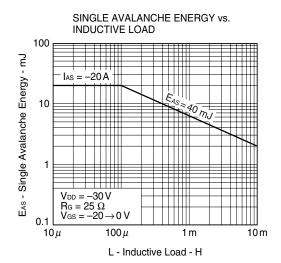


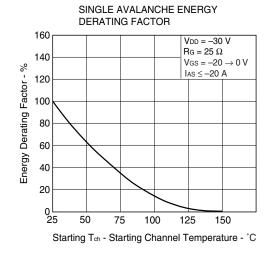


VsD - Source to Drain Voltage - V

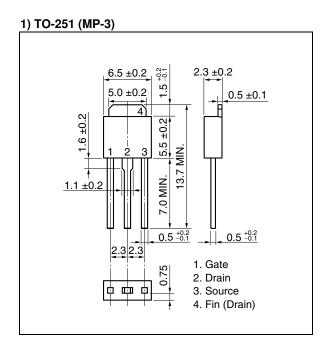


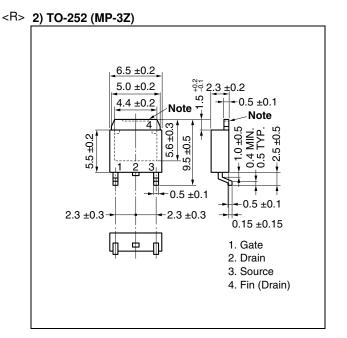






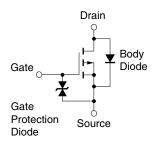
PACKAGE DRAWINGS (Unit: mm)





Note The depth of notch at the top of the fin is from 0 to 0.2 mm.

EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD.

When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

Data Sheet D14644EJ4V0DS 7

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