ADS7142-Q1 Automotive, 2-Channel, 12-Bit, 140-kSPS, I²C-Compatible ADC With Programmable Threshold and Host Wake-Up Features

1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: –40°C to +125°C, T_A
- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- Small package size: 3 mm × 2 mm
- 12-bit noise-free resolution
- Up to 140-kSPS sampling rate
- Efficient host sleep and wake-up:
  - Autonomous monitoring at 900 nW
  - Windowed comparator for event-triggered host wake-up
- Independent configuration and calibration:
  - Dual-channel, pseudo-differential, or ground-sense input configuration
  - Programmable thresholds for calibration
  - Internal calibration improves offset and drift
- False trigger prevention:
  - Programmable thresholds per channel
  - Programmable hysteresis for noise immunity
  - Event counter for transient rejection
- I²C interface:
  - Compatible from 1.65 V to 3.6 V
  - 8 configurable addresses
  - Up to 3.4 MHz (high speed)
- Analog supply: 1.65 V to 3.6 V

2 Applications

General-purpose voltage, current and temperature monitoring in:

- Digital cockpit processing unit
- Driver monitoring
- Automotive head unit
- Automotive camera module without processing

3 Description

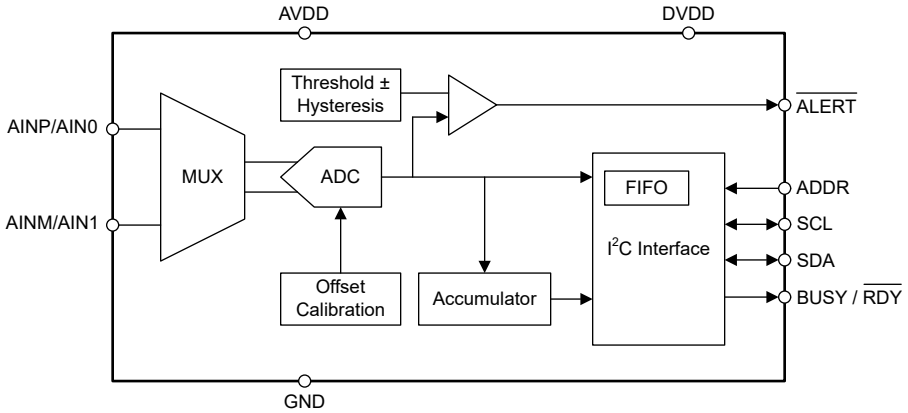
The ADS7142-Q1 is a 12-bit, 140-kSPS successive-approximation register (SAR) analog-to-digital converter (ADC) that can autonomously monitor signals while maximizing system power, reliability, and performance. The device implements event-triggered interrupts per channel using a digital window comparator with programmable high and low thresholds, hysteresis, and event counter. The device includes a dual-channel analog multiplexer in front of a SAR ADC followed by an internal data buffer for converting and capturing data from sensors.

The ADS7142-Q1 is available in a 10-pin WSON package and can achieve low power consumption of only 900 nW. The small form-factor and low-power consumption make this device designed for space-constrained applications.

Package Information(1)

PART NAME	PACKAGE	BODY SIZE (NOM)
ADS7142-Q1	WSON (10)	3.00 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Block Diagram

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (October 2019) to Revision B (September 2022)	Page
• *Updated the numbering format for tables, figures, and cross-references throughout the document*	1
• Changed all instances of legacy terminology to *controller* and *peripheral* where SPI is mentioned	1
• Added *Functional Safety-Capable* bullets to *Features* section	1
• Added links to *Applications* section	1
• Changed *Block Diagram* image in *Description* section	1
• Changed low-power oscillator to high-speed oscillator in test condition for analog supply current in *Electrical Characteristics : Autonomous Modes* section	7
• Changed high-power oscillator to high-speed oscillator in test condition for digital supply current in *Electrical Characteristics : Autonomous Modes* section	7
• digital	8
• Changed *Functional Block Diagram* figure	19
• Added remote ground sense to single-ended configuration discussion of *Single-Channel, Single-Ended Configuration With Remote Ground Sense* section	21
• Clarified normal device operation in *Offset Calibration* section	21

Changes from Revision * (November 2018) to Revision A (October 2019)	Page
• Changed document status from advance information to production data	1

5 Pin Configuration and Functions

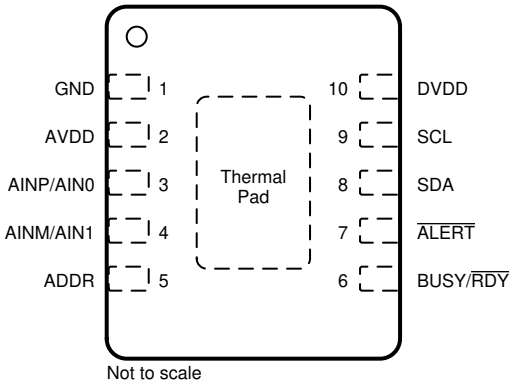


Figure 5-1. DQC Package, 10-Pin WSON (Top View)

Table 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	GND	Supply	Ground for power supply, all analog and digital signals are referred to this pin.
2	AVDD	Supply	Analog supply input, also used as the reference voltage for analog-to-digital conversion.
3	AINP/AIN0	Analog input	Single-channel operation: positive analog signal input. Two-channel operation: analog signal input, channel 0.
4	AINM/AIN1	Analog input	Single-channel operation: negative analog signal input. Two-channel operation: analog signal input, channel 1.
5	ADDR	Analog Input	Input for selecting the I^2C address of the device. See the *I^2C Address Selector* section for details.
6	BUSY/ $\overline{\text{RDY}}$	Digital output	The device pulls this pin high when scanning through channels in a sequence and brings this pin low when the sequence is completed or aborted.
7	$\overline{\text{ALERT}}$	Digital output	Active low, open-drain output. The status of this pin is controlled by the digital window comparator block. Connect a pullup resistor from DVDD to this pin.
8	SDA	Digital input/output	Serial data input/output for the I^2C interface. Connect a pullup resistor from DVDD to this pin.
9	SCL	Digital input	Serial clock for the I^2C interface. Connect a pullup resistor from DVDD to this pin.
10	DVDD	Supply	Digital I/O supply voltage.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
ADDR to GND	–0.3	AVDD + 0.3	V
AVDD to GND	–0.3	3.9	V
DVDD to GND	–0.3	3.9	V
AINP/AIN0 to GND	–0.3	AVDD + 0.3	V
AINM/AIN1 to GND	–0.3	AVDD + 0.3	V
Input current on any pin except supply pins	–10	10	mA
Digital input to GND	–0.3	DVDD + 0.3	V
Junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}	–60	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged-device model (CDM), per AEC Q100-011	Corner pins (1, 5, 6, and 10)	±750	
			All other pins	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
AVDD	Analog supply voltage range	1.65		3.6	V
DVDD	Digital supply voltage range	1.65		3.6	V
T_A	Ambient temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		ADS7142-Q1 DQC (WSON) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	61.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	66.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	29.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	2.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	29.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	6.1	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics: All Modes

at T_A = -40°C to 125°C, AVDD = 3 V, DVDD = 1.65 V to 3.6 V, All Channel Configurations (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT (Two-Channel Single-Ended Configuration)						
	Full-scale input voltage span(1)	AINP/AIN0 to GND or AINM/AIN1 to GND	0		AVDD	V
	Absolute input voltage range	AINP/AIN0 to GND or AINM/AIN1 to GND	–0.1		AVDD + 0.1	V
ANALOG INPUT (Single-Channel Single-Ended Configuration with Remote Ground Sense)						
	Full-scale input voltage span(1)	AINP/AIN0 to AINM/AIN1	0		AVDD	V
	Absolute input voltage range	AINP/AIN0 to GND	–0.1		AVDD + 0.1	V
		AINM/AIN1 to GND	–0.1		0.1	
ANALOG INPUT (Single-Channel Pseudo-Differential Configuration with Remote Ground Sense)						
	Full-scale input voltage span(1)	AINP/AIN0 to AINM/AIN1	–AVDD/2		AVDD/2	V
	Absolute input voltage range	AINP/AIN0 to GND	–0.1		AVDD + 0.1	V
		AINM/AIN1 to GND	AVDD/2 – 0.1		AVDD/2 + 0.1	
INTERNAL OSCILLATOR						
t_{HSO}	Time period for high-speed oscillator			50	110	ns
t_{LPO}	Time period for low-power oscillator			95.2	300	µs
DIGITAL INPUT/OUTPUT (SCL, SDA)						
V_{IH}	High-level input voltage		0.7 × DVDD		DVDD	V
V_{IL}	Low-level input voltage		0		0.3 × DVDD	V
V_{OL}	Low-level output voltage	With 3 mA sink current and DVDD > 2 V	0		0.4	V
		With 3 mA sink current and 1.65 V < DVDD < 2 V	0		0.2 × DVDD	
I_{OL}	Low-level output current (sink)	V_{OL} = 0.4 V for standard and fast mode (100, 400 kHz)	3			mA
		V_{OL} = 0.6 V for fast mode (400 kHz)	6			
		V_{OL} = 0.4 V fast mode Plus (1 MHz)	20			
I_{OL}	Low-level output current (sink)	V_{OL}= 0.4 V high speed (1.7 MHz, 3.4 MHz)	25			mA
I_I	Input current on pin				10	µA
C_I	Input capacitance on pin				10	pF
DIGITAL OUTPUT (BUSY/$\overline{\text{RDY}}$)						
V_{OH}	High-level output voltage	I_{source} = 200 µA	0.8 × DVDD		DVDD	V
		I_{source} = 2 mA	0.7 × DVDD		DVDD	
V_{OL}	Low-level output voltage	I_{sink} = 200 µA	0		0.2 × DVDD	V
		I_{sink} = 2 mA	0		0.3 × DVDD	
DIGITAL OUTPUT ($\overline{\text{ALERT}}$)						
I_{OL}	Low-level output current	V_{OL} < 0.25 V		5		mA
V_{OL}	Low-level output voltage	I_{sink} = 5 mA	0		0.25	V
POWER-SUPPLY REQUIREMENTS						
AVDD	Analog supply voltage		1.65		3.6	V
DVDD	Digital I/O supply voltage		1.65		3.6	V

(1) Ideal Input span, does not include gain or offset error.

6.6 Electrical Characteristics: Manual Mode

at T_A = -40°C to 125°C, AVDD = 3 V, DVDD = 1.65 V to 3.6 V, All Channel Configurations (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SAMPLING DYNAMICS						
t_{conv}	Conversion time	AVDD = 1.65 V to 3.6 V			1.8	µs
t_{acq}	Acquisition time	AVDD = 1.65 V to 3.6 V		18		T_{SCL}
t_{cycle}	Cycle time	AVDD = 1.65 V to 3.6 V, SCL = 3.4 MHz			7.1	µs
DC SPECIFICATIONS						
	Resolution			12		Bits
NMC	No missing codes	AVDD = 1.65 V to 3.6 V	12			Bits
DNL	Differential nonlinearity	AVDD = 1.65 V to 3.6 V	–0.99	±0.3	1	LSB(1)
INL	Integral nonlinearity		–2.75	±0.5	2.75	LSB
E_O	Offset error	Post offset calibration	–4	±0.5	4	LSB
dV_{OS}/dT	Offset drift with temperature	Post offset calibration		5		ppm/°C
E_G	Gain error		–0.1	±0.03	0.1	%FSR
	Gain error drift with temperature			5		ppm/°C
AC SPECIFICATIONS						
SNR(2)	Signal-to-noise ratio	f_{IN} = 2 kHz, AVDD = 3 V, f_{SAMPLE} = 140 kSPS	68.75	70		dB
		f_{IN} = 2 kHz, AVDD = 1.8 V, f_{SAMPLE} = 140 kSPS		68		
THD(2) (3)	Total harmonic distortion	f_{IN} = 2 kHz, AVDD = 3 V, f_{SAMPLE} = 140 kSPS		–85		dB
		f_{IN} = 2 kHz, AVDD = 1.8 V, f_{SAMPLE} = 140 kSPS		–80		
SINAD(2)	Signal-to-noise and distortion	f_{IN} = 2 kHz, AVDD = 3 V, f_{SAMPLE} = 140 kSPS	68.5	69.5		dB
		f_{IN} = 2 kHz, AVDD = 1.8 V, f_{SAMPLE} = 140 kSPS		67.5		
SFDR(2)	Spurious-free dynamic range	f_{IN} = 2 kHz, AVDD = 3 V, f_{SAMPLE} = 140 kSPS		90		dB
BW	–3-dB small-signal bandwidth			25		MHz
POWER CONSUMPTION						
I_{AVDD}	Analog supply current	f_{SAMPLE} = 140 kSPS, SCL = 3.4 MHz		265	300	µA
		f_{SAMPLE}= 5.5 kSPS, SCL = 100 kHz		8		
		f_{SAMPLE} = 140 kSPS, SCL = 3.4 MHz, AVDD = 1.8 V		160		
		f_{SAMPLE} = 5.5 kSPS, SCL = 100 kHz, AVDD = 1.8 V		5		
I_{DVDD}	Digital supply current	f_{SAMPLE} = 140 kSPS, SCL = 3.4 MHz, SDA = AAA0h		25		µA
		f_{SAMPLE} = 5.5 kSPS, SCL = 100 kHz, SDA = AAA0h		2		
		f_{SAMPLE} = 140 kSPS, SCL = 3.4 MHz, AVDD = 1.8 V, SDA = AAA0h		15		
I_{AVDD}	Static analog supply current	No activity on SCL and SDA		6		nA
I_{DVDD}	Static digital supply current	No activity on SCL and SDA		2		nA

(1) LSB means least significant byte. See the ADC Transfer Function for details.
(2) All specifications expressed in decibels (dB) refer to the full-scale input (FSR) and are tested with an input signal 0.5 dB below full-scale, unless otherwise specified.
(3) Calculated on the first nine harmonics of the input frequency.

6.7 Electrical Characteristics: Autonomous Modes

at T_A = -40°C to 125°C, AVDD = 3 V, DVDD = 1.65 V to 3.6 V, All Channel Configurations (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SAMPLING DYNAMICS						
t_{conv}	Conversion time	High-speed oscillator		14		t_{HSO}
		Low-power oscillator		14		t_{LPO}
t_{acq}	Acquisition time	High-speed oscillator	7			t_{HSO}
		Low-power oscillator	4			t_{LPO}
t_{cycle}	Cycle time	High-speed oscillator		nCLK		t_{HSO}
		Low-power oscillator		nCLK		t_{LPO}
DC SPECIFICATIONS						
	Resolution			12		Bits
E_O	Offset error	Post offset calibration		±0.5		LSB
E_G	Gain error			±0.03		%FSR
POWER CONSUMPTION						
I_{AVDD}	Analog supply current	With low-power oscillator, nCLK = 18		0.75		µA
		With low-power oscillator, AVDD = 1.8 V, nCLK = 18		0.45		
		With low-power oscillator, nCLK = 250		0.5		
		With high-speed oscillator, nCLK = 21		940		
I_{DVDD}	Digital supply current	With low-power oscillator, nCLK = 18, DVDD = 3.3 V		0.15		µA
		With low-power oscillator, DVDD = 1.8 V, nCLK = 18		0.25		
		With low-power oscillator, nCLK = 250, DVDD = 3.3 V		0.15		
		With high-speed oscillator, nCLK = 21, DVDD = 3.3 V		0.15		
I_{AVDD}	Static analog supply current	No activity on SCL and SDA		5		nA
I_{DVDD}	Static digital supply current	No activity on SCL and SDA		0.6		nA

6.8 Electrical Characteristics: High Precision Mode

at T_A = -40°C to 125°C, AVDD = 3 V, DVDD = 1.65 V to 3.6 V, All Channel Configurations (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC SPECIFICATIONS						
	Resolution(2)			16		Bits
ENOB	Effective number of bits	With DC input of AVDD / 2(3)		15.4		
E_O	Offset error	Post offset calibration		±10		LSB
E_G	Gain error			±0.03		%FSR
POWER CONSUMPTION						
I_{AVDD}	Analog supply current	With low-power oscillator, nCLK = 18		0.6		µA
		With low-power oscillator, AVDD = 1.8 V, nCLK = 18		0.3		
		With low-power oscillator, nCLK = 250		0.5		
		With high-speed oscillator, nCLK = 21		980		
I_{DVDD}	Digital supply current	With low-power oscillator, nCLK = 21, DVDD = 3.3 V		0.2		µA
		With low-power oscillator, DVDD = 1.8 V, nCLK = 21		0.25		
		With low-power oscillator, nCLK = 250, DVDD = 3.3 V		0.2		
		With high-speed oscillator, nCLK = 21, DVDD = 3.3 V		0.2		
I_{AVDD}	Static analog supply current	No activity on SCL and SDA		5		nA
I_{DVDD}	Static supply current	No activity on SCL and SDA		0.7		nA

(1) Sampling dynamics for high precision mode are same as for autonomous modes.
(2) See Equation 5
(3) For DC input, ENOB = Ln[FSR/Standard deviation of Codes]/Ln[2].

6.9 Timing Requirements

at T_A = -40°C to 125°C, AVDD = 3 V, DVDD = 1.65 V to 3.6 V, All Channel Configurations (unless otherwise noted)(1)

PARAMETER		MIN	MAX	UNIT
STANDARD MODE (100 kHz)				
f_{SCL}	SCL clock frequency	0	100	kHz
t_{HD-STA}	Hold time (repeated) START condition	4		µs
t_{LOW}	Low period of SCL	4.7		µs
t_{HIGH}	High period of SCL	4		µs
t_{SU-STA}	Setup time for a repeated start condition	4.7		µs
t_{HD-DAT} (2) (3)	Data hold time	0		µs
t_{SU-DAT}	Data setup time	250		ns
t_{SU-STO}	Data setup time	4		µs
t_{BUF}	Bus free time between a STOP and START condition	4.7		µs
C_b	Capacitive load on each line		400	pF
FAST MODE (400 kHz)				
f_{SCL}	SCL clock frequency	0	400	kHz
t_{HD-STA}	Hold time (repeated) START condition	0.6		µs
t_{LOW}	Low period of SCL	1.3		µs
t_{HIGH}	High period of SCL	0.6		µs
t_{SU-STA}	Setup time for a repeated start condition	0.6		µs
t_{HD-DAT}	Data hold time	0		µs

6.9 Timing Requirements (continued)

at T_A = -40°C to 125°C, AVDD = 3 V, DVDD = 1.65 V to 3.6 V, All Channel Configurations (unless otherwise noted)(1)

PARAMETER		MIN	MAX	UNIT
t_{SU-DAT}	Data setup time	100		ns
t_{SU-STO}	Data setup time	0.6		µs
t_{BUF}	Bus free time between a STOP and START condition	1.3		µs
C_b	Capacitive load on each line		400	pF
FAST MODE PLUS (1000 kHz)				
f_{SCL}	SCL clock frequency	0	1000	kHz
t_{HD-STA}	Hold time (repeated) START condition	0.26		µs
t_{LOW}	Low period of SCL	0.5		µs
t_{HIGH}	High period of SCL	0.26		µs
t_{SU-STA}	Setup time for a repeated start condition	0.26		µs
t_{HD-DAT}	Data hold time	0		µs
t_{SU-DAT}	Data setup time	50		ns
t_{SU-STO}	Data setup time	0.26		µs
t_{BUF}	Bus free time between a STOP and START condition	0.5		µs
C_b	Capacitive load on each line		550	pF
HIGH SPEED MODE (1.7 MHz, C_b = 400 pF max)				
f_{SCLH}	SCLH clock frequency	0	1.7	MHz
t_{HD-STA}	Hold time (repeated) START condition	160		ns
t_{LOW}	Low period of SCL	320		ns
t_{HIGH}	High period of SCL	120		ns
t_{SU-STA}	Setup time for a repeated start condition	160		ns
t_{HD-DAT}	Data hold time	0	150	ns
t_{SU-DAT}	Data setup time	10		ns
t_{SU-STO}	Data setup time	160		ns
C_b	Capacitive load on each line		100	pF
HIGH SPEED MODE (3.4 MHz, C_b = 100 pF max)				
f_{SCLH}	SCLH clock frequency	0	3.4	MHz
t_{HD-STA}	Hold time (repeated) START condition	160		ns
t_{LOW}	Low period of SCL	160		ns
t_{HIGH}	High period of SCL	60		ns
t_{SU-STA}	Setup time for a repeated start condition	160		ns
t_{HD-DAT}	Data hold time	0	70	ns
t_{SU-DAT}	Data setup time	10		ns
t_{SU-STO}	Data setup time	160		ns
C_b	Capacitive load on each line		100	pF

(1) All values referred to $V_{IH(min)}$ (0.7 DVDD) and $V_{IL(max)}$ (0.3 DVDD).
(2) t_{HD-DAT} is the data hold time that is measured from the falling edge of SCL and applies to data in transmission and the acknowledge.
(3) The maximum t_{HD-DAT} can be 3.45 µs and 0.9 µs for standard-mode and fast-mode, but must be less than the maximum of t_{VD-DAT} or t_{VD-ACK} by a transition time. This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock is streched, the data must be valid by the setup time before being released.

6.10 Switching Characteristics

at T_A = -40°C to 125°C, AVDD = 3 V, DVDD = 1.65 V to 3.6 V, All Channel Configurations (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
STANDARD MODE (100 kHz)					
t_{rCL}	Rise time of SCL			1000	ns
t_{rDA}	Rise time of SDA			1000	ns
t_{fCL}	Fall time of SCL			300	ns
t_{fDA}	Fall time of SDA			300	ns
t_{VD-DAT} (2)	Data valid time			3.45	µs
t_{VD-ACK} (2)	Data hold time			3.45	µs
FAST MODE (400 kHz)					
t_{rCL}	Rise time of SCL		20	300	ns
t_{rDA}	Rise time of SDA		20	300	ns
t_{fCL}	Fall time of SCL		20 × DVDD/3.6	300	ns
t_{fDA}	Fall time of SDA		20 × DVDD/3.6	300	ns
t_{VD-DAT}	Data valid time			0.9	µs
t_{VD-ACK}	Data hold time			0.9	µs
t_{SP} (3)	Pulse duration of spikes suppressed by the input filter		0	50	ns
FAST MODE PLUS (1000 kHz)					
t_{rCL}	Rise time of SCL			120	ns
t_{rDA}	Rise time of SDA			120	ns
t_{fCL}	Fall time of SCL		20 × DVDD/3.6	120	ns
t_{fDA}	Fall time of SDA		20 × DVDD/3.6	120	ns
t_{VD-DAT}	Data valid time			0.45	µs
t_{VD-ACK}	Data hold time			0.45	µs
t_{SP}	Pulse duration of spikes suppressed by the input filter		0	50	ns
HIGH SPEED MODE (1.7 MHz, C_b = 400 pF max)					
t_{rCL}	Rise time of SCLH		20	80	ns
t_{rCL1}	Rise time of SCLH after a repeated start condition and after an acknowledge bit		20	160	ns
t_{rDA}	Rise time of SDAH		20	160	ns
t_{fCL}	Fall time of SCLH		20	80	ns
t_{fDA}	Fall time of SDAH		20	160	ns
t_{SP}	Pulse duration of spikes suppressed by the input filter		0	10	ns
HIGH SPEED MODE (3.4 MHz, C_b = 100 pF max)					
t_{rCL}	Rise time of SCLH		10	40	ns
t_{rCL1}	Rise time of SCLH after a repeated start condition and after an acknowledge bit		10	80	ns
t_{rDA}	Rise time of SDAH		10	80	ns
t_{fCL}	Fall time of SCLH		10	40	ns
t_{fDA}	Fall time of SDAH		10	80	ns
t_{SP}	Pulse duration of spikes suppressed by the input filter		0	10	ns

(1) All values referred to $V_{IH(min)}$ (0.7 DVDD) and $V_{IL(max)}$ (0.3 DVDD).
(2) t_{VD-DAT} = time for data signal from SCL LOW to SDA output.
(3) Input filters on the SDA and SCL inputs suppress noise spikes of less than 50 ns.

6.11 Timing Diagrams

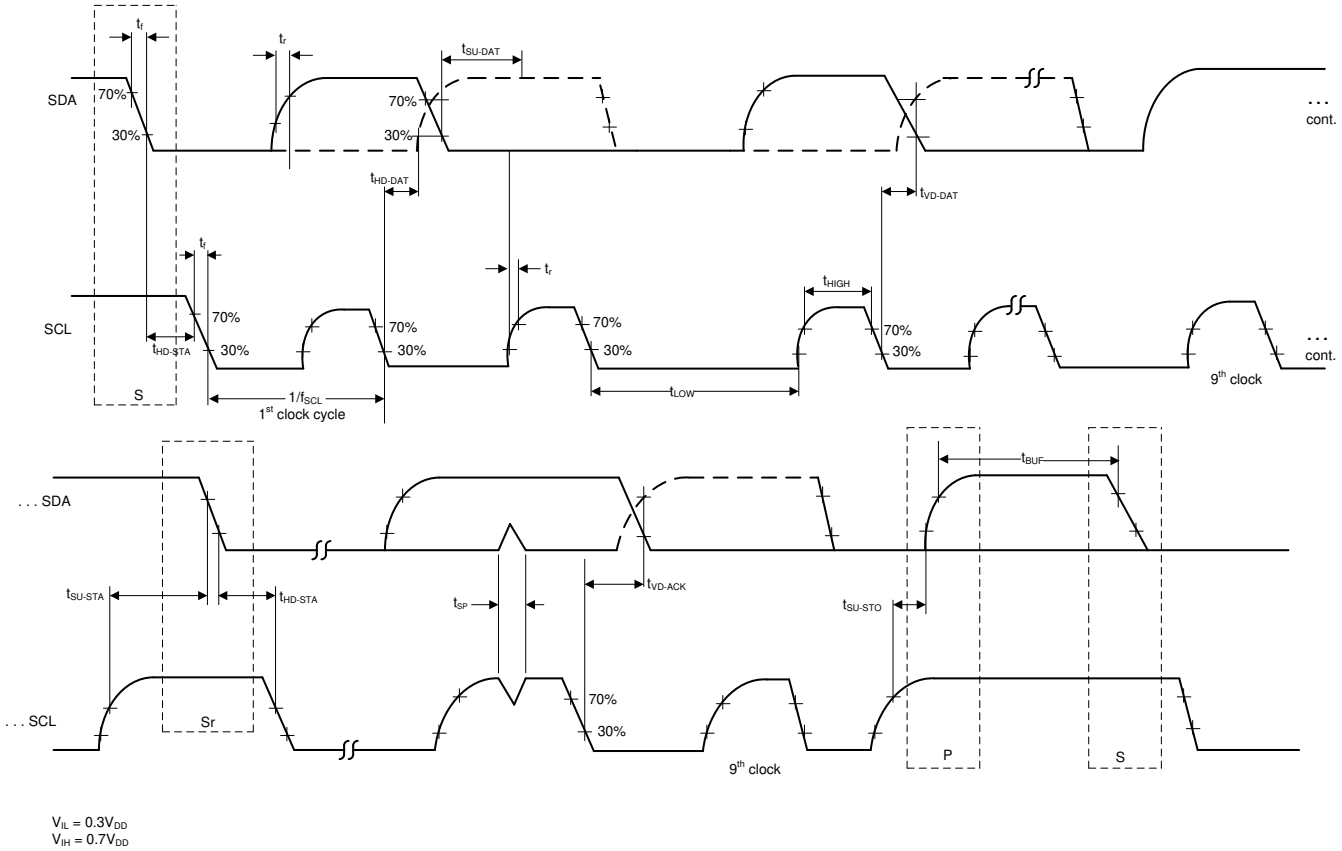
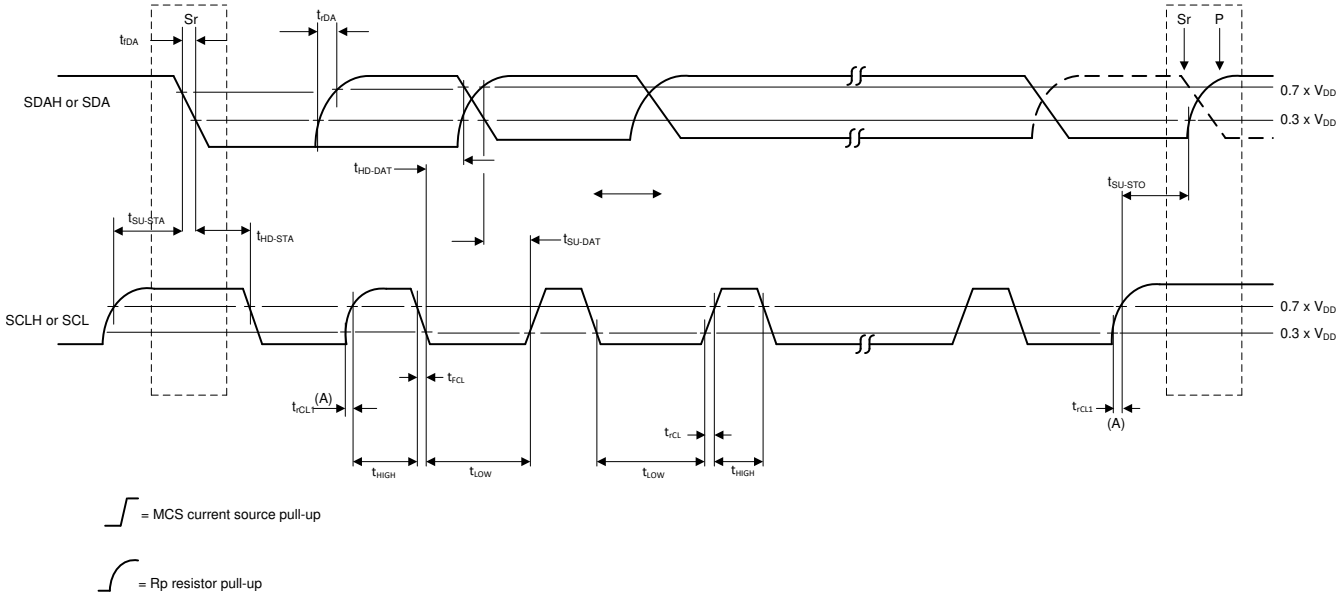


Figure 6-1. Timing Diagram for Standard Mode, Fast Mode, and Fast Mode Plus



A. First rising edge of the SCLH signal after Sr and after each acknowledge bit.

Figure 6-2. Timing Diagram for High-Speed Mode

6.12 Typical Characteristics: All Modes

at T_A = 25°C, AVDD = 3 V, DVDD = 3.3 V, and two-channel single-ended configuration (unless otherwise noted)

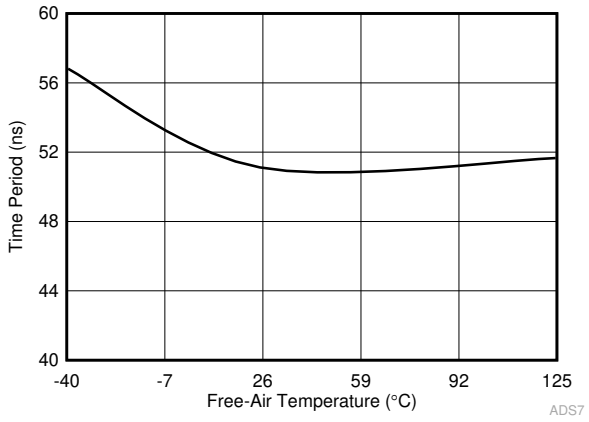


Figure 6-3. High-Speed Oscillator Time Period vs Temperature

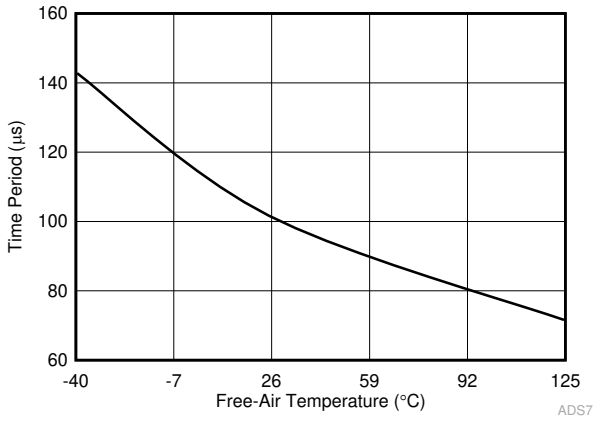
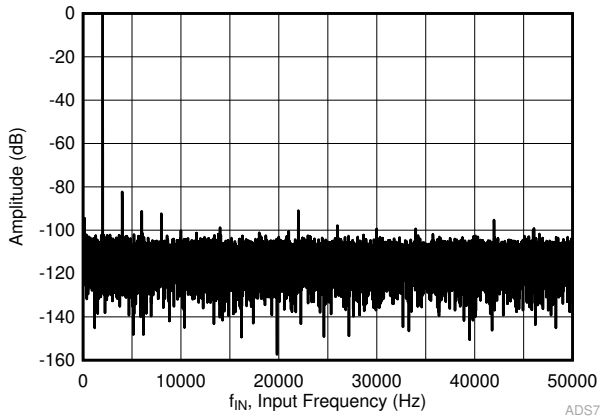


Figure 6-4. Low-Power Oscillator Time Period vs Temperature

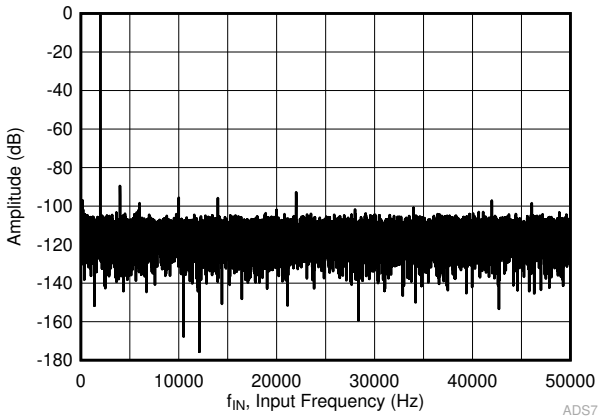
6.13 Typical Characteristics: Manual Mode

at T_A = 25°C, AVDD = 3 V, DVDD = 3.3 V, and two-channel single-ended configuration (unless otherwise noted)



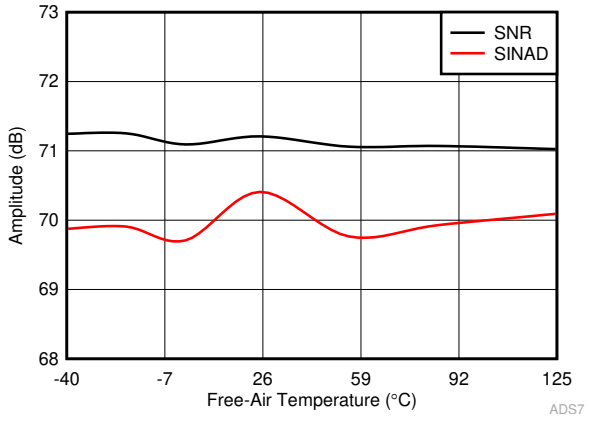
SNR = 69.6 dB, THD = –84 dB, ENOB = 11.2,
f_{sample} = 140 kSPS, SFDR = 87 dB, AVDD = 1.8 V

Figure 6-5. Typical FFT in Manual Mode



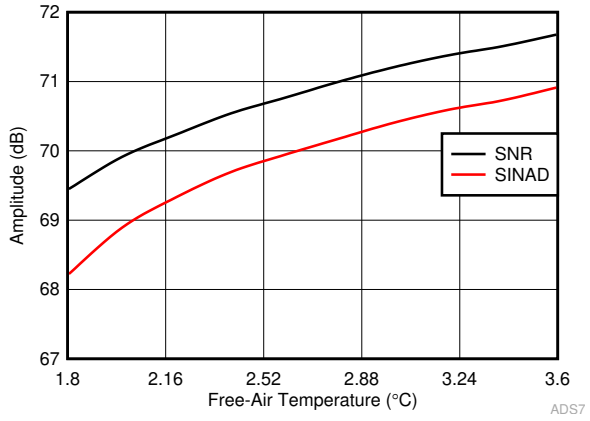
SNR = 71.3 dB, THD = –87 dB, ENOB = 11.5,
f_{sample} = 140 kSPS, SFDR = 89.3 dB, AVDD = 3 V

Figure 6-6. Typical FFT in Manual Mode



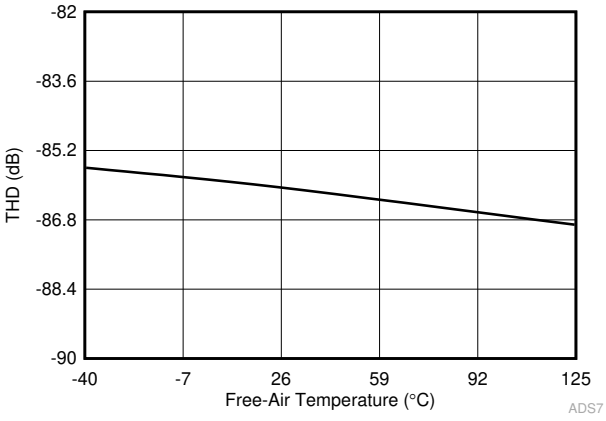
f_{sample} = 140 kSPS

Figure 6-7. SNR and SINAD in Manual Mode vs Temperature



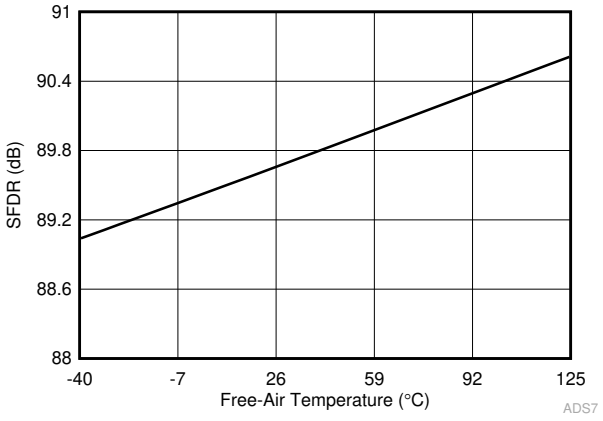
f_{sample} = 140 kSPS

Figure 6-8. SNR and SINAD in Manual Mode vs AVDD



f_{sample} = 140 kSPS

Figure 6-9. THD in Manual Mode vs Temperature

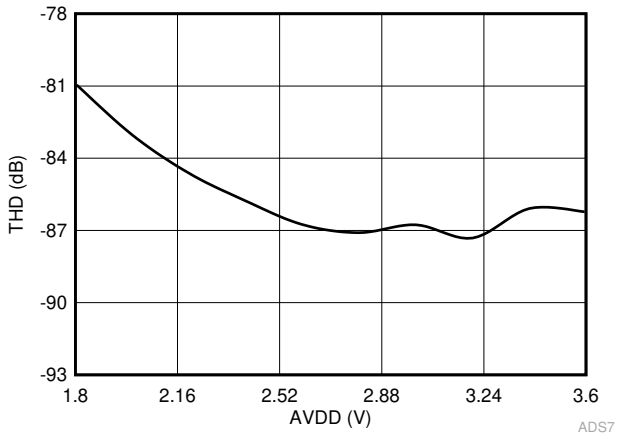


f_{sample} = 140 kSPS

Figure 6-10. SFDR in Manual Mode vs Temperature

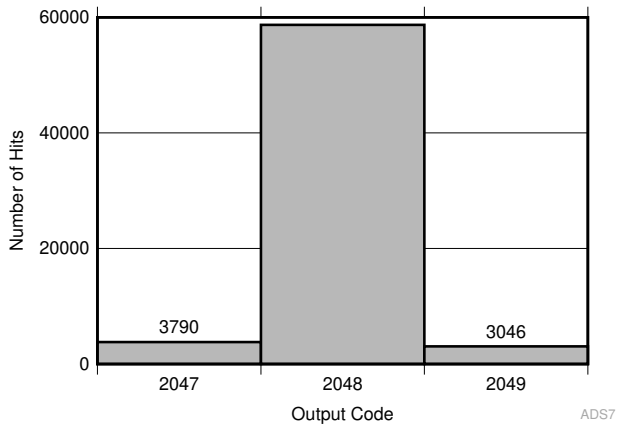
6.13 Typical Characteristics: Manual Mode (continued)

at T_A = 25°C, AVDD = 3 V, DVDD = 3.3 V, and two-channel single-ended configuration (unless otherwise noted)



f_{sample} = 140 kSPS

Figure 6-11. THD in Manual Mode vs AVDD



Mean code = 2047.9, standard deviation = 0.32

Figure 6-12. Typical DC Code Spread in Manual Mode

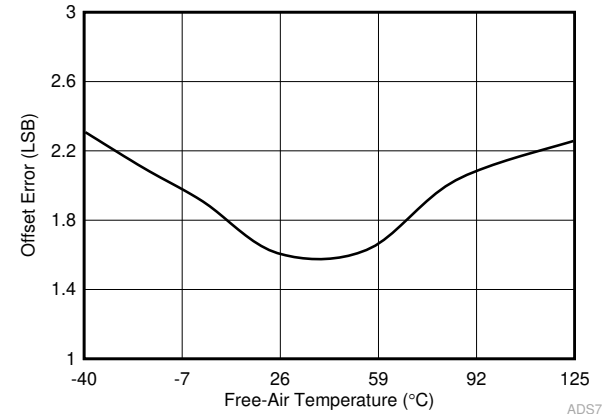


Figure 6-13. Offset Error in Manual Mode vs Temperature

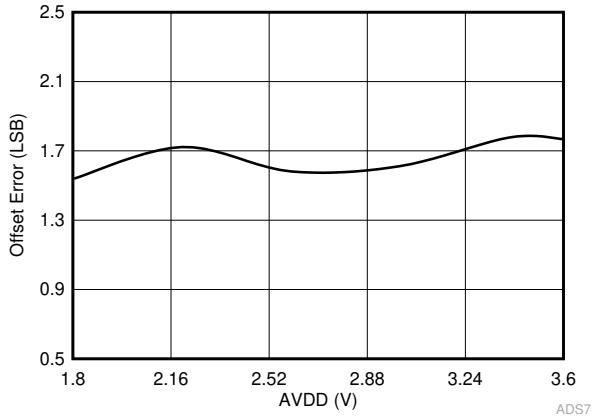


Figure 6-14. Offset Error in Manual Mode vs AVDD

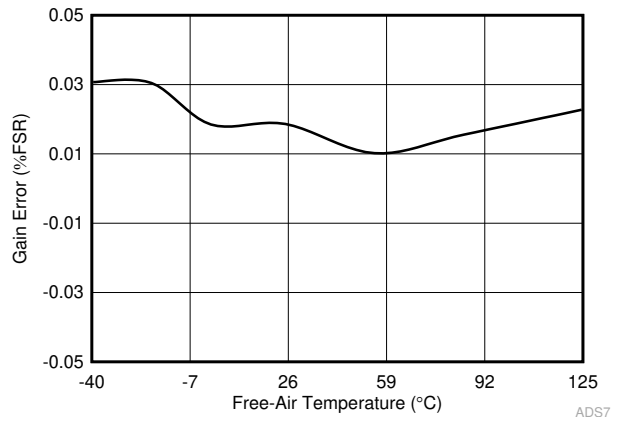


Figure 6-15. Gain Error in Manual Mode vs Free-Air Temperature

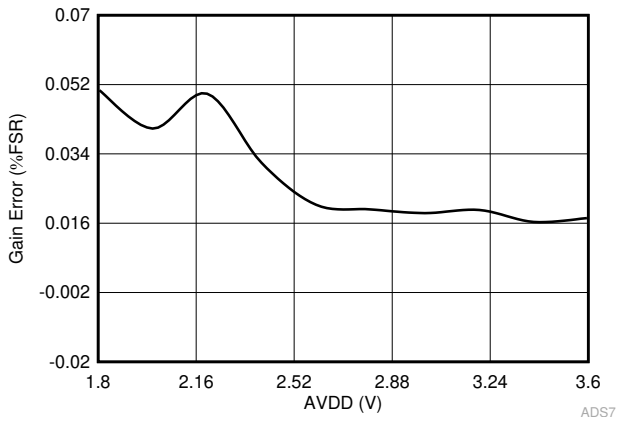
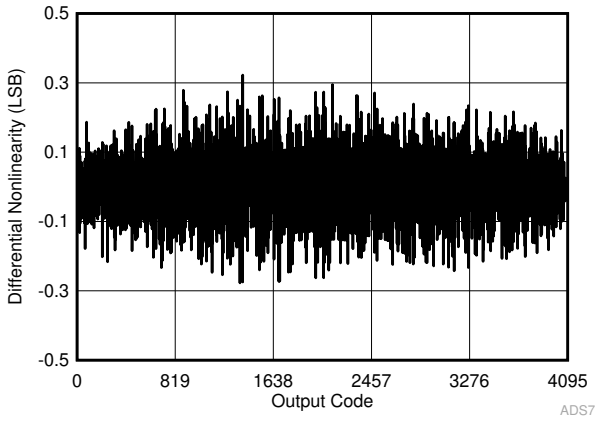


Figure 6-16. Gain Error in Manual Mode vs AVDD

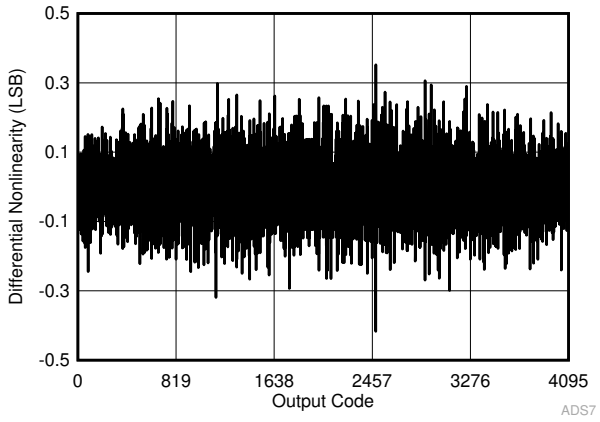
6.13 Typical Characteristics: Manual Mode (continued)

at T_A = 25°C, AVDD = 3 V, DVDD = 3.3 V, and two-channel single-ended configuration (unless otherwise noted)



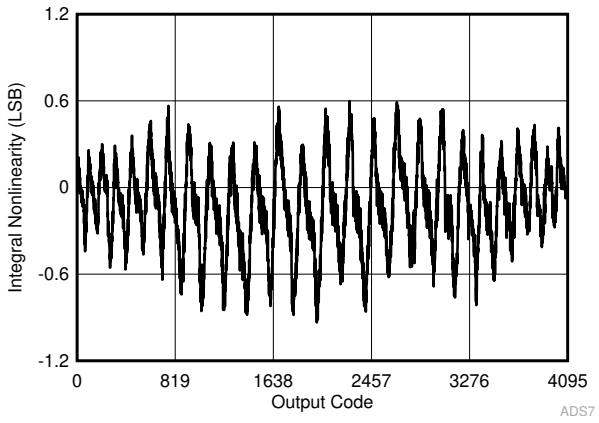
AVDD = 3 V

Figure 6-17. Typical DNL in Manual Mode



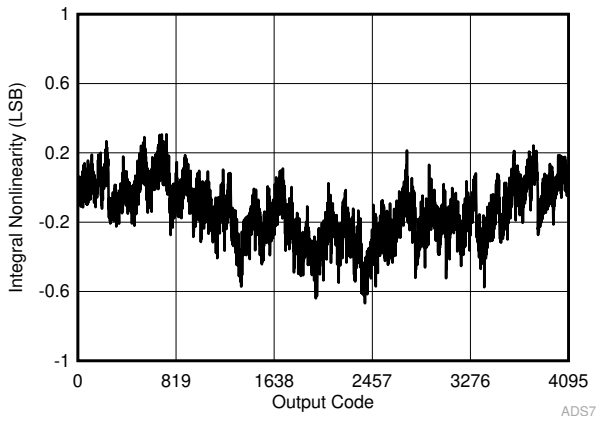
AVDD = 1.8 V

Figure 6-18. Typical DNL in Manual Mode



AVDD = 3 V

Figure 6-19. Typical INL in Manual Mode



AVDD = 1.8 V

Figure 6-20. Typical INL in Manual Mode

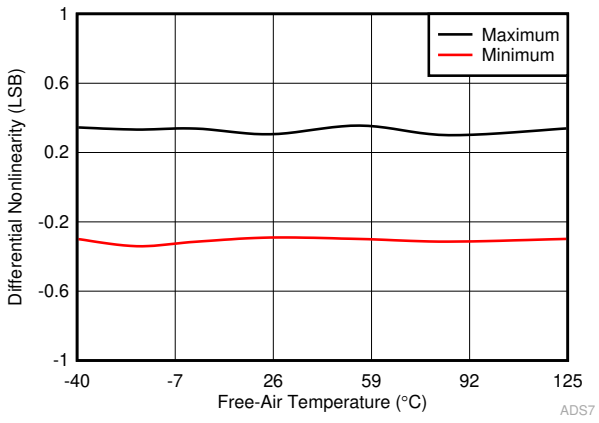


Figure 6-21. DNL in Manual Mode vs Temperature

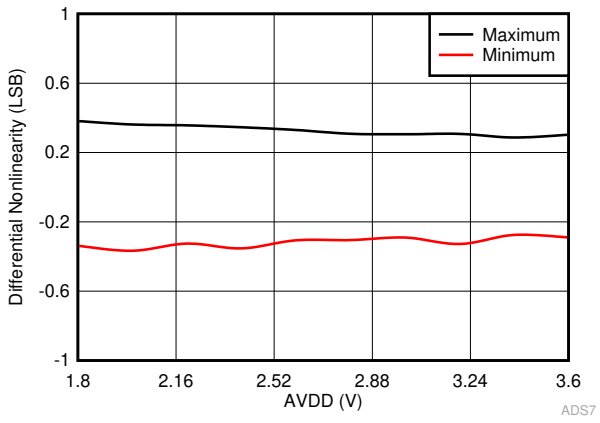


Figure 6-22. DNL in Manual Mode vs AVDD

6.13 Typical Characteristics: Manual Mode (continued)

at T_A = 25°C, AVDD = 3 V, DVDD = 3.3 V, and two-channel single-ended configuration (unless otherwise noted)

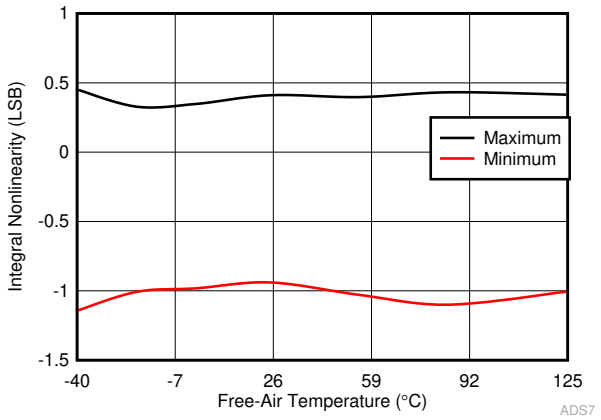


Figure 6-23. INL in Manual Mode vs Temperature

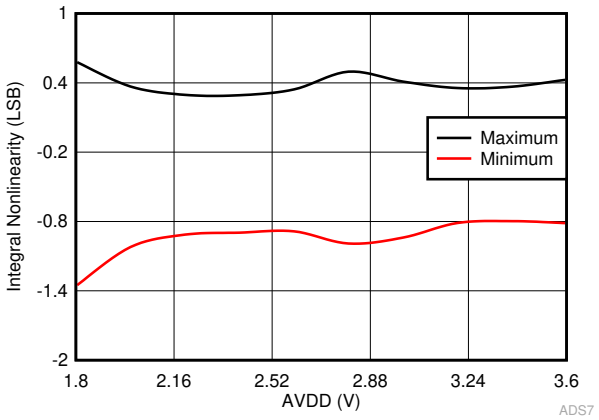
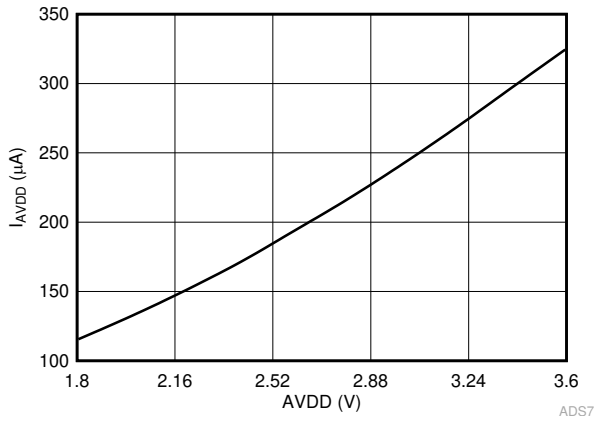


Figure 6-24. INL in Manual Mode vs AVDD



f_{Sample} = 140 kSPS, SCL = 3.4 MHz

Figure 6-25. I_{AVDD} in Manual Mode vs AVDD

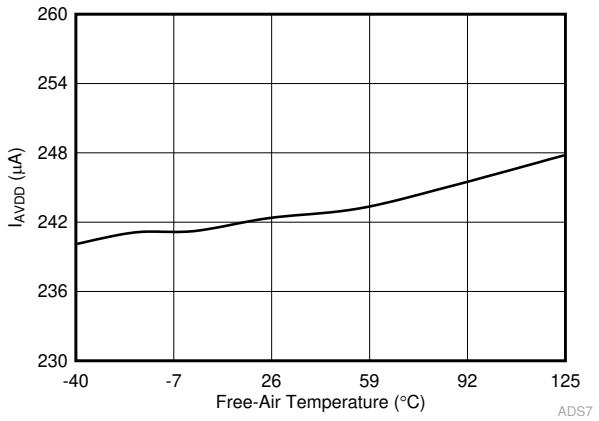
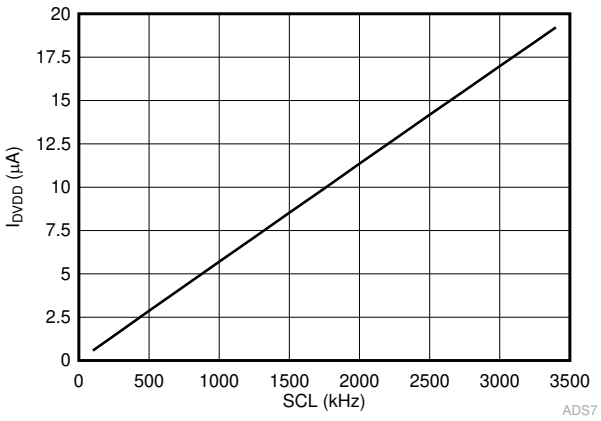
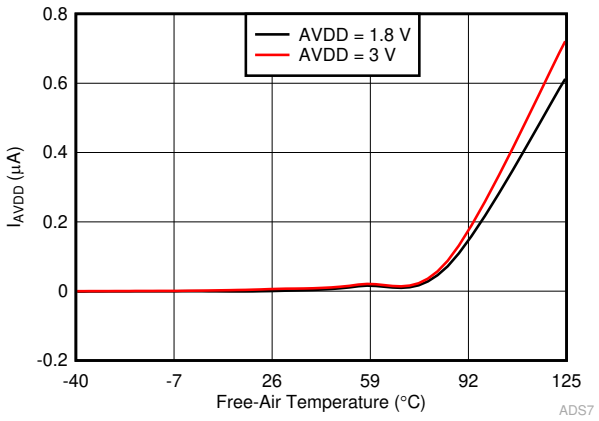


Figure 6-26. I_{AVDD} in Manual Mode vs Temperature



DVDD = 1.8 V

Figure 6-27. I_{DVDD} in Manual Mode vs SCL

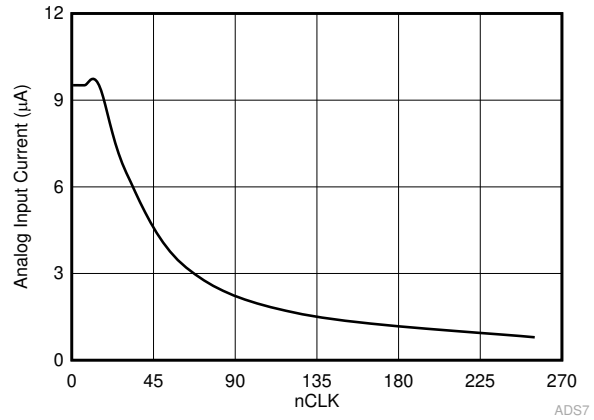


No activity on SCL and SDA

Figure 6-28. Static I_{AVDD} in Manual Mode vs Temperature

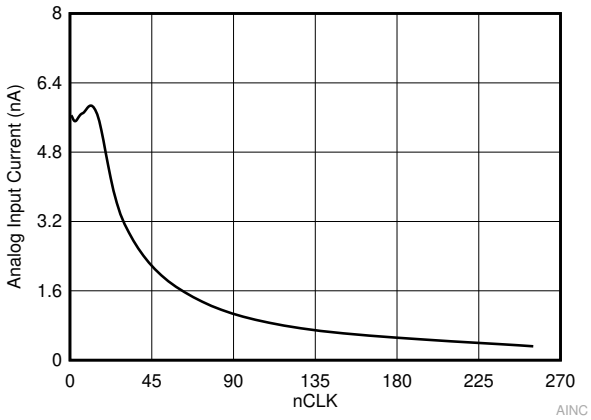
6.14 Typical Characteristics: Autonomous Modes

at T_A = 25°C, AVDD = 3 V, DVDD = 3.3 V, and two-channel single-ended configuration (unless otherwise noted)



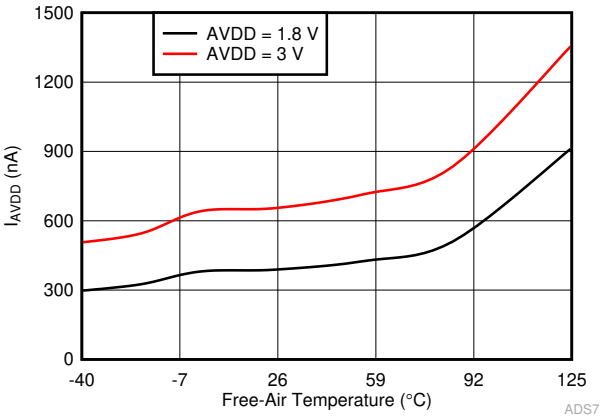
Input voltage = 1.5 V, CH0, high-speed oscillator, stop burst mode

Figure 6-29. Analog Input Current in Autonomous Modes vs nCLK



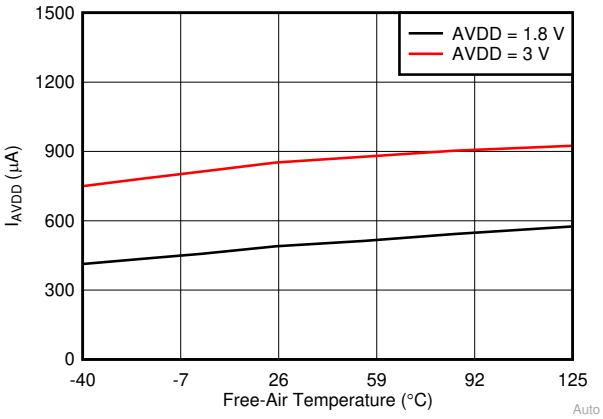
Input voltage = 1.5 V, CH0, low-power oscillator, stop burst mode

Figure 6-30. Analog Input Current in Autonomous Modes vs nCLK



Stop burst mode, low-power oscillator, nCLK = 25

Figure 6-31. I_{AVDD} in Autonomous Modes vs Temperature



Stop burst mode, high-speed oscillator, nCLK = 25

Figure 6-32. I_{AVDD} in Autonomous Modes vs Temperature

6.15 Typical Characteristics: High-Precision Mode

at T_A = 25°C, AVDD = 3 V, DVDD = 3.3 V, and two-channel single-ended configuration (unless otherwise noted)

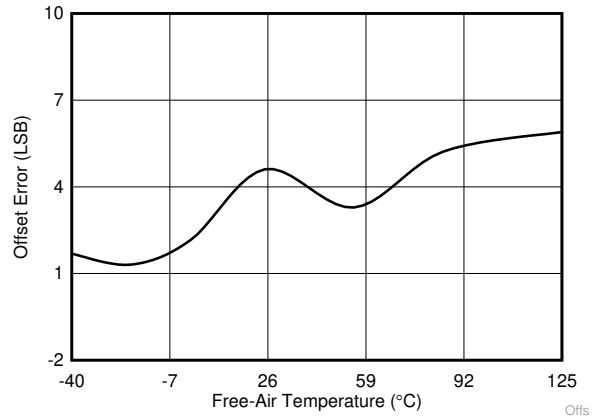


Figure 6-33. Offset Error in High-Precision Mode vs Temperature

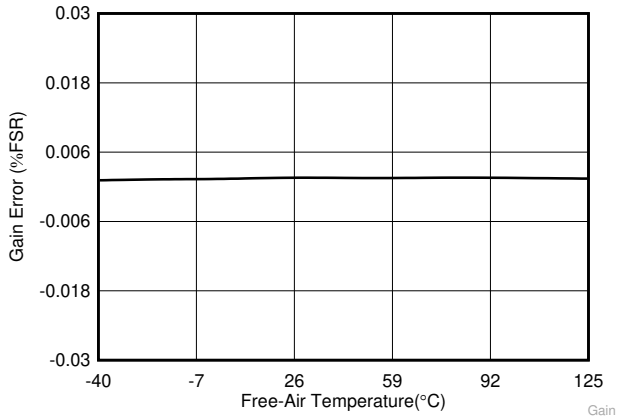
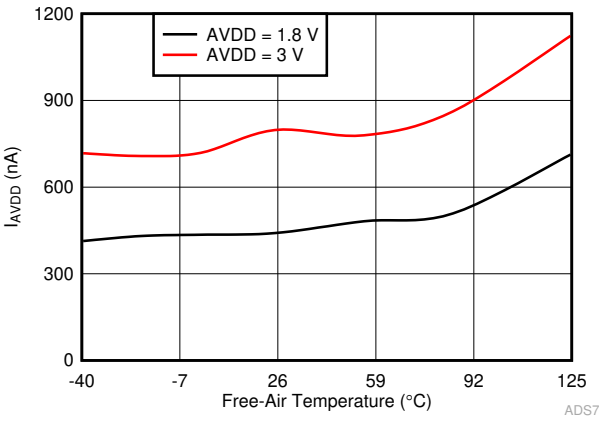
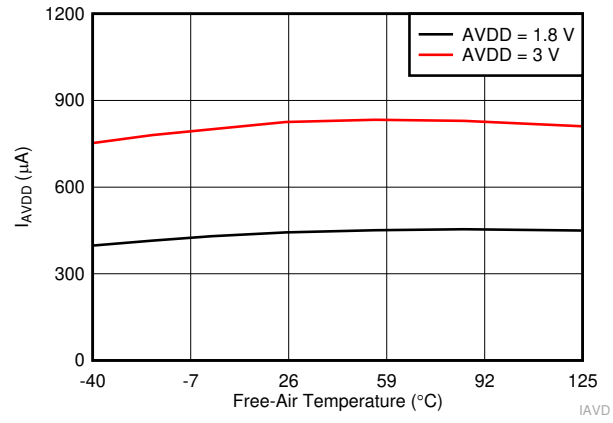


Figure 6-34. Gain Error in High-Precision Mode vs Temperature



Low-power oscillator, nCLK = 25

Figure 6-35. I_{AVDD} in High-Precision Mode vs Temperature



High-speed oscillator, nCLK = 25

Figure 6-36. I_{AVDD} in High-Precision Mode vs Temperature

7 Detailed Description

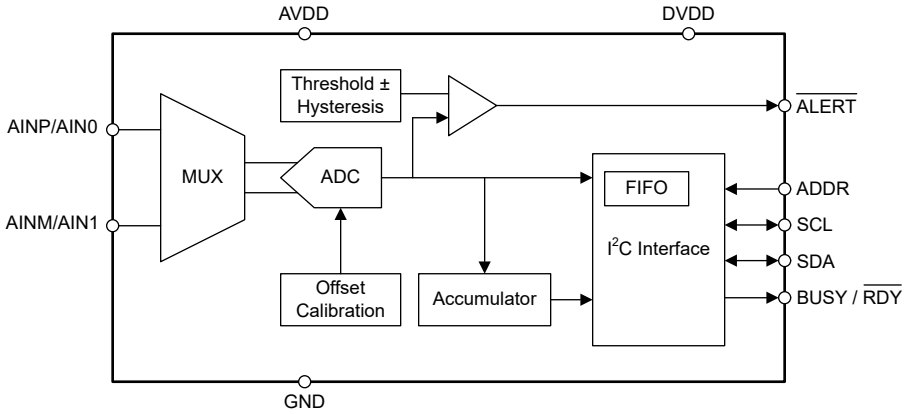
7.1 Overview

The ADS7142-Q1 is a small size, dual-channel, 12-bit programmable sensor monitor with an integrated analog-to-digital converter (ADC), input multiplexer, digital comparator, data buffer, accumulator, and internal oscillator. The *input multiplexer* can be either configured as two single-ended channels, one single-ended channel with remote ground sensing, or one pseudo-differential channel where the input can swing to approximately AVDD / 2. The device includes a *digital window comparator* with a dedicated $\overline{\text{ALERT}}$ pin, which can be used to alert the host when a programmed high or low threshold is crossed. The device address is configured by the I2C address selector block. The device uses *internal oscillators* (low power or high speed) for conversion. The start of conversion is controlled by the host in *manual mode* or by the device in the *autonomous modes*.

The device also features a data buffer and an accumulator. The data buffer can store up to 16 conversion results of the ADC in the autonomous modes and the accumulator can accumulate up to 16 conversion results of the ADC in *high-precision mode*.

The device includes an offset calibration to calibrate the offset.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Analog Input and Multiplexer

Figure 7-1 shows a small-signal equivalent circuit for the analog input pins. The device includes a two-channel analog multiplexer with each input pin having ESD protection diodes to AVDD and GND. The sampling switches are represented by ideal switches SW_1 and SW_2 in series with resistors $R_{s\ 1}$ and R_{s2} (typically 150 Ω). The sampling capacitors, C_{s1} and C_{s2}, are typically 15 pF. The multiplexer configuration is set by the CH_INPUT_CFG register.

During acquisition, switches SW_1 and SW_2 are closed to allow the input signal to charge the internal sampling capacitors.

During conversion, switches SW_1 and SW_2 are opened to disconnect the input signal from the sampling capacitors.

The analog inputs of the device are optimized to be driven by a high-impedance source (up to 100 kΩ) in *autonomous modes* or in *high precision mode* with a low-power oscillator. When using the high-speed oscillator, drive the analog inputs of the ADC with an external amplifier in *autonomous modes* or in *high precision mode*. Figure 6-29 and Figure 6-30 provide the analog input current for CH0 and CH1 of the device.

Figure 7-2, Figure 7-3, and Figure 7-4 provide a simplified circuit for analog input for input configurations described in the *Two-Channel, Single-Ended Configuration*, *Single-Channel, Single-Ended Configuration With Remote Ground Sense*, and *Single-Channel, Pseudo-Differential Configuration* sections, respectively. The analog multiplexer supports following input configurations (set by writing into the CH_INPUT_CFG register).

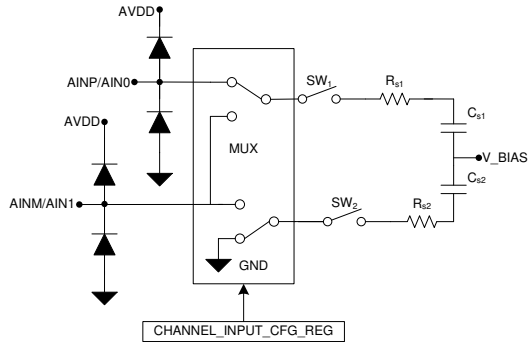


Figure 7-1. Equivalent Circuit for Analog Input

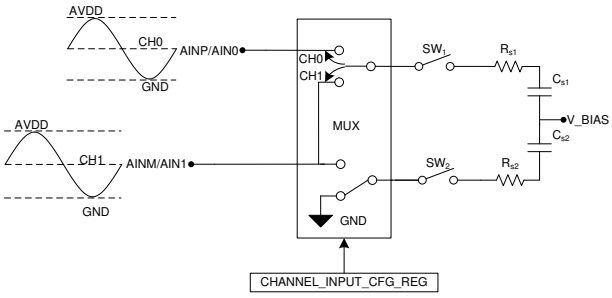


Figure 7-2. Two-Channel, Single-Ended Configuration

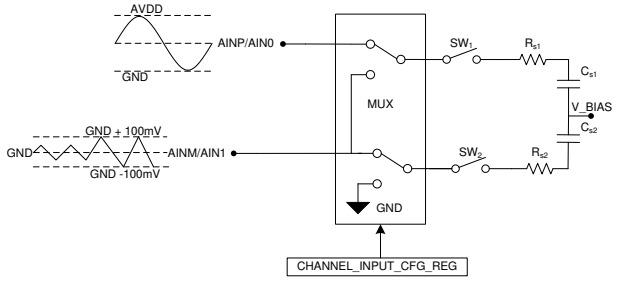


Figure 7-3. Single-Channel, Single-Ended Configuration With Remote Ground Sensing

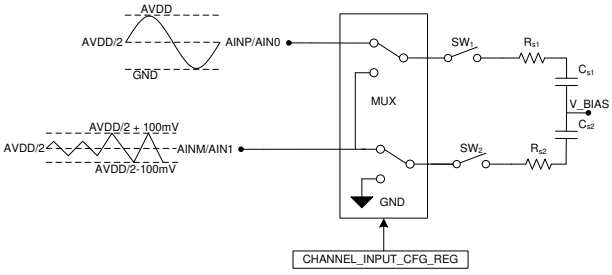


Figure 7-4. Single-Channel, Pseudo-Differential Configuration

7.3.1.1 Two-Channel, Single-Ended Configuration

Figure 7-2 shows a simplified block diagram showing a two-channel, single-ended configuration. Set the CH0_CH1_IP_CFG bits = 00b or 11b to select this configuration. This configuration is also the default for the device after power up. In this configuration, C_{S2} always samples the GND pin and C_{S1} samples the input signal provided on channel 0 (AINP/AIN0) or channel 1 (AINM/AIN1) based on the channel selection. Each analog input channel can accept input signals in the range 0 V to AVDD V.

On power-up, the device wakes up in manual mode with two-channel, single-ended configuration and samples CH0 only. This configuration can also be set by setting OPMODE_SEL to 000b or 001b,

The device can be configured to sample either CH0 or CH1 or both channels by setting bits in the AUTO_SEQ_CHEN register to select the channels.

- To select a channel in AUTO sequence, set the AUTO_SEQ_CHx bit in the AUTO_SEQ_CHEN register to 1.
- Set the bits in the OPMODE_SEL register to 100b or 101b for manual mode with AUTO sequence.
- Set the bits in the OPMODE_SEL register to 110b for *autonomous modes* with AUTO sequence.
- Set the bits in the OPMODE_SEL register to 111b for *high-precision mode* with AUTO sequence.

7.3.1.2 Single-Channel, Single-Ended Configuration With Remote Ground Sense

See Figure 7-3 for a simplified block diagram showing a single-channel, single-ended configuration with remote ground sense. Set the CH0_CH1_IP_CFG bits = 01b to select this configuration. In this configuration, C_{S1} samples the input signal provided on the AINP/AIN0 pin, whereas C_{S2} samples the input signal provided on the AINM/AIN1 pin. The AINP/AIN0 pin can accept input signals in the range 0 V to AVDD V and the AINM/AIN1 pin can accept input signals in the range –100 mV to +100 mV. This input configuration is useful in systems where the sensor or the signal conditioning block is placed far from the device and there can be a small difference between the ground potentials. In this channel configuration, remove channel 1 from the AUTO sequence by setting the AUTO_SEQ_CH1 bit to 0. Selecting channel 1 in the AUTO sequence leads to an error condition and the device sets an error flag in the SEQUENCE_STATUS register.

7.3.1.3 Single-Channel, Pseudo-Differential Configuration

See Figure 7-4 for a simplified block diagram showing a single-channel, pseudo-differential configuration. Set the CH0_CH1_IP_CFG bits = 10b to select this configuration. In this configuration, C_{S1} samples the input signal provided on the AINP/AIN0 pin, whereas C_{S2} samples the input signal provided on the AINM/AIN1 pin. The AINP/AIN0 pin can accept input signals in the range of 0 V to AVDD V and the AINM/AIN1 pin can accept input signals in the range of (AVDD / 2) – 100 mV to (AVDD / 2) + 100 mV. This input configuration is useful to interface with sensors that provide a pseudo-differential signal with a negative output of AVDD / 2 (such as an electrochemical gas sensor). In this channel configuration, remove channel 1 from the AUTO sequence by setting the AUTO_SEQ_CH1 bit to 0. Selecting channel 1 in the AUTO sequence leads to an error condition and the device sets an error flag in the SEQUENCE_STATUS register.

7.3.2 Offset Calibration

The device automatically calibrates the offset on power up. The offset can also be calibrated during normal device operation by setting the TRIG_OFFCAL bit in the OFFSET_CAL register. During offset calibration, the sampling switches are open (Figure 7-1) and the device keep the BUSY/$\overline{\text{RDY}}$ pin high. The device calculates the offset error and corrects for this error for subsequent conversions. To nullify the change in offset resulting from change in temperature or in AVDD voltage, periodically perform this calibration.

7.3.3 Reference

The device uses the analog supply voltage (AVDD) as a reference for the analog-to-digital conversion process. Place a 220-nF, low-ESR ceramic decoupling capacitor between the AVDD pin and the GND pin, close to the AVDD pin; see the *Power Supply Recommendations* section.

7.3.4 ADC Transfer Function

The ADC provides data in straight binary format. The ADC resolution can be computed by Equation 1:

$$1\ \text{LSB} = V_{REF} / 2^{N} \quad (1)$$

where:

- V_{REF} = AVDD
- N = 12 for autonomous monitoring modes and manual mode

Figure 7-5 and Figure 7-6 show the ideal transfer characteristics for single-ended input and pseudo-differential input, respectively. Table 7-1 lists the digital output codes for the transfer functions.

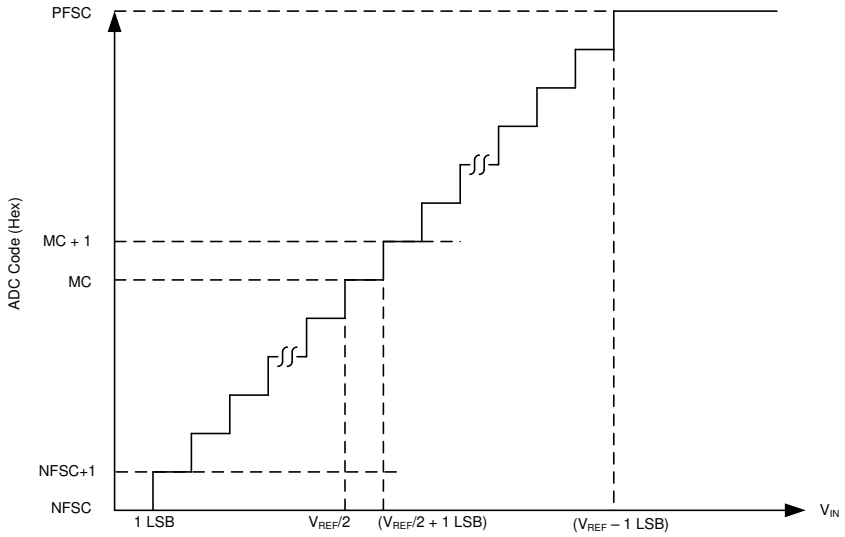


Figure 7-5. Ideal Transfer Characteristics for Single-Ended Configurations

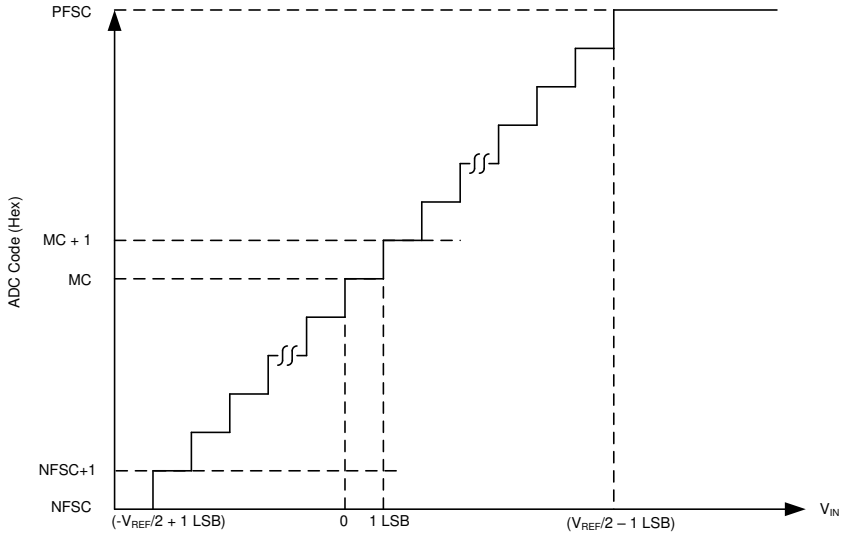


Figure 7-6. Ideal Transfer Characteristics for Pseudo-Differential Configuration

Table 7-1. Transfer Characteristics

INPUT VOLTAGE FOR SINGLE-ENDED INPUT	INPUT VOLTAGE FOR PSEUDO DIFFERENTIAL INPUT	CODE	DESCRIPTION	IDEAL OUTPUT CODE
≤1 LSB	≤ (–V_{REF} / 2 + 1) LSB	NFSC	Negative full-scale code	000
1 LSB to 2 LSBs	(–V_{REF} / 2 + 1) to (–V_{REF} / 2 + 2) LSB	NFSC + 1	—	001
(V_{REF} / 2) to (V_{REF} / 2) + 1 LSB	0 LSB to 1 LSB	MC	Mid code	800
(V_{REF} / 2) + 1 LSB to (V_{REF} / 2) + 2 LSBs	1 LSB to 2 LSB	MC + 1	—	801
≥ V_{REF} – 1 LSB	≥ V_{REF} / 2 – 1 LSB	PFSC	Positive full-scale code	FFF

7.3.5 Oscillator and Timing Control

The device uses one of the two internal oscillators (low-power oscillator or high-speed oscillator) for converting the analog input voltage into a digital output code.

The steps for selecting the oscillator and setting the sampling speed are:

1. Select the low-power oscillator (OSC_SEL = 1b) to monitor slow-moving signals (< 300 Hz) at extremely low-power consumption and sampling speeds (< 600 SPS). Select the high-speed oscillator (OSC_SEL = 0b) to scan the sensor signals with faster sampling speed (> 50 kHz).
2. Set the sampling speed by programming the NCLK_SEL register:

$$f_S = \frac{Oscillator\ frequency}{nCLK} \quad (2)$$

- f_s = Sampling speed.
- Oscillator frequency = 1 / t_{HSO} or 1 / t_{LPO} depending on the OSC_SEL bit; see the *Specifications* section for 1 / t_{HSO} or 1 / t_{LPO}.
- nCLK is the number of clocks in one conversion cycle (see the NCLK_SEL register).

7.3.6 I²C Address Selector

The I²C address for the device is determined by connecting external resistors on the ADDR pin. The device address is selected on power-up based on the resistor values. The device retains this address until the next power up, until the next device reset, or until the device receives a command to program the address (*General Call With Write Software Programmable Part of the Target Address*). Figure 7-7 provides the connection diagram for the ADDR pin and Table 7-2 provides the resistor values for selecting a different addresses of the device.

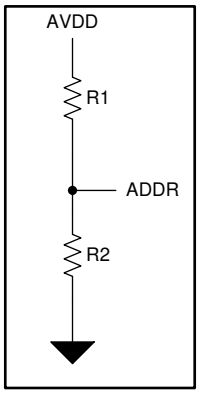


Figure 7-7. External Resistor Connection Diagram for the ADDR Pin

Table 7-2. I²C Address Selection

RESISTORS		ADDRESS
R1 (2)	R2(2)	
0 Ω	DNP(1)	0011111b (1Fh)
11 kΩ	DNP(1)	0011110b (1Eh)
33 kΩ	DNP(1)	0011101b (1Dh)
100 kΩ	DNP(1)	0011100b (1Ch)
DNP(1)	0Ω or DNP(1)	0011000b (18h)
DNP(1)	11 kΩ	0011001b (19h)
DNP(1)	33 kΩ	0011010b (1Ah)
DNP(1)	100 kΩ	0011011b (1Bh)

(1) DNP = Do not populate.
(2) Tolerance for R1, R2 < ±5%.

7.3.7 Data Buffer

When operating in autonomous monitoring mode, the device can use the internal data buffer for data storage. The internal data buffer is 16-bit wide and 16-words deep and follows the first-in, first-out (FIFO) approach.

7.3.7.1 Filling of the Data Buffer

The write operation to the data buffer starts and stops as per the settings in the DATA_BUFFER_OPMODE register. The DATA_BUFFER_STATUS register provides the number of entries filled in the data buffer and this register can be read during an active sequence to get the current status of the data buffer.

The time between two consecutive conversions is set by the NCLK_SEL register and Equation 3 provides the relationship for time between two consecutive conversions of the same channel and nCLK parameter.

$$t_{cc} = k \times nCLK \times OscillatorTimePeriod \quad (3)$$

where:

- t_{cc} = Time between two consecutive conversions of the same channel, $t_{cc} = k \times t_{cycle}$
- k = Number of channels enabled in the device sequence
- nCLK = Number of clocks used by the device for one conversion cycle
- Oscillator timer period = t_{LPO} or t_{HSO} depending on the OSC_SEL value; see the *Specifications* section for t_{LPO} or t_{HSO}

The format of the 16-bit contents of each entry in the data buffer are set by programming the DOUT_FORMAT_CFG register. The DATA_OUT_CFG register enables the channel ID and DATA_VALID flag in the data buffer. The channel ID represents the channel number for the data entry in the data buffer. DATA_VALID is set to zero in either of the following conditions:

- If the entry in the data buffer is not filled after the last start of the sequence
- If the I^2C controller tries to read more than 16 entries from the data buffer, the device provides zeros with DATA_VALID set to zero

At the end of the write operation, the data buffer always has results of 16 (or less) consecutive conversions. The data buffer is filled in the order that the data are converted by the ADC. The channels converted by the ADC are controlled by the AUTO_SEQ_CHEN register. The entries that are not filled during an active sequence are filled with zeros.

7.3.7.2 Reading Data From the Data Buffer

The ADC drives a logic 0 on the BUSY/$\overline{RDY}$ pin after completion of the sequence when auto-sequencing is disabled or after the SEQ_ABORT bit is set. As illustrated in Figure 7-8, the device provides the contents of the data buffer (in FIFO fashion) on receiving the I^2C read frame, which consists of the device address and the read bit set to 1.

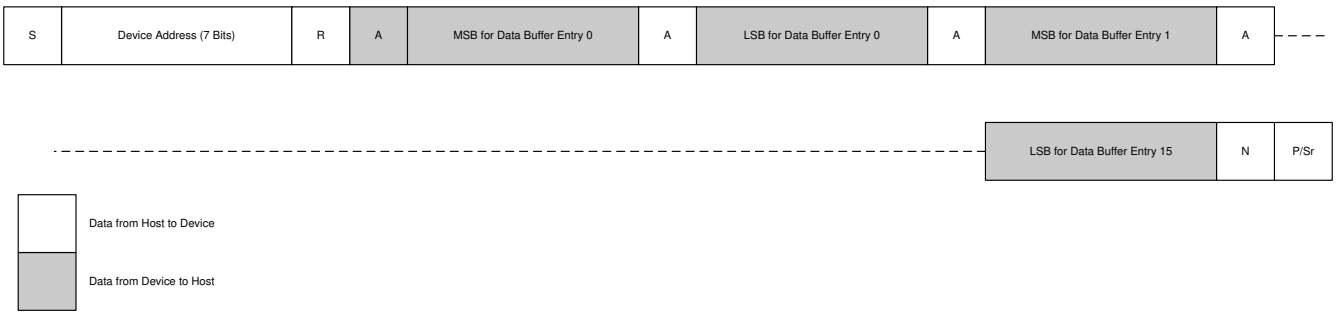


Figure 7-8. Reading Data Buffer (16 Bit Words × 16 Words)

The device returns zeroes with the DATA VALID flag set to zero for all I^2C read frames received after all the valid data words from the data buffer are read or when an I^2C read frame is issued during an active sequence (indicated by a high on the BUSY/$\overline{RDY}$ pin). The I^2C controller must provide a NACK followed by a STOP or RESTART condition in an I^2C frame to finish the reading process. The data buffer is reset by setting the SEQ_START bit or after resetting the device.

7.3.8 Accumulator

When operating in *high-precision mode*, the device offers a 16-bit internal accumulator per channel. The accumulator for a channel is enabled only if that channel is selected in the channel scanning sequence. The accumulator adds sixteen 12-bit conversion results. The result of adding sixteen 12-bit words is one 16-bit word. The time between two consecutive conversions for accumulation is controlled by the NCLK_SEL register and Equation 3 provides the relationship for time between two consecutive conversions of same channel and nCLK parameter.

The accumulated data can be read from the ACC_CHx_MSB and ACC_CHx_LSB registers in the device. The ACCUMULATOR_STATUS register provides the number of accumulations done in the accumulator since last conversion. This register can be read during an active sequence to get the current status of the accumulator. The accumulator is reset when setting the SEQ_START bit or on resetting the device.

Equation 4 provides the relationship between high precision data and ADC conversion results.

$$\text{High Precision Data for CHx} = \sum_{k=1}^{16} \text{Conversion Result[k] for CHx} \tag{4}$$

Equation 5 provides the value of LSB in high precision mode for the accumulated result.

$$1\ LSB = \frac{AVDD}{2^{16}} \tag{5}$$

7.3.9 Digital Window Comparator

The internal digital window comparator is available in all modes. In *autonomous modes* with thresholds monitoring and diagnostics, the digital window comparator controls the filling of the data into the FIFO and the output of the $\overline{\text{ALERT}}$ pin. In the remaining modes, the digital window comparator only controls the output of the $\overline{\text{ALERT}}$ pin. Figure 7-9 provides the block diagram for digital window comparator.

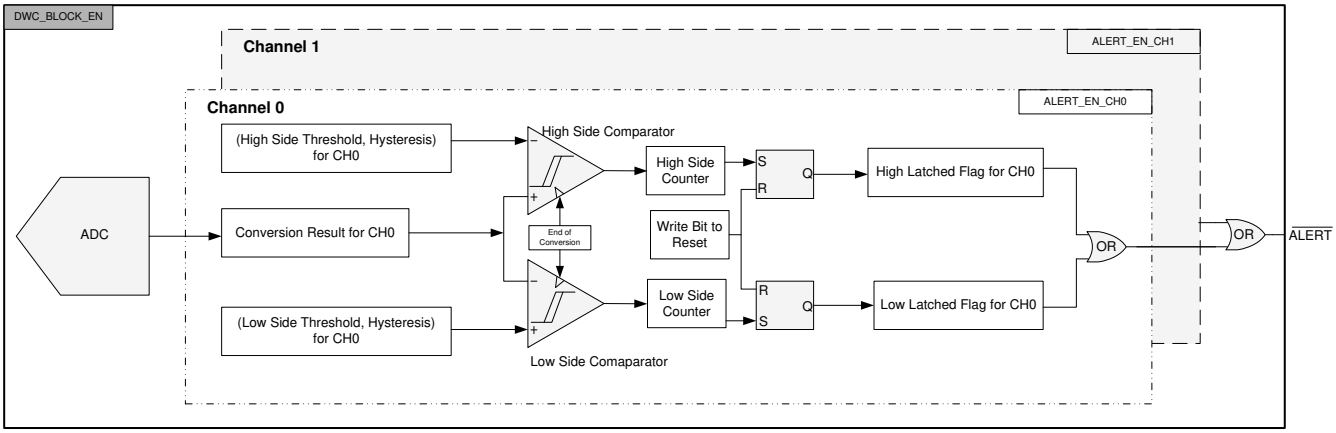


Figure 7-9. Digital Comparator Block Diagram

The low-side threshold, high-side threshold, and hysteresis parameters are independently programmable for each input channel. Figure 7-10 illustrates the comparison thresholds and hysteresis for the two comparators. A pre-$\overline{\text{ALERT}}$ event counter after each comparator counts the output of the comparator and sets the latched flags. The pre-$\overline{\text{ALERT}}$ event counter settings are common to the two channels.

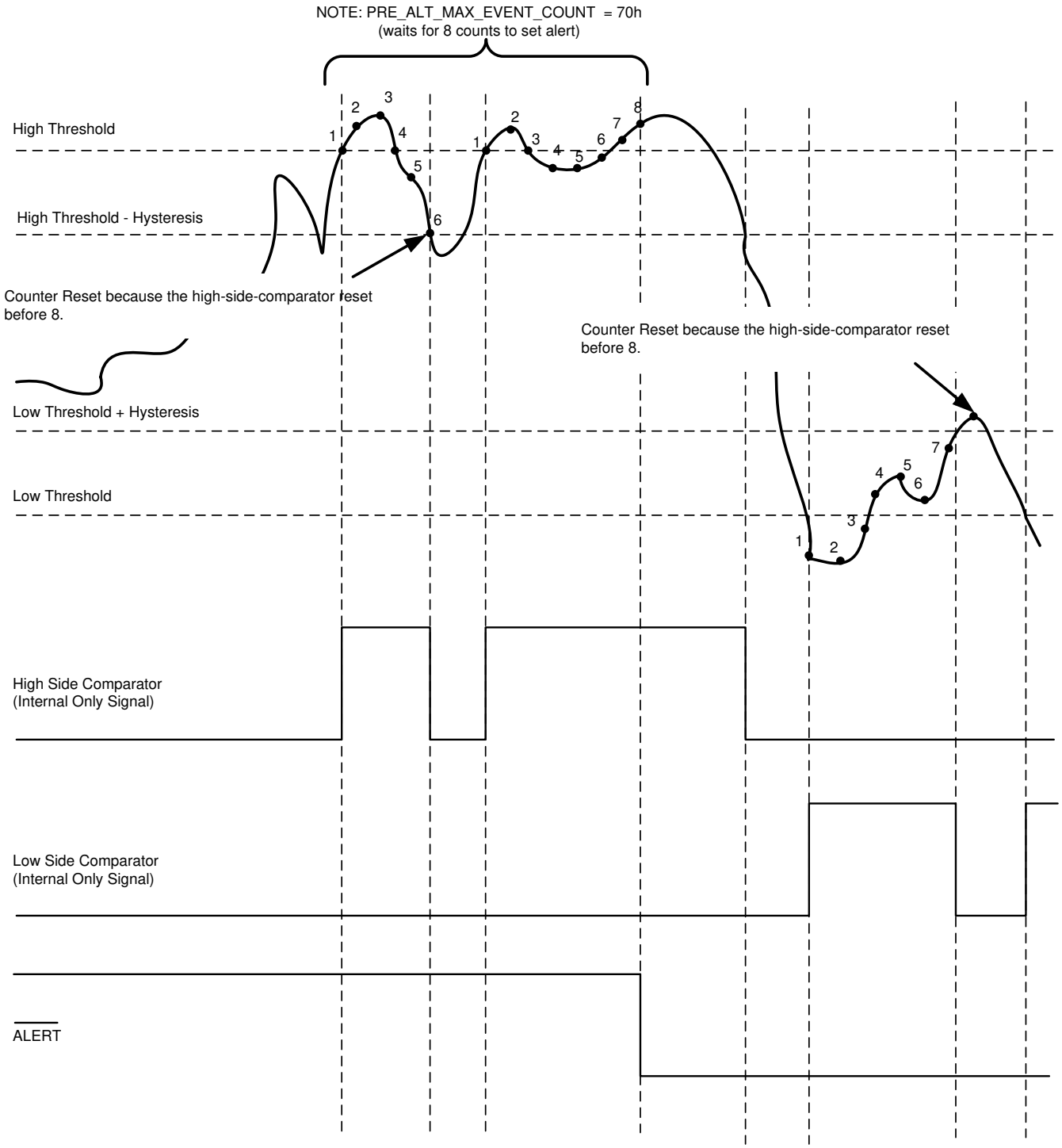


Figure 7-10. Thresholds, Hysteresis, and Event Counter for the Digital Window Comparator

The DWC_BLOCK_EN bit in the ALERT_DWC_EN register enables and disables the complete digital window comparator block (disabled at power-up) and the ALERT_EN_CHx bits in the ALERT_CHEN register enables the digital window comparator for individual channels. Possible responses when using the digital comparator when a new ADC conversion is completed include:

1. The output of the high-side comparator transitions to a logic high when the conversion result is greater than the high threshold. This comparator resets when the conversion result is less than the high threshold – hysteresis.

2. The output of the low-side comparator transitions to a logic high when the conversion result is less than the low threshold. This comparator resets when the conversion result is greater than the low threshold + hysteresis.
3. When the output of either the high-side or low-side comparator transitions high, the pre-$\overline{\text{ALERT}}$ event counter begins to increment for each subsequent conversion. This counter continues to increment until the value stored in the PRE_ALT_MAX_EVENT_COUNT register is reached. When the counter reaches PRE_ALT_MAX_EVENT_COUNT, the alert becomes active and sets the latched flags. If the comparator output becomes zero before the counter reaches PRE_ALT_MAX_EVENT_COUNT, then the event counter is reset to zero, $\overline{\text{ALERT}}$ is not set, and the latched flag is not set.

Therefore, the latched flags (high and low) for the channel are updated only if the respective comparator output remains 1 for the specified number of consecutive conversions (set by PRE_ALT_MAX_EVENT_COUNT).

The latched flags can be read from the ALERT_LOW_FLAGS and ALERT_HIGH_FLAGS registers. To clear a latched flag, write 1 to the applicable bit location. The $\overline{\text{ALERT}}$ pin status is re-evaluated when an applicable latched flag is set or is cleared.

The response time for the $\overline{\text{ALERT}}$ pin can be estimated by Equation 6

$$t_{response} = [1 + k \times (PRE\_ALT\_MAX\_EVENT\_COUNT + 1)\ ] \times nCLK \times Oscillator\ TimePeriod \quad (6)$$

where:

- k = Number of channels enabled in device sequence
- nCLK = Number of clocks used by device for one conversion cycle
- Oscillator timer period = t_{LPO} or t_{HSO} depending on the OSC_SEL value; see the *Specifications* section for t_{LPO} or t_{HSO}

7.3.10 I²C Protocol Features

7.3.10.1 General Call

On receiving a general call (00h), the device provides an ACK.

7.3.10.2 General Call With Software Reset

On receiving a general call (00h) followed by a software reset (06h), the device resets.

7.3.10.3 General Call With Write Software Programmable Part of the Target Address

On receiving a general call (00h) followed by 04h, the ADC configures the I²C address configured by the ADDR pin. During this operation, the ADC keeps the BUSY/$\overline{\text{RDY}}$ pin high and does not respond to other I²C commands except a general call.

7.3.10.4 Configuring the ADC Into High-Speed I²C Mode

The ADC can be configured in high-speed I²C mode by providing an I²C frame with one of the HS-mode codes (08h to 0Fh).

After receiving one of the HS-mode codes, the ADC sets the HS_MODE bit in the OPMODE_I2CMODE_STATUS register and remains in high-speed I²C mode until a STOP condition is received in an I²C frame.

7.3.10.5 Bus Clear

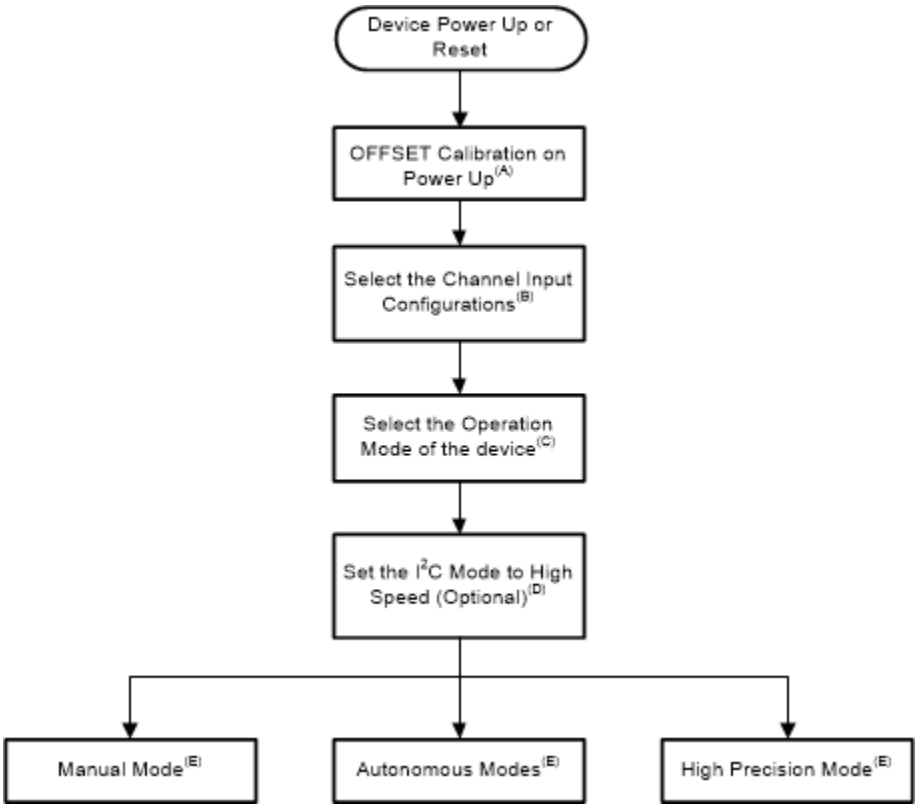
If the SDA line is stuck low because of an incomplete I²C frame, providing nine clocks on SCL is recommended. The device releases the SDA line within these nine clocks, and then the next I²C frame can be started.

7.4 Device Functional Modes

The ADC has the following functional modes:

- Manual mode:
  - Manual mode with CH0 only
  - Manual mode with auto-sequence
- Autonomous modes:
  - Autonomous mode with threshold monitoring and diagnostics
  - Autonomous mode with burst data
- High-precision mode

The ADC powers up in manual mode with CH0 only and can be configured into one of the other modes by writing the configuration registers for the desired mode. Steps for configuring ADC into different modes are shown in Figure 7-11.



A. Offset can also be calibrated anytime during normal operation by setting the bit in the OFFSET_CAL register.
B. Configure the CH_INPUT_CFG register.
C. Configure the OPMODE_SEL register for the desired operation mode.
D. See the *Configuring the ADC Into High-Speed I²C Mode* section.
E. The operating mode is selected by configuring the OPMODE_SEL register in step 3.
F. For reading and writing registers, see the *Programming* section.

Figure 7-11. Configuring the ADC Into Different Modes

7.4.1 Device Power Up and Reset

On power up, the device calibrates the offset and calculates the address from the resistors connected on the ADDR pin. During this time, the device keeps BUSY/$\overline{\text{RDY}}$ high.

The device can be reset by cycling power on the AVDD pin, by a general call (00h) followed by software reset (06h), or by writing the WKEY register followed by setting the bit in the DEVICE_RESET register.

When cycling power on the AVDD pin and on general call (00h) followed by software reset (06h), all the device configurations are reset, and the device initiates an offset calibration and re-evaluates the I^2C address.

When setting the bit in the DEVICE_RESET register, all the device configurations except latched flags for the digital window comparator and the WKEY register are reset, The device does not initiate offset calibration and does not re-evaluate the I^2C address.

7.4.2 Manual Mode

On power-up, the ADC is in manual mode using the single-ended and dual-channel configuration and samples the analog input applied on channel 0. In this mode, the ADC uses the high-frequency oscillator for conversions. Manual mode allows the external host processor to directly request and control when the data are sampled. The data capture is initiated by an I^2C command from the host processor and the data are then returned over the I^2C bus at a throughput rate of up to 140 kSPS.

After setting the operation mode to manual mode as illustrated in Figure 7-11, steps for operating the ADC to be in manual mode and reading data are illustrated in Figure 7-12. The host can either configure the ADC to scan through one channel or both channels by configuring the CH_INPUT_CFG and AUTO_SEQ_CHEN registers.

7.4.2.1 Manual Mode With CH0 Only

Set the OPMODE_SEL register to 000b or 001b for manual mode with channel 0 only. The host must provide the ADC address and read bit to start the conversions. To continue with conversions and reading data, the host must provide continuous SCL (Figure 7-13). In this mode, a NACK followed by a STOP condition in the I^2C frame is required to abort the operation. Then the ADC operation mode can be changed to another operation mode.

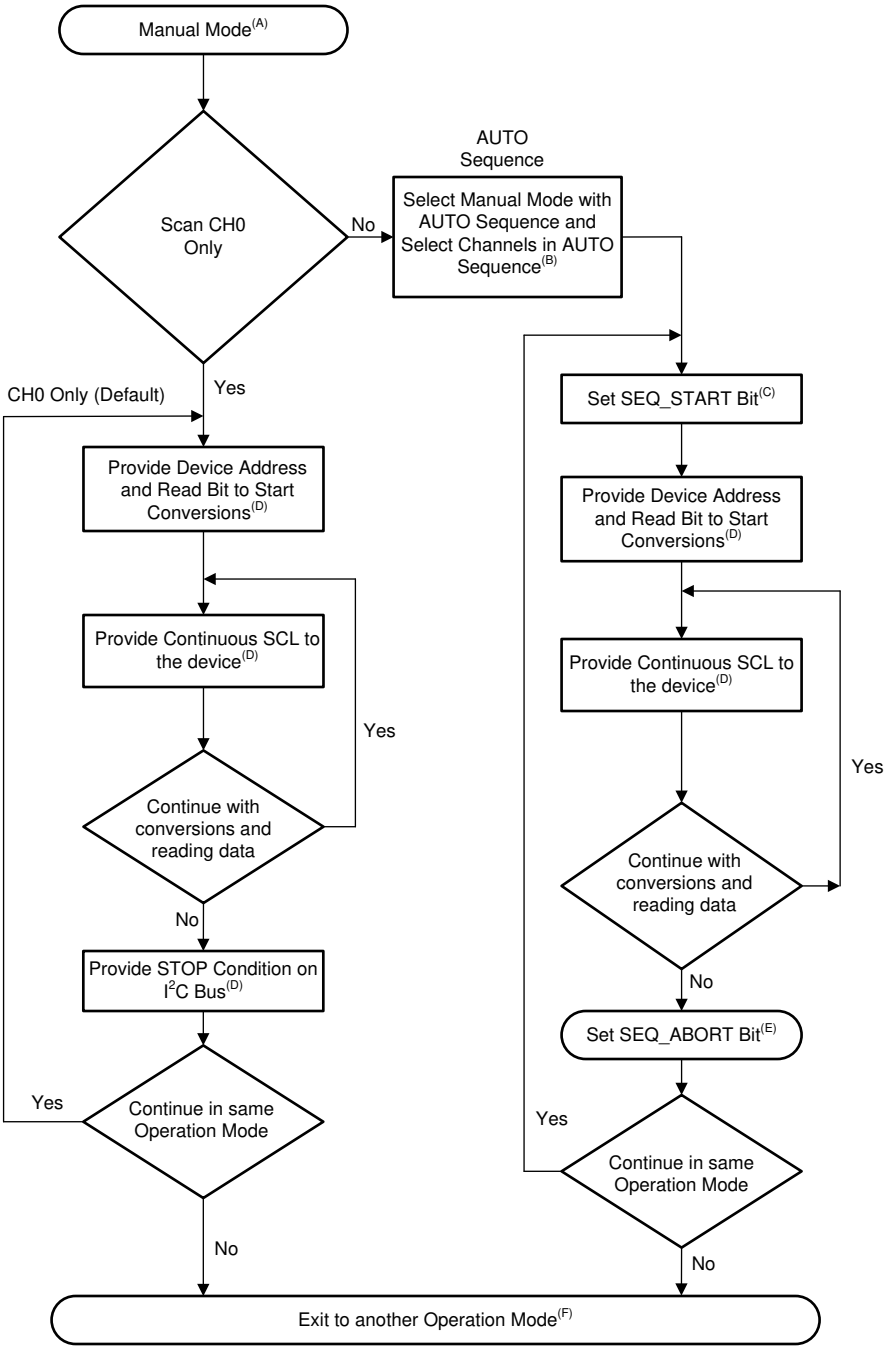
7.4.2.2 Manual Mode With AUTO Sequence

Set the OPMODE_SEL register to 100b or 101b for manual mode with AUTO sequence. The host must set the SEQ_START bit in the START_SEQUENCE register and provide the device address and read bit to start the conversions. To continue with conversions and reading data, the host must provide continuous SCL (Figure 7-13). In this mode, the SEQ_ABORT bit in the ABORT_SEQUENCE register must be set to abort the operation. Then the device operation mode can be changed to another operation mode. In this mode, a register read aborts the AUTO sequence.

In manual mode, the device always uses the high-speed oscillator and the nCLK parameter has no effect. The maximum scan rate is given by Equation 7:

$$f_S = \frac{1000}{\left[18 \times T_{SCL} + k\right]} \tag{7}$$

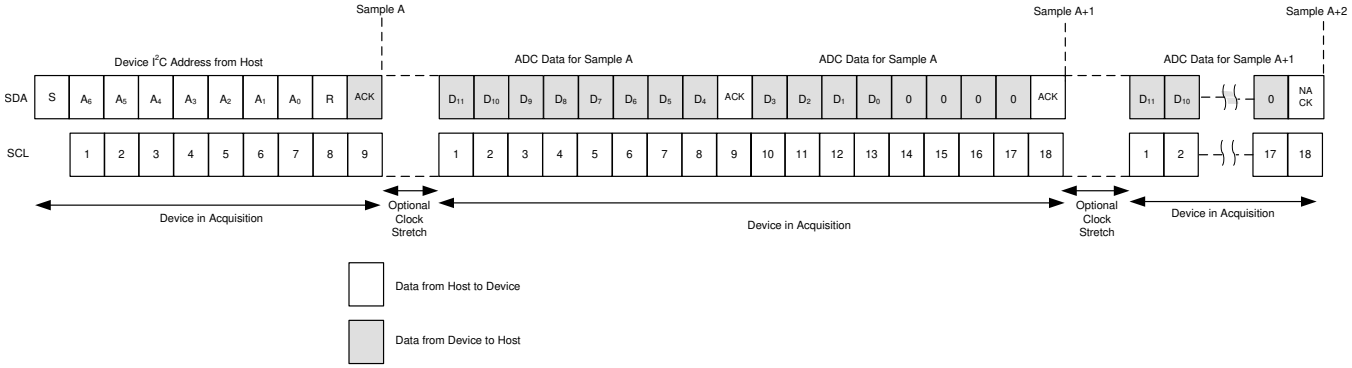
- f_s = Maximum sampling speed in kSPS
- T_{SCL}= Time period of SCL clock (in µs)
- if $T_{SCL\text{-}LOW}$ (low period of SCL) < 1.8.µs, k = (1.8 – $T_{SCL\text{-}LOW}$) and the device stretches clock in manual mode; not applicable for standard I^2C mode (100 kHz)
- if $T_{SCL\text{-}LOW}$ (low period of SCL) ≥ 1.8.µs, k = 0, and the device does not stretch clock in manual mode



A. For setting the operation mode to manual mode, see Figure 7-11.
B. Select manual mode with AUTO sequence in the OPMODE_SEL register. Select channels in the AUTO_SEQ_CHEN register.
C. Set the SEQ_START bit in the START_SEQUENCE register.
D. See Figure 7-13.
E. Set the SEQ_ABORT bit in the ABORT_SEQUENCE register.
F. Select another operation mode in the OPMODE_SEL register.
G. For reading and writing registers, see the *Programming* section.

Figure 7-12. Device Operation in Manual Mode

Data can be read from the device by providing a device address and read bit followed by continuous SCL, as shown in Figure 7-13.



A. See Equation 7 for sampling speed in manual mode.
B. If the device scans both channels in AUTO sequence, the first data (for sample A) is from channel 0 and the second data (for sample A +1) is from channel 1.

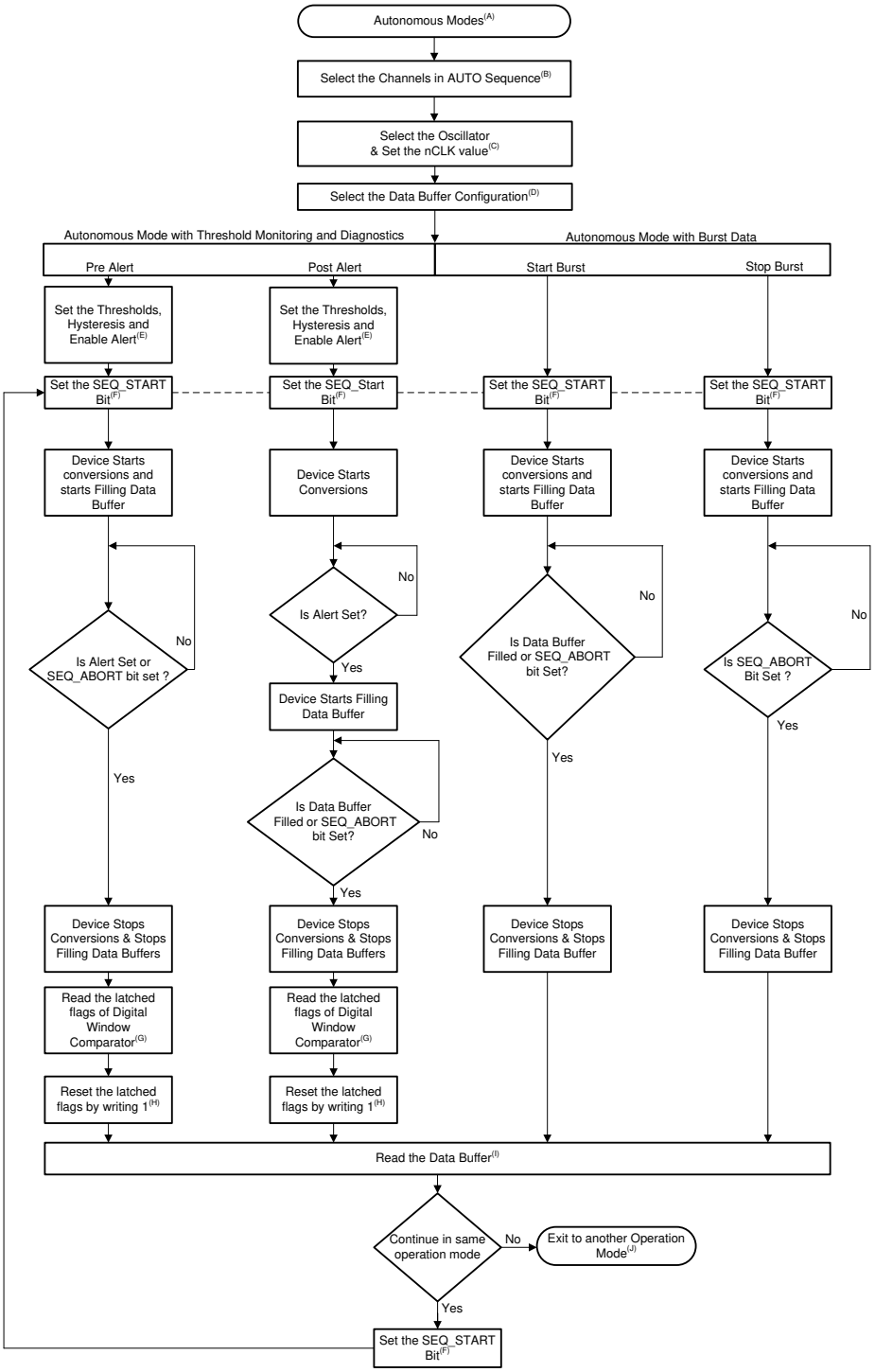
Figure 7-13. Starting Conversion and Reading Data in Manual Mode

7.4.3 Autonomous Modes

In autonomous mode, the ADC can be programmed to monitor the voltage applied on the analog input pins. The ADC generates a signal on the $\overline{\text{ALERT}}$ pin when the programmable high or low threshold values are crossed. The host processor can read the ADC conversion results from the internal data buffer.

In autonomous mode, the first start of conversion must be provided by the host and the ADC generates the subsequent start of conversions. The ADC initiates the following start of conversions using the internal oscillator.

After configuring the operation mode to autonomous mode (set the OPMODE_SEL register to 110b), as illustrated in Figure 7-11, steps for operating the ADC to be in different autonomous modes are illustrated in Figure 7-14.



A. For setting the operation mode to Autonomous modes, see Figure 7-11.
B. Select channels in the AUTO_SEQ_CHEN register.
C. Select the oscillator by configuring the OSC_SEL register and configure the NCLK_SEL register.
D. Select the data buffer mode in the DATA_BUFFER_OPMODE register.
E. Configure the thresholds in the DWC_xTH_CHx_xxx registers and hysteresis in the DWC_HYS_CHx registers. Enable the alert for channels in the ALERT_CHEN register and set the DWC_BLOCK_EN bit in the ALERT_DWC_EN register.
F. Set the bit SEQ_START bit in the START_SEQUENCE register.
G. Read the ALERT_LOW_FLAGS and ALERT_HIGH_FLAGS registers.
H. Reset the ALERT_LOW_FLAGS and ALERT_HIGH_FLAGS registers by writing 03h.
I. See the *Reading Data From the Data Buffer* section.

J. Select another operation mode in the OPMODE_SEL register.
K. For reading and writing registers, see the *Programming* section.

Figure 7-14. Configuring ADC in Autonomous Modes

Abort the present sequence by setting the SEQ_ABORT bit in the ABORT_SEQUENCE register before changing the ADC operation mode or ADC configuration.

7.4.3.1 Autonomous Mode With Threshold Monitoring and Diagnostics

In this mode, the ADC automatically scans the input voltage on the analog input channels and asserts the $\overline{\text{ALERT}}$ pin when the programmable high or low thresholds are crossed. The conversion results of the ADC corresponding to the pre-$\overline{\text{ALERT}}$ or post-$\overline{\text{ALERT}}$ can be stored in the internal data buffer, as described in *Autonomous Mode With Pre-$\overline{\text{ALERT}}$ Data* and *Autonomous Mode With Post-$\overline{\text{ALERT}}$ Data* respectively. This mode is useful for applications where the output of the sensor must be continuously monitored and where action is only taken when the sensor output deviates outside of an acceptable range.

7.4.3.1.1 Autonomous Mode With Pre-$\overline{\text{ALERT}}$ Data

In this mode, the ADC stores the 16 conversions prior to the assertion of the $\overline{\text{ALERT}}$ pin. Upon assertion of $\overline{\text{ALERT}}$, conversions stop. For this mode, set DATA_BUFFER_OPMODE to 100b. In this mode, the ADC starts converting and stores the data when setting the SEQ_START bit in the START_SEQUENCE register and continues to store data into the data buffer until one of the digital comparator flags is set for crossing a high threshold or a low threshold for the channels selected in the sequence. If the SEQ_ABORT bit is set before the data buffer is filled, the ADC aborts the sequence and stops storing conversion results. If more than 16 conversions occur between start of sequence and alert output, the first entries written into the data buffer are overwritten.

Figure 7-15 and Figure 7-16 show the filling of the data buffer in autonomous mode with pre-$\overline{\text{ALERT}}$ data.

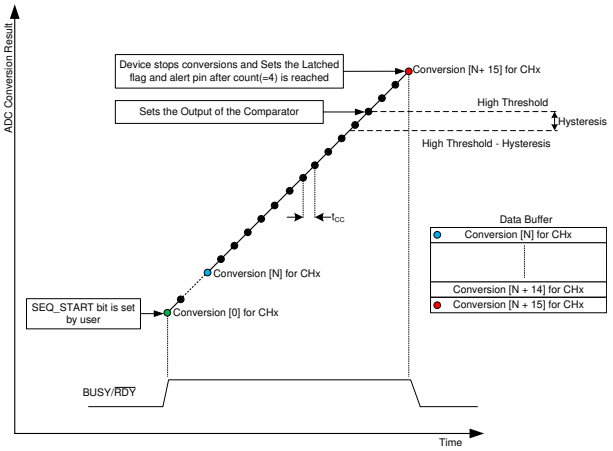


Figure 7-15. Pre-$\overline{\text{ALERT}}$ Data for Single-Channel Configurations

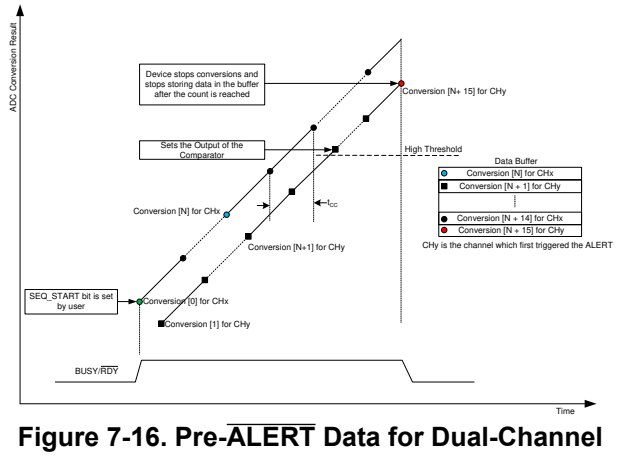


Figure 7-16. Pre-$\overline{\text{ALERT}}$ Data for Dual-Channel Configuration

7.4.3.1.2 Autonomous Mode With Post-$\overline{\text{ALERT}}$ Data

In this mode, the ADC captures the next sixteen conversion results after the $\overline{\text{ALERT}}$ pin is asserted. Once these sixteen conversions are stored in the data buffer, all conversion stops. For this mode, Set DATA_BUFFER_OPMODE to 110b. In this mode, the ADC starts converting the data on setting the SEQ_START bit and stores the data in the data buffer when one of the digital comparator flags is set after the crossing a high threshold or a low threshold for the channels selected in the sequence. if the SEQ_ABORT bit is set before the data buffer is filled, the ADC aborts the sequence and stops storing the conversion results.

Figure 7-17 and Figure 7-18 show the filling of the data buffer in autonomous mode with post-$\overline{\text{ALERT}}$ data.

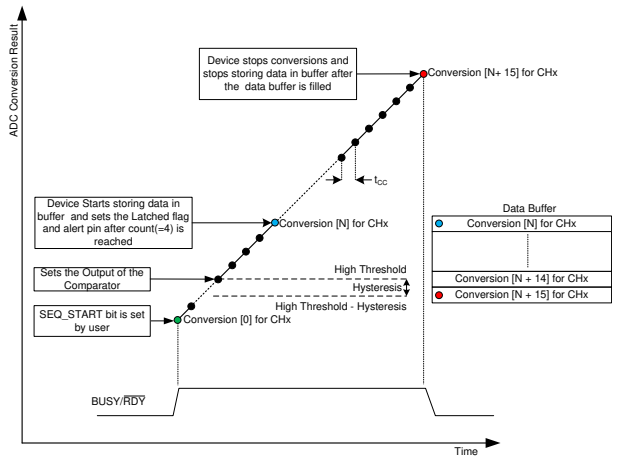


Figure 7-17. Post-$\overline{\text{ALERT}}$ Data for Single Channel Configurations

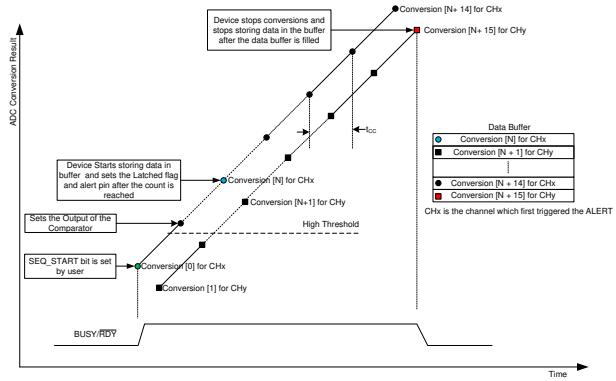


Figure 7-18. Post-$\overline{\text{ALERT}}$ Data for Dual Channel Configuration

7.4.3.2 Autonomous Mode With Burst Data

In this mode, the ADC can be configured to store up to 16 conversion results in the data buffer based on user command. In this mode, the user can either start or stop the burst of data as described in the following two sections.

7.4.3.2.1 Autonomous Mode With Start Burst

For this mode, set DATA_BUFFER_OPMODE to 001b. With start burst, the user can configure the device to start the filling of the data buffer with conversion results by setting the SEQ_START bit and the device stops converting data and filling the data buffer after the data buffer is filled.

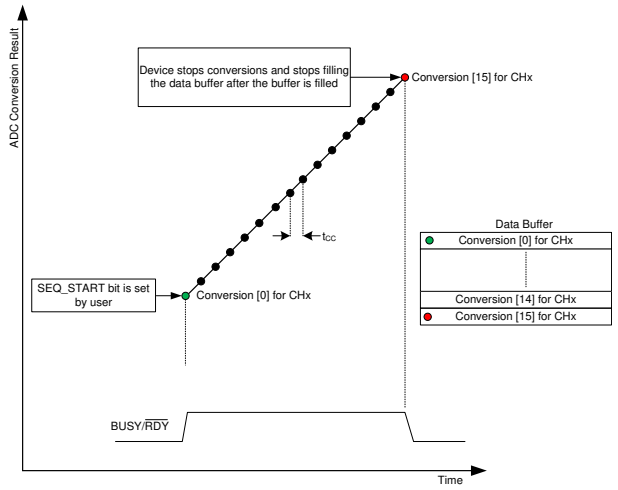


Figure 7-19. Start Burst With a Single-Channel Configuration

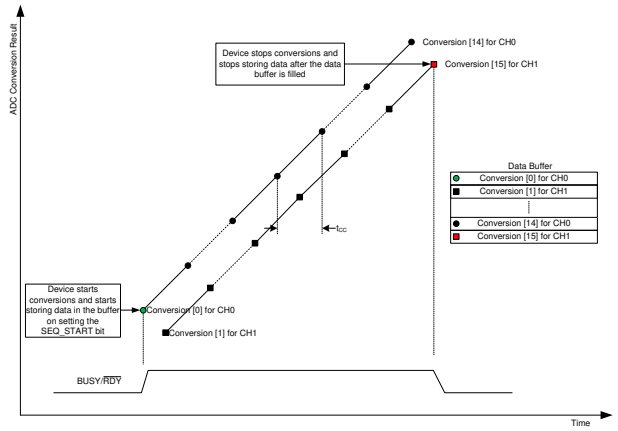


Figure 7-20. Start Burst With a Dual-Channel Configuration

7.4.3.2.2 Autonomous Mode With Stop Burst

For this mode, set DATA_BUFFER_OPMODE to 000b. With stop burst, the user can configure the device to stop filling the data buffer with conversion results by setting the SEQ_ABORT bit. If more than 16 conversions occur between start of sequence and abort of sequence, the entries first written into the data buffer are overwritten. Figure 7-21 and Figure 7-22 illustrate the filling of the data buffer in autonomous mode with stop burst.

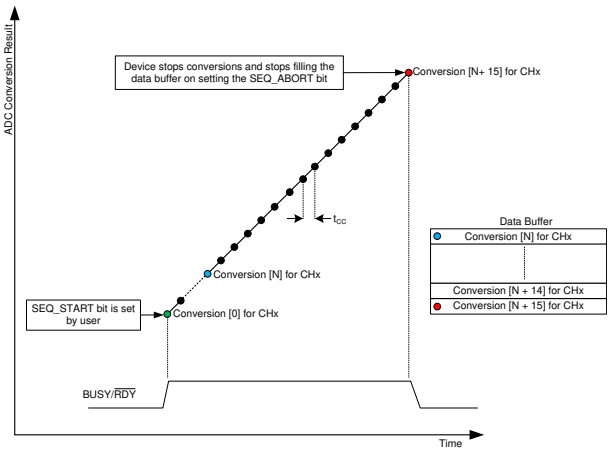


Figure 7-21. Stop Burst With a Single-Channel Configuration

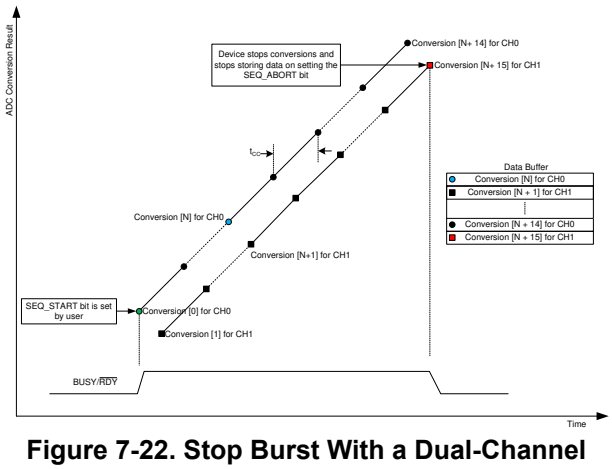
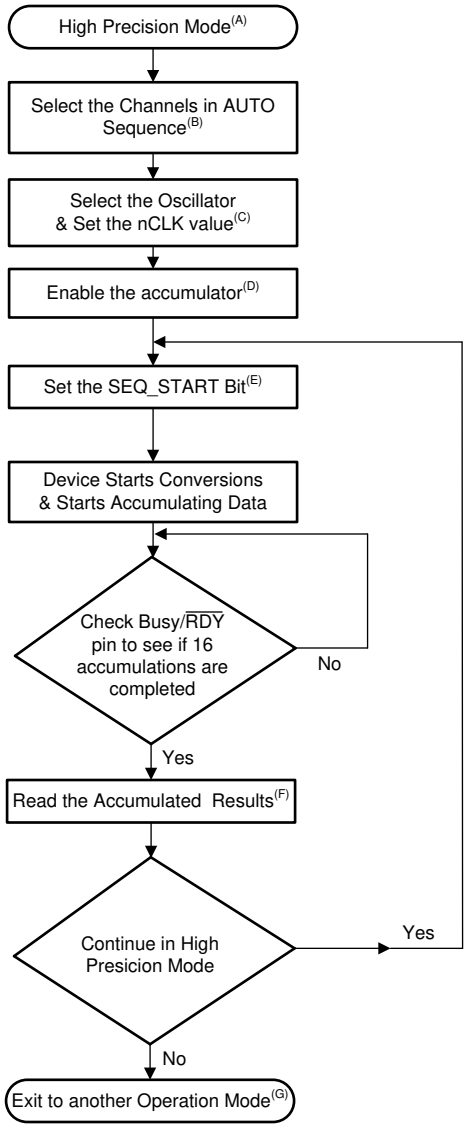


Figure 7-22. Stop Burst With a Dual-Channel Configuration

7.4.4 High-Precision Mode

High-precision mode increases the accuracy of the data measurement by accumulating ADC conversion results. This accumulation is useful for applications where the level of precision required to accurately measure the sensor output must be higher than 12 bits.

For this mode, set the OPMODE_SEL register to 111b. In this mode, the ADC starts converting and starts accumulating the conversion results in an accumulator when the SEQ_START bit is set. The ADC stops accumulating after 16 conversion results. The accumulator contains one 16-bit conversion result. The ADC has an accumulator for each analog input channel. If the operation of the ADC is aborted in high-precision mode before the BUSY/$\overline{\text{RDY}}$ pin goes low because the SEQ_ABORT bit is set by the user, the ADC provides invalid data and the internal data buffer (Figure 7-8), provides zeroes as output. In this mode, the BUSY/$\overline{\text{RDY}}$ can wake up the MCU or host from sleep or hibernation when accumulation completes. The steps for configuring the ADC into high-precision mode are illustrated in Figure 7-23.



A. For setting the operation mode to high-precision mode, see Figure 7-11.
B. Select the channels in the AUTO_SEQ_CHEN register.
C. Select the oscillator by configuring the OSC_SEL register and configure the NCLK_SEL register.
D. Enable the accumulator by setting the bits in the ACC_EN register.
E. Set the SEQ_START bit in the START_SEQUENCE register.
F. Read the ACC_CHx_xxx registers.
G. Select another operation mode in the OPMODE_SEL register.
H. For reading and writing registers, see the *Programming* section.

Figure 7-23. Configuring ADC in High-Precision Mode

Abort the current sequence by setting the SEQ_ABORT bit before changing the ADC operation mode or ADC configuration.

Figure 7-24 and Figure 7-25 show the accumulation of conversion results in high-precision mode.

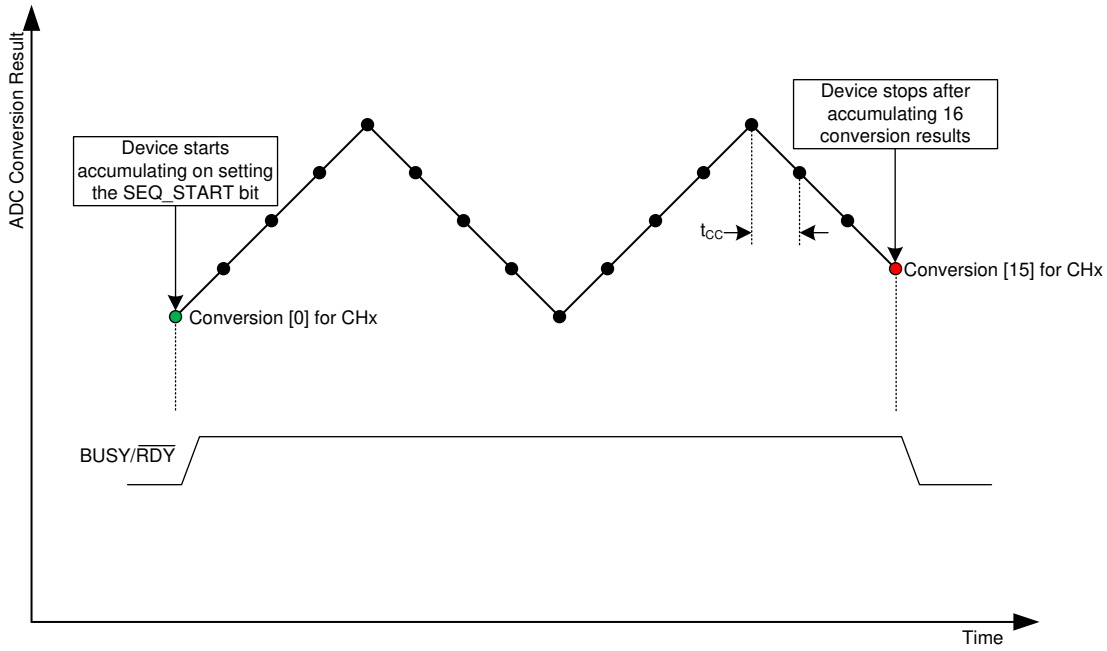


Figure 7-24. High-Precision Mode With Single-Channel Configurations

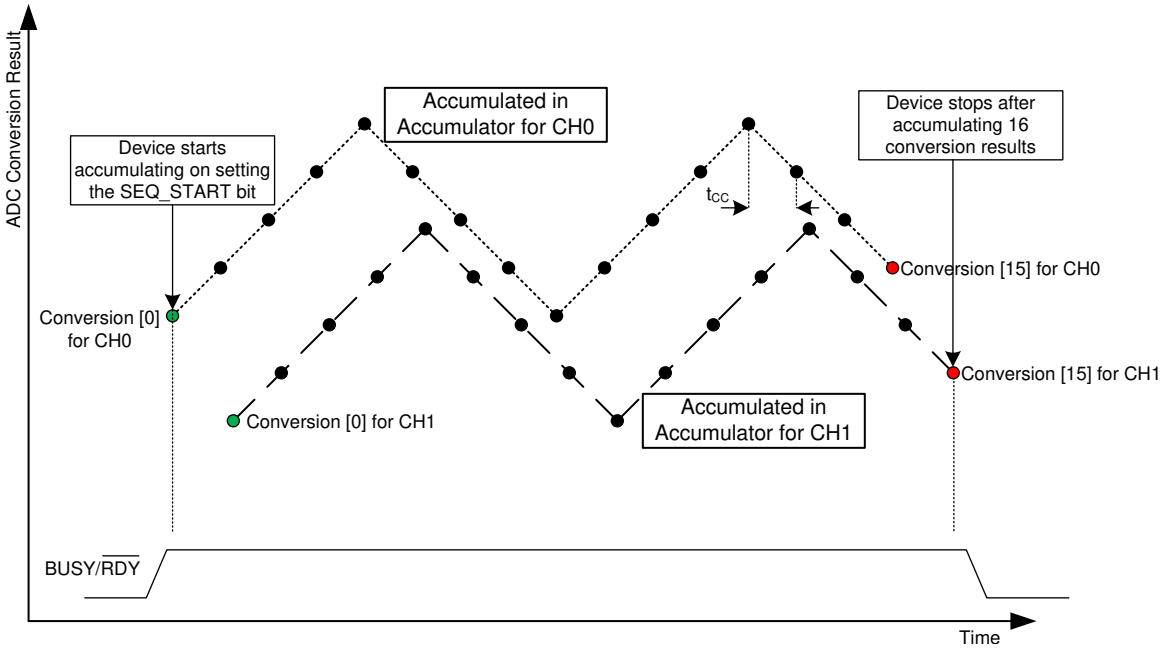


Figure 7-25. High-Precision Mode With Dual-Channel Configurations

7.5 Programming

Table 7-3 provides the acronyms for different conditions in an I²C frame.

Table 7-3. I²C Frame Acronyms

SYMBOL	DESCRIPTION
S	START condition for I²C frame
Sr	RESTART condition for I²C frame
P	STOP condition for I²C frame
A	ACK (low)
N	NACK (high)
R	Read bit (high)
W	Write bit (low)

Table 7-4. Opcodes for Commands

OPCODE	COMMAND DESCRIPTION
00010000b	Single register read
00001000b	Single register write
00011000b	Set bit
00100000b	Clear bit
00110000b	Reading a continuous block of registers
00101000b	Writing a continuous block of registers

7.5.1 Reading Registers

The I²C controller can either read a single register or a continuous block registers from the ADC, as described in the *Single Register Read* and *Reading a Continuous Block of Registers* sections.

7.5.1.1 Single Register Read

To read a single register from the ADC, the I²C controller must first provide an I²C command with three frames (of eight bits each) to set the address as shown in Figure 7-26. The register address is the address of the register that must be read. The opcode for register read command is listed in Table 7-4.

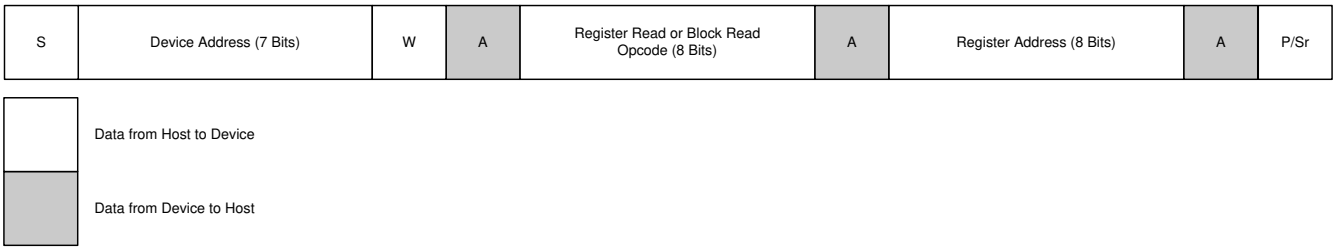


Figure 7-26. Setting Register Address for Reading Registers

Next, the I²C controller must provide another I²C frame containing the ADC address and read bit as illustrated in Figure 7-27. After this frame, the ADC provides register data. If the host provides more clocks, the ADC provides the same register data. To end the register read command, the controller must provide a STOP or a RESTART condition in the I²C frame.

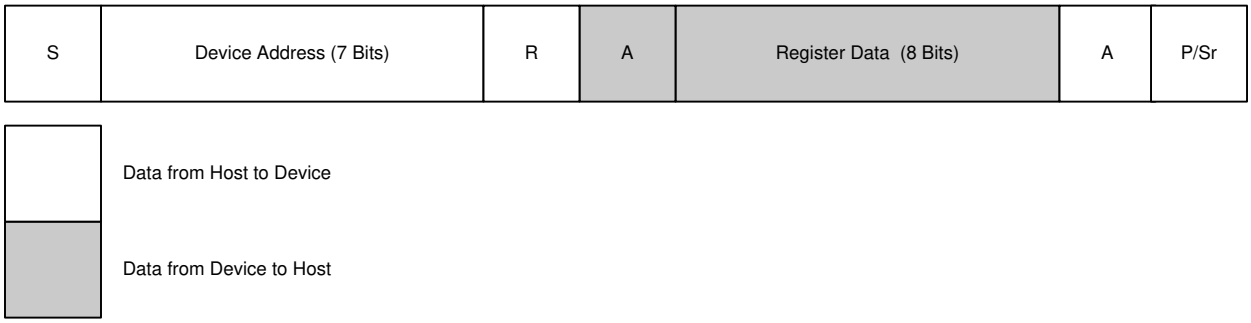


Figure 7-27. Reading Register Data

7.5.1.2 Reading a Continuous Block of Registers

To read a continuous block of registers, the I^{2}C controller must first provide an I^{2}C command to set the address, as illustrated in Figure 7-26. The register address is the address of the first register in the block that must be read. The opcode for reading a continuous block of register is listed in Table 7-4.

Next, the I^{2}C controller must provide another I^{2}C frame containing the ADC address and read bit, as shown in Figure 7-28. After this frame, the ADC provides register data. On providing more clocks, the ADC provides data for the next register. On reading data from addresses that do not exist in the *Register Map* of the ADC, the ADC returns zeros. If the ADC does not have any further registers to provide the data, the ADC provides zeros. To end the register read command, the controller must provide a STOP or a RESTART condition in the I^{2}C frame.

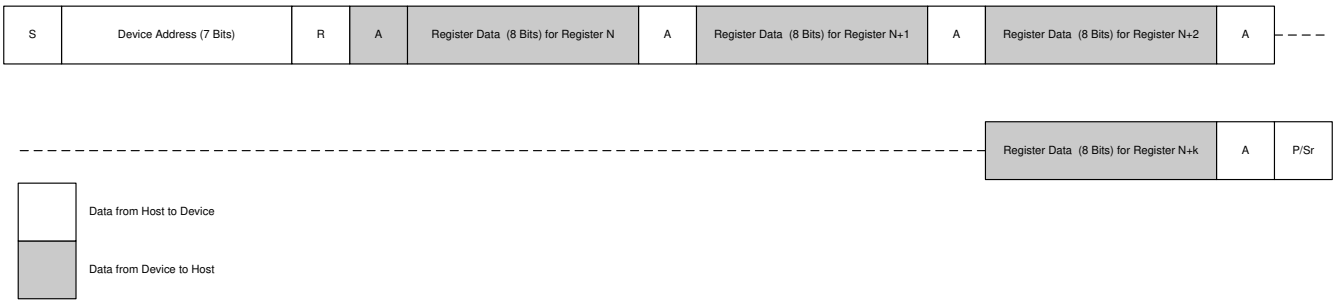


Figure 7-28. Reading a Continuous Block of Registers

7.5.2 Writing Registers

The I^{2}C controller can either write a single register or a continuous block registers to the ADC. The I^{2}C controller can also set or clear a few bits in a register.

7.5.2.1 Single Register Write

To write to a single register in the ADC, the I^{2}C controller has to provide an I^{2}C command with four frames as shown in Figure 7-29. The register address is the address of the register which must be written and register data is the value that must be written. The opcode for single register write is listed in Table 7-4. To end the register write command, the controller has to provide a STOP or a RESTART condition in the I^{2}C frame.

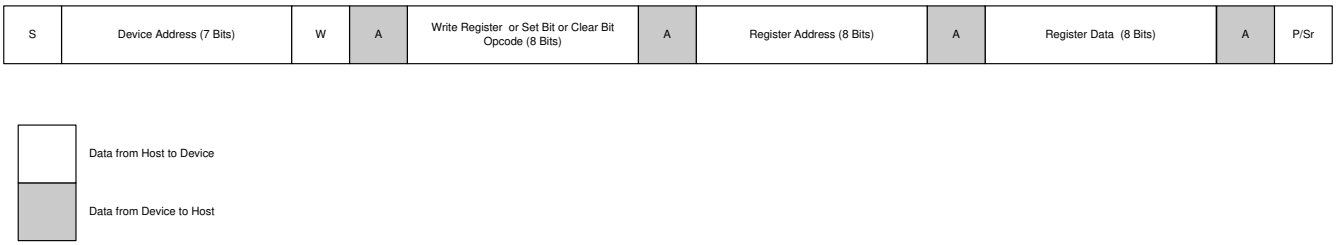


Figure 7-29. Writing a Single Register

7.5.2.2 Writing a Continuous Block of Registers

To write to a continuous block of registers, the I²C controller must provide an I²C command as shown in Figure 7-30. The register address is the address of the first register in the block that must be written. The I²C controller must provide data for registers in subsequent I²C frames in an ascending order of register addresses. Writing data to addresses that do not exist in the *Register Map* of the ADC has no effect. The opcode for writing a continuous block of registers is listed in Table 7-4. If the data provided by the I²C controller exceeds the address space of the ADC, the ADC neglects the data beyond the address space. To end the register write command, the controller must provide a STOP or a RESTART condition in the I²C frame.

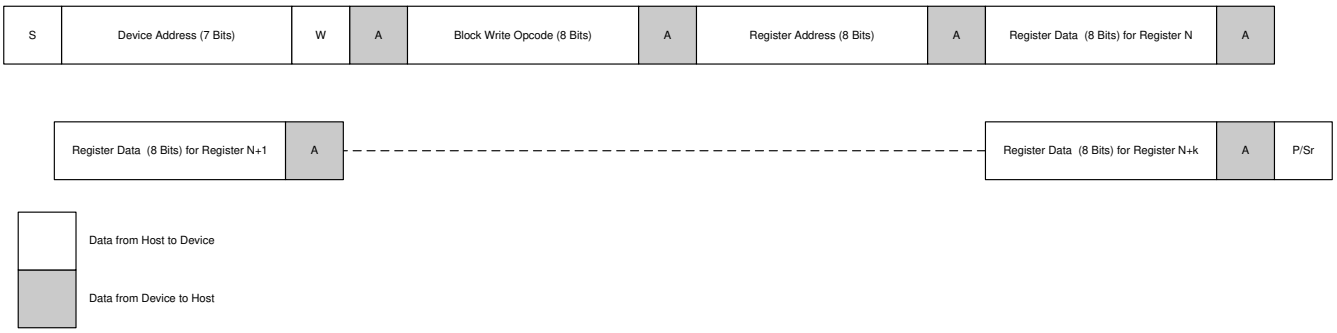


Figure 7-30. Writing a Continuous Block of Registers

7.5.2.3 Set Bit

To set bits in a register without changing the other bits, the I²C controller must provide an I²C command with four frames, as illustrated in Figure 7-29. The register address is the address of the register in which the bits must be set and the register data are the values representing the bits that must be set. Bits with a value of 1 in register data are set and bits with a value of 0 in register data are not changed. The opcode for set bit is listed in Table 7-4. To end this command, the controller must provide a STOP or RESTART condition in the I²C frame.

7.5.2.4 Clear Bit

To clear bits in a register without changing the other bits, the I²C controller must provide an I²C command with four frames, as illustrated in Figure 7-29. The register address is the address of the register where the bits must be cleared and where the register data are the values representing the bits that must be cleared. Bits with a value of *1* in register data are cleared and bits with a value of *0* in register data are not changed. The opcode for clearing a bit is listed in Table 7-4. To end this command, the controller must provide a STOP or a RESTART condition in the I²C frame.

7.6 Register Map

7.6.1 Page1 Registers

Table 7-5 lists the memory-mapped registers for the Page1 registers. All register offset addresses not listed in Table 7-5 should be considered as reserved locations and the register contents should not be modified.

Table 7-5. PAGE1 Registers

Address	Acronym	Register Name	Section
0x0	OPMODE_I2CMODE_STATUS	Device operation mode register	Section 7.6.1.1
0x1	DATA_BUFFER_STATUS	Data buffer status register	Section 7.6.1.2
0x2	ACCUMULATOR_STATUS	Status of ADC accumulator	Section 7.6.1.3
0x3	ALERT_TRIG_CHID	Alert trigeer channel ID	Section 7.6.1.4
0x4	SEQUENCE_STATUS	Sequence status register	Section 7.6.1.5
0x8	ACC_CH0_LSB	CH0 accumulator data register (LSB)	Section 7.6.1.6
0x9	ACC_CH0_MSB	CH0 accumulated data register (MSB)	Section 7.6.1.7
0xA	ACC_CH1_LSB	CH1 accumulated data register (LSB)	Section 7.6.1.8
0xB	ACC_CH1_MSB	CH1 accumulated data register (MSB)	Section 7.6.1.9
0xC	ALERT_LOW_FLAGS	Alert low flags register	Section 7.6.1.10
0xE	ALERT_HIGH_FLAGS	Alert high flags register	Section 7.6.1.11
0x14	DEVICE_RESET	Device reset register	Section 7.6.1.12
0x15	OFFSET_CAL	Offset calibration register	Section 7.6.1.13
0x17	WKEY	Write key for writing into DEVICE_RESET register	Section 7.6.1.14
0x18	OSC_SEL	Oscillator selection register	Section 7.6.1.15
0x19	NCLK_SEL	nCLK selection register	Section 7.6.1.16
0x1C	OPMODE_SEL	Device operation mode selection	Section 7.6.1.17
0x1E	START_SEQUENCE	Start channel scanning sequence register	Section 7.6.1.18
0x1F	ABORT_SEQUENCE	Abort channel sequence register	Section 7.6.1.19
0x20	AUTO_SEQ_CHEN	Auto sequencing channel select register	Section 7.6.1.20
0x24	CH_INPUT_CFG	Channel input configuration register	Section 7.6.1.21
0x28	DOUT_FORMAT_CFG	Data buffer word configuration register	Section 7.6.1.22
0x2C	DATA_BUFFER_OPMODE	Data buffer operation mode register	Section 7.6.1.23
0x30	ACC_EN	Accumulator control register	Section 7.6.1.24
0x34	ALERT_CHEN	Alert channel enable register	Section 7.6.1.25
0x36	PRE_ALT_MAX_EVENT_COUNT	Pre-alert count register	Section 7.6.1.26
0x37	ALERT_DWC_EN	Alert digital window comparator register	Section 7.6.1.27
0x38	DWC_HTH_CH0_LSB	CH0 high threshold LSB register	Section 7.6.1.28
0x39	DWC_HTH_CH0_MSB	CH0 high threshold MSB register	Section 7.6.1.29
0x3A	DWC_LTH_CH0_LSB	CH0 low threshold LSB register	Section 7.6.1.30
0x3B	DWC_LTH_CH0_MSB	CH0 low threshold MSB register	Section 7.6.1.31
0x3C	DWC_HTH_CH1_LSB	CH1 high threshold LSB register	Section 7.6.1.32
0x3D	DWC_HTH_CH1_MSB	CH1 high threshold MSB register	Section 7.6.1.33
0x3E	DWC_LTH_CH1_LSB	CH1 low threshold LSB register	Section 7.6.1.34
0x3F	DWC_LTH_CH1_MSB	CH1 low threshold MSB register	Section 7.6.1.35
0x40	DWC_HYS_CH0	CH0 comparator hysterisis register	Section 7.6.1.36
0x41	DWC_HYS_CH1	CH1 comparator hysterisis register	Section 7.6.1.37

Complex bit access types are encoded to fit into small table cells. Table 7-6 shows the codes that are used for access types in this section.

Table 7-6. Page1 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value
Register Array Variables		
i,j,k,l,m,n		When these variables are used in a register name, an offset, or an address, they refer to the value of a register array where the register is part of a group of repeating registers. The register groups form a hierarchical structure and the array is represented with a formula.
y		When this variable is used in a register name, an offset, or an address this variable refers to the value of a register array.

7.6.1.1 OPMODE_I2CMODE_STATUS Register (Address = 0x0) [Reset = 0x0]

OPMODE_I2CMODE_STATUS is shown in Figure 7-31 and described in Table 7-7.

Return to the Table 7-5.

Device operation mode register

Figure 7-31. OPMODE_I2CMODE_STATUS Register

7	6	5	4	3	2	1	0
RESERVED					HS_MODE	DEV_OPMODE[1:0]	
R-00000b					R-0b	R-00b	

Table 7-7. OPMODE_I2CMODE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	00000b	Reserved bits. Read returns 00000b.
2	HS_MODE	R	0b	This bit indicates when device is in high speed mode for I2C Interface. 0b = Device is not in high speed mode for I2C Interface. 1b = Device is in high speed mode for I2C Interface.
1-0	DEV_OPMODE[1:0]	R	00b	These bits indicate funtional mode of the device. 00b = Device is operating in manual mode. 01b = Not used. 10b = Device is operating in autonomous monitoring mode. 11b = Device is operating in high precision mode.

7.6.1.2 DATA_BUFFER_STATUS Register (Address = 0x1) [Reset = 0x0]

DATA_BUFFER_STATUS is shown in Figure 7-32 and described in Table 7-8.

Return to the Table 7-5.

Data buffer status register

Figure 7-32. DATA_BUFFER_STATUS Register

7	6	5	4	3	2	1	0
RESERVED			DATA_WORDCOUNT[4:0]				
R-000b			R-00000b				

Table 7-8. DATA_BUFFER_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	000b	Reserved bits. Read returns 000b.
4-0	DATA_WORDCOUNT[4:0]	R	00000b	DATA_WORDCOUNT [00000] to [10000] = Number of entries filled in data buffer (0 to 16)

7.6.1.3 ACCUMULATOR_STATUS Register (Address = 0x2) [Reset = 0x0]

ACCUMULATOR_STATUS is shown in Figure 7-33 and described in Table 7-9.

Return to the Table 7-5.

Status of ADC accumulator

Figure 7-33. ACCUMULATOR_STATUS Register

7	6	5	4	3	2	1	0
RESERVED				ACC_COUNT[3:0]			
R-0000b				R-0000b			

Table 7-9. ACCUMULATOR_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0000b	Reserved bits. Read returns 0000b.
3-0	ACC_COUNT[3:0]	R	0000b	ACC_COUNT = Number of accumulation completed till last finished conversion.

7.6.1.4 ALERT_TRIG_CHID Register (Address = 0x3) [Reset = 0x0]

ALERT_TRIG_CHID is shown in Figure 7-34 and described in Table 7-10.

Return to the Table 7-5.

Alert trigeer channel ID

Figure 7-34. ALERT_TRIG_CHID Register

7	6	5	4	3	2	1	0
ALERT_TRIG_CHID[3:0]				RESERVED			
R-0000b				R-0000b			

Table 7-10. ALERT_TRIG_CHID Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	ALERT_TRIG_CHID[3:0]	R	0000b	These bits provide the channel ID of channel which was first to set the alert output. 0000b = Channel 0. 0001b = Channel 1.
3-0	RESERVED	R	0000b	Reserved bits. Reads returns 0000b.

7.6.1.5 SEQUENCE_STATUS Register (Address = 0x4) [Reset = 0x0]

SEQUENCE_STATUS is shown in Figure 7-35 and described in Table 7-11.

Return to the Table 7-5.

Sequence status register

Figure 7-35. SEQUENCE_STATUS Register

7	6	5	4	3	2	1	0
RESERVED					SEQ_ERR_ST[1:0]		RESERVED
R-00000b					R-00b		R-0b

Table 7-11. SEQUENCE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	00000b	Reserved bits. Read returns 00000b.
2-1	SEQ_ERR_ST[1:0]	R	00b	These bits give status of device sequence. 00b = Auto sequencing disabled, no error. 01b = Auto sequencing enabled, no error. 10b = Not used. 11b = Auto sequencing enabled, device in error.
0	RESERVED	R	0b	Reserved bit. Read returns 0b.

7.6.1.6 ACC_CH0_LSB Register (Address = 0x8) [Reset = 0x0]

ACC_CH0_LSB is shown in Figure 7-36 and described in Table 7-12.

Return to the Table 7-5.

CH0 accumulator data register (LSB)

Figure 7-36. ACC_CH0_LSB Register

7	6	5	4	3	2	1	0
CH0_LSB[7:0]							
R-00000000b							

Table 7-12. ACC_CH0_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CH0_LSB[7:0]	R	00000000b	LSB of accumulated data for CH0.

7.6.1.7 ACC_CH0_MSB Register (Address = 0x9) [Reset = 0x0]

ACC_CH0_MSB is shown in Figure 7-37 and described in Table 7-13.

Return to the Table 7-5.

CH0 accumulated data register (MSB)

Figure 7-37. ACC_CH0_MSB Register

7	6	5	4	3	2	1	0
CH0_MSB[7:0]							
R-00000000b							

Table 7-13. ACC_CH0_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CH0_MSB[7:0]	R	00000000b	MSB of accumulated data for CH0.

7.6.1.8 ACC_CH1_LSB Register (Address = 0xA) [Reset = 0x0]

ACC_CH1_LSB is shown in Figure 7-38 and described in Table 7-14.

Return to the Table 7-5.

CH1 accumulated data register (LSB)

Figure 7-38. ACC_CH1_LSB Register

7	6	5	4	3	2	1	0
CH1_LSB[7:0]							
R-00000000b							

Table 7-14. ACC_CH1_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CH1_LSB[7:0]	R	00000000b	LSB of accumulated data for CH1.

7.6.1.9 ACC_CH1_MSB Register (Address = 0xB) [Reset = 0x0]

ACC_CH1_MSB is shown in Figure 7-39 and described in Table 7-15.

Return to the Table 7-5.

CH1 accumulated data register (MSB)

Figure 7-39. ACC_CH1_MSB Register

7	6	5	4	3	2	1	0
CH1_MSB[7:0]							
R-00000000b							

Table 7-15. ACC_CH1_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CH1_MSB[7:0]	R	00000000b	MSB of accumulated data for CH1.

7.6.1.10 ALERT_LOW_FLAGS Register (Address = 0xC) [Reset = 0x0]

ALERT_LOW_FLAGS is shown in Figure 7-40 and described in Table 7-16.

Return to the Table 7-5.

Alert low flags register

Figure 7-40. ALERT_LOW_FLAGS Register

7	6	5	4	3	2	1	0
RESERVED						ALERT_LOW_CH1	ALERT_LOW_CH0
R-000000b						R/W-0b	R/W-0b

Table 7-16. ALERT_LOW_FLAGS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	000000b	Reserved bits. Read returns 000000b.
1	ALERT_LOW_CH1	R/W	0b	This bit indicates alert on low side comparator for CH1. 0b = Alert is not set for low side comparator for CH1. 1b = Alert is set for low side comparator for CH1.
0	ALERT_LOW_CH0	R/W	0b	This bit indicates alert on low side comparator for CH0. 0b = Alert is not set for low side comparator for CH0. 1b = Alert is set for low side comparator for CH0.

7.6.1.11 ALERT_HIGH_FLAGS Register (Address = 0xE) [Reset = 0x0]

ALERT_HIGH_FLAGS is shown in Figure 7-41 and described in Table 7-17.

Return to the Table 7-5.

Alert high flags register

Figure 7-41. ALERT_HIGH_FLAGS Register

7	6	5	4	3	2	1	0
RESERVED						ALERT_HIGH_CH1	ALERT_HIGH_CH0
R-000000b						R/W-0b	R/W-0b

Table 7-17. ALERT_HIGH_FLAGS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	000000b	Reserved bits. Read returns 000000b.
1	ALERT_HIGH_CH1	R/W	0b	This bit indicates alert on high side comparator of CH1. 0b = Alert is not set for high side comparator for CH1. 1b = Alert is set for high side comparator for CH1.
0	ALERT_HIGH_CH0	R/W	0b	This bit indicates alert on high side comparator for CH0. 0b = Alert is not set for high side comparator for CH0. 1b = Alert is set for high side comparator for CH0.

7.6.1.12 DEVICE_RESET Register (Address = 0x14) [Reset = 0x0]

DEVICE_RESET is shown in Figure 7-42 and described in Table 7-18.

Return to the Table 7-5.

Device reset register

Figure 7-42. DEVICE_RESET Register

7	6	5	4	3	2	1	0
RESERVED							DEV_RST
R-0000000b							W-0b

Table 7-18. DEVICE_RESET Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0000000b	Reserved bits. Read returns 0000000b.
0	DEV_RST	W	0b	Writing 1 to this bit resets the device.

7.6.1.13 OFFSET_CAL Register (Address = 0x15) [Reset = 0x0]

OFFSET_CAL is shown in Figure 7-43 and described in Table 7-19.

Return to the Table 7-5.

Offset calibration register

Figure 7-43. OFFSET_CAL Register

7	6	5	4	3	2	1	0
RESERVED							TRIG_OFFCAL
R-0000000b							W-0b

Table 7-19. OFFSET_CAL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0000000b	Reserved bits. Read returns 0000000b.
0	TRIG_OFFCAL	W	0b	Writing 1 into this bit triggers internal offset calibration.

7.6.1.14 WKEY Register (Address = 0x17) [Reset = 0x0]

WKEY is shown in Figure 7-44 and described in Table 7-20.

Return to the Table 7-5.

Write key for writing into DEVICE_RESET register

Figure 7-44. WKEY Register

7	6	5	4	3	2	1	0
RESERVED				WKEY[3:0]			
R-0000b				R/W-0000b			

Table 7-20. WKEY Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0000b	Reserved bits. Do not write. Read returns 0000b.
3-0	WKEY[3:0]	R/W	0000b	Write 1010b into these bits to get write access for the DEVICE_RESET register. WKEY register is not reset to default value on device reset (see Reset section). After coming out of device reset, write 00h to the WKEY register to prevent erroneous reset.

7.6.1.15 OSC_SEL Register (Address = 0x18) [Reset = 0x0]

OSC_SEL is shown in Figure 7-45 and described in Table 7-21.

Return to the Table 7-5.

Oscillator selection register

Figure 7-45. OSC_SEL Register

7	6	5	4	3	2	1	0
RESERVED							HSZ_LP
R-0000000b							R/W-0b

Table 7-21. OSC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0000000b	Reserved bits. Read returns 0000000b.
0	HSZ_LP	R/W	0b	This bit selects oscillator used for the conversion process and cycle time for a single conversion. 0b = Device uses high speed oscillator. 1b = Device uses low power oscillator.

7.6.1.16 NCLK_SEL Register (Address = 0x19) [Reset = 0x0]

NCLK_SEL is shown in Figure 7-46 and described in Table 7-22.

Return to the Table 7-5.

nCLK selection register

Figure 7-46. NCLK_SEL Register

7	6	5	4	3	2	1	0
NCLK[7:0]							
R/W-00000000b							

Table 7-22. NCLK_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	NCLK[7:0]	R/W	00000000b	Sets number of clocks of the oscillator that the device uses for one conversion cycle. When using the High Speed Oscillator: For Value x written into the nCLK register • if x ≤ 21, nCLK is set to 21 (00010101b) • if x > 21, nCLK is set to x When using the Low Power Oscillator, For Value x written into the nCLK register: • if x ≤ 18, nCLK is set to 18 (00010010b) • if x > 18, nCLK is set to x

7.6.1.17 OPMODE_SEL Register (Address = 0x1C) [Reset = 0x0]

OPMODE_SEL is shown in Figure 7-47 and described in Table 7-23.

Return to the Table 7-5.

Device operation mode selection

Figure 7-47. OPMODE_SEL Register

7	6	5	4	3	2	1	0
RESERVED					SEL_OPMODE[2:0]		
R-00000b					R/W-000b		

Table 7-23. OPMODE_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	00000b	Reserved bits. Read returns 00000b
2-0	SEL_OPMODE[2:0]	R/W	000b	These bits set the functional mode for the device. 000b = Manual mode with CH0 only (Default mode). 001b = Manual mode with CH0 only (Default mode). 010b = Reserved. Do not use. 011b = Reserved. Do not use. 100b = Manual mode with AUTO Sequencing enabled. 101b = Manual Mode with AUTO Sequencing enabled. 110b = Autonomous monitoring mode with AUTO sequencing enabled. 111b = High precision mode with AUTO sequencing enabled.

7.6.1.18 START_SEQUENCE Register (Address = 0x1E) [Reset = 0x0]

START_SEQUENCE is shown in Figure 7-48 and described in Table 7-24.

Return to the Table 7-5.

Start channel scanning sequence register

Figure 7-48. START_SEQUENCE Register

7	6	5	4	3	2	1	0
RESERVED							SEQ_START
R-0000000b							W-0b

Table 7-24. START_SEQUENCE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0000000b	Reserved bits. Read returns 0000000b.
0	SEQ_START	W	0b	Setting this bit to 1 brings the BUSY/RDY pin high and starts the first conversion in the sequence.

7.6.1.19 ABORT_SEQUENCE Register (Address = 0x1F) [Reset = 0x0]

ABORT_SEQUENCE is shown in Figure 7-49 and described in Table 7-25.

Return to the Table 7-5.

Abort channel sequence register

Figure 7-49. ABORT_SEQUENCE Register

7	6	5	4	3	2	1	0
RESERVED							SEQ_ABORT
R-0000000b							W-0b

Table 7-25. ABORT_SEQUENCE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0000000b	Reserved bits. Read returns 0000000b.
0	SEQ_ABORT	W	0b	Setting this bit to 1 aborts the ongoing conversion and brings the BUSY/RDY pin low.

7.6.1.20 AUTO_SEQ_CHEN Register (Address = 0x20) [Reset = 0x3]

AUTO_SEQ_CHEN is shown in Figure 7-50 and described in Table 7-26.

Return to the Table 7-5.

Auto sequencing channel select register

Figure 7-50. AUTO_SEQ_CHEN Register

7	6	5	4	3	2	1	0
RESERVED						AUTOSEQ_EN_CH1	AUTOSEQ_EN_CH0
R-000000b						R/W-1b	R/W-1b

Table 7-26. AUTO_SEQ_CHEN Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	000000b	Reserved bits. Read returns 000000b.
1	AUTOSEQ_EN_CH1	R/W	1b	This bit selects CH1 for auto sequencing. 0b = Channel 1 is not selected for auto sequencing. 1b = Channel 1 is selected for auto sequencing.
0	AUTOSEQ_EN_CH0	R/W	1b	This bit selects CH0 for auto sequencing. 0b = Channel 0 is not selected for auto sequencing. 1b = Channel 0 is selected for auto sequencing.

7.6.1.21 CH_INPUT_CFG Register (Address = 0x24) [Reset = 0x0]

CH_INPUT_CFG is shown in Figure 7-51 and described in Table 7-27.

Return to the Table 7-5.

Channel input configuration register

Figure 7-51. CH_INPUT_CFG Register

7	6	5	4	3	2	1	0
RESERVED						CH0_CH1_IP_CFG[1:0]	
R-000000b						R/W-00b	

Table 7-27. CH_INPUT_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	000000b	Reserved bits. Read returns 000000b.
1-0	CH0_CH1_IP_CFG[1:0]	R/W	00b	This bit selects configuration for the input pins. 00b = Two-channel, single-ended configuration. 01b = Single-channel, single-ended configuration with remote ground sensing. 10b = Single-channel, pseudo-differential configuration. 11b = Two-channel, single-ended configuration.

7.6.1.22 DOUT_FORMAT_CFG Register (Address = 0x28) [Reset = 0x0]

DOUT_FORMAT_CFG is shown in Figure 7-52 and described in Table 7-28.

Return to the Table 7-5.

Data buffer word configuration register

Figure 7-52. DOUT_FORMAT_CFG Register

7	6	5	4	3	2	1	0
RESERVED						DOUT_FORMAT[1:0]	
R-000000b						R/W-00b	

Table 7-28. DOUT_FORMAT_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	000000b	Reserved bits. Read returns 000000b.
1-0	DOUT_FORMAT[1:0]	R/W	00b	These bits select 16-bit content of the data word in the data buffer. 00b = 12-bit conversion result followed by 0000b. 01b = 12-bit conversion result followed by 3-bit channel ID (000b for CH0, 001b for CH1). 10b = 12-bit conversion result followed by 3-bit channel ID (000b for CH0, 001b for CH1) followed by DATA_VALID bit. 11b = 12-bit conversion result followed by 0000b.

7.6.1.23 DATA_BUFFER_OPMODE Register (Address = 0x2C) [Reset = 0x1]

DATA_BUFFER_OPMODE is shown in Figure 7-53 and described in Table 7-29.

Return to the Table 7-5.

Data buffer operation mode register

Figure 7-53. DATA_BUFFER_OPMODE Register

7	6	5	4	3	2	1	0
RESERVED					STARTSTOP_CNTRL[2:0]		
R-00000b					R/W-001b		

Table 7-29. DATA_BUFFER_OPMODE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	00000b	Reserved bits. Read returns 00000b.
2-0	STARTSTOP_CNTRL[2:0]	R/W	001b	These bits select data buffer mode of operation. 000b = Stop burst mode. 001b = Start burst mode, default. 010b = Reserved, do not use. 011b = Reserved, do not use. 100b = Pre alert data mode. 101b = Reserved, do not use. 110b = Post alert data mode. 111b = Reserved, do not use.

7.6.1.24 ACC_EN Register (Address = 0x30) [Reset = 0x0]

ACC_EN is shown in Figure 7-54 and described in Table 7-30.

Return to the Table 7-5.

Accumulator control register

Figure 7-54. ACC_EN Register

7	6	5	4	3	2	1	0
RESERVED				EN_ACC[3:0]			
R-0000b				R/W-0000b			

Table 7-30. ACC_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0000b	Reserved bits. Read returns 0000b.
3-0	EN_ACC[3:0]	R/W	0000b	These bits enable accumulator function of device. 0001b to 1110b settings are reserved. Do not use. 0000b = Accumulator is disabled. 1111b = Accumulator is enabled.

7.6.1.25 ALERT_CHEN Register (Address = 0x34) [Reset = 0x0]

ALERT_CHEN is shown in Figure 7-55 and described in Table 7-31.

Return to the Table 7-5.

Alert channel enable register

Figure 7-55. ALERT_CHEN Register

7	6	5	4	3	2	1	0
RESERVED						ALERT_EN_CH1	ALERT_EN_CH0
R-000000b						R/W-0b	R/W-0b

Table 7-31. ALERT_CHEN Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	000000b	Reserved bits. Read returns 000000b.
1	ALERT_EN_CH1	R/W	0b	This bit enables alert functionality of CH1. 0b = Alert is disabled for CH1, default. 1b = Alert is enabled for CH1.
0	ALERT_EN_CH0	R/W	0b	This bit enables alert functionality for CH0. 0b = Alert is disabled for CH0, default. 1b = Alert is enabled for CH0.

7.6.1.26 PRE_ALT_MAX_EVENT_COUNT Register (Address = 0x36) [Reset = 0x0]

PRE_ALT_MAX_EVENT_COUNT is shown in Figure 7-56 and described in Table 7-32.

Return to the Table 7-5.

Pre-alert count register

Figure 7-56. PRE_ALT_MAX_EVENT_COUNT Register

7	6	5	4	3	2	1	0
PREALERT_COUNT[3:0]				RESERVED			
R/W-0000b				R-0000b			

Table 7-32. PRE_ALT_MAX_EVENT_COUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	PREALERT_COUNT[3:0]	R/W	0000b	These bits set the Pre-Alert Event Count = PREALERT_COUNT [7:4] + 1
3-0	RESERVED	R	0000b	Reserved bits. Read returns 0000b.

7.6.1.27 ALERT_DWC_EN Register (Address = 0x37) [Reset = 0x0]

ALERT_DWC_EN is shown in Figure 7-57 and described in Table 7-33.

Return to the Table 7-5.

Alert digital window comparator register

Figure 7-57. ALERT_DWC_EN Register

7	6	5	4	3	2	1	0
RESERVED							DWC_BLOCK_EN
R-0000000b							R/W-0b

Table 7-33. ALERT_DWC_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0000000b	Reserved bits. Read returns 0000000b.
0	DWC_BLOCK_EN	R/W	0b	This bit enables digital window comparator block. 0b = Disables digital window comparator. 1b = Enables digital window comparator.

7.6.1.28 DWC_HTH_CH0_LSB Register (Address = 0x38) [Reset = 0x0]

DWC_HTH_CH0_LSB is shown in Figure 7-58 and described in Table 7-34.

Return to the Table 7-5.

CH0 high threshold LSB register

Figure 7-58. DWC_HTH_CH0_LSB Register

7	6	5	4	3	2	1	0
HTH_CH0_LSB[7:0]							
R/W-00000000b							

Table 7-34. DWC_HTH_CH0_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	HTH_CH0_LSB[7:0]	R/W	00000000b	These are 8 least significant bits of high threshold for CH0.

7.6.1.29 DWC_HTH_CH0_MSB Register (Address = 0x39) [Reset = 0x0]

DWC_HTH_CH0_MSB is shown in Figure 7-59 and described in Table 7-35.

Return to the Table 7-5.

CH0 high threshold MSB register

Figure 7-59. DWC_HTH_CH0_MSB Register

7	6	5	4	3	2	1	0
RESERVED				HTH_CH0_MSB[3:0]			
R-0000b				R/W-0000b			

Table 7-35. DWC_HTH_CH0_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0000b	Reserved bits. Read returns 0000b.
3-0	HTH_CH0_MSB[3:0]	R/W	0000b	These are 4 most significant bits of high threshold for CH0.

7.6.1.30 DWC_LTH_CH0_LSB Register (Address = 0x3A) [Reset = 0x0]

DWC_LTH_CH0_LSB is shown in Figure 7-60 and described in Table 7-36.

Return to the Table 7-5.

CH0 low threshold LSB register

Figure 7-60. DWC_LTH_CH0_LSB Register

7	6	5	4	3	2	1	0
LTH_CH0_LSB[7:0]							
R/W-00000000b							

Table 7-36. DWC_LTH_CH0_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LTH_CH0_LSB[7:0]	R/W	00000000b	These are 8 least significant bits of low threshold for CH0.

7.6.1.31 DWC_LTH_CH0_MSB Register (Address = 0x3B) [Reset = 0x0]

DWC_LTH_CH0_MSB is shown in Figure 7-61 and described in Table 7-37.

Return to the Table 7-5.

CH0 low threshold MSB register

Figure 7-61. DWC_LTH_CH0_MSB Register

7	6	5	4	3	2	1	0
RESERVED				LTH_CH0_MSB[3:0]			
R-0000b				R/W-0000b			

Table 7-37. DWC_LTH_CH0_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0000b	Reserved bits. Read returns 0000b.
3-0	LTH_CH0_MSB[3:0]	R/W	0000b	These are 4 most significant bits of low threshold for CH0.

7.6.1.32 DWC_HTH_CH1_LSB Register (Address = 0x3C) [Reset = 0x0]

DWC_HTH_CH1_LSB is shown in Figure 7-62 and described in Table 7-38.

Return to the Table 7-5.

CH1 high threshold LSB register

Figure 7-62. DWC_HTH_CH1_LSB Register

7	6	5	4	3	2	1	0
HTH_CH1_LSB[7:0]							
R/W-00000000b							

Table 7-38. DWC_HTH_CH1_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	HTH_CH1_LSB[7:0]	R/W	00000000b	These are 8 least significant bits of high threshold for CH1.

7.6.1.33 DWC_HTH_CH1_MSB Register (Address = 0x3D) [Reset = 0x0]

DWC_HTH_CH1_MSB is shown in Figure 7-63 and described in Table 7-39.

Return to the Table 7-5.

CH1 high threshold MSB register

Figure 7-63. DWC_HTH_CH1_MSB Register

7	6	5	4	3	2	1	0
RESERVED				HTH_CH1_MSB[3:0]			
R-0000b				R/W-0000b			

Table 7-39. DWC_HTH_CH1_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0000b	Reserved bits. Read returns 0000b.
3-0	HTH_CH1_MSB[3:0]	R/W	0000b	These are 4 most significant bits of high threshold for CH1.

7.6.1.34 DWC_LTH_CH1_LSB Register (Address = 0x3E) [Reset = 0x0]

DWC_LTH_CH1_LSB is shown in Figure 7-64 and described in Table 7-40.

Return to the Table 7-5.

CH1 low threshold LSB register

Figure 7-64. DWC_LTH_CH1_LSB Register

7	6	5	4	3	2	1	0
LTH_CH1_LSB[7:0]							
R/W-00000000b							

Table 7-40. DWC_LTH_CH1_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LTH_CH1_LSB[7:0]	R/W	00000000b	These are 8 least significant bits of low threshold for CH1.

7.6.1.35 DWC_LTH_CH1_MSB Register (Address = 0x3F) [Reset = 0x0]

DWC_LTH_CH1_MSB is shown in Figure 7-65 and described in Table 7-41.

Return to the Table 7-5.

CH1 low threshold MSB register

Figure 7-65. DWC_LTH_CH1_MSB Register

7	6	5	4	3	2	1	0
RESERVED				LTH_CH1_MSB[3:0]			
R-0000b				R/W-0000b			

Table 7-41. DWC_LTH_CH1_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0000b	Reserved bits. Read returns 0000b.
3-0	LTH_CH1_MSB[3:0]	R/W	0000b	These are 4 most significant bits of low threshold for CH1.

7.6.1.36 DWC_HYS_CH0 Register (Address = 0x40) [Reset = 0x0]

DWC_HYS_CH0 is shown in Figure 7-66 and described in Table 7-42.

Return to the Table 7-5.

CH0 comparator hysterisis register

Figure 7-66. DWC_HYS_CH0 Register

7	6	5	4	3	2	1	0
RESERVED		HYS_CH0[5:0]					
R-00b		R/W-000000b					

Table 7-42. DWC_HYS_CH0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	00b	Reserved bits. Read returns 00b.
5-0	HYS_CH0[5:0]	R/W	000000b	These bits set hysteresis for both comparators for CH0.

7.6.1.37 DWC_HYS_CH1 Register (Address = 0x41) [Reset = 0x0]

DWC_HYS_CH1 is shown in Figure 7-67 and described in Table 7-43.

Return to the Table 7-5.

CH1 comparator hysterisis register

Figure 7-67. DWC_HYS_CH1 Register

7	6	5	4	3	2	1	0
RESERVED		HYS_CH1[5:0]					
R-00b		R/W-000000b					

Table 7-43. DWC_HYS_CH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	00b	Reserved bits. Read returns 00b.
5-0	HYS_CH1[5:0]	R/W	000000b	These bits set hysteresis for both comparators for CH1.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

In an increasing number of industrial applications, data acquisition sub-systems are collecting more data about the environment in which the system is operating and applying deep learning algorithms in order to improve system reliability, implement preventative maintenance, and enhance the quality of data collected by the system. The ADS7142-Q1 can be used to connect to a variety of sensors and can provide deeper data analytics at lower power levels than existing solutions. The depth of analysis that can be performed on the data collected by the ADS7142-Q1 is enhanced by the internal data buffer, programmable alarm thresholds and hysteresis, event counter, and internal calibration circuitry. The applications circuits described in this section highlight specific use cases of the ADS7142-Q1 for data collection that can further increase the depth and quality of the data being measured by the system.

8.2 Typical Applications

8.2.1 ADS7142-Q1 as a Programmable Comparator With False Trigger Prevention and Diagnostics

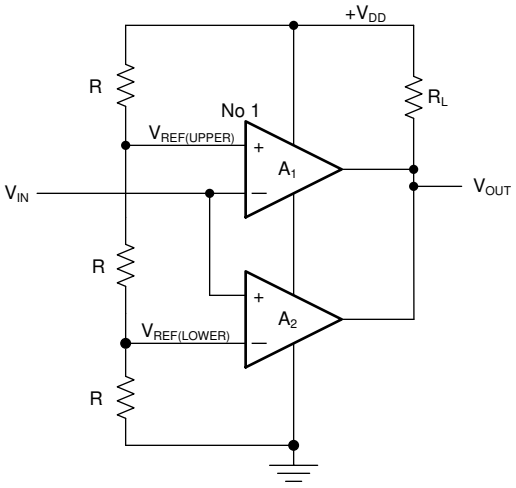


Figure 8-1. Analog Window Comparator

8.2.1.1 Design Requirements

In many automotive sensor monitors, a decision must be made at the system-level when the input signal crosses a predefined threshold. Analog window comparators are used extensively in such applications.

An analog window comparator has a set of comparators. The external input signal is connected to the inverting terminal of one comparator and the noninverting terminal of the other comparator. The remaining input of each comparator is connected to the internal reference. The outputs are tied together and are often connected to a reset or general-purpose input of a processor (such as a digital signal processor, field-programmable gate array, or application-specific integrated circuit) or the enable input of a voltage regulator (such as a DC/DC or low-dropout regulator). Figure 8-1 shows the circuit diagram for an analog window comparator.

Though analog comparators are easy to design, there are certain disadvantages associated with analog comparators.

- Higher power consumption: If the voltage being monitored is greater than the window comparator supply voltage, then a resistive divider ladder must scale down that voltage. This resistive ladder draws a constant current and adds to the power consumption of the system. In battery-powered applications, this current draw becomes a challenge and can adversely affect the battery life.
- Fixed threshold voltages: The window comparator thresholds cannot be changed on-the-fly because these thresholds are set by hardware (typically with a resistive ladder). These fixed voltages may add a limitation if the comparator thresholds must be changed during operation without switching in a new resistor ladder.

Automotive systems often require a device that monitors either critical voltage rails, temperature of the critical blocks or sensors, and gives an alert or interrupt to the host MCU only when the input being monitored crosses a predefined, programmable threshold. The ADS7142-Q1 is an excellent fit for such system level monitoring because this device can autonomously monitor sensor outputs and can wake up the host controller whenever the sensor output crosses predefined thresholds. Additionally, the ADS7142-Q1 has an internal data buffer that can store 16 sample data that can read in case further analysis is required. Figure 8-2 shows a typical block diagram of the ADS7142-Q1 as a sensor monitor. As is shown in this figure, the sensor can be connected directly to the input of the ADC (depending on the sensor output signal characteristics).

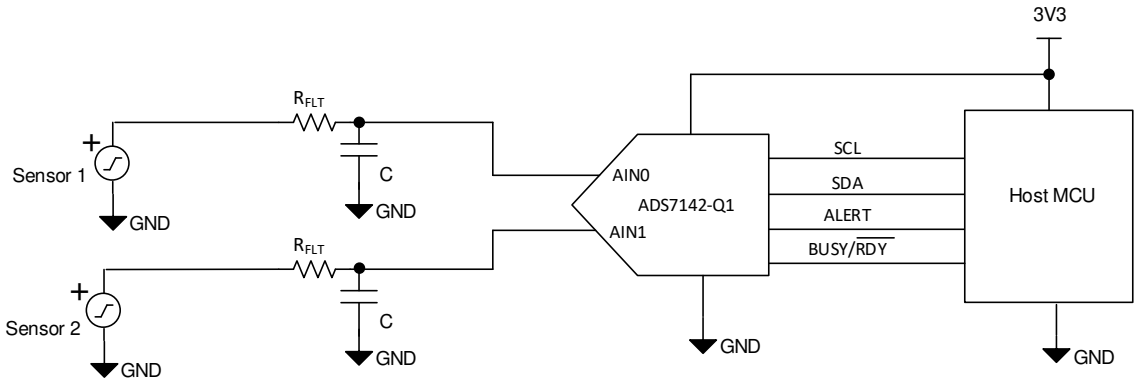


Figure 8-2. Sensor Monitor Circuit With the ADS7142-Q1

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Programmable Thresholds and Hysteresis

The ADS7142-Q1 can be programmed to monitor sensor output voltages and generate an $\overline{\text{ALERT}}$ signal to the host controller if the sensor output voltage crosses a threshold.

The device can be configured to monitor for signals rising above a programmed threshold. Figure 8-3 illustrates the operation of the device when monitoring for signal crossings on the low threshold by setting the high threshold to 0xFFF. In this case, the output of the low-side comparator is set whenever the ADC conversion result is less than or equal to the low threshold, and the output of the high-side comparator is only set when the ADC conversion result is equal to 0xFFF.

The device can also be configured to monitor for signals falling below a programmed threshold. Figure 8-4 illustrates the operation of the device when monitoring for signal crossings on the high threshold by setting the low threshold to 0x000. In this case, the output of high-side comparator is set whenever the ADC conversion result is greater than or equal to the high threshold and the output of the low-side comparator is only set when the ADC conversion result is equal to 0x000.

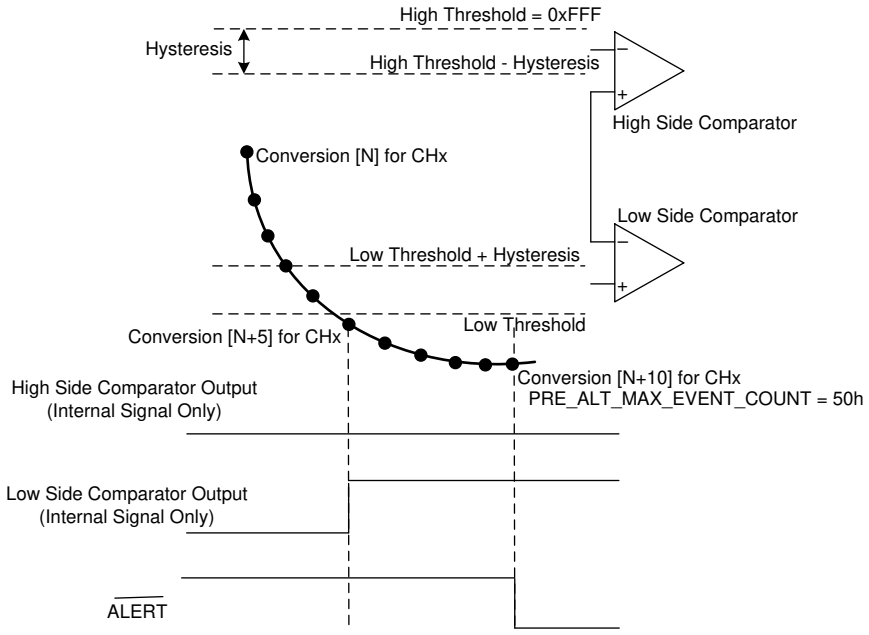


Figure 8-3. Low Alert With the ADS7142-Q1

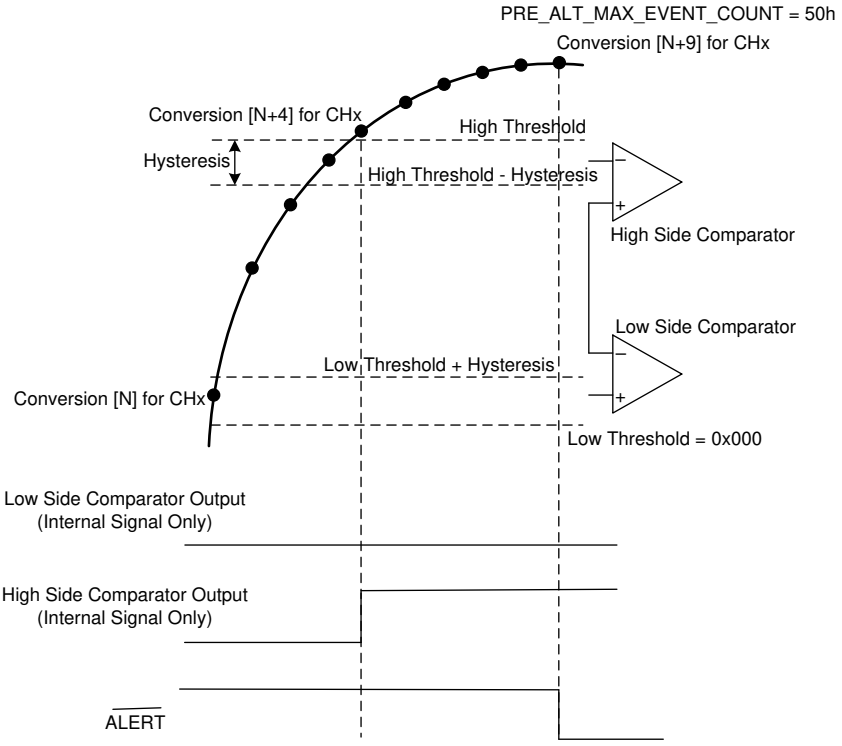


Figure 8-4. High Alert With the ADS7142-Q1

The device can also be configured to monitor for signals falling outside of a programmed window. Figure 8-5 shows the device operation for an out-of-range alert where the signal leaves the predefined window and crosses either the high or low threshold. In this case, the output of the low-side comparator is set whenever the ADC conversion result is less than or equal to the low threshold, and the output of the high-side comparator is set when the ADC conversion result is greater than or equal to the high threshold.

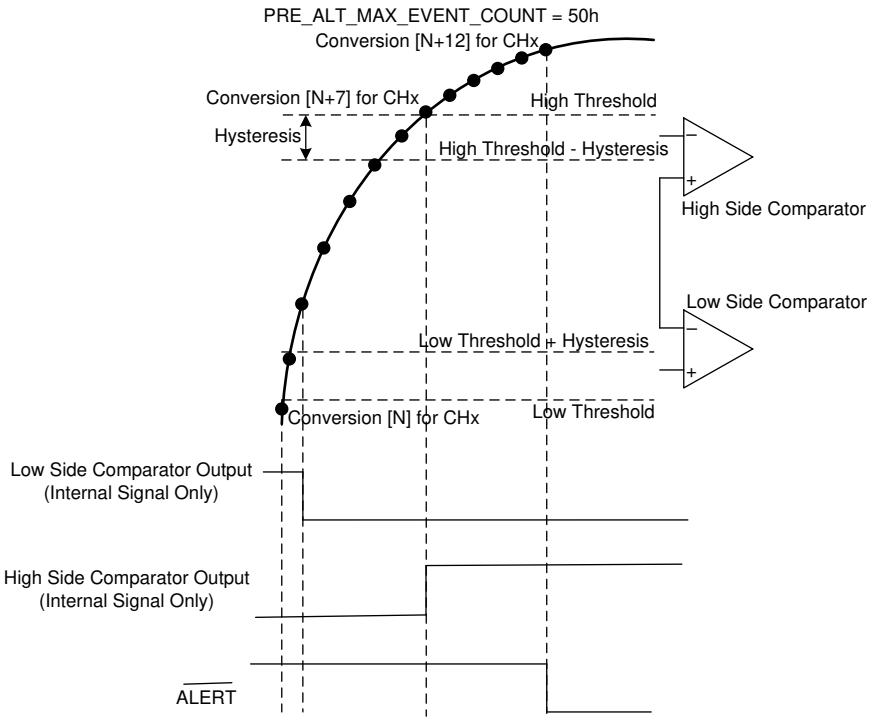


Figure 8-5. Out of Range Alert With the ADS7142-Q1

8.2.1.2.2 False Trigger Prevention With an Event Counter

The pre-alert event counter in the *digital window comparator* helps prevent false triggers. The alert output is not set until the output of the comparator remains set for a predefined number (count) of consecutive conversions.

8.2.1.2.3 Fault Diagnostics With the Data Buffer

The modes that are specifically designed for autonomous sensor monitor applications are pre-alert mode and post-alert mode. In pre-alert mode, the ADS7142-Q1 can be configured to monitor sensor outputs and continuously fill the internal data buffer until a threshold crossing occurs. The ADS7142-Q1 generates an ALERT signal when the sensor output falls outside of the predefined window of operation. In this particular mode, the ADS7142-Q1 stops filling the data buffer when the threshold is crossed and provides the last 16 samples (15 sample data preceding the sample at which the ALERT is generated and 1 sample data for which the ALERT is generated). Figure 8-6 depicts the ADS7142-Q1 operation in pre-alert mode showing 16 data samples before the sensor output crosses the low threshold. This operation is useful for applications where the state of the signal before the threshold is crossed is important to capture. Using the data captured before the alert, deep data analysis can be performed to determine the state of the system before the alert. This type of data is not available with analog comparators.

In post-alert mode, ADS7142-Q1 can be configured to monitor sensor outputs and start filling the internal data buffer after a threshold crossing occurs. The ADS7142-Q1 generates an ALERT signal when the sensor output falls outside of the predefined window of operation. In this particular mode, the ADS7142-Q1 continues to fill the data buffer after the threshold is crossed for a total of 16 samples (1 sample data for which ALERT is generated and 15 sample data after the sample at which ALERT is generated). Figure 8-7 illustrates the ADS7142-Q1 operation in post-alert mode showing 16 data samples after the sensor output crosses the high threshold. This operation is useful for applications where the state of the signal after the threshold is crossed is important to capture. Using the data captured after the alert, deep data analysis can be performed for to determine the state of the system after the alert to detect system-level events such as saturation. This data is not available with analog comparators.

8.2.1.3 Application Curves

Figure 8-6. Pre-Alert Data Capture

Figure 8-7. Post-Alert Data Capture

8.2.2 Voltage and Temperature Monitoring in Remote Camera Modules Using the ADS7142-Q1

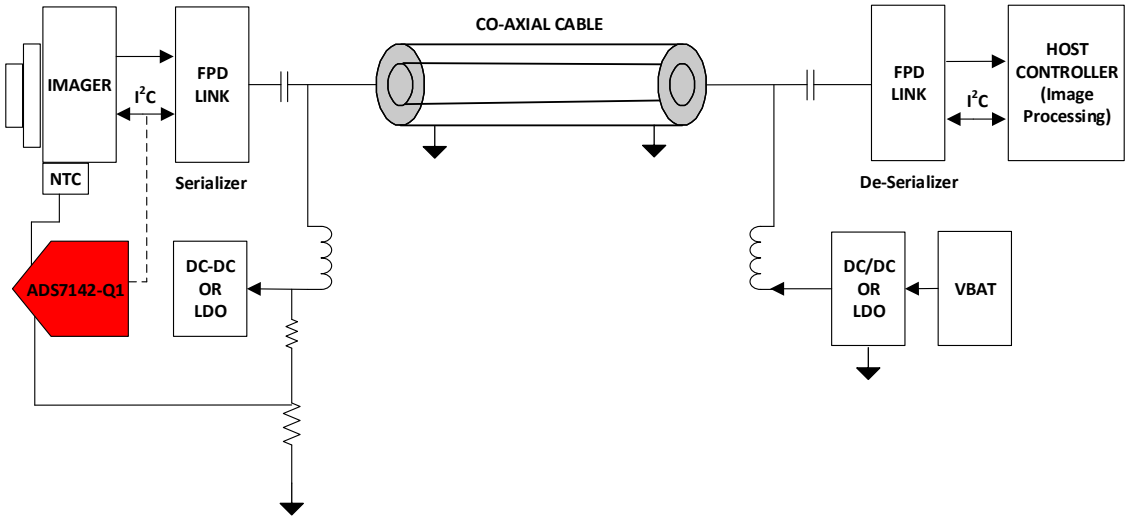


Figure 8-8. Voltage and Temperature Sensing in Remote Camera Modules Using the ADS7142-Q1

8.2.2.1 Design Requirements

Camera modules are an integral part of advanced driver assistance systems (ADAS), which are designed to make cars safer. Automotive cameras and camera modules are often assist in blind spot detection, nap prevention, lane and border detection, surround view and parking. Based on application, there are multiple types of camera modules available such as front camera, rear camera, night vision camera. Figure 8-8 shows the typical block diagram of camera module used in an automotive environment with key electronics building blocks in the system.

The camera module is usually situated externally at front, back or either side of the vehicle. Many times the main controller that does the data processing can not be used on camera module side due to size constraints. The camera module unit communicates with central processor over co-axial cable. The camera module data is transmitted over a coaxial cable using a serializer. On the data processing unit, a deserializer is used to communicate this data with the host processor. The power to the camera module is also transmitted over a coaxial cable. Because the camera module is remotely placed and power is transferred over a coaxial cable that can be few meters long, voltage received by camera module and critical voltage rails powering image sensors are often monitored against permissible variations. Also, the difference between camera lens and external ambient temperature can introduce dampness and degrade video quality. To ensure optimal video quality, camera lens temperature is often monitored for any possible correction. The device monitoring these system-level parameters must be a small size because of the limited board space available on the camera module side. Also, the I^2C interface is preferred because this interface enables the user to connect multiple monitoring and sensing devices on the same I^2C bus. The ADS7142-Q1 small footprint (2-mm × 3-mm, WSON package) and the I^2C interface capable of working over wide digital I/O voltages enable this device in camera module monitoring applications without demanding extra board space.

8.3 Power Supply Recommendations

8.3.1 AVDD and DVDD Supply Recommendations

The ADS7142-Q1 has two separate power supplies: AVDD and DVDD. The device operates on AVDD; DVDD is used for the interface circuits. AVDD and DVDD can be independently set to any value within the permissible ranges. The AVDD supply also defines the full-scale input range of the device. Always set the AVDD supply to be greater than or equal to the maximum input signal to avoid saturation of codes. Decouple the AVDD and DVDD pins respectively with C_{AVDD} = 220 nF and C_{DVDD} = 100 nF ceramic decoupling capacitors, as illustrated in Figure 8-9.

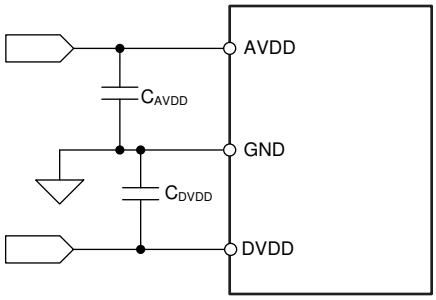


Figure 8-9. Power-Supply Decoupling

8.4 Layout

8.4.1 Layout Guidelines

- Use a solid ground plane underneath the device and partition the PCB into analog and digital sections.
- Avoid crossing digital lines with the analog signal path and keep the analog input signals and the reference input signals away from noise sources.
- The power sources to the device must be clean and well-bypassed. Use C_{AVDD} decoupling capacitors in close proximity to the analog (AVDD) power-supply pin.
- Use a C_{DVDD} decoupling capacitor close to the digital (DVDD) power-supply pin.
- Avoid placing vias between the AVDD and DVDD pins and the bypass capacitors.
- Connect the ground pin to the ground plane using a short, low-impedance path. Also connect the thermal pad to the ground plane.
- Place the charge kickback filter components close to the device.

Among ceramic surface-mount capacitors, COG (NPO) ceramic capacitors are recommended because these components provide the most stable electrical properties over voltage, frequency, and temperature changes.

Figure 8-10 shows the typical connection diagram of the ADS7142-Q1.

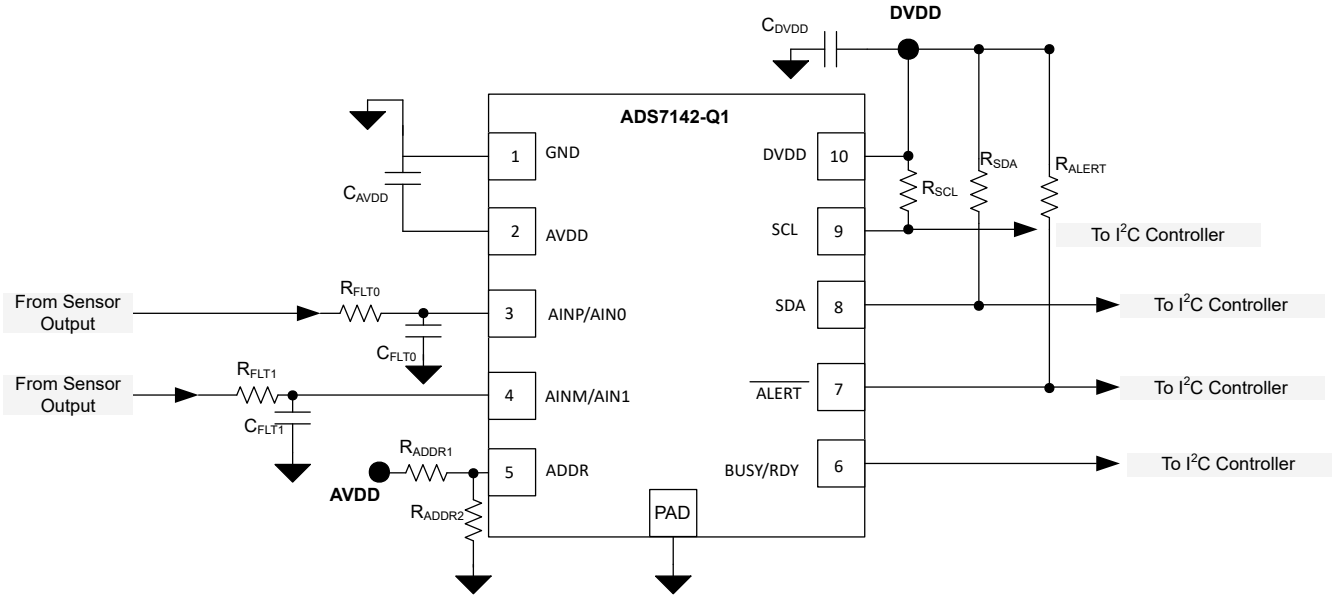


Figure 8-10. Example Schematic

8.4.2 Layout Example

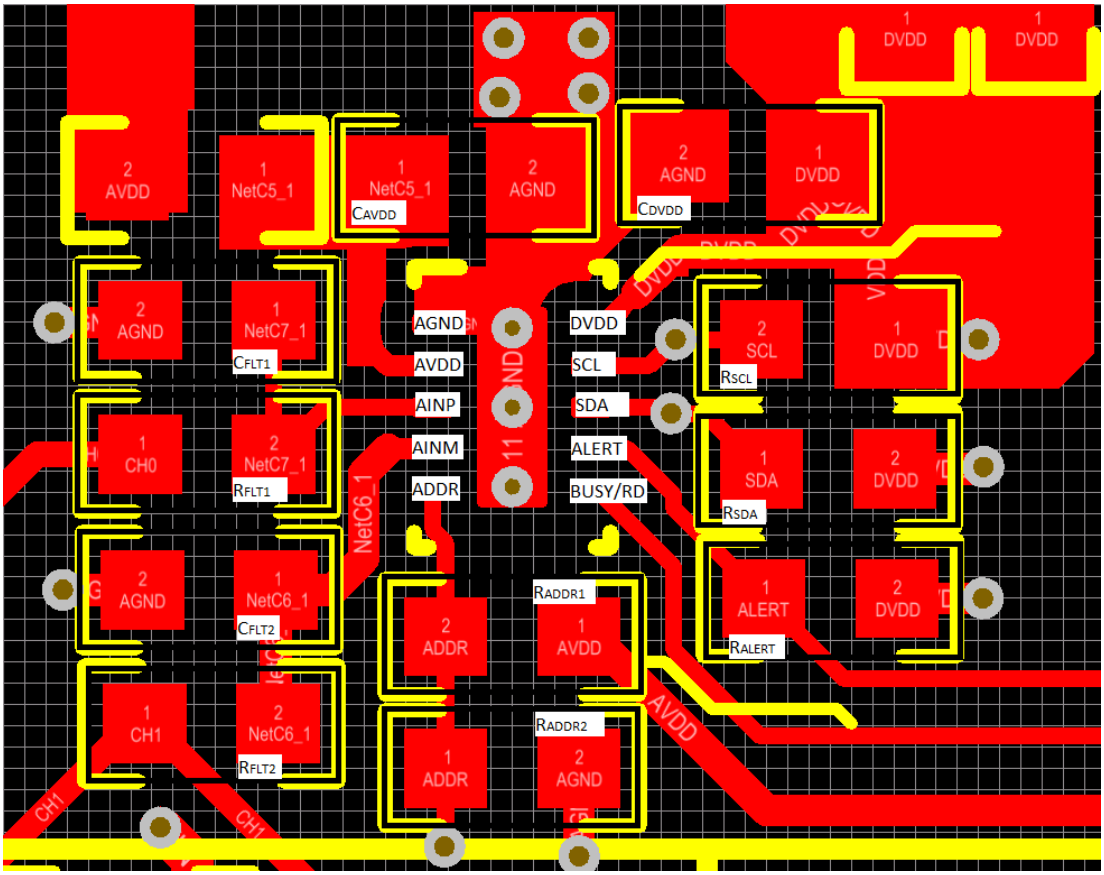


Figure 8-11. Example Layout

9 Device and Documentation Support

9.1 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.2 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.5 Support Resources

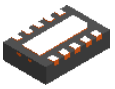
TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

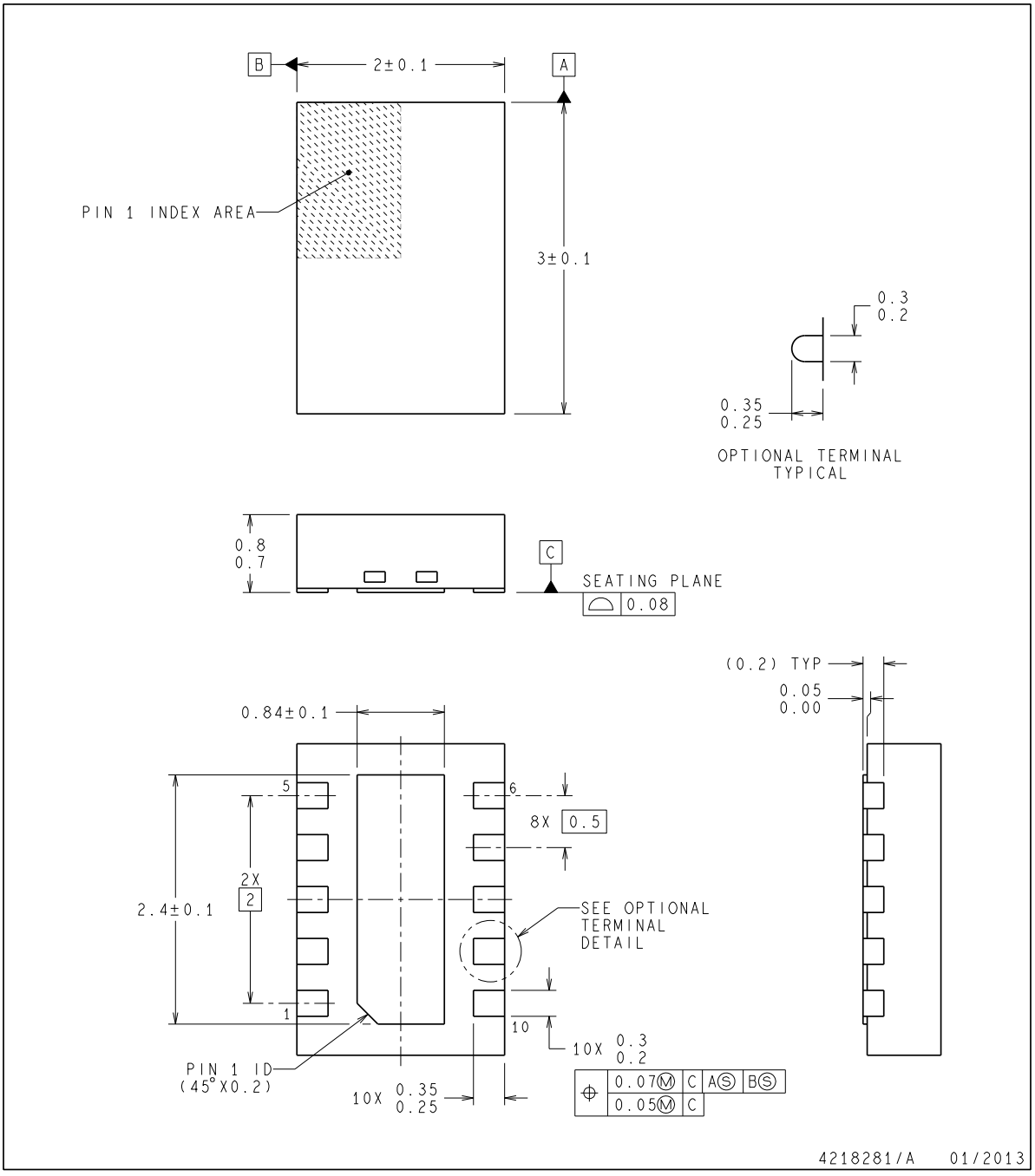
MECHANICAL DATA



DQC0010A

WSON - 0.8mm max height

QFN (PLASTIC QUAD FLATPACK-NO LEAD)



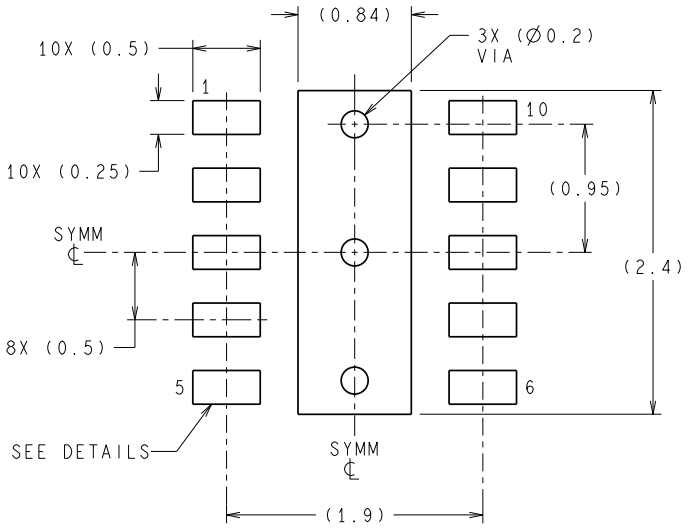
NOTES:
1. DIMENSIONS ARE IN MILLIMETERS. DIMENSIONS IN PARENTHESIS ARE FOR REFERENCE ONLY.
2. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
3. THE PACKAGE THERMAL PAD MUST BE SOLDERED TO THE PRINTED CIRCUIT BOARD FOR THERMAL AND MECHANICAL PERFORMANCE.
4. R-PWSON-N10.

MECHANICAL DATA

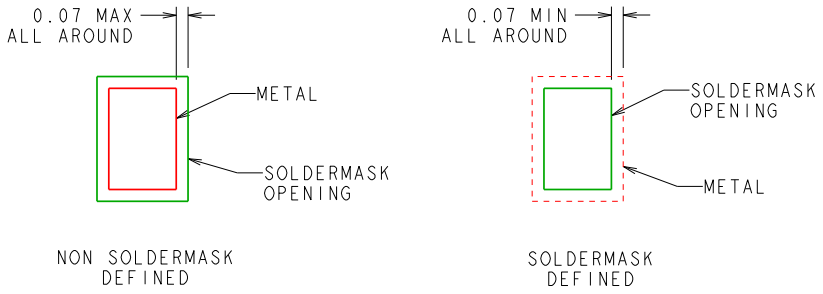
DQC0010A

WSON - 0.8mm max height

QFN (PLASTIC QUAD FLATPACK-NO LEAD)



RECOMMENDED LAND PATTERN



SOLDERMASK DETAILS

4218281/A 01/2013

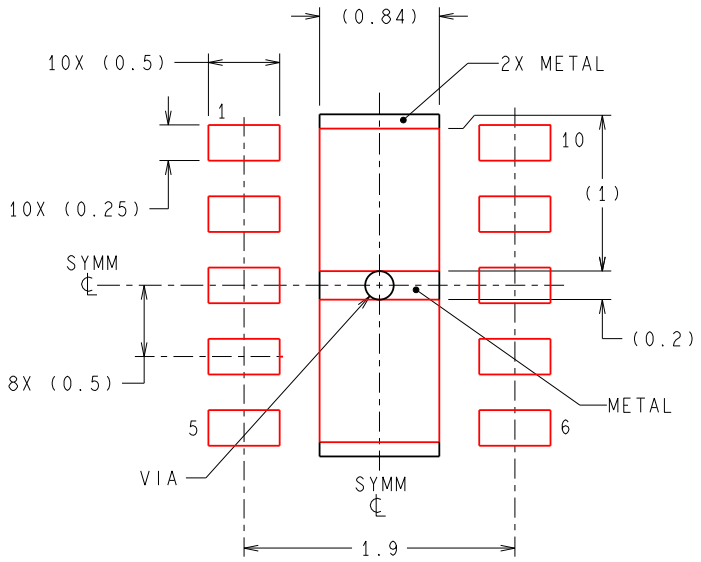
NOTES: 1. FOR PCB LAYOUT AND ASSEMBLY CONSIDERATIONS PLEASE REFER TO SLUA271 APPLICATION REPORT AVAILABLE AT www.ti.com.

MECHANICAL DATA

DQC0010A

WSON - 0.8mm max height

QFN (PLASTIC QUAD FLATPACK-NO LEAD)



RECOMMENDED SOLDERPASTE
EXPOSED PAD
83% PRINTED SOLDER COVERAGE BY AREA

4218281/A 01/2013

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS7142QDQCRQ1	ACTIVE	WSON	DQC	10	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	1AU	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

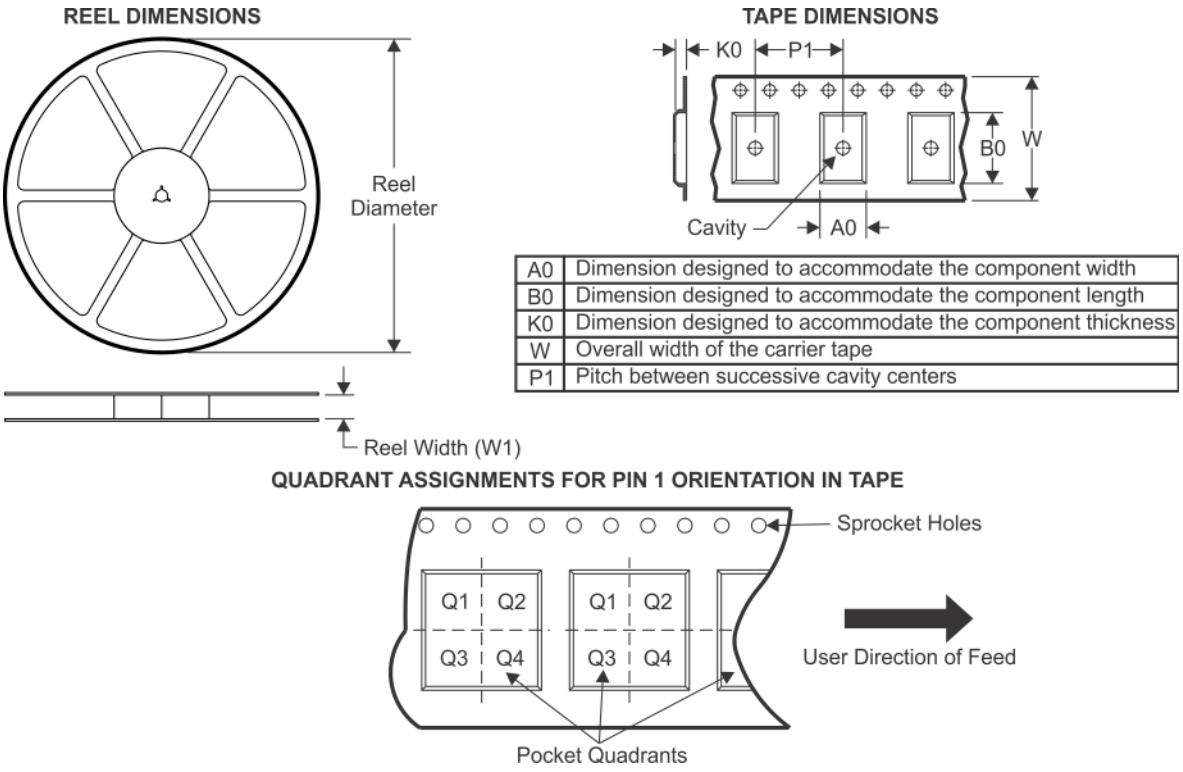
OTHER QUALIFIED VERSIONS OF ADS7142-Q1 :

- Catalog : ADS7142

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

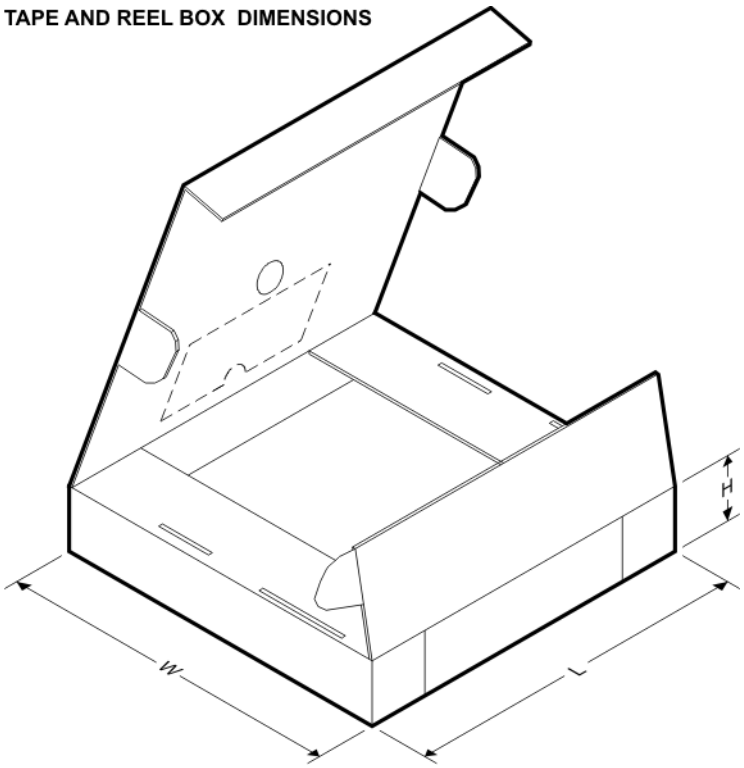


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS7142QDQCRQ1	WSON	DQC	10	3000	180.0	8.4	2.3	3.2	1.0	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



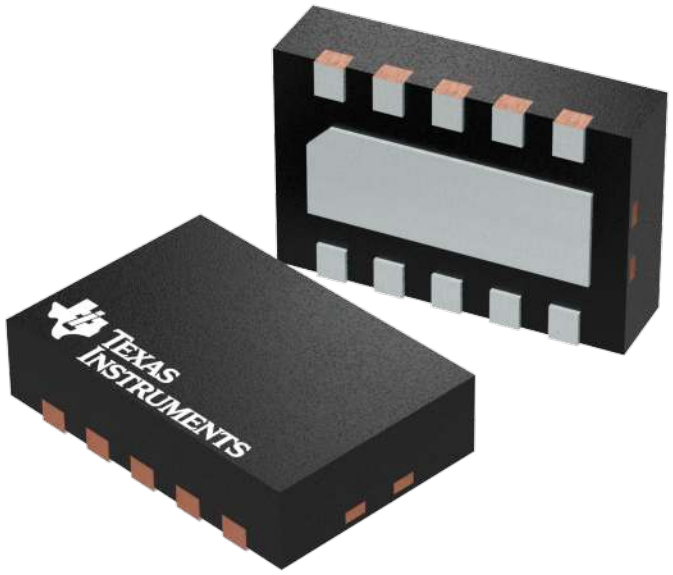
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS7142QDQCRQ1	WSON	DQC	10	3000	213.0	191.0	35.0

GENERIC PACKAGE VIEW

DQC 10 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

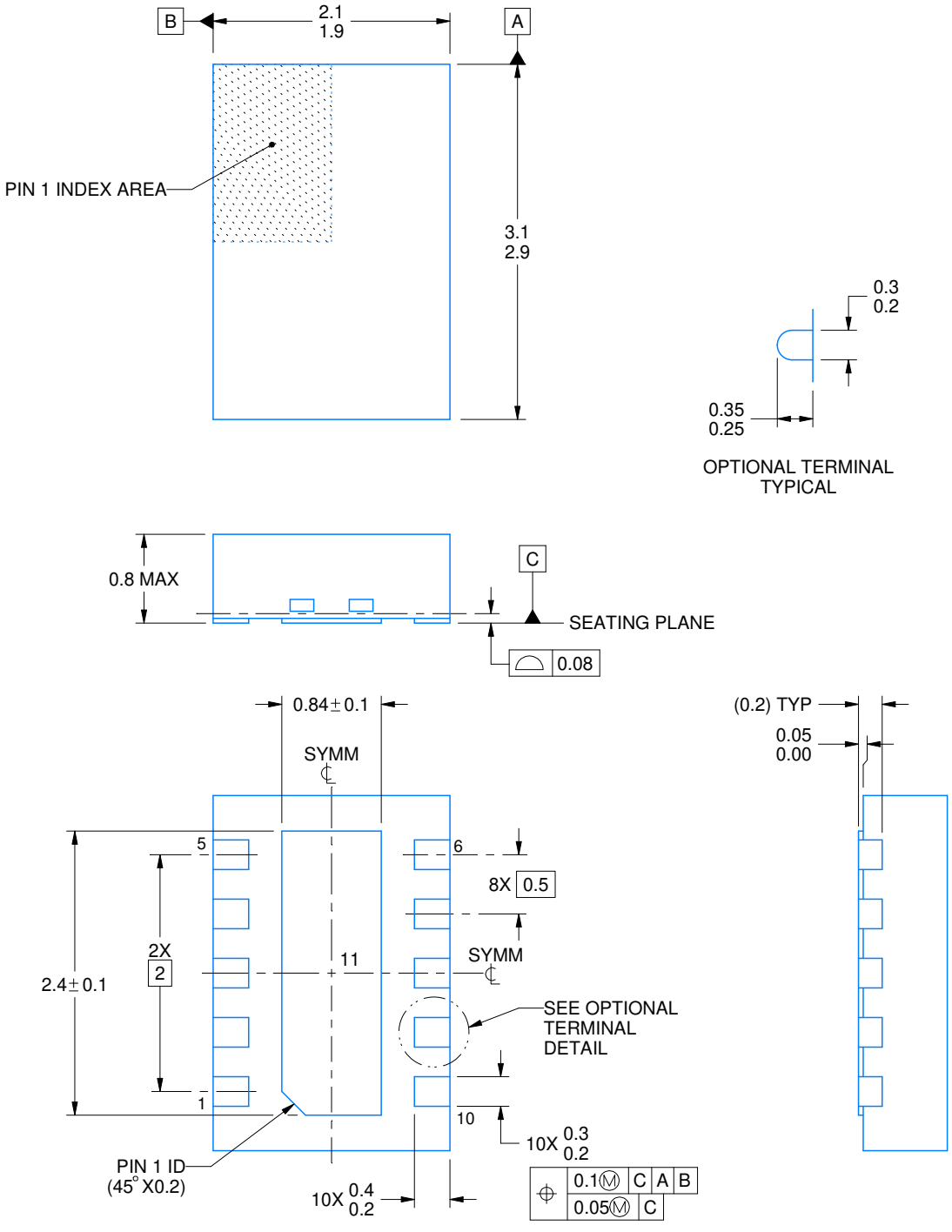
4209674/B

PACKAGE OUTLINE

DQC0010A

WSON - 0.8mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

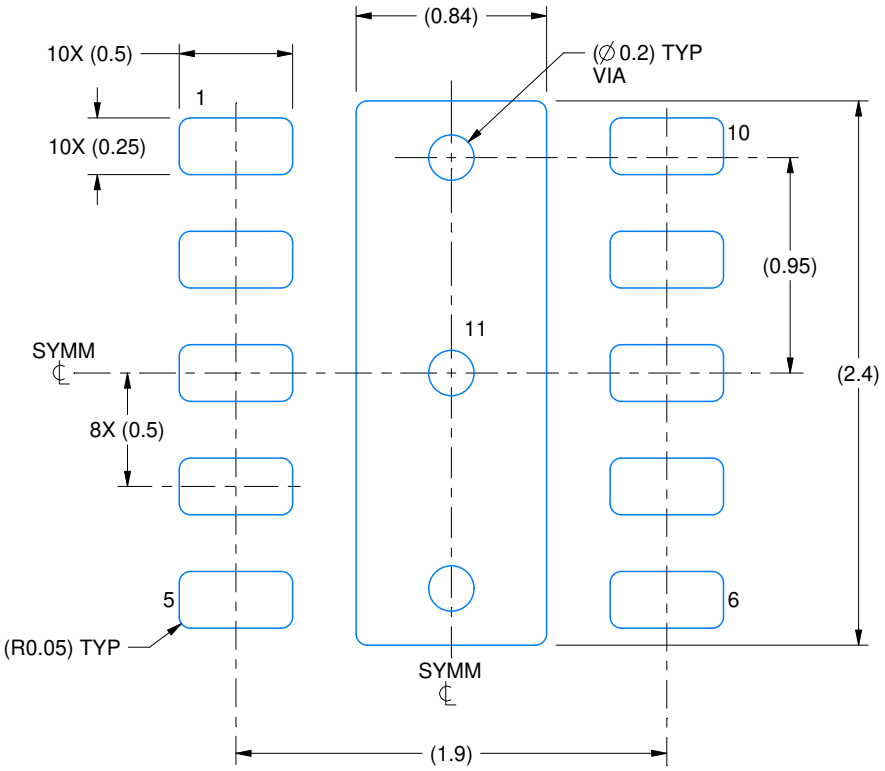
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

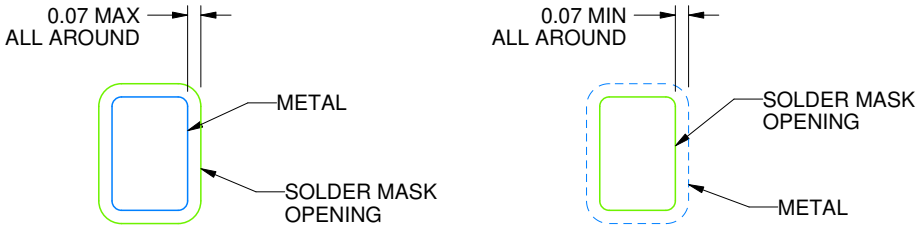
DQC0010A

WSON - 0.8mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SCALE: 30X



SOLDER MASK DETAILS

4218281/C 11/2022

NOTES: (continued)

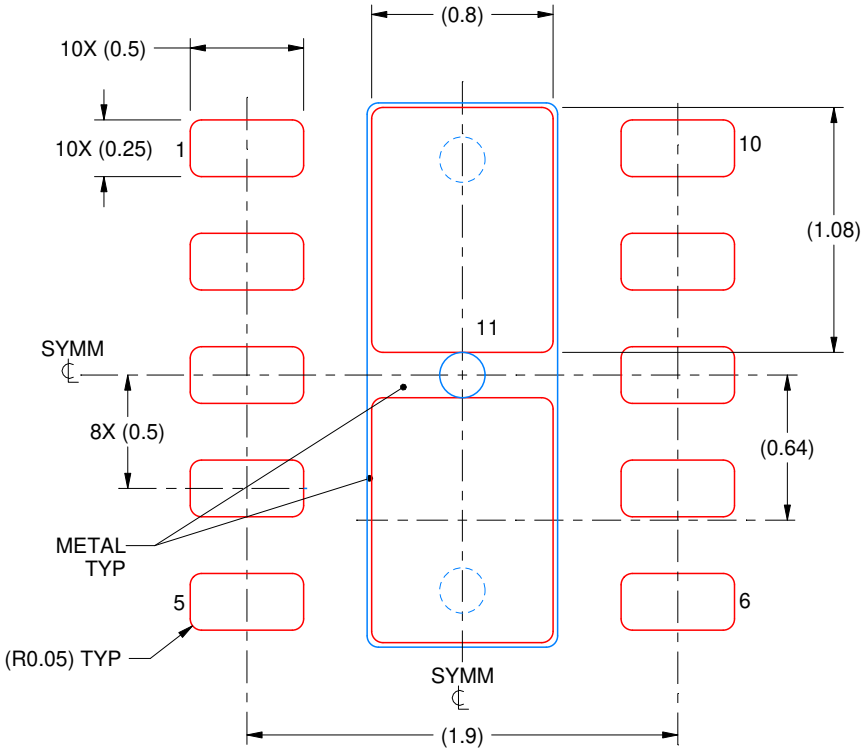
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DQC0010A

WSON - 0.8mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
86% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE: 30X

4218281/C 11/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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