CW25-GDO-DK Series GPS Receiver and Disciplined Oscillator Module

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DATA SHEET

RoHS COMPLIANT

Overview

The CW25-GDO-DK Series is a GPS receiver and GPS disciplined oscillator module combined. Designed specifically for time and frequency synchronization applications, this module incorporates a GPS receiver and a digital PLL circuit for disciplining the 1PPS signal derived from the receiver's GPS solution. Autonomous phase calibration capability offsets sawtooth error eliminating hanging bridge conditions.

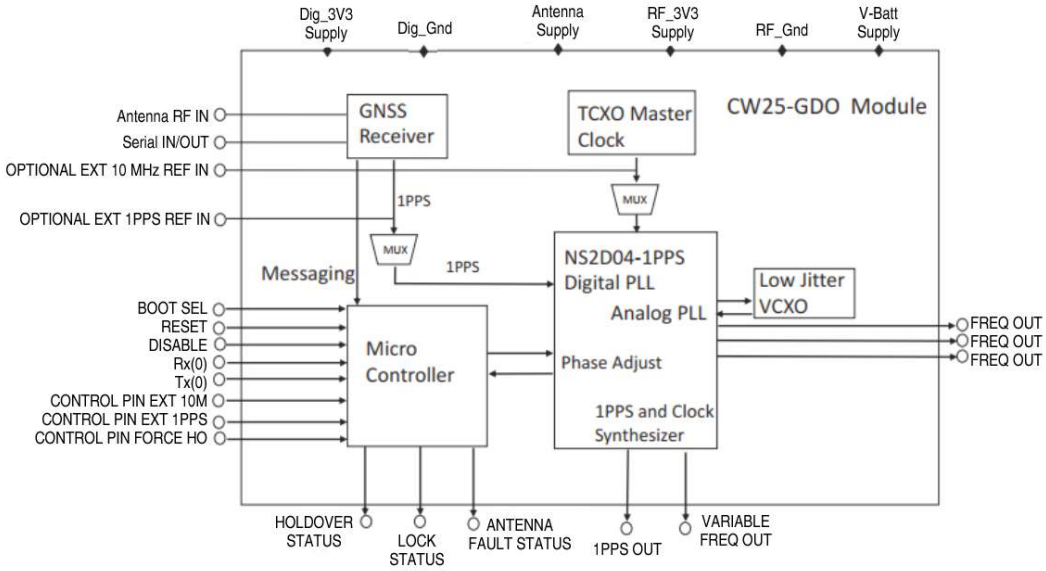
In addition to generating a phase aligned 1PPS output, the module generates three clock signals phase aligned to the 1PPS signal. Output clocks include one digitally synthesized clock output at frequencies from 150Hz to 80MHz and two low jitter 10MHz clock outputs generated from an integrated APLL block with options for 3.3V CMOS and/or differential LVPECL/LVDS signals at frequencies up to 700MHz

An on-board TCXO provides the system's master clock for holdover performance. The module supports an optional external 1PPS input as well as an optional external 10MHz clock input that can be used for improving holdover performance. This product can be used to generate a high-stability frequency reference for use in wireless systems, Software Defined Radio systems, time stamping, IEEE 1588v2, and applications employing a 1PPS frequency source for high precision, long term time and frequency generation.

Features

- On-board GPS receiver with optional 1 PPS Reference input
- 1PPS phase aligned output
- 2x 10MHz phase aligned clock output
- Programmable frequency output from 150Hz to 80MHz.
- Locked, Freq. aligned, Holdover indication.
- Automatic entry into holdover
- 3.3VDC Supply Voltage
- -20°C to +70°C operating temperature range
- Low G sensitivity option for <0.1ppb/G
- Optional external 10MHz input option, e.g. OCXO, Rb for improved holdover
- OEM SM footprint 25 x 27 mm
- RoHS Compliant ✓RoHS

Figure 1: CW25-GDO-DK Series Functional Block Diagram



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1 INTRODUCTION

The CW25-GDO-DK Series module is a specific configuration of the CW25-GDO series GNSS receiver and disciplined oscillator. This highly integrated, small surface mount time and frequency device specifically designed for use in synchronization and timing applications. This module incorporates Connor-Winfield's advanced NS2D04 synchronizing ASIC which integrates a digital phase lock loop (DPLL) system with an analog phase lock loop system and multiple clock output transmitters. The system's DPLL disciplines the 1PPS signal generated by the module's internal GPS receiver. A system master clock (MCLK) is used to support the internal DPLL and provides a basis for holdover operation when the 1PPS signal from the receiver is unavailable. A high precision 10 MHz TCXO is used internally to provide the MCLK function. Phase aligned clock signals are generated from a digital synthesizer, one of which is used to generate a 1PPS output, one is brought out directly and can be programmed to frequencies from 150Hz to 80MHz in 8kHz increments, and a third is sent to an internal analog PLL block/chain. The analog PLL circuit is supported by an internal, low jitter VCXO to provide a clean clock signal for the user. The CW25-GDO-DK Series generates two LVCMOS 10MHz clock outputs. However, the CW25-GDO series offers a variety of frequencies and output logic options which can be generated in the analog PLL chain based on the frequency of the VCXO specified. The two 10MHz output clocks are phase locked and phase aligned to the 1PPS reference, as is the variable output clock and the 3.3V LVCMOS 1PPS output.

In the CW25-GDO-DK Series, an on-board high precision TCXO provides the basis of the module's holdover capability when the GPS receiver loses satellite lock. When even higher holdover precision levels are required, an external 10MHz clock signal can be used as an input to the module. This external clock signal internally clocks both the DPLL system, allowing for higher performance filtering of the 1PPS solution derived from the internal receiver and a higher precision option for holdover performance. Because this 10MHz reference clocks the DPLL system, the 10MHz clock signal must be in place prior to powering up the module. Once the module is started with either the internal or external 10MHz reference, the control pin cannot be toggled to change reference sources in run time.

The module's DPLL system integrates an internal phase detector with calibration adjustment capability. This phase calibration capability allows the module to null the quantization error in the 1PPS signal, based on reacting to the internal receiver's quantization error messaging capability, thereby eliminating "hanging bridge" scenarios and allowing for smoother filtering of the 1PPS signal. The internal phase detector can be set to generate a "fixed" phase offset to adjust for phase delays caused by long antenna cable runs. This module has an optional ability to accept and discipline an external 1PPS signal input, if required.

The CW25-GDO-DK Series incorporates a micro controller that moderates the internal ASIC, setting the registers and monitoring run-time operations. The module is programmed at the factory but some system commands are available for enabling optional functionality and messaging.

The CW25-GDO-DK Series is RoHS and REACH compliant. It's highly integrated architecture is packaged in a small 22x25mm surface mount footprint allowing for easy integration into host systems.

For more detailed information on the operation of the internal system ASIC NS2D04-1PPS, see the following data sheet. http://www.conwin.com/datasheets/tm/tm138.pdf

2 BASIC OPERATION

The CW25-GDO-DK Series incorporates a high quality 72 channel GPS timing receiver chip with tracking sensitivity to -167 dBm. The receiver generates a UTC aligned 1PPS output signal that is disciplined by the modules DPLL block. The module generates clock outputs from the systems APLL block, in conjunction with the dividers at the programmable output transmitter circuits.

The digital PLL system design supports multiple bandwidth settings used for disciplining the receiver's 1PPS signal. The DPLL system is supported by a master clock (MCLK) which can be derived from either an on-board TCXO or an external 10 MHz 3.3V CMOS clock signal via the sync control pin configuration. The optional external clock reference allows the ability to use a high precision/low ADEV clock source, i.e. OCXO to take advantage of the DPLL's multiple bandwidth setting options. Bandwidth settings from 50mHz to as low as < 1mHz are available. The external 10MHz input is also used to clock the internal GPS receiver chip, thus improving the overall performance of the GPS receiver itself. Using a higher precision MCLK option at a lower DPLL bandwidth setting enhances the performance of the DPLL's filtering capability as well as improves the short term stability of the output clocks generated by the system. The frequency stability of the MCLK chosen is also the basis for the module's frequency stability in hold-over mode during times when the incoming 1PPS signal is lost or not available.

The CW25-GDO-DK Series module's system includes a phase calibration capability that is used to generate an offset to the sawtooth error commonly found in the 1PPS solution generated by the GPS receiver. Quantization error messages issued by the GPS receiver are used to predict the location next 1PPS pulse. A corresponding phase calibration adjustment is made to offset this "sawtooth" noise. This enhances the system's DPLL filtering capability to discipline the 1PPS signal for improved phase alignment with UTC as well as keeps the module from experiencing "hanging bridge" anomalies.

Once the receiver obtains satellite lock and a valid 1PPS signal is generated, multiple phases of locking begin, each at different bandwidth settings. These include a frequency locking, phase rebuild, fast phase locking, phase locking, phase locked, ending with frequency alignment. For phase alignment to take place, frequencies chosen must be divisible by 8kHz.

The DPLL system integrates a digital synthesizer that generates three independent, phase aligned clock signals. The first generates a 1PPS pulse signal. The second generates variable frequency synthesized clock capable of being programmed from 10MHz to 80MHz in 8kHz increments. This user programmable synthesized output (OUTPUT 1) also has a 16 bit divider circuit to generate 3.3V CMOS frequencies down to 152 Hz. The third synthesized clock is sent to an Analog PLL block/chain which supports up to three output transmitter ports. An on-board, low jitter VCXO is used to generate up to three clean output clocks. In the CW25-GDO series, integer related clock outputs can be derived directly from the VCXO frequency, either passed through to the output transmitter ports or integer divisible at the output transmitter ports. Conversely, a secondary high frequency VCO based APLL can take the VCXO frequency, multiply into the range of 1.2 to 1.5 GHZ which can be integer divided using a 20-bit divider at the output transmitter ports. Output 2 can be configured as either a differential LVPECL or LVDS signal, or as 2x CMOS clock signals. Output 3 generates a 3.3V CMOS only output. Zero phase alignment with the 1PPS signal requires frequencies to be integer divisible by 8kHz.

3 PHYSICAL CHARACTERISTICS

The CW25-GDO-DK Series is a multi-chip module (MCM) built on an FR4 fiberglass PCB. All digital and power connections to the CW25-GDO-DK Series are via castellations on the 25 x 27 mm PCB. The general arrangement of the CW25-GDO is shown in the diagram below.

Dimension units are inches (mm).

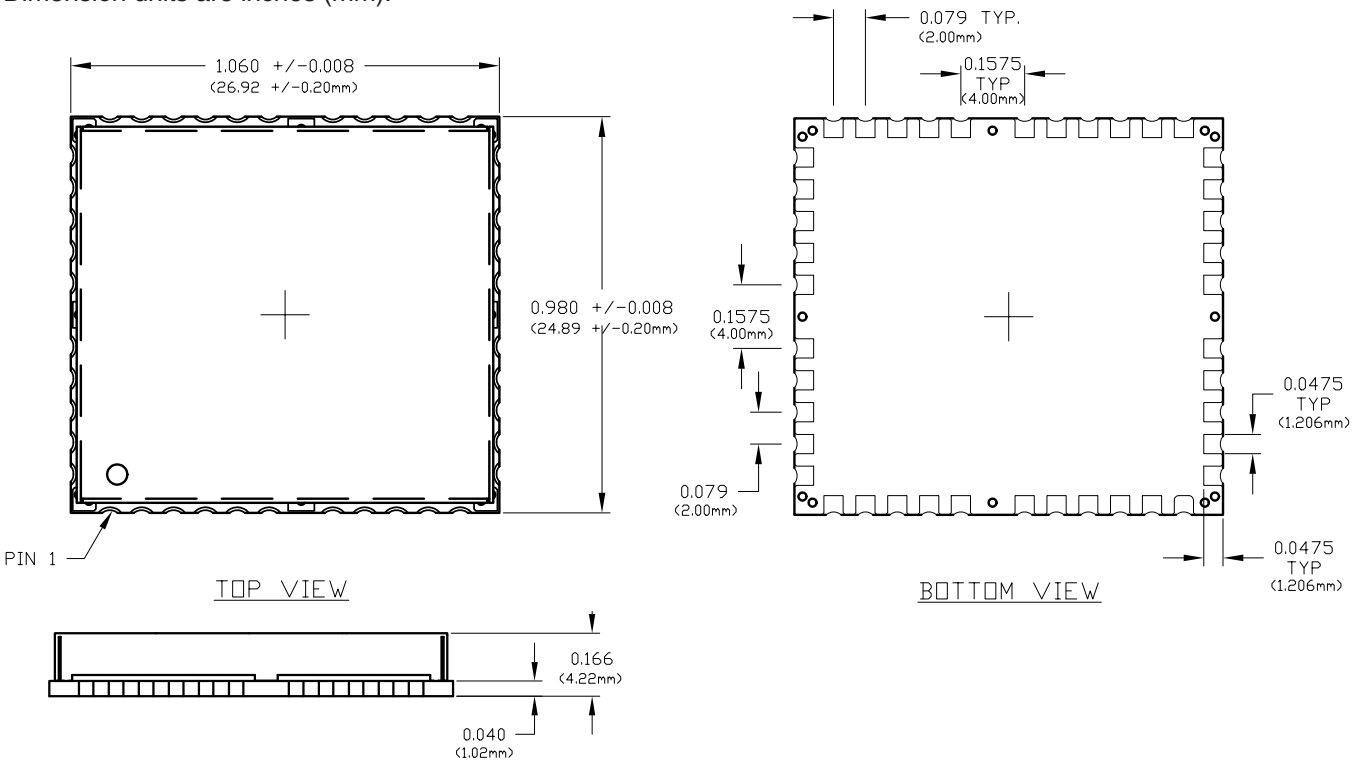


Figure 2 CW25-GDO-DK Series Form and Size

3.1 Physical Interface Details

The pin functions of the CW25-GDO-DK Series are defined below.

Pin	Function	Pin	Function	Pin	Function
1	TX[0]	15	N/C	29	DNC
2	RX[0]	16	RESET_N	30	DNC
3	3.3V 10MHz OUTPUT	17	N/C	31	DNC
4	3.3V 10MHz OUTPUT	18	RF_GND	32	EXT 1 PPS_IN
5	ANALOG_GND	19	RF_3V3	33	Control Pin Ext. 10MHz Ref Select
6	3.3V LVCMOS Output	20	DNC	34	N/C
7	EXT 10MHz CLK IN	21	N/C	35	DIGITAL GND
8	HOLDOVER	22	DNC	36	DIGITAL VCC_3V3
9	LOCKED	23	RF_GND	37	EVENT_IN
10	N/C	24	RF_IN	38	1PPS_OUT
11	BOOTSEL	25	RF_GND	39	FREQ_OUT (Variable)
12	DNC	26	ANT_SUPPLY	40	DNC
13	DNC	27	VBATT	41	CONTROL PIN 1PPS REF SELECT
14	DNC	28	DNC	42	CONTROL PIN FORCE HOLDOVER

3.2 CW25-GDO-DK Series Suggested Pad Layout

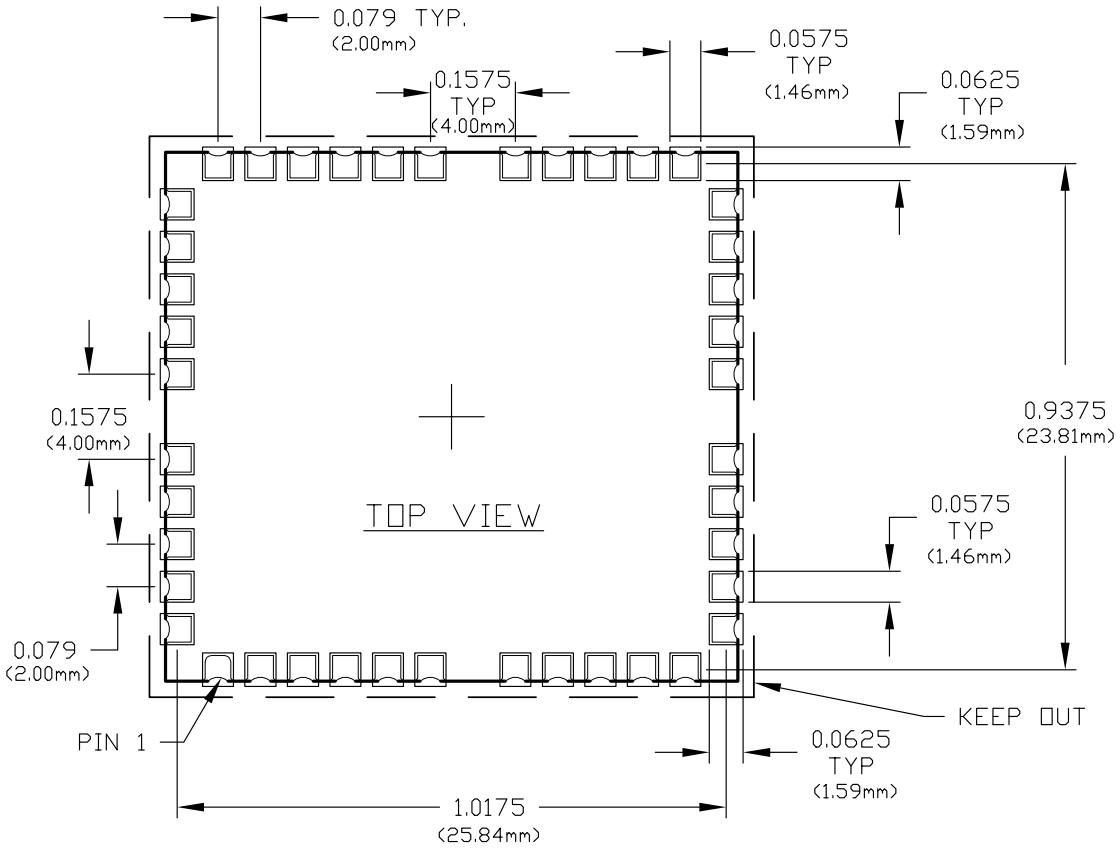


Figure 3 CW25-GDO-DK Series Suggested Pad Layout

4 SIGNAL DESCRIPTION

The signals on the CW25-GDO-DK Series are described in the table below.

4.1 I/O Signals

TX[0]	Type: I/O	Direction: Output	Pin: 1
	The Transmit Signal for UART 0. This is a standard UART output signal. The baud rate is 115200 N81.		
RX[0]	Type: I/O	Direction: Input	Pin: 2
	The Receive Signal for UART 0. This is a standard UART input signal. The baud rate is 115200 N81.		
10 MHz OUTPUT	Type: I/O	Direction: Output	Pin: 3
	3.3V LVCMOS Output signal.		
10 MHz OUTPUT	Type: I/O	Direction: Output	Pin: 4
	3.3V LVCMOS Output signal.		
10 MHz or 100MHz OUTPUT	Type: I/O	Direction: Output	Pin: 6
	3.3V LVCMOS Output 10MHz (-DK1 model) or 100MHz (-DK2 model)		
EXT CLOCK IN	Type: I/O	Direction: Input	Pin: 7
	Accepts a 10MHz 3.3V CMOS Signal input from an external source. The internal system uses this clock signal to support the receiver chip and the MCLK input to the DPLL system		
HOLDOVER	Type: I/O	Direction: Output	Pin: 8
	Standard software builds use this signal to indicate Holdover status. High indicates hold-over mode. This signal has a 3.3V CMOS drive.		
LOCKED	Type: I/O	Direction: Output	Pin: 9
	Standard software builds use this signal to indicate LOCK status. High indicates locked to 1pps. This signal has a 3.3V CMOS drive.		
EXT 1PPS IN	Type: I/O	Direction: Input	Pin: 32
	Accepts a 1 Pulse Per Second 3.3V Signal input from an external source. The internal system locks to the externally provided 1PPS signal.		
EVENT IN	Type:	Direction: Output	Pin: 37
	The Event Input Signal with internal connection to Pin 39 (GPIO[1] / Time Sync) allows phase measurement of the Frequency Output. The signal return path is DIG_GND.		
1PPS OUTPUT	Type: I/O	Direction: Output	Pin: 38
	1 Pulse Per Second 3.3V Signal. This is a 1PPS pulse aligned with 1PPS signal from the internal GPS receiver solution or the externally applied 1PPS signal when in “locked” mode. This 1PPS output signal is generated within the internal digital PLL and will continue to be present in initial free run and holdover modes, however it will be based on the internal TCXO or external MCLK and is not a “valid” 1PPS unless the module is in a “locked” state		

FREQ_OUT (VARIABLE) Type: I/O Direction: Output Pin: 39

Frequency Output that defaults to 10 MHz and is user configurable. The output is enabled on power-up and is steered by the incoming 1PPS signal. This clock output is a 3.3V LVCMOS single ended signal generated by the internal NCO with output frequency values achievable from 152Hz to 80MHz.
Internally, the frequency output is a value determined by two separate register settings. An initial value of M is used to multiply 8kHz to a frequency in the range between 10MHz and 80MHz. Once the M value is determined, a 16-bit post divider can be employed to generate a set of lower rate frequencies by choosing an N value which divides the base frequency by that number. Valid M values are integer numbers >= 1250 and <=10,000. Valid N values are integer numbers =>1 and <= 65536. A "0" value for M will disable the output while a "0" value for N will disable the post divider.

To simplify the process for the user to set the output frequency, a command system is in place to for changing the frequency of the output on the fly. The format of the command sentence that sets the frequency of the NCO and the output divider is: $PRTHS, FREQ, XXXXXXXX,YY

Form

$PRTHS,FREQ,<freq>,<divisor>

where

<freq >: In range of 10 MHz to 80 MHz, 8 kHz steps

<divisor> : In range of 0 to 65535, 0=Off

X is the frequency of the NCO and YY is the divide ratio of the output divider. For example if you sent $PRTHS, FREQ, 10000000, 10 The output frequency would be 1 MHz. The response from the module would be $PRTHR, FREQ, 10000000, 10*CS where "CS" is a checksum.

If the frequency or divider is out of range, the module responds with $POLYD,FREQ,BADPARAMS*15. In the case where an out of range parameter setting is used, the module will set the output to the nearest legal value.

Example: Set with incorrect or out-of-range parameters
Sent $PRTHS,FREQ,307200,1
Response $POLYD,FREQ,BADPARAMS*15

Set with acceptable parameters
Sent $PRTHS,FREQ,10000000,1
Response $PRTHR,FREQ,10000000,1*50

Startup
$POLYD,CW25-GDO-DK1,17:45:38,Aug-14-2019*5D
$PRTHR,FREQ,40000000,4*50

Query Current
Sent $PRTHQ,FREQ
Response $PRTHR,FREQ,40000000,4*50

NOTE: Phase alignment between the 1PPS incoming reference and the frequency output is possible only if the synthesized output frequency is integer related to 8kHz. All frequencies generated by values of only M will be phased aligned with the incoming 1PPS signal. However, using the 16 bit post divider, only N values chosen that result in an output frequency that has an integer relationship with 8kHz will be phase aligned to the incoming 1PPS signal.

The power signals on the CW25-GDO are described in the table below.

4.2 Power Signals

RF_3V3	Type: Power	Direction: Input	Pin: 19
	The RF Supply Input. This 3.3V ± 10% input supplies the 2.9V LDO regulator in the RF section of the module . It is important that this supply is well filtered with no more that 50mV peak to peak noise with respect to RF_GND.		
RF_GND	Type: Power	Direction: Input/Output	Pin: 18, 23, 25
	The RF Input Ground. This is the return path for the RF_3V3 supply and the ground for the antenna feed. The RF_GND must be tied to the DIG)GND esternally to the module.		
RFV_OUT	Type: Power	Direction: Output	Pin: 17
	The output from the LDO regulator that is powered by the RF_3V3 signal. This supplies the power to the RF subsystem of the module. This may also be used to power external RF components but care must be taken not to inject noise onto this signal. No more than an additional 30mA may be taken from this signal by external circuitry.		
ANT_SUPPLY	Type: Power	Direction: Input	Pin: 26
	The Antenna Supply Voltage. This may be used to supply power to the RF_IN signal, for use by an active antenna. The maximum voltage should not exceed ±15V and the current should be limited to 50mA.		
DIG_3V3	Type: Power	Direction: Input	Pin: 36
	The Digital Supply Input. This 3.3V ± 10% input supplies the LDO regulator in the digital section of the module . It is important that this supply is well filtered with no more that 50mV peak to peak noise with respect to DIG_GND.		
DIG_GND	Type: Power	Direction: Input/Output	Pin: 35
	The Digital Ground. This is the return path for the DIG_3V3 supply and the ground reference for all the digital I/O. The DIG_GND must be tied to the RF_GND externally to the module.		
ANALOG_GND	Type: Power	Direction: Input/Output	Pin: 5
	The Analog Ground. This is the return path for the analog PLL section and the ground reference for outputs 2P, 2N and 3. ANALOG_GND must be tied to the DIG_GND externally to the module.		
VBATT	Type: Power	Direction: Input/Output	Pin: 27
	The Battery Backup Supply. The CW25-GDO has an on board Real Time Clock (RTC). This is powered from the VBATT signal. A supply of typically 3v (greater than 2.5V and less than DIG_3V3) should be applied to this signal. This signal can be left floating if not required. The input has a blocking diode and so rechargeable batteries will need an external charging circuit. Typically, a 1K resister in series with this signal and the external battery will provide an easy method of measuring the current consumption from VBATT during test.		

4.3 RF Signals

RF_IN	Type: Signals	Direction: Input	Pin: 24
	The RF Input Signal. This attaches to the GPS antenna. Standard RF design rules must be used when tracking to this signal. This signal has an RF blocked connection to the ANT_SUPPLY signal. This is the same signal presented on the RF connector on the Wi125 . Only one antenna connection should be made. If the RF connector is to be used, then there should be no connection, even an unconnected pad, to this castellation.		

4.4 Controls

BOOTSEL	Type: Control	Direction: Input	Pin: 11
	The Boot Select Signal is not used in regular operation. This pin is connected to the on board micro controller to be used for potential updates to the firmware. If the BOOTSEL signal is high or left floating, then the module boots from its on-chip FLASH memory. If the BOOTSEL signal is pulled low, the module boots from its on-chip ROM.		
RESET_N	Type: Control	Direction: Input	Pin: 16
	Pin RESET_N is an I/O input pin used to initiate a “hard” reset to the IC. The RESET_N pin is internally “pulled-high”. Driving this pin “Low” for at least 1uS and releasing it, or driving it “High” again will reset the device. The IC will be ready to access through the control bus interface in 10 mS after the reset operation.		
EXT REF SELECT	Type: Control	Direction: Input	Pin: 33
	Hardware Control Signal. Setting this pin High or Low configures external 10MHz Reference input select. Internally pulled HIGH for internal TCXO Reference. Pull pin LOW to enable External 10MHz 3.3V LVCMOS clock signal input on pin 7. *PLEASE NOTE: When using an external 10MHz reference, this pin must be set low prior to power up of the module and the external 10MHz clock signal must be available upon power-up in order for the internal DPLL system to start properly. Once the module is in operation, the reference source cannot be changed without a full reset of the module.*		
SYNC1	Type: Control	Direction: Input/Output	Pin: 41
	Hardware Control Signal. Setting this pin High or Low configures external 1PPS Input Reference select. Internally pulled HIGH for internal 1PPS Reference. Pull pin LOW to accept External 1PPS, 3.3V LVCMOS clock signal input on pin 32. **NOTE If External 1PPS is used, quantization error smoothing is disabled.*		
SYNC2	Type: Control	Direction: Input/Output	Pin: 42
	Hardware Control Signal. Setting this pin High or Low forces the module into HOLDOVER mode. Internally pulled HIGH. Pull pin LOW to put the module into FORCED HOLDOVER mode.		

4.5 Emulation/Test Signals

TDO	Type: Test	Direction: Output	Pin: 13
	The Test Data Out Signal. This is the standard JTAG test data output. The signal return path is DIG_GND.		
TDK	Type: Test	Direction: Input	Pin: 20
	The Test Mode Select Signal. This is the standard JTAG test clock input. The signal return path is DIG_GND.		
TMS	Type: Test	Direction: Om[it	Pin: 22
	The Test Mode Select Signal. This is the standard JTAG mode input. The signal return path is DIG_GND.		

5 SPECIAL FEATURES

While most of the features on the CW25-GDO are just a subset of the capabilities of the internal NS2D04-1PPS IC and so are described in the NS2D04-1PPS Data Sheet, there are some additional features specific to the CW25-GDO that require explanation.

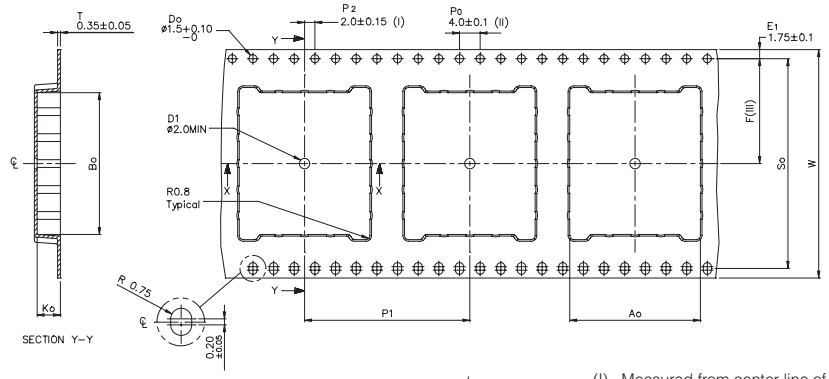
5.1 User Commands

The CW25-GDO can accept a number of specific user commands for setting parameters such as UART baud rate and NMEA message subset, output frequency, etc. Many of these parameters are stored in Non- Volatile Memory (NVM) so that the settings are retained when the receiver loses power. The available commands are defined in detail in the Appendix below.

5.2 CW25-GDO Embedded Identification

The hardware version number is hard coded onto the CW25-GDO; firmware also contains a version number allowing for easy identification of the hardware and software version in embedded applications.

6 TAPE AND REEL SPECIFICATIONS



Ao	25.30	+/−	0.1
Bo	27.30	+/−	0.1
Ko	4.50	+/−	0.1
F	20.20	+/−	0.15
P1	32.00	+/−	0.1
So	40.40	+/−	0.1
W	44.00	+/−	0.3

General Tolerance ±0.2
Drawing not to Scale

(I) Measured from center line of sprocket hole to center line of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20.
(III) Measured from center line of sprocket hole to center line of pocket.
(IV) Other material available.

ALL DIMENSIONS IN MILLIMETERS UNLESS OTHERWISE STATED

Figure 4 Tape and Reel

7 SOLDER PROFILE

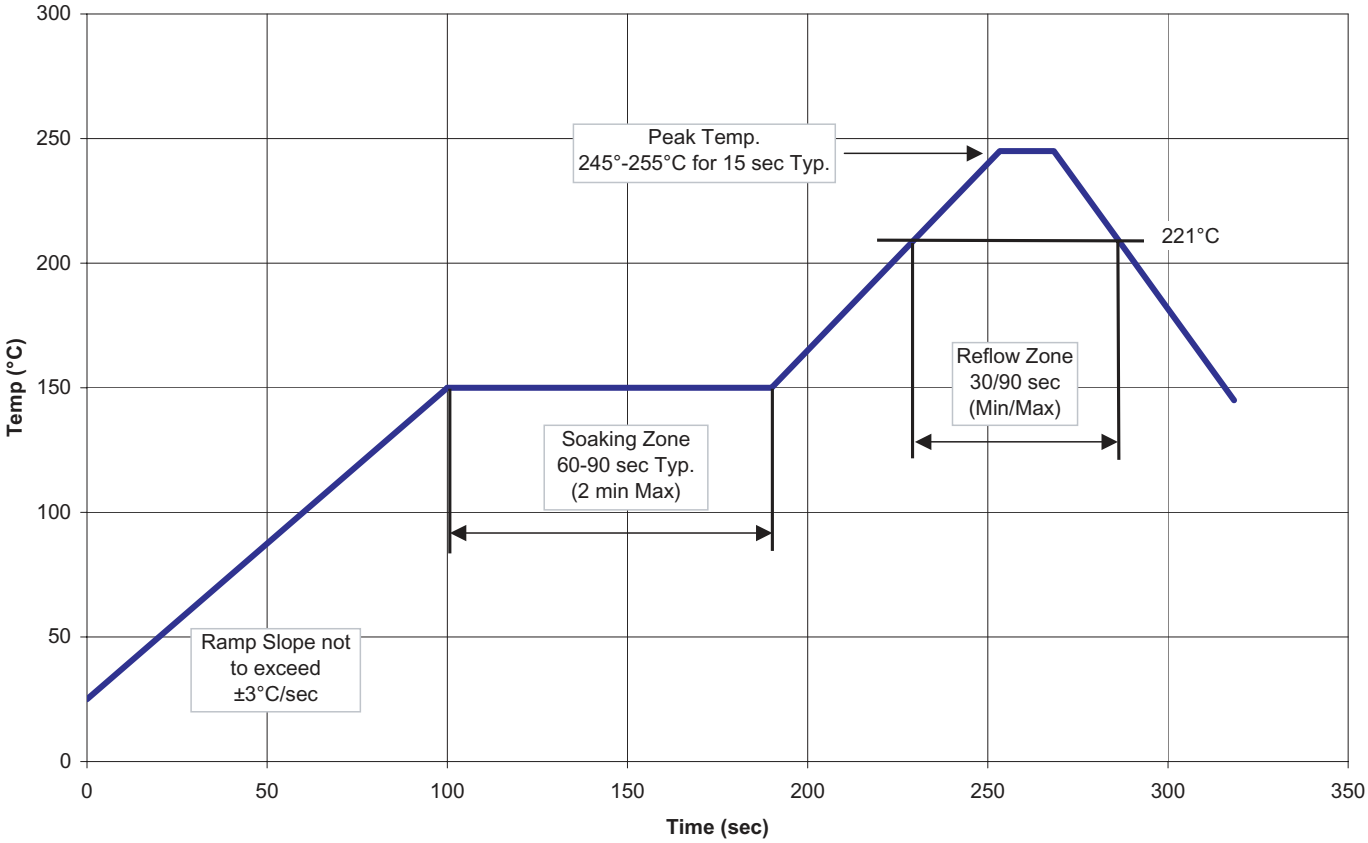


Figure 5 Solder Profile

8 COMMUNICATIONS PROTOCOLS

8.1 Port Configuration

There is one serial port available on the CW25, RX[0]/TX[0] configured as follows:

Port	Baud Rate	Function
serial port RX[0]/TX[0]	38400	NMEA

This port is configured as 8, bits no Parity, with no handshaking.

8.2 Output Format

Messages that can be output from the CW25 receiver are NMEA sentences .

8.2.1 NMEA Messages

There are two main types of sentence, 'Approved' and 'Proprietary'. All sentences start with $ delimited with commas and ending with <CR><LF>. Approved sentences are recognized by the first 5 characters after the $, which define both the kind of talker providing the information (2 characters, GP in the case of a GPS), and the type of information (3 characters).

Proprietary sentences are indicated by a P following the $, as the first of the 5 characters, the next 3 indicating the manufacturer (from a listing of mnemonic codes), and the 5th character being selected by that manufacturer for the particular sentence structure. Proprietary sentences must conform to the general NMEA structures, but are otherwise undefined out-side of the Manufacturers own documentation.

The following Approved messages are available from the CW25 receiver:

GPGLL - Geographic Position - Latitude longitude

GPGGA - Global Positioning System Fix Data

GPGSA - GNSS DOP and Active Satellites

GPGSV - GNSS Satellites in View

GPRMC - Minimum required sentence

POLYT - Proprietary status message

POLYS - Proprietary satellite status message (GPGGA + GPGSV)

POLYZ - Proprietary DPLL Status information message

Approved NMEA messages

8.2.1.1 GPGLL - Geographic position, Lat/Lon

Latitude and longitude, with time of position fix and status.

*$GPGLL, Latitude, N, Longitude,E, hhmmss.sss, Status, Mode*cs*

Name	Description
$GPGLL	NMEA sentence header (Position Data)
Latitude	User datum latitudedegrees, minutes, decimal minutes format (ddmm.mmmmmm)
N	Hemisphere 'N'= North, or 'S' = South
Longitude	User datum longitudedegrees, minutes, decimal minutes format (dddmm.mmmmmm)
E	Longitude Direction 'E'= East, or 'W' = West
hhmmss.sss	UTC Time in hours, minutes, seconds and decimal seconds format.
Status	StatusV=navigation receiver warning, A=data valid
Mode	Mode indicator:A=Valid, Autonomous, D=Valid, Differential, E=Invalid, Estimated, N=Invalid, Not valid
Cs	Message checksum in hexadecimal

8.2.1.2 GPGGA - GPS fix data

Time and position, together with GPS fixing related data.

*$GPGGA, hhmmss.sss, Latitude, N, Longitude , E, FS, NoSV, HDOP , Altref , M, msl , M, DiffAge , DiffStation*cs*

Name	Description
$GPGGA	NMEA sentence header (Position Data)
hhmmss.sss	UTC Time in hours, minutes, seconds and decimal seconds format.
Latitude	User datum latitude degrees, minutes, decimal minutes format (ddmm.mmmmmm)
N	Hemisphere 'N'= North, or 'S' = South
Longitude	User datum longitudedegrees, minutes, decimal minutes format (dddmm.mmmmmm)
E	Longitude Direction: 'E'= East, 'W' = West
FS	Fix Status: 0 No fix 1 Standard GPS 2 Differential GPS
NoSv	Number of satellites used in the position solution
HDOP	2-D Horizontal Dilution of Precision (0.00 to 99.99)
AltRef	Altitude (metres) above user datum ellipsoid
M	Units of height (metres)
msl	Mean Sea Level
M	Units of Mean Sea Level (meters)
DiffAge	Age of differential correction
DiffStation	Differential base station ID
cs	Message checksum in hexadecimal

8.2.1.3 GPGSA - GPS DOP and Active satellites

GPS receiver operating mode, satellites used for navigation, and DOP values.

*$GPGSA,Smode,FS,sv,sv,sv,sv,,,,,,,,PDOP,HDOP,VDOP*cs*

Name	Description
$GPGSA	NMEA sentence header (Satellite Data)
Smode	A= Automatic switching 2D/3D M=Manually fixed 2D/3D
FS	Fix Status: 1 No fix 2 2D GPS Fix 3 3D GPS Fix
sv	Satellites in use, null for unused fields (12 available fields)
PDOP	3-D Position Dilution of Precision (0.00 to 99.99)
HDOP	2-D Horizontal Dilution of Precision (0.00 to 99.99)
VDOP	Vertical Dilution of Precision (0.00 to 99.99)
cs	Message checksum in hexadecimal

8.2.1.4 GPGSV - GPS Satellites in View

The number of satellites in view, together with each PRN, elevation and azimuth, and C/No value. Up to four satellite details are transmitted in one message, with up to three messages used as indicated in the first field.

*$GPGSV, NoMsg, MsgNo, NoSv{,sv,elv,az,cno}{,sv,elv,az,cno….}*cs*

Note: {} designate optional sections that appear only if there is satellite data.

Name	Description
$GPGSV	NMEA sentence header (Satellite Data)
NoMsg	Total number of GPGSV messages being output
MsgNo	Number of this messages
NoSv	Number of satellites in view
sv	Satellites ID
elv	Satellite elevation angle (degrees)
az	Satellite azimuth angle (degrees)
cno	Satellite signal/Noise ration (dB/Hz)
cs	Message checksum in hexadecimal

8.2.1.5 GPRMC - Recommended Minimum data

The 'Recommended Minimum' sentence is defined by NMEA for GPS/Transit system data.

*$GPRMC,hhmmss.sss,status,latitude,N,Hemisphere,longitude,E,spd,cmg,ddmmyy,mv,mvd,Mode*cs*

Name	Description
$GPRMC	NMEA sentence header (Recommended Minimum Sentence)
hhmmss.sss	UTC Time in hours, minutes, seconds.
status	Status:V=navigation receiver warning, A=data valid
Latitude	User datum latitudedegrees, minutes, decimal minutes format (ddmm.mmmmmm)
N	Hemisphere: 'N'= North, or 'S' = South
Longitude	User datum longitude degrees, minutes, decimal minutes format (dddmm.mmmmmm)
E	Longitude Direction: 'E'= East, 'W' = West
spd	Speed over ground (knots).
cmg	Course made good
ddmmyy	Date in Day, Month Year format
mv	Magnetic variation
mvd	Magnetic variation direction
Mode	Mode Indicator: D = Valid, Differential, A = Valid, Autonomous, E = Invalid, Estimated, N = Invalid, Not Valid
cs	Message checksum in hexadecimal

8.2.1.6 GPVTG - Course over ground and Ground speed.

Velocity is given as Course over Ground (COG) and Ground Speed

*$GPVTG,cogt,T,cogm ,M ,knots,N,kph,K,Mode*cs*

Name	Description
$GPVTG	NMEA sentence header (Speed and heading)
cogt	Course over ground (true)
T	True - fixed field
cogm	Course over ground (magnetic)
M	Magnetic - fixed field
knots	Speed over ground (knots)
N	Knots - fixed field
kph	Speed over ground (kph)
K	Kilometers per hour – fixed field
Mode	Mode Indicator:D = Valid, Differential, A = Valid, Autonomous, E = Invalid, Estimated, N = Invalid, Not Valid
cs	Message checksum in hexadecimal

8.2.1.7 GPZDA - UTC Time and Date

This message transfers UTC Time and Date. Since the latency of preparing and transferring the message is variable, and the time does not refer to a particular position fix, the seconds' precision is reduced to 2 decimal places.

*$GPZDA,hhmmss.sss,dd,mm,yyyy,Int,Unsigned*cs*

Name	Description
$GPZDA	NMEA sentence header (Time and Date)
hhmmss.sss	UTC Time in hours, minutes, seconds.
dd	UTC day
mm	UTC month
yyyy	UTC year
Int Unsigned	Local zone hours
Int Unsigned	Local zone minutes
kph	Speed over ground (kph)
K	Kilometers per hour – fixed field
cs	Message checksum in hexadecimal

8.2.1.8 POLYT - Time of Day – **Proprietary NMEA Messages**

*$POLYT,hhmmss.sss,ddmmyy, UTC_TOW ,week, GPS_TOW ,Clk_B , Clk_D ,PG,LocalTTag,BAcc,TAcc,BLANK*cs*

Name	Description
$POLYT	Connor-Winfield Proprietary NMEA sentence header (Position Data)
hhmmss.sss	UTC Time in hours, minutes, seconds and decimal seconds format.
ddmmyy	Date in day, month, year format.
UTC_TOW	UTC Time of Week (seconds with microseconds resolution)
week	GPS week number (continues beyond 1023)
GPS_TOW	GPS Time of Week (seconds with microseconds resolution)
Clk_B	Receiver clock Bias (nanoseconds)
Clk_D	Receiver clock Drift (nanoseconds/second)
PG	1PPS Granularity (nanoseconds)
LocalTTag	Local receiver time-tag since start-up [msec]
BAcc	Bias Accuracy
TAcc	Time Accuracy
cs	Message checksum in hexadecimal

8.2 Output Format continued

8.2.1.9 POLYS - Satellite Status

*$POLYS,GT{,ID,s,AZM,EL,SN,LK}{,ID,s,AZM,EL,SN,LK}{,ID,s,AZM,EL,SN,LK}{,ID,s,AZM,EL,SN,LK}{,ID,s,AZM,EL,SN,LK}{,ID,s,AZM,EL,SN,LK}{,ID,s,AZM,EL,SN,LK}{,ID,s,AZM,EL,SN,LK}{,ID,s,AZM,EL,SN,LK}{,ID,s,AZM,EL,SN,LK}{,ID,s,AZM,EL,SN,LK}{,ID,s,AZM,EL,SN,LK}*cs*

Note: {} designate optional sections that appear only if there is satellite data

Name	Description
$POLYS	Connor-Winfield Proprietary NMEA sentence header (Satellite Data)
GT	Number of GPS satellites tracked
ID	Satellite PRN number (1-32)
s	Satellite status - = not used U = used in solution e = available for use, but no ephemeris
AZM	Satellite azimuth angle (range 000 - 359 degrees)
EL	Satellite elevation angle (range 00 - 90 degrees)
SN	Signal to noise ratio in (range 0 - 55 dB/Hz)
LK	Satellite carrier lock count (range 0 - 255 seconds) 0 = code lock only 255 = lock for 255 or more seconds
cs	Message checksum in hexadecima

8.3 Command Format*

The CW25 receiver has a unique set of proprietary commands.

The commands to and from the unit have the following general formats:

$PRTH<Q|S|R>,<id>,<msg fields>[<checksum>]<cr><lf>*

Where:

< |Q|S|R> is the single ASCII character as follows:

Q: Command, a query command to the CW25 receiver.

S: Command, requires the CW25 receiver to set system settings.

R: Response to a CW25 receiver, response to a $PRTH Query or an acknowledgement of a $PRTH Set.

< id> is a 4 character command identifier.

<msg fields> are the message fields for the message and are all positional. Optional or unknown fields are shown as nulls (ie adjacent commas). Trailing commas to the end of a message (ie nothing but null message fields) are not required.

*<checksum> An optional checksum byte for checking accuracy defined as follows:

The checksum is displayed as a pair of ASCII characters, (0-9 and A-F inclusive) whose value represents the “HEX” value of the checksum byte. When used, it always appears as the last field of the sentence and is prefixed by field delimiter “*” (HEX 2A) instead of “,” and followed by <CR><LF> (HEX 0D 0A). The checksum value is calculated by XOR’ing (exclusive OR’ing also known as Modulo 2 Sum) the 8 binary data bits of each valid data character in the sentence between the “$” (HEX 24) and “*” (HEX 2A) characters.

The “$” (HEX 24) and the “*” (HEX 2A) characters are not included in the checksum.
<cr><lf> are the ASCII codes 0Dh and 0Ah (carriage return and line feed) respectively.

Some commands use multiple sentences to transfer data: multiple sentence transfer shall be accomplished by means of 2 fields within the sentence for which this format is used:

t: Total number of sentences forming the data transfer (minimum value 1)

x: ID number of the current sentence ranging from 1 to t inclusive

Null fields within a command shall be interpreted as “use current value” where appropriate. Null fields must be delimited by adjacent commas when they exist between two non-null fields. If all trailing fields after a given field are null, further commas are not required.

8.3.1 PRTH<Q|R>, VERS: Software Version

Purpose

This message Queries and Responds with the current software version information.

Query Format

$PRTHQ,VERS[*checksum]<cr><lf>

Response /Acknowledge Format

$PRTHR,VERS,Build_Name,Version_Number,Version_Date,Version_Time, Serial_Num, BB_Releaset*<checksum><cr><lf>

Explanation of Parameters

Build_Name Product name (i.e. CW25-TIM or CW25-NAV)

Version_Number Software version number

Version_Date Software build date in Mmm_dd_yyyy format where Mmm is the Three character abbreviation of the month name\

Version_Time Software build time in hh:mm:ss format

Serial_Num Product serial number is current not implemented and always outputs “Serial_Num”

BB_Release Baseband version number

8.3.2 PRTH<Q|S|R>, DYNA: RECEIVER DYNAMICS **Purpose**

This message Sets, Queries and Responds to the receiver host dynamics and hence the maximum receiver tracking dynamics expected.

The degree of filtering performed by the navigation and timing Kalman filter is dependant on the selected receiver platform.

Query Format

$PRTHQ,DYNA[*checksum]<cr><lf>

Set Format

$PRTHS,DYNA,platform[*checksum]<cr><lf>

Response / Acknowledge Format

$PRTHR,DYNA,platform*<checksum><cr><lf>

Explanation of Parameters

Platform	Receiver platform (integer, range 0 – 7)
0	Fixed base station, the default setting for CW25-GDO is Fixed base station mode.
1	Stationary, but unknown position
2	Pedestrian: Man pack / walking
3	Automotive / Land Vehicle
4	Marine
5	Airborne 1G
6	Airborne 2G
7	Airborne 4G

CW25-GDO-DK Series
Multi-Frequency GPS Receiver Module

2111 Comprehensive Drive
Aurora, Illinois 60505
Phone: 630-851-4722
Fax: 630-851-5040
www.conwin.com

List of Figures

Ordering Information

Model Number	Base Frequency (MHz)	Pin 3	Pin 4	Pin 6	Pin 39
CW25-GDO-DK1	10.0 MHz	10 MHz	10 MHz	10 MHz	Variable
	TCXO	Thermal Stability		±280ppb; -20 to 70°C	
CW25-GDO-DK2	100 MHz	10 MHz	10 MHz	100 MHz	Variable
	TCXO	Thermal Stability		±280ppb; -20 to 70°C	

**For additional configurations, contact factory for details.*

Revision History

Revision	Date	Note
00	11/18/20	New Release of CW25-GDO-DK Series Data Sheet
01	03/17/21	Updated functionality of Pins 33 and 42
02	06/29/21	Updated Pins 41 and 42, added Communication Protocols and updated Temp Range
03	09/08/21	Pins 41 and 42 (Sync1/2) pin description changes p. 9, and Explanation of Parameters changes p. 18
04	09/23/21	Updated Pin 6 from N/C to LVCMOS output signal
05	10/19/21	Updated RF Signals Description - Pin 33 and Holdover Information