Integrated Device Technology, Inc.

FAST CMOS 16-BIT BUFFER/LINE DRIVER

IDT54/74FCT16244T/AT/CT/ET
IDT54/74FCT162244T/AT/CT/ET
IDT54/74FCT166244T/AT/CT
IDT54/74FCT162H244T/AT/CT/ET

FEATURES:

- **Common features:**
  - 0.5 MICRON CMOS Technology
  - **High-speed, low-power CMOS replacement for ABT functions**
  - **Typical $t_{SK(o)}$ (Output Skew) < 250ps**
  - **Low input and output leakage ≤ 1μA (max.)**
  - ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
  - Packages include 25 mil pitch SSOP, 19.6 mil pitch TSSOP, 15.7 mil pitch TVSOP and 25 mil pitch Cerpack
  - Extended commercial range of -40°C to +85°C
- **Features for FCT16244T/AT/CT/ET:**
  - High drive outputs (-32mA I_{OH}, 64mA I_{OL})
  - Power off disable outputs permit "live insertion"
  - Typical V_{OLP} (Output Ground Bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C
- **Features for FCT162244T/AT/CT/ET:**
  - Balanced Output Drivers: ±24mA (commercial), ±16mA (military)
  - Reduced system switching noise
  - Typical V_{OLP} (Output Ground Bounce) < 0.6V at V_{CC} = 5V, T_A = 25°C
- **Features for FCT166244T/AT/CT:**
  - Light Drive Balanced Output: ±8mA (commercial), ±6mA (military)
  - Minimal system switching noise
  - Typical V_{OLP} (Output Ground Bounce) < 0.25V at V_{CC} = 5V, T_A = 25°C
- **Features for FCT162H244T/AT/CT/ET:**
  - Bus-Hold retains last active bus state during 3-state
  - Eliminates the need for external pull up resistors

DESCRIPTION:

The 16-Bit Buffer/Line Driver is for bus interface or signal buffering applications requiring high speed and low power dissipation. These devices have a flow through pin organization, and shrink packaging to simplify board layout. All inputs are designed with hysteresis for improved noise margin. The three-state controls allow independent 4-bit, 8-bit or combined 16-bit operation. These parts are plug in replacements for 54/74ABT16244 where higher speed, lower noise or lower power dissipation levels are desired.

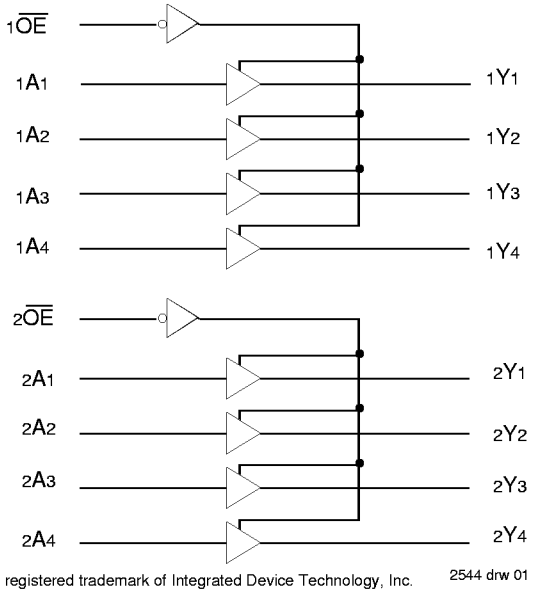
The FCT16244T/AT/CT/ET are ideally suited for driving high capacitance loads (>200pF) and low impedance backplanes. These "high drive" buffers are designed with power off disable capability to allow "live insertion" of boards when used in a backplane interface.

The FCT162244T/AT/CT/ET have balanced output current levels and current limiting resistors. These offer low ground bounce, minimal undershoot, and controlled output fall times, reducing the need for external series terminating resistors while still providing very high speed operation for loads of less than 200pF.

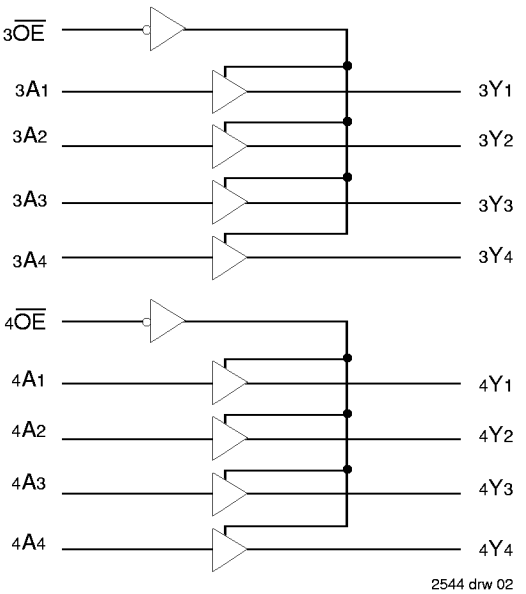
The FCT166244T/AT/CT are suited for very low noise, point-to-point driving where there is a single receiver, or a very light lumped load (<100pF). The buffers are designed to limit the output current to levels which will avoid noise and ringing on the signal lines without using external series terminating resistors.

The FCT162H244T/AT/CT/ET have "Bus-Hold" which retains the input's last state whenever the input goes to high impedance. This prevents "floating" inputs and eliminates the need for pull-up/down resistors.

FUNCTIONAL BLOCK DIAGRAM



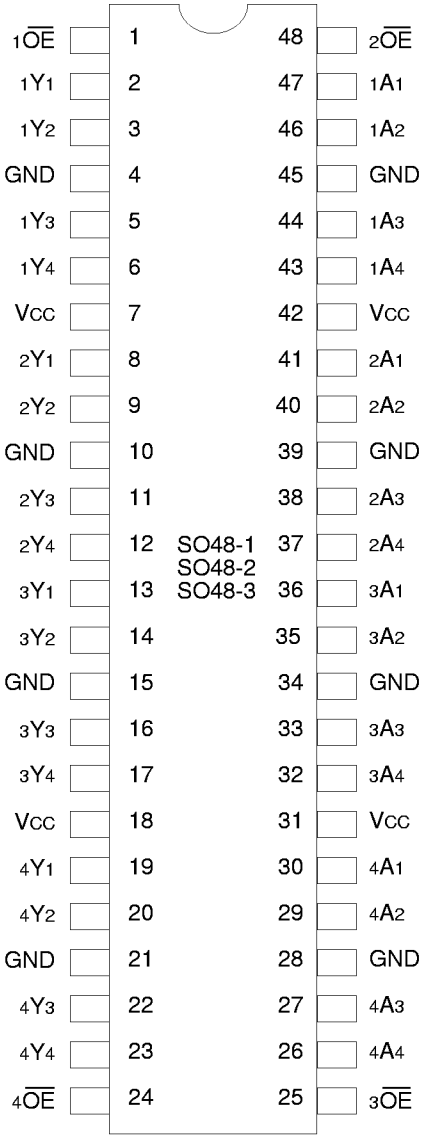
2544 drw 01



2544 drw 02

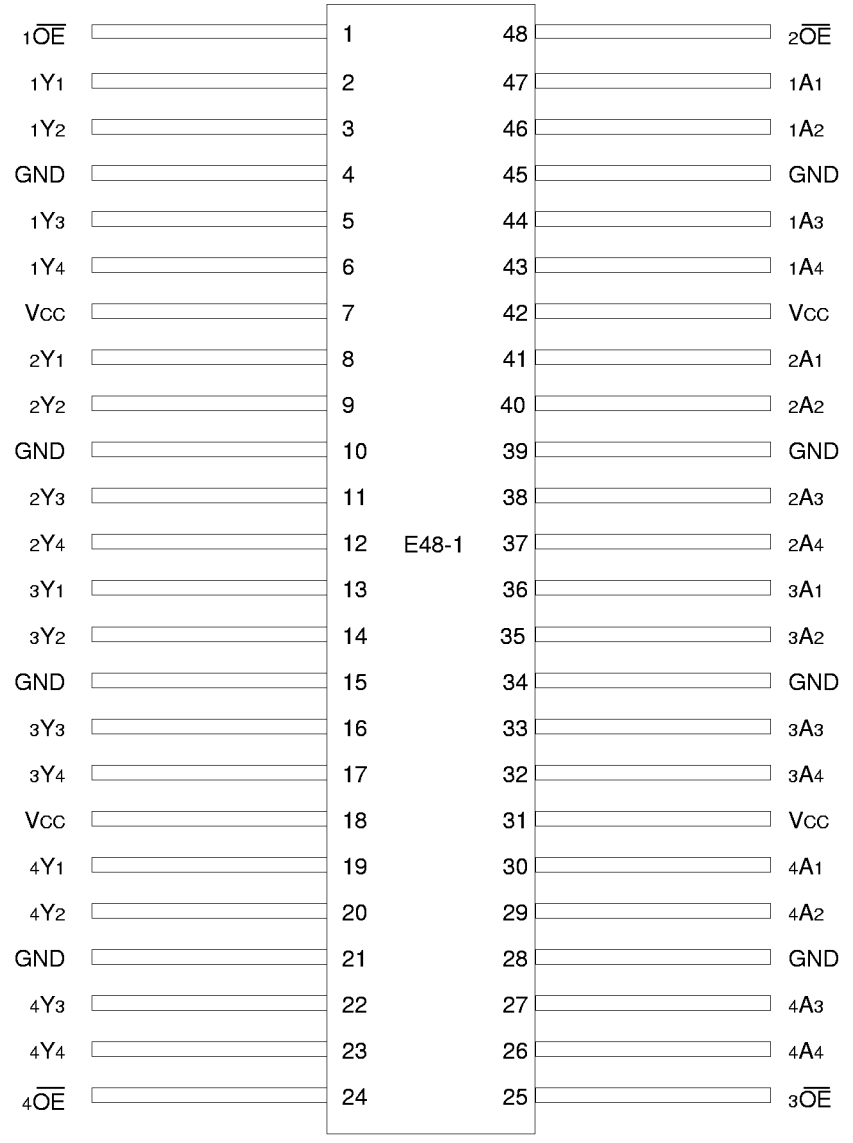
The IDT logo is a registered trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



SSOP/ TSSOP/TVSOP TOP VIEW

2544 drw 03



CERPACK TOP VIEW

2544 drw 04

PIN DESCRIPTION

Pin Names	Description
x$\overline{OE}$	3–State Output Enable Inputs (Active LOW)
xAx	Data Inputs[1]
xYx	3-State Outputs

NOTE: 2544 tbl 01

1. On FCT16xH these pins have "Bus-hold". All other pins are standard inputs, outputs or I/Os.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max.	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC} +0.5	V
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	DC Output Current	–60 to +120	mA

2544 lnk 03

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All device terminals except FCT162XXXT and FCT166XXXT output and I/O terminals.
3. Output and I/O terminals for FCT162XXXT and FCT166XXXT.

FUNCTION TABLE(1)

Inputs		Outputs
$x\overline{OE}$	xAx	xYx
L	L	L
L	H	H
H	X	Z

2544 tbl 02

NOTE:
1. H = HIGH Voltage Level
   X = Don't Care
   L = LOW Voltage Level
   Z = High Impedance

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	3.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	3.5	8.0	pF

2544 lnk 04

NOTE:
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (STANDARD PARTS)

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 5.0V ± 10%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)(5)	V_{CC} = Max.	V_I = V_{CC}	—	—	±1	µA
	Input HIGH Current (I/O pins)(5)			—	—	±1	
I_{IL}	Input LOW Current (Input pins)(5)		V_I = GND	—	—	±1	
	Input LOW Current (I/O pins)(5)			—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}	(3-State Output pins)(5)		V_O = 0.5V	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND(3)		–80	–140	–225	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	5	500	µA

2544 lnk 05

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.
5. The test limit for this parameter is ± 5µA at T_A = –55°C.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (BUS-HOLD)

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 5.0V ± 10%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter		Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level		Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level		Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current[4]	Standard Input[5]	V_{CC} = Max.	V_I = V_{CC}	—	—	±1	µA
		Standard I/O[5]			—	—	±1	
		Bus-hold Input			—	—	±100	
		Bus-hold I/O			—	—	±100	
I_{IL}	Input LOW Current[4]	Standard Input[5]		V_I = GND	—	—	±1	
		Standard I/O[5]			—	—	±1	
		Bus-hold Input			—	—	±100	
		Bus-hold I/O			—	—	±100	
I_{BHH}	Bus Hold Sustain Current[4]	Bus-hold Input	V_{CC} = Min.	V_I = 2.0V	–50	—	—	µA
I_{BHL}				V_I = 0.8V	+50	—	—	
I_{OZH}	High Impedance Output Current (3-State Output pins)[5,6]		V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}				V_O = 0.5V	—	—	±1	
V_{IK}	Clamp Diode Voltage		V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current		V_{CC} = Max., V_O = GND[3]		–80	–140	–225	mA
V_H	Input Hysteresis		—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current		V_{CC} = Max., V_{IN} = GND or V_{CC}		—	5	500	µA

NOTES:

2544 lnk 06

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Pins with Bus-hold are identified in the pin description.
5. The test limit for this parameter is ± 5µA at T_A = –55°C.
6. Does not include Bus-hold I/O pins.

OUTPUT DRIVE CHARACTERISTICS FOR FCT16244T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_O	Output Drive Current	V_{CC} = Max., V_O = 2.5V[3]		–50	—	–180	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –3mA	2.5	3.5	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.4	3.5	—	V
			I_{OH} = –24mA MIL. I_{OH} = –32mA COM'L.[4]	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	—	0.2	0.55	V
I_{OFF}	Input/Output Power Off Leakage[5]	V_{CC} = 0V, V_{IN} or $V_O \leq$ 4.5V		—	—	±1	µA

2544 lnk 07

OUTPUT DRIVE CHARACTERISTICS FOR FCT162244T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		60	115	200	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		–60	–115	–200	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –16mA MIL. I_{OH} = –24mA COM'L.	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA MIL. I_{OL} = 24mA COM'L.	—	0.3	0.55	V

2544 lnk 08

OUPUT DRIVE CHARACTERISTICS FOR FCT166244T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		16	48	96	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		–16	–48	–96	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 6mA MIL. I_{OL} = 8mA COM'L.	—	0.3	0.55	V

2544 lnk 09

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.
5. The test limit for this parameter is ± 5µA at T_A = –55°C.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $x\overline{OE}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	60	100	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open fi = 10MHz	V_{IN} = V_{CC} V_{IN} = GND	—	0.6	1.5	mA
		50% Duty Cycle $x\overline{OE}$ = GND One Bit Toggling	V_{IN} = 3.4V V_{IN} = GND	—	0.9	2.3	
		V_{CC} = Max. Outputs Open fi = 2.5MHz	V_{IN} = V_{CC} V_{IN} = GND	—	2.4	4.5[5]	
		50% Duty Cycle $x\overline{OE}$ = GND Sixteen Bits Toggling	V_{IN} = 3.4V V_{IN} = GND	—	6.4	16.5[5]	

2544 tbl 10

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR FCT16244T/FCT162244T

Symbol	Parameter	Condition[1]	FCT16244T/162244T/166244T				FCT16244AT/162244AT/166244AT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay xAx to xYx	C_L = 50pF R_L = 500Ω	1.5	6.5	1.5	7.0	1.5	4.8	1.5	5.1	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	8.0	1.5	8.5	1.5	6.2	1.5	6.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	7.0	1.5	7.5	1.5	5.6	1.5	5.9	ns
$t_{SK(o)}$	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	0.5	ns

2544 tbl 11

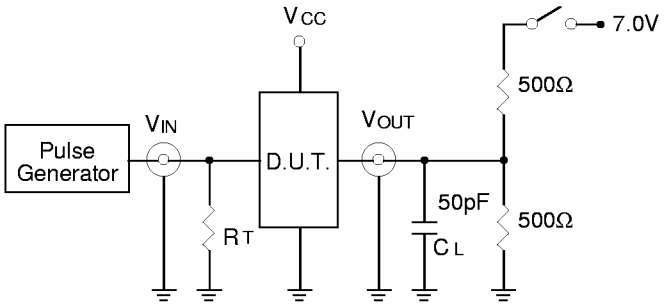
Symbol	Parameter	Condition[1]	FCT16244CT/162244CT/166244CT				FCT16244ET/162244ET				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay xAx to xYx	C_L = 50pF R_L = 500Ω	1.5	4.1	1.5	4.6	1.5	3.2	—	—	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	5.8	1.5	6.5	1.5	4.4	—	—	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	5.2	1.5	5.7	1.5	3.6	—	—	ns
$t_{SK(o)}$	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	—	ns

2544 tbl 12

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2544 drw 05

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

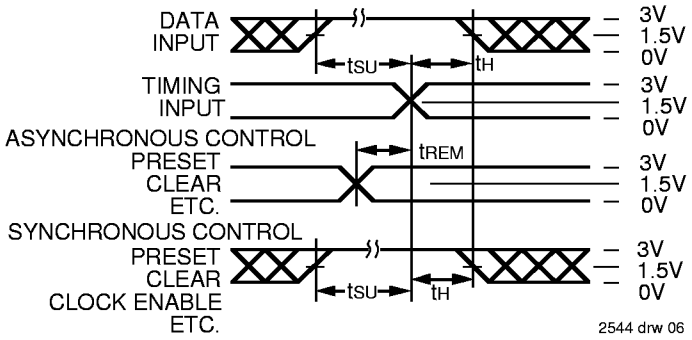
2544 lnk 13

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

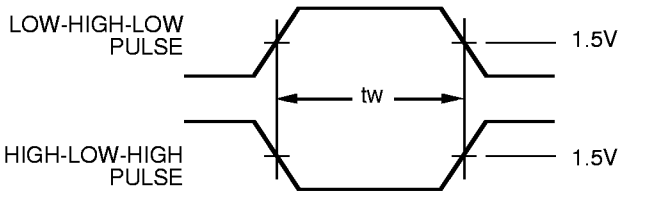
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



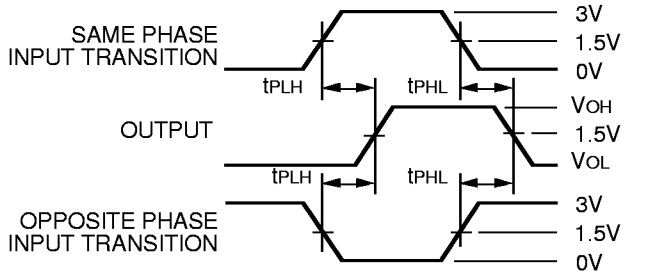
2544 drw 06

PULSE WIDTH



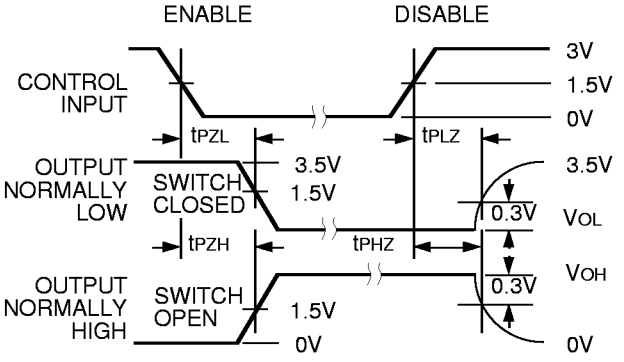
2544 drw 07

PROPAGATION DELAY



2544 drw 08

ENABLE AND DISABLE TIMES

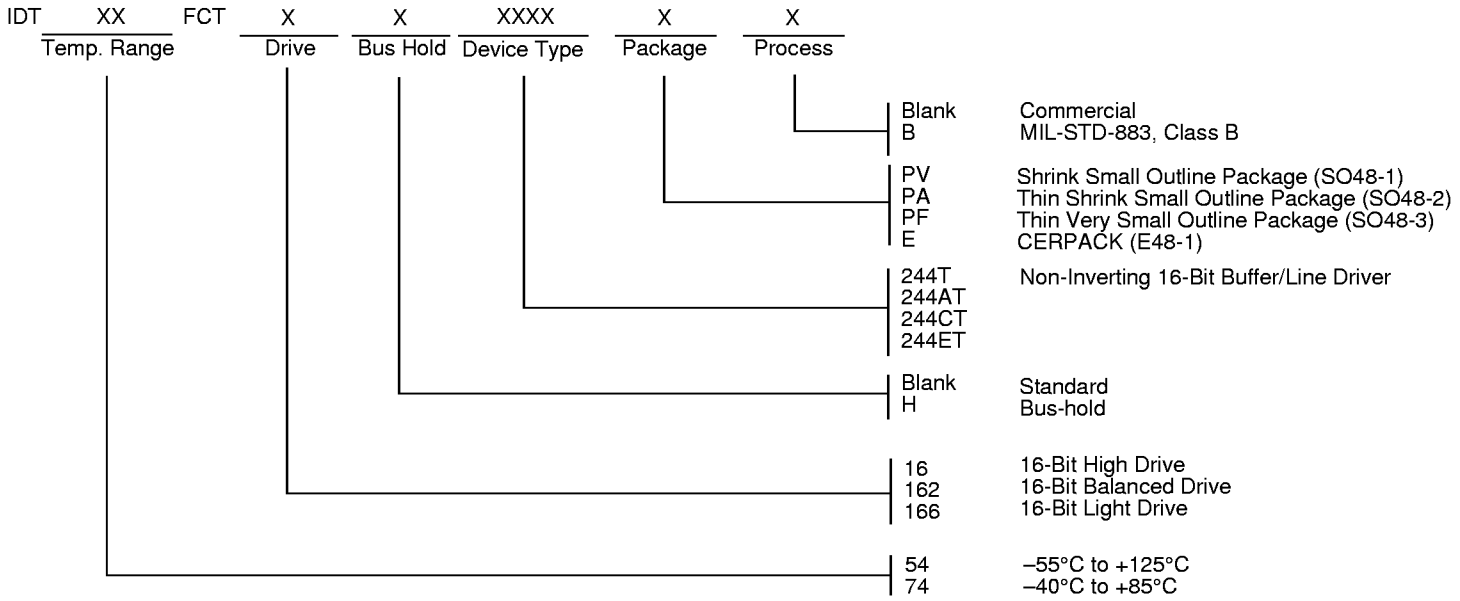


2544 drw 09

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

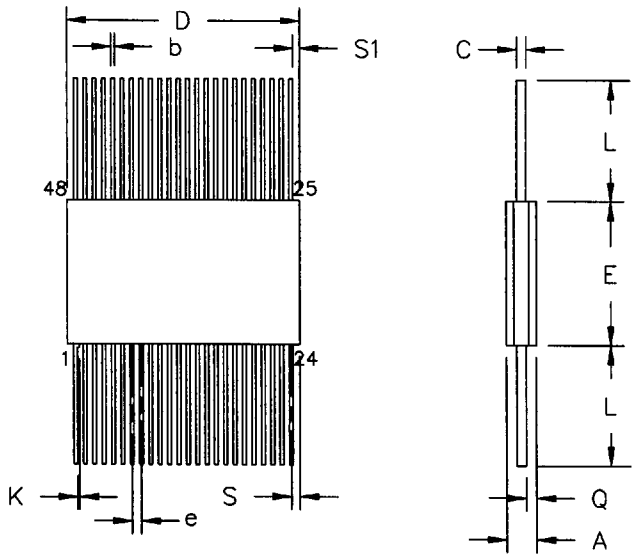
ORDERING INFORMATION



2544 drw 10

CERPACK (Continued)

REV	DCN	DESCRIPTION	DATE	APPROVED
00	21269	ORIGINAL ISSUE	1/13/92	Chris Wyland
01	23370	UPDATED DWG TO MEET JEDEC		



DWG #	E48-1		E56-1	
SYMBOL	MIN	MAX	MIN	MAX
A	.075	.095	.075	.095
b	.008	.013	.008	.013
C	.0045	.006	.0045	.006
D	.610	.640	.710	.740
E	.370	.390	.370	.390
e	.025 BSC		.025 BSC	
K	.003	.007	.003	.007
L	.250	.370	.250	.370
N	48		56	
Q	.025	.045	.025	.045
S	–	.035	–	.035
S1	.005	–	.005	–
MIL-M-38510	NOT LISTED		NOT LISTED	
EXCEPTIONS				
JEDEC EXCEPTIONS	IN PROGRESS		IN PROGESS	

NOTES: (UNLESS OTHERWISE SPECIFIED)
1. ALL DIMENSIONS ARE IN INCHES.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "N" REPRESENTS THE NUMBER OF LEADS.
4. THIS DWG REPRESENTS A 48 LEAD CERPACK.

TOLERANCES UNLESS OTHERWISE SPECIFIED
FRAC ± – DEC ± – ANGLES ± –

APPROVALS	DATE
DRAWN AA	10/91
CHECKED	

Integrated Device Technology, Inc.
3236 Scott Blvd., Santa Clara, CA 95051
(408) 727-6116 FAX: (408) 727-2328

CERPACK MARKETING DWG (.025" LEAD PITCH)

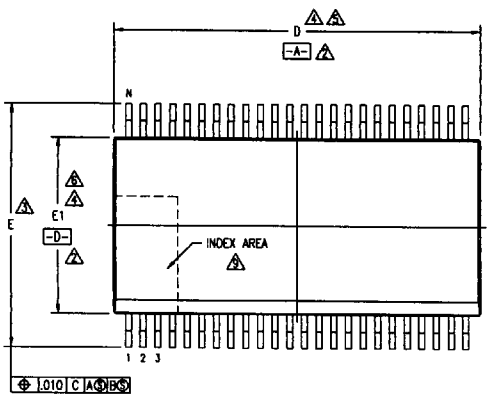
SCALE	SIZE	DRAWING NO.	REV
N/A	A	PSC-2101	01

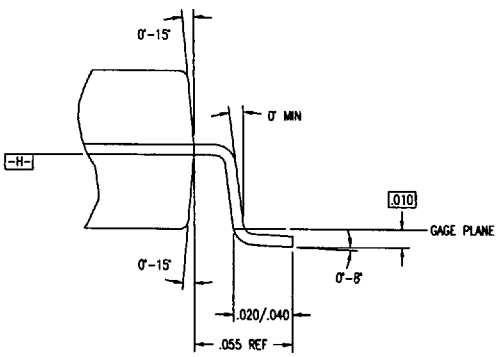
DO NOT SCALE DRAWING | SHEET 2

PACKAGE DIAGRAM OUTLINES

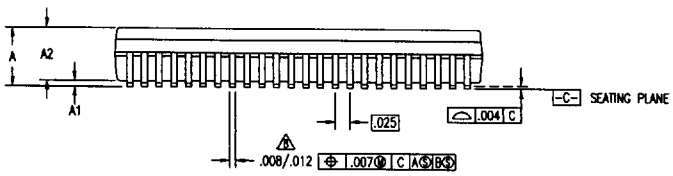
SSOP

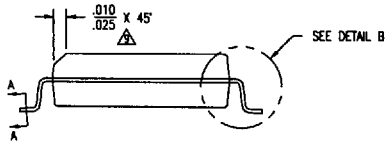
REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
17893	00	INITIAL RELEASE	07/15/90	A. FUNCELL
22377	01	REMOVE CHAMFER FROM PACKAGE	04/15/92	T. VU
27492	02	REDRAW TO JEDEC FORMAT	02/01/95	

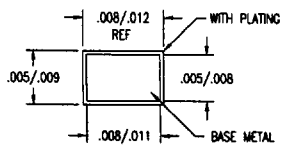




DETAIL B







SECTION A-A

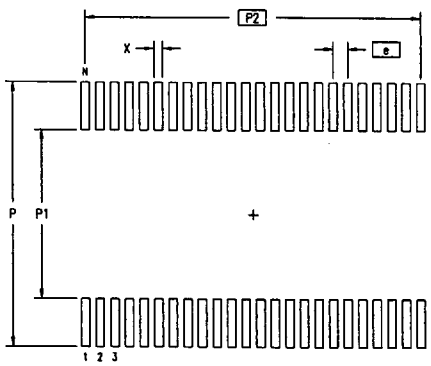
TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc. 2975 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674 TWX: 910-338-2070	
DECIMAL XX± XXX± XXXX±	ANGULAR ±		
APPROVALS	DATE	TITLE PV PACKAGE OUTLINE .300" BODY WIDTH SSOP .025" PITCH	
DRAWN AA	08/15/90		
CHECKED		SIZE C	DRAWING No. PSC-4029 REV 02
		DO NOT SCALE DRAWING	

SSOP (Continued)

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
17893	00	INITIAL RELEASE	07/15/90	A. FUNCELL
22377	01	REMOVE CHAMFER FROM PACKAGE	04/15/92	T. VU
27492	02	REDRAW TO JEDEC FORMAT	02/01/95	

DWG #		S048-1			DWG #		S056-1		
SYMBOL	JEDEC VARIATION AA			NOTE	JEDEC VARIATION AB			NOTE
	MIN	NOM	MAX		MIN	NOM	MAX	
A	.095	.102	.110		.095	.102	.110	
A1	.008	.012	.016		.008	.012	.016	
A2	.088	.090	.092		.088	.090	.092	
D	.620	.625	.630	4,5	.720	.725	.730	4,5
E	.395	.405	.420	3	.395	.405	.420	3
E1	.291	.295	.299	4,6	.291	.295	.299	4,6
N	48				56			

LAND PATTERN DIMENSIONS



	MIN	MAX	MIN	MAX
P	.450	.458	.450	.458
P1	.282	.290	.282	.290
P2	.575 BSC		.675 BSC	
X	.010	.018	.010	.018
e	.025 BSC		.025 BSC	
N	48		56	

NOTES:

1 ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982

2 DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-

3 DIMENSION E TO BE DETERMINED AT SEATING PLANE -C-

4 DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE -H-

5 DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 PER SIDE

6 DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED .015 PER SIDE

7 THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND .010 FROM LEAD TIP

8 LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .004 IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT

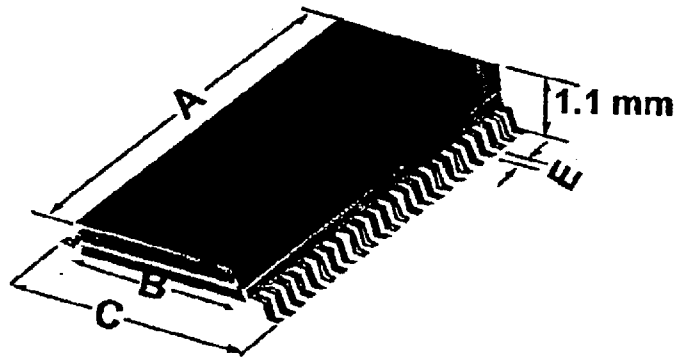
9 THE CHAMFER ON THE PACKAGE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE ZONE INDICATED

10 ALL DIMENSIONS ARE IN INCHES

11 THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-118, VARATION AA & AB

TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc.
DECIMAL XX± XXX± XXXX±	ANGULAR ±	2975 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674 TWX: 910-338-2070
APPROVALS	DATE	TITLE PV PACKAGE OUTLINE .300" BODY WIDTH SSOP .025" PITCH
DRAWN AA	05/15/90	
CHECKED		SIZE C DRAWING No. PSC-4029 REV 02
		DO NOT SCALE DRAWING

TVSOP
The Most Compact Double Density Package



TVSOP Package	Typical Dimensions (in mm)				Area (mm2)
	A	B	C	E	
48 Pin	9.80	4.40	6.40	0.40	63.00
56 Pin	11.30	4.40	6.40	0.40	72.30
80 Pin	17.00	6.10	8.10	0.40	137.80
100 Pin	20.80	6.10	8.10	0.40	168.50

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Double Density Packaging

48-Pin

16.0 x 10.3 x 2.6 mm
pin pitch = 0.635 mm
Area = 164.8 mm²

12.5 x 8.1 x 1.1 mm
pin-pitch = 0.5 mm
Area = 101.3 mm²

9.8 x 6.4 x 1.1 mm
pin-pitch = 0.4 mm
Area = 62.7 mm²

56-Pin

18.4 x 10.3 x 2.6 mm
pin-pitch = 0.635 mm
Area = 189.5 mm²

14.0 x 8.1 x 1.1 mm
pin-pitch = 0.5 mm
Area = 113.4 mm²

11.3 x 6.4 x 1.1 mm
pin-pitch = 0.4 mm
Area = 72.3 mm²

TVSOP	Area (mm^2)	%Smaller Than SSOP	%Smaller Than TSSOP
48 pin	63.00	61.9	38.0
56 pin	72.30	62.2	36.0

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