

TMS320F28388D controlCARD Information Guide

The F28388D controlCARD (TMDSCNCD28388D) from Texas Instruments (TI) provides a great way to learn and experiment with the F2838x device. The F2838x device is a member of TI's C2000™ family of microcontrollers (MCUs). This 180-pin controlCARD is intended to provide a well-filtered robust design that is capable of working in most environments. This document provides the hardware details of the F28388D controlCARD and explains the functions, locations of jumpers, and connectors present on the board.

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1 Introduction

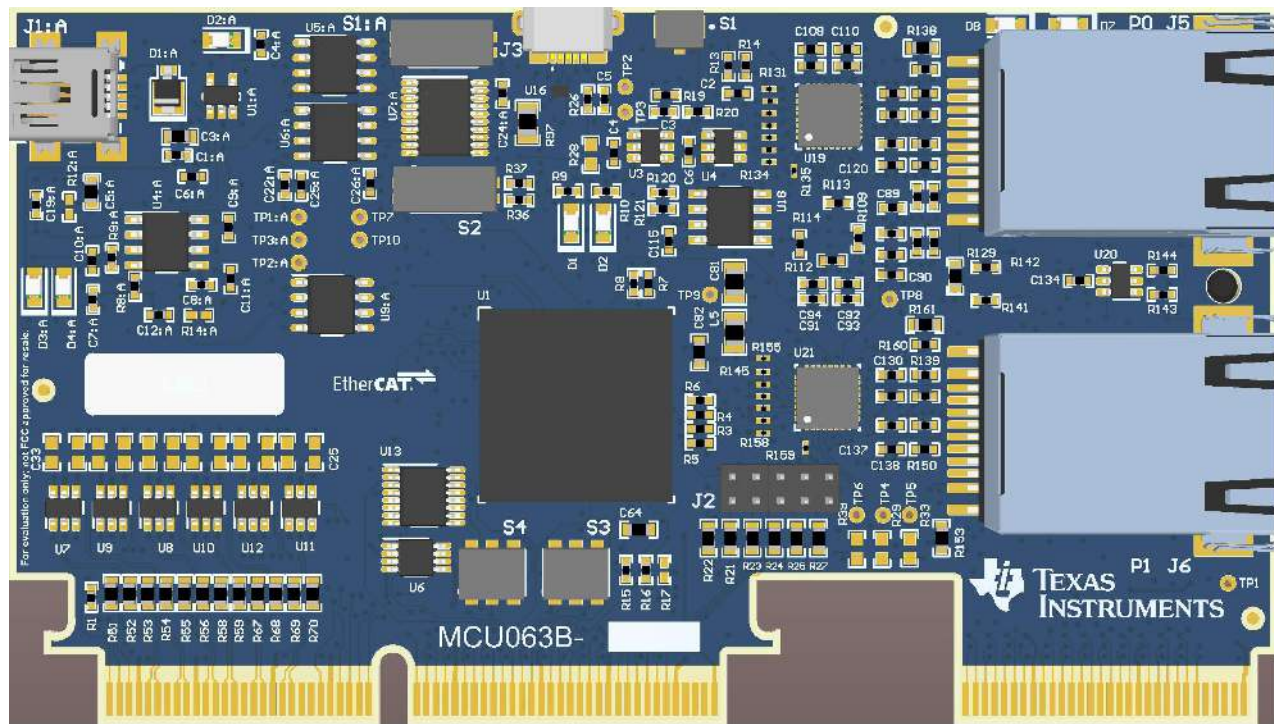


Figure 1. F28388D controlCARD

Each controlCARD comes with a Hardware Developer’s Kit that is a full set of files necessary to evaluate and develop with a C2000 device. These files include:

- Schematics – Designed in Altium
- Bill of Materials (BOM)
- Layout PCB files - Designed in Altium
- Gerber files

NOTE: This kit is designed to explore the functionality of the F2838x microcontroller. The controlCARD can be treated as a good reference design; it is not intended to be a complete customer design. Full compliance to safety, EMI/EMC, and other regulations are left to the designer of the customer’s system.

2 Hardware Quick Setup Guide

1. Connect and power embedded emulator.
 - a. Connect USB-B "mini" connector to J1:A
2. Provide power to the isolated F28388D device.
 - a. Option 1:
 - i. Insert the TMDSCNCD28388D controlCARD into a TMDSHSECDOCK, or other compatible docking station.
 - ii. Connect USB-B "mini" connector to J17 on the TMDSHSECDOCK.
 - iii. Set S1 to the "USB-ON" position. D3 on the controlCARD should illuminate.
 - b. Option 2:
 - i. Connect USB-B "micro" connector to J3 of the F28388D controlCARD
3. Verify clock input frequency and software PLL configuration are compatible for your version of the controlCARD, see [Section 3.2](#).
4. For a detailed explanation of the hardware configuration, see [Section 4.3](#).

3 Errata

Current revision of controlCARD as of 5/29/2020: PCB rev - B , ASSY rev - none.

3.1 Warnings, Notes, and Errata

- The F28388D controlCARD supports USB host/device connectivity. However, the micro-USB port, J3, is not isolated from the board ground. Care should be taken when this controlCARD is being used in a high-power application and this USB port is also being used. Note that external USB isolation buffers may be required for these types of applications.
- The F28388D Experimenter's Kit ships with a USB cable and is designed to be powered via USB. However, in extreme cases the board/controlCARD may require more power than the 5 V @ 500 mA (USB 3.0 - 900 mA) that a computer's USB port can provide. This is especially true when additional circuitry has been added to the docking station. In such cases, it is recommended to use an external 5 V power supply (2.5 mm inner diameter x 5.5 mm outer diameter) and plug it into J1. A compatible supply such as:
 - Pihong PSAC05R-050(P)-R-C2 + Pihong RPBAG
- By default in Boot-from-SCI mode, the MCU will now expect GPIO28 and GPIO29 to be the IO pins responsible for sending the program to the device. The default GPIOs were different on other C2000 devices. These new GPIOs are connected to the isolated USB-to-serial interface via the FTDI chip.
- R98 on the controlCARD is populated to allow a customer to evaluate the controlCARD without a baseboard, if desired. Because R98 is populated, the controlCARD will have more capacitance on the USB 5 V supply than the USB specification allows. R98 should be removed in order to meet the specification.

3.2 Warnings and Notes for All controlCARDS

The controlCARD was modified to use a 25 MHz clock input by default. This change was needed to meet compliance requirements for the EtherCAT Slave Controller(ESC). The ESC, located inside of the F28388D device, is required to share the same clock source as the EtherCAT physical layer (PHYs). This change allows both to share the 25 MHz clock input. For customers not using the ESC, this change is not a requirement.

Early versions of the controlCARDS (MCU063E1, MCU063E2, MCU063A) use a 20 MHz clock. This is compatible with C2000Ware versions V3.01.00.00 and earlier. When using with C2000Ware versions V3.02.00.00 and later, modifications to the PLL settings are necessary. Additionally, controlCARD versions MCU063B and later use a 25 MHz input clock and are only compatible with C2000Ware versions V3.02.00.00 or later.

NOTE: Early versions of the MCSDK and DPSDK that use a C2000Ware version before V3.02.00.00 are also affected. Hardware damage may occur to the power electronics if the code is not modified before running these examples.

3.3 Warnings About Specific controlCARD Revisions

For more information, see [Section 3.2](#).

MCU063E1

- The E1 version of the controlCARD contains an error. These controlCARDS have had two cut traces and a blue wire soldered between U17 and R111 to correct this issue.
 - Fix: None, functionality is identical to later versions of the controlCARD.
- U20 is a non-inverting buffer. D7 and D8 will be inverted when driven by the ECAT module
 - Fix: You must drive D7 and D8 using the GPIO function. Later versions of the controlCARD use an inverting buffer.
- R44 is populated by default.
 - Fix: None, you can choose to depopulate R44.
- A 56 Ω resistor is missing from this design, which can effect long-term system reliability.
 - A single 56 Ω resistor (10% or better tolerance) should be placed between VDD and VSS in all end systems. This resistor provides a load to consume an internal VDD3VFL to VDD current source and avoid VDD voltage rising during low power device conditions.

MCU063E2

- A 56 Ω resistor is missing from this design, which can effect long-term reliability.
 - A single 56 Ω resistor (10% or better tolerance) should be placed between VDD and VSS in all end systems. This resistor provides a load to consume an internal VDD3VFL to VDD current source and avoid VDD voltage rising during low power device conditions.

MCU063A

- A 56 Ω resistor is missing from this design, which can effect long-term reliability.
 - A single 56 Ω resistor (10% or better tolerance) should be placed between VDD and VSS in all end systems. This resistor provides a load to consume an internal VDD3VFL to VDD current source and avoid VDD voltage rising during low power device conditions.

MCU063B

- Defaults to a 25 MHz clock input. For more information, see [Section 3.2](#).

4 Getting Familiar With the controlCARD

4.1 F28388D controlCARD Features

- **F28388D Microcontroller** – High performance C2000 microcontroller is located on the controlCARD.
- **180-pin HSEC8 Edge Card Interface** – Allows for compatibility with all of C2000's 180-pin controlCARD-based application kits and controlCARDS. Compatibility with 100-pin controlCARDS can be accomplished using the TMSADAP180TO100 adapter card (sold separately).
- **Built-in Isolated JTAG Emulation** – An XDS100v2 emulator provides a convenient interface to Code Composer Studio™ without additional hardware. Setting a switch allows an external JTAG emulator to be used.
- **Connectivity** – The controlCARD contains connectors that allow you to experiment with USB, a microSD card, and isolated universal asynchronous receiver/transmitter (UART)/SCI with the F2838x MCU.
- **Key Signal Breakout** – Most GPIO, analog-to-digital converter (ADC) and other key signals routed to hard gold connector fingers.
- **Robust Power Supply Filtering** – Single 5 V input supply powers an on-card 3.3 V LDO. All MCU inputs are then decoupled using LC filters near the device.

- **ADC Clamping** – ADC inputs are clamped by protection diodes.
- **Anti-Aliasing Filters** – Noise filters (small RC filters) can be easily added on the ADC input pins.

The controlCARD uses DP83822 10/100M Ethernet PHY for EtherCAT communication. This PHY has low round trip (TX+RX) latency of 242 ns and robust EMI/EMC performance. DP83826E/I is an alternative 10/100M Ethernet PHY and is also recommended for use with F2838x devices. DP83826E has a reduced and more deterministic latency of $< 216 \text{ ns} \pm 2 \text{ ns}$. In addition the XI to TX_CLK clock phase delay is $\pm 2 \text{ ns}$. These features, along with robust EMI/EMC performance, make DP83826E/I suitable for real time applications. For more details, see the [DP83826 Deterministic, Low-Latency, Low-Power, 10/100 Mbps, Industrial Ethernet PHY Data Sheet](#).

4.2 Assumed Operating Conditions

This kit is assumed to run at standard room conditions. Standard ambient temperature and pressure (SATP) with moderate-to-low humidity is assumed.

4.3 Using the controlCARD

In order for the controlCARD to operate, the controlCARD's MCU must be powered. This is most often done by inputting 5 V through the HSEC connector via an accompanying baseboard. For example, if using a docking station baseboard, 5 V DC should be input into the docking station's J1 or J17. Then, SW1 needs to be toggled to the appropriate position.

Optionally, the MCU could also be powered via the micro-USB connector on the controlCARD (J3). Based on the way the controlCARD is used, additional hardware settings will be necessary (see [Table 1](#)).

Table 1. Emulator Switch Selections

	Debug Using CCS and the On-Card XDS100v2 Emulator	Debug Using CCS and an External Emulator via the Baseboard	Standalone (Boot From FLASH or Other Boot Mode)
S1:A	Position 1: ON (right)	Position 1: OFF (left)	Position 1: OFF (left)
J1:A	Connect a mini USB cable between J1:A and your computer. In CCS, use this target configuration: TMS320F28388D device with an XDS100v2 emulator.	---	---
S2	Position 1: OFF (left- Logic 1) Position 2: ON (right- Logic 0) Putting the C2000 device into WaitMode can reduce the risk of connectivity issues.	Position 1: OFF (right- Logic 1) Position 2: ON (left- Logic 0) - Putting the C2000 device into Wait Mode can reduce the risk of connectivity issues.	Set S1 as desired
Baseboard's JTAG connector (J2 on Docking Station)	---	Connect an external emulator.	---

Code Composer Studio is an Integrated Development Environment (IDE) used to debug and develop software for the C2000 series of MCUs. It can be downloaded from the following link:
<http://www.ti.com/tool/ccstudio>.

The following PDF documents are provided, as part of C2000Ware, to describe where each of the F2838x MCU's pins will appear on the controlCARD connector/docking station:

- **TMDSCNCD28388D_180cCARD_map** – tells where each MCU pin will go on the HSEC controlCARD connector or the 120/180-pin controlCARD docking station.
- **TMDSCNCD28388D_100DIM_map** – tells where each MCU pin will go to on the DIM100 controlCARD connector or the DIM100 docking station. This assumes that the TMDSadap180TO100 adapter card is used.

More information on the controlCARD docking station can be found at the following location:

- <install directory>\c2000\C2000Ware_x_xx_xx_xx\boards\controlCARDs\TMDSCNCD28388D\R_x

4.3.1 Clocking Configuration

The clocking tree on this controlCARD is configurable. Both a 20 MHz clock source and a 25 MHz clock source can be provided to the F28388D device. To change this configuration, the R43 0-Ω resistor must be de-soldered and moved to the R39 location.

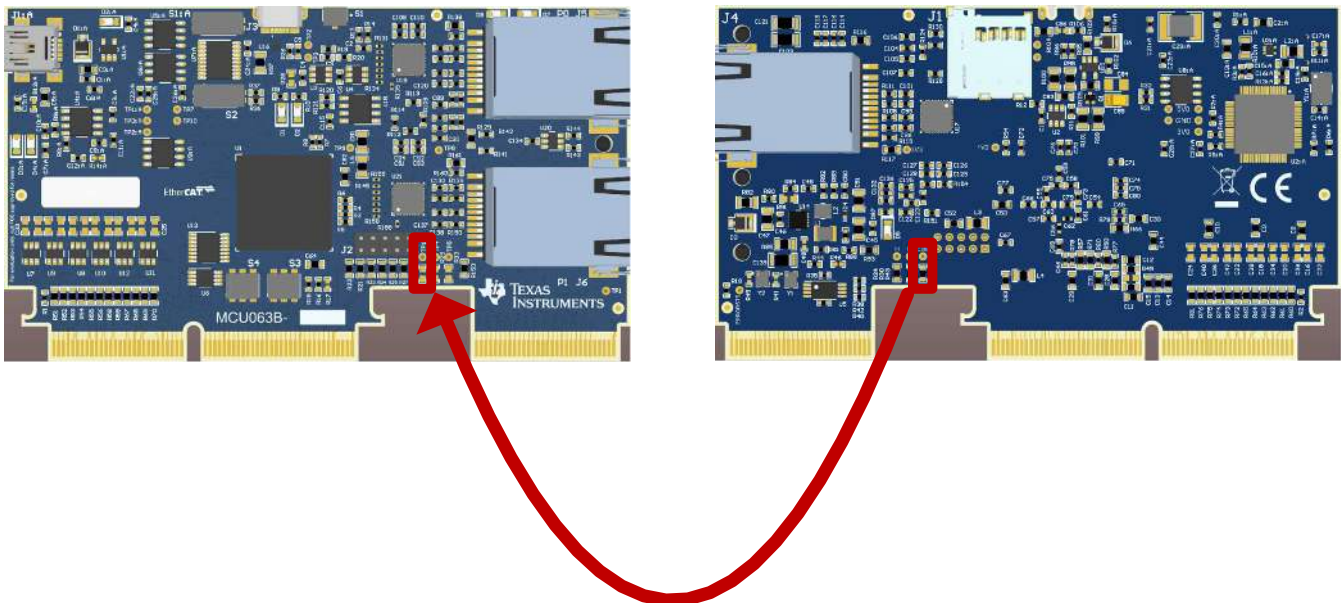
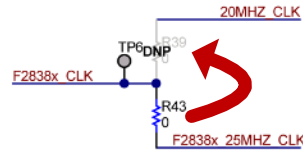


Figure 2. Changing the Clock Source From 25 MHz to 20 MHz

4.4 Experimentation Software

[Code Composer Studio \(CCS\) Integrated Development Environment \(IDE\)](#) is recommended for developing and debugging software for the C2000 series of MCUs. CCS is free to download and use with the controlCARD. Introductory videos for CCS are available at training.ti.com.

[C2000Ware](#) contains a full suite of example software designed to work with the F2838x controlCARD. For information about software compatibility with your version of the controlCARD, see [Section 3.2](#).

This software package includes many example projects that allow the user to experiment with the ADC, PWM, and other C2000 peripherals.

Support files for both register-level and driver-level programming are included with C2000Ware:

- Register header files are located at: `\ti\c2000\C2000Ware_XXXX\device_support\f2838x\examples`
- Driverlib programming examples are located at: `\ti\c2000\C2000Ware_XXXX\driverlib\f2838x\examples`

5 Special Notes

5.1 XDS100v2 Emulator and SCI (UART) Connectivity

The F28388D controlCARD provides emulation and USB-to-UART adapter functionality on the controlCARD. This allows for a convenient method to debug and demonstrate the F2838x MCU.

Note that the FTDI chip, its support circuitry, and associated isolation components are placed in Macro A (the left section of the controlCARD). Each of these components contains an additional “A” within the component reference designator (that is, R2:A for resistor 2 in Macro A) (see [Figure 3](#)).

The configuration of the switches on S1:A determine if the on-board emulator is active, if an external emulator can be used, or if the device will boot from FLASH/peripherals (see [Table 1](#)).

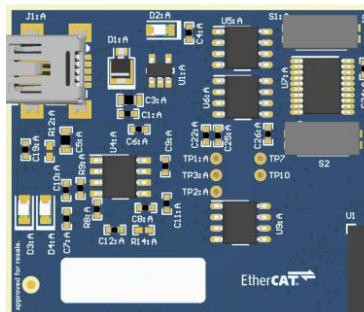


Figure 3. XDS100v2 Emulation Circuitry and Isolation Circuitry

5.2 External Connector

The TMDSCNCD28379D controlCARD has a high-density connector denoted by J9 in that design. This connector is no longer supported by the TMDSCNCD28388D controlCARD.

6 Hardware References

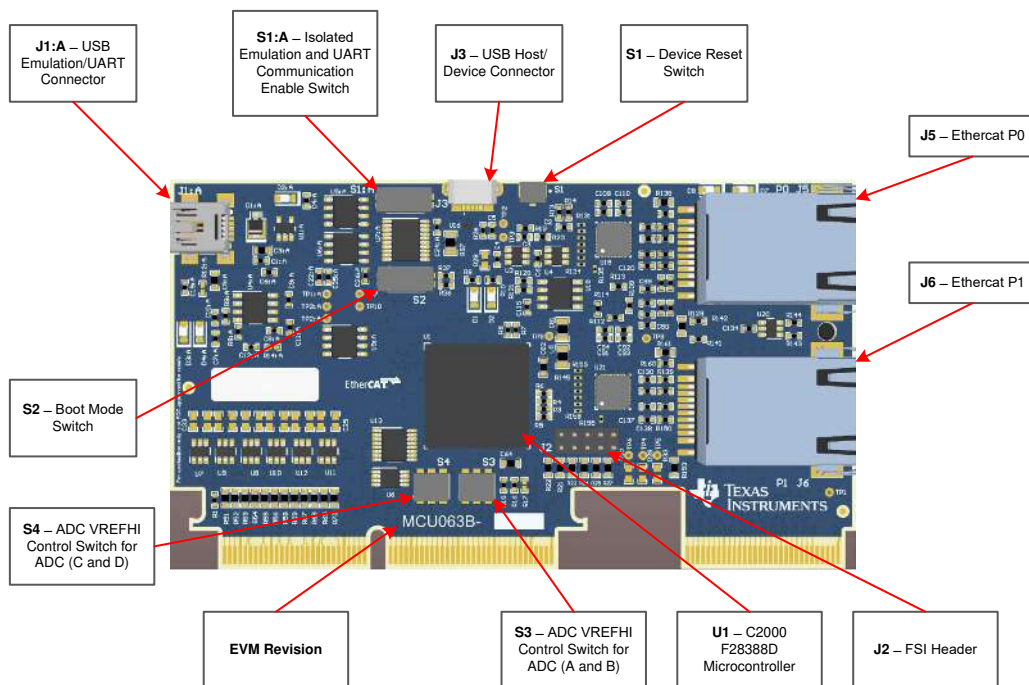


Figure 4. Key Components on the controlCARD - Front

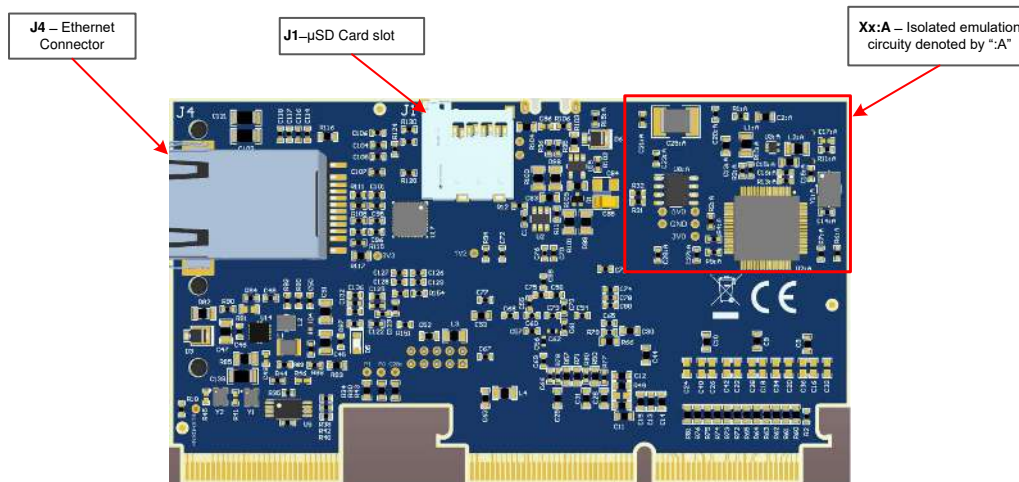


Figure 5. Key Components on the controlCARD - Back

Table 2. Hardware Connections

Connectors	
J1:A	Emulation/UART connector - USB mini A connector used to provide XDS100v2 emulation and USB-to-UART (SCI) communication through FTDI logic. S1:A determines which connections are enabled to the MCU.
J1	microSD card slot – connects to MCU via SPI
J2	FSI Header
J3	USB connector – USB micro AB connector supports USB 2.0 host/device
J4	Ethernet connector – RJ45 connector
J5	EtherCAT P0 – RJ45 connector
J6	EtherCAT P1 – RJ45 connector

LEDs	
D2:A	Turns on when ISO JTAG logic is powered on (green)
D3:A	JTAG/UART RX toggle indicator (blue)
D4:A	JTAG/UART TX toggle indicator (blue)
D1	Controlled by GPIO–31 with negative logic (red)
D2	Controlled by GPIO–34 with negative logic (red)
D5	Turns on when the controlCARD is powered ON (green)
D7	Controlled by GPIO–145, EtherCAT Error LED (red)
D8	Controlled by GPIO–146, EtherCAT Run LED (green)

Resistors and Capacitors	
R47, R48	<p>Alternate Reference Configuration Resistors: These resistors allow the user to choose whether the alternate reference for the ADCs will be given by:</p> <ul style="list-style-type: none"> • If R47 is unpopulated & R48 is populated: A precision 3.0V reference (REF5030) • If R47 is populated & R48 is unpopulated: The reference will be given by pin 45 of the HSEC controlCARD connector. This will allow the baseboard to provide the desired voltage reference.
C16-C27, C32-C43	Optional RC input filter for all ADC inputs

Switches	
S1:A	Isolated emulation and UART communication enable switches:
	<p>S1:A Position 1 – JTAG Enable:</p> <ul style="list-style-type: none"> • ON – All signals between the XDS100v2 emulation logic and the MCU will be connected. This setting is valid when the MCU is being debugged or programmed via the on-card XDS100v2 emulator. • OFF – The XDS100v2 emulation logic will NOT be connected to the MCU. This setting is valid when the device will boot from FLASH, boot from a peripheral directly, or when an external JTAG emulator will be used. <p>S1:A Position 2 – ISO UART communication enable:</p> <ul style="list-style-type: none"> • ON – The C2000 MCU's GPIO-28 (and pin76 of the 180pin controlCARD connector) will be coupled to the FTDI's USB-to-Serial adapter. This allows UART communication to a computer via the FTDI chip. However, in this position, GPIO-28 will be forced high by the FTDI chip. Functionality of pin76 of the connector will be limited. • OFF – The C2000 MCU will NOT be connected to the FTDI USB-to-Serial adapter. Pin76 of the 180pin controlCARD connector will be directly connected to GPIO-28.
S1	Reset switch: Switch connected to the XRSn line of the F28388D. Pressing this button will pull the device reset low.
S2	Boot Mode Switch: Controls the Boot Options of the F2838x device, see Table 3 . For a full description see the device datasheet.
S3	ADC VREFHI Control Switch for ADC modules A & B:
	<p>S3 Position 1 (upper switch) – VREFHI Control Switch for ADC module A:</p> <ul style="list-style-type: none"> • In the left position – ADC-A is configured to use VDDA (3.3 V) as the ADC's voltage reference. The full-scale range of this ADC will be 0-3.3 V, but the ADC will have reduced accuracy/precision. • In the right position – ADC-A is configured to either use a precise 3.0V voltage reference or an external voltage may be used as a reference. R47 and R48 determine which setting is used (see description for R47/R48, above) <p>S3 Position 2 (lower switch) – VREFHI Control Switch for ADC module B:</p> <ul style="list-style-type: none"> • In the left position – ADC-B is configured to use VDDA (3.3 V) as the ADC's voltage reference. The full-scale range of this ADC will be 0-3.3 V, but the ADC will have reduced accuracy/precision. • In the right position – ADC-B is configured to either use a precise 3.0V voltage reference or an external voltage may be used as a reference. R47 and R48 determine which setting is used (see description for R47/R48, above)
S4	ADC VREFHI Control Switch for ADC modules C & D:
	<p>S4 position 1 (upper switch) – VREFHI Control Switch for ADC module C:</p> <ul style="list-style-type: none"> • In the left position – ADC-C is configured to use VDDA (3.3 V) as the ADC's voltage reference. The full-scale range of this ADC will be 0-3.3 V, but the ADC will have reduced accuracy/precision. • In the right position – ADC-C is configured to either use a precise 3.0V voltage reference or an external voltage may be used as a reference. R47 and R48 determine which setting is used (see description for R47/R48, above) <p>S4Position 2 (lower switch) – VREFHI Control Switch for ADC module D:</p> <ul style="list-style-type: none"> • In the left position – ADC-D is configured to use VDDA (3.3 V) as the ADC's voltage reference. The full-scale range of this ADC will be 0-3.3 V, but the ADC will have reduced accuracy/precision. • In the right position – ADC-D is configured to either use a precise 3.0V voltage reference or an external voltage may be used as a reference. R47 and R48 determine which setting is used (see description for R47/R48, above).

Test Points	
TP1:A	Emulator 5.0 V input: This power domain is isolated from the other 5.0V domain.
TP2:A	Emulator 3.3 V input: This power domain is isolated from the other 3.3 V domains.
TP3:A	Emulator ground
TP1	ERRORSTS of F2838xD device
TP2	XRSn of F2838xD device: Connected to the under-voltage outputs from both the 1.2 V and 3.3 V voltage supervisors.
TP3	Over-voltage output: Connected to the over-voltage outputs from both the 1.2 V and 3.3 V voltage supervisors.
TP4	P0 PHY clock source
TP5	P1 PHY clock source
TP6	F2838xD clock source
TP7	HSEC 5.0 V input: 5.0 V input provided to the 3.3 V voltage regulator to create the unfiltered 3.3 V power.
TP8	Filtered 3.3 V: Provides power to the F2838xD device.
TP9	Filtered 1.2 V: Provides power to the F2838xD device.
TP10	Device Ground

NOTE: On the front of the controlCARD test points are indicated by their TPx number.
On the back of the controlCARD test points are indicated by their signal.

Table 3. S2, Bootmode Selection Table

Mode	Switch Position 1 (GPIO-84)	Switch Position 2 (GPIO-72)	Boot From
00	0 (right)	0 (right)	Parallel I/O
01	1 (left)	0 (right)	SCI/Wait Boot
02	0 (right)	1 (left)	CAN
03	1 (left)	1 (left)	Flash/USB

NOTE: S2 pulls the connected pin to a logic 0 when 'closed'. The 'ON' position of the switch indicates the 'closed' status of the switch NOT the logic level.

- S2 'ON' = Logic 0
- S2 'OFF' = Logic1

7 References

- Texas Instruments: [DP83826 Deterministic, Low-Latency, Low-Power, 10/100 Mbps, Industrial Ethernet PHY Data Sheet](#)

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from A Revision (September 2019) to B Revision	Page
• Updates were made in Section 1	2
• Added new Section 2	3
• Updates were made in Section 3	3
• Update was made in Section 3.2	3
• Updates was made in Section 3.3	4
• Updates were made in Section 4.1	4
• Added new Section 4.3.1	6
• Updates were made in Section 4.4	6
• Updates were made in Section 6	7

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