LM124AQML LM124QML Low Power Quad Operational Amplifiers

Check for Samples: LM124AQML, LM124QML

FEATURES

- **Available with Radiation Specification**
  - **High Dose Rate 100 krad(Si)**
  - **ELDRS Free 100 krad(Si)**
- **Internally Frequency Compensated for Unity Gain**
- **Large DC Voltage Gain 100 dB**
- **Wide Bandwidth (Unity Gain) 1 MHz (Temperature Compensated)**
- **Wide Power Supply Range:**
  - **Single Supply 3V to 32V**
  - **Or Dual Supplies ±1.5V to ±16V**
- **Very Low Supply Current Drain (700 µA) — Essentially Independent of Supply Voltage**
- **Low Input Biasing Current 45 nA (Temperature Compensated)**
- **Low Input Offset Voltage 2 mV and Offset Current: 5 nA**
- **Input Common-Mode Voltage Range Includes Ground**
- **Differential Input Voltage Range Equal to the Power Supply Voltage**
- **Large Output Voltage Swing 0V to V^+ − 1.5V**

DESCRIPTION

The LM124/124A consists of four independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, DC gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the LM124/124A can be directly operated off of the standard +5Vdc power supply voltage which is used in digital systems and will easily provide the required interface electronics without requiring the additional +15Vdc power supplies.

Unique Characteristics

- In the Linear Mode, the Input Common-Mode Voltage Rrange Includes Ground and the Output Voltage can also Swing to Ground, even though Operated from Only a Single Power Supply Voltage
- The Unity Gain Cross Frequency is Temperature Compensated
- The Input Bias Current is also Temperature Compensated

Advantages

- Eliminates Need for Dual Supplies
- Four Internally Compensated Op Amps in a Single Package
- Allows Directly Sensing near GND and V_{OUT} also Goes to GND
- Compatible with all Forms of Logic
- Power Drain Suitable for Battery Operation

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

LCCC Package

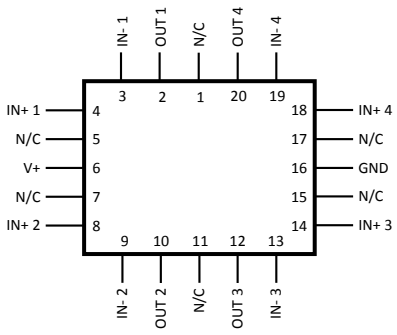


Figure 1. Package Number NAJ0020A

CDIP Package

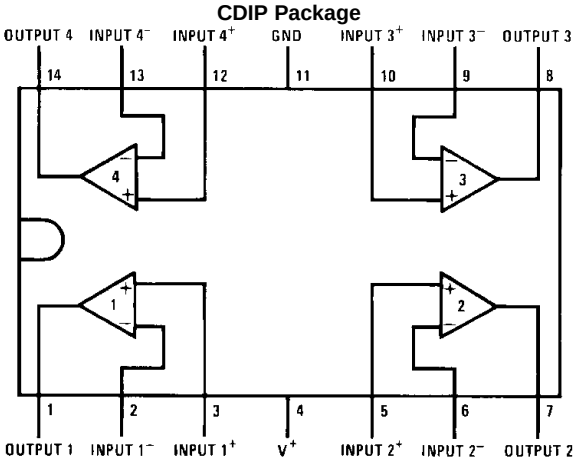


Figure 2. Top View
Package Number J0014A

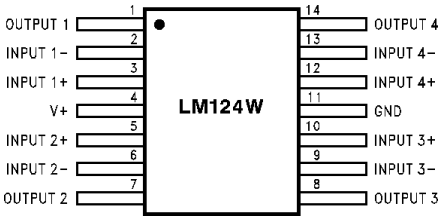
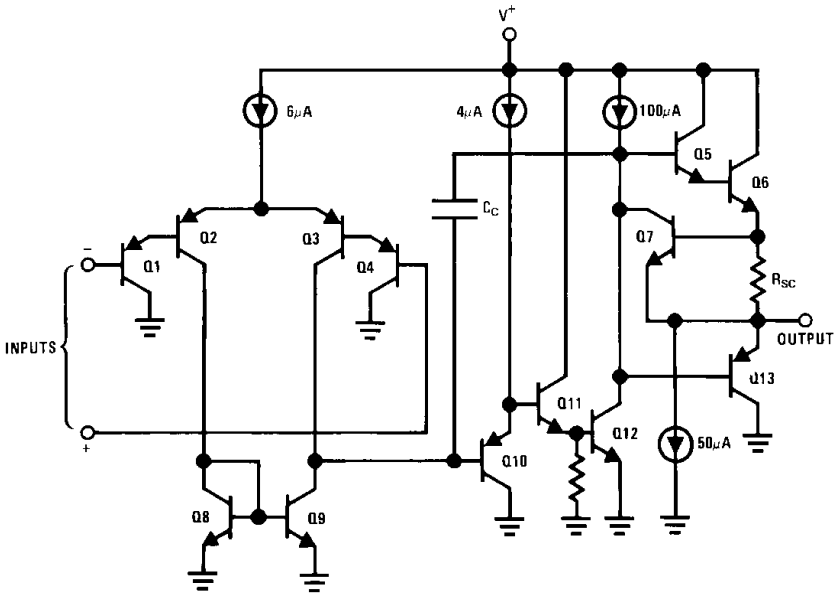


Figure 3. Package Number NAD0014B or NAC0014A

Schematic Diagram

(Each Amplifier)



Absolute Maximum Ratings (1)

Supply Voltage, V^+	32Vdc or ±16Vdc
Differential Input Voltage	32Vdc
Input Voltage	−0.3Vdc to +32Vdc
Input Current (V_{IN} < −0.3Vdc) (2)	50 mA
Power Dissipation (3)	
CDIP	1260mW
CLGA	700mW
LCCC	1350mW
CLGA	700mW
Output Short-Circuit to GND (One Amplifier) (4) V^+ ≤ 15Vdc and T_A = 25°C	Continuous
Operating Temperature Range	−55°C ≤ T_A ≤ +125°C
Maximum Junction Temperature	150°C
Storage Temperature Range	−65°C ≤ T_A ≤ +150°C
Lead Temperature (Soldering, 10 seconds)	260°C
Thermal Resistance ThetaJA	
CDIP (Still Air)	103°C/W
(500LF/Min Air flow)	51°C/W
CLGA (Still Air)	176°C/W
(500LF/Min Air flow)	116°C/W
LCCC (Still Air)	91°C/W
(500LF/Min Air flow)	66°C/W
CLGA (Still Air)	176°C/W
(500LF/Min Air flow)	116°C/W
ThetaJC	
CDIP	19°C/W
CLGA	18°C/W
LCCC	24°C/W
CLGA	18°C/W
Package Weight (Typical)	
CDIP	2200mg
CLGA	460mg
LCCC	470mg
CLGA	410mg
ESD Tolerance (5)	250V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

(2) This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the V+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than -0.3V_{DC} (at 25°C).

(3) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), ThetaJ_A (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is P_{Dmax} = (T_{Jmax} - T_A)/ThetaJ_A or the number given in the Absolute Maximum Ratings, whichever is lower.

(4) Short circuits from the output to V+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 40mA independent of the magnitude of V+. At values of supply voltage in excess of +15V_{DC}, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

(5) Human body model, 1.5 kΩ in series with 100 pF.

Quality Conformance Inspection

MIL-STD-883, Method 5005 - Group A

Subgroup	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

LM124/883 Electrical Characteristics SMD: 77043 DC Parameters

(The following conditions apply to all the following parameters, unless otherwise specified.)
All voltages referenced to device ground.

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-Groups
I_{CC}	Power Supply Current	V+ = 5V			1.2	mA	1, 2, 3
		V+ = 30V			3.0	mA	1
					4.0	mA	2, 3
I_{SINK}	Output Sink Current	V+ = 15V, V_{OUT} = 200mV, $+V_{IN}$ = 0mV, $-V_{IN}$ = +65mV		12		uA	1
		V+ = 15V, V_{OUT} = 2V, $+V_{IN}$ = 0mV, $-V_{IN}$ = +65mV		10		mA	1
				5		mA	2, 3
I_{SOURCE}	Output Source Current	V+ = 15V, V_{OUT} = 2V, $+V_{IN}$ = 0mV, $-V_{IN}$ = -65mV			-20	mA	1
					-10	mA	2, 3
I_{OS}	Short Circuit Current	V+ = 5V, V_{OUT} = 0V		-60		mA	1
V_{IO}	Input Offset Voltage	V+ = 30V, V_{CM} = 0V		-5	5	mV	1
				-7	7	mV	2, 3
		V+ = 30V, V_{CM} = 28V		-5	5	mV	1
				-7	7	mV	2, 3
		V+ = 5V, V_{CM} = 0V		-5	5	mV	1
				-7	7	mV	2, 3
		V+ = 30V, V_{CM} = 28.5V		-5	5	mV	1
CMRR	Common Mode Rejection Ratio	V+ = 30V, V_{IN} = 0V to 28.5V	(1)	70		dB	1
$+I_{IB}$	Input Bias Current	V+ = 5V, V_{CM} = 0V	(2)	-150	10	nA	1
				-300	10	nA	2, 3
I_{IO}	Input Offset Current	V+ = 5V, V_{CM} = 0V		-30	30	nA	1
				-100	100	nA	2, 3
PSRR	Power Supply Rejection Ratio	V+ = 5V to 30V, V_{CM} = 0V		65		dB	1
V_{CM}	Common Mode Voltage Range	V+ = 30V	(3) (1)		28.5	V	1
					28	V	2, 3
A_{VS}	Large Signal Gain	V+ = 15V, R_L = 2K Ω, V_O = 1V to 11V		50		V/mV	4
				25		V/mV	5, 6
V_{OH}	Output Voltage High	V+ = 30V, R_L = 2K Ω		26		V	4, 5, 6
		V+ = 30V, R_L = 10K Ω		27		V	4, 5, 6
V_{OL}	Output Voltage Low	V+ = 30V, R_L = 10K Ω			40	mV	4, 5, 6
		V+ = 30V, I_{SINK} = 1uA			40	mV	4
					100	mV	5, 6
		V+ = 5V, R_L= 10K Ω			20	mV	4, 5, 6
	Channel Separation (Amp to Amp Coupling)	1KHz, 20KHz	(4) (5)	80		dB	4

(1) The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V (at 25°C). The upper end of the common-mode voltage range is V+ −1.5V (at 25°C), but either or both inputs can go to +32V without damage independent of the magnitude of V+.
(2) The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
(3) Specified by V_{IO} tests.
(4) Ensured, not tested
(5) Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitance increases at higher frequencies.

LM124A/883 Electrical Characteristics SMD: 77043 DC Parameters

(The following conditions apply to all the following parameters, unless otherwise specified.)
All voltages referenced to device ground.

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-Groups
I_{CC}	Power Supply Current	V+ = 5V			1.2	mA	1, 2, 3
		V+ = 30V			3.0	mA	1
					4.0	mA	2, 3
I_{SINK}	Output Sink Current	V+ = 15V, V_{OUT} = 200mV, $+V_{IN}$ = 0mV, $-V_{IN}$ = +65mV		12		uA	1
		V+ = 15V, V_{OUT} = 2V, $+V_{IN}$ = 0mV, $-V_{IN}$ = +65mV		10		mA	1
				5		mA	2, 3
I_{SOURCE}	Output Source Current	V+ = 15V, V_{OUT} = 2V, $+V_{IN}$ = 0mV, $-V_{IN}$ = -65mV			-20	mA	1
					-10	mA	2, 3
I_{OS}	Short Circuit Current	V+ = 5V, V_{OUT} = 0V		-60		mA	1
V_{IO}	Input Offset Voltage	V+ = 30V, V_{CM} = 0V		-2	2	mV	1
				-4	4	mV	2, 3
		V+ = 30V, V_{CM} = 28.5V		-2	2	mV	1
		V+ = 30V, V_{CM} = 28V		-4	4	mV	2, 3
		V+ = 5V, V_{CM} = 0V		-2	2	mV	1
				-4	4	mV	2, 3
CMRR	Common Mode Rejection Ratio	V+ = 30V, V_{IN} = 0V to 28.5V	(1)	70		dB	1
$\pm I_{IB}$	Input Bias Current	V+ = 5V, V_{CM} = 0V	(2)	-50	10	nA	1
				-100	10	nA	2, 3
I_{IO}	Input Offset Current	V+ = 5V, V_{CM} = 0V		-10	10	nA	1
				-30	30	nA	2, 3
PSRR	Power Supply Rejection Ratio	V+ = 5V to 30V, V_{CM} = 0V		65		dB	1
V_{CM}	Common Mode Voltage Range	V+ = 30V	(3) (1)		28.5	V	1
					28	V	2, 3
A_{VS}	Large Signal Gain	V+ = 15V, R_L = 2K Ω, V_O = 1V to 11V	(4)	50		V/mV	4
				25		V/mV	5, 6
V_{OH}	Output Voltage High	V+ = 30V, R_L = 2K Ω		26		V	4, 5, 6
		V+ = 30V, R_L = 10K Ω		27		V	4, 5, 6
V_{OL}	Output Voltage Low	V+ = 30V, R_L = 10K Ω			40	mV	4, 5, 6
		V+ = 30V, I_{SINK} = 1uA			40	mV	4
					100	mV	5, 6
		V+ = 5V, R_L = 10K Ω			20	mV	4, 5, 6
	Channel Separation Amp to Amp Coupling	1KHz, 20KHz	(5) (6)	80		dB	4

(1) The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V (at 25°C). The upper end of the common-mode voltage range is V+ −1.5V (at 25°C), but either or both inputs can go to +32V without damage independent of the magnitude of V+.
(2) The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
(3) Specified by V_{IO} tests.
(4) Datalog reading in K=V/mV
(5) Ensured, not tested
(6) Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitance increases at higher frequencies.

LM124A RAD HARD Electrical Characteristics SMD: 5962R99504 DC Parameters(1) (2)

(The following conditions apply to all the following parameters, unless otherwise specified.)

All voltages referenced to device ground.

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-Groups
V_{IO}	Input Offset Voltage	V_{CC}+ = 30V, V_{CC}- = Gnd, V_{CM} = +15V		-2	2	mV	1
				-4	4	mV	2, 3
		V_{CC}+ = 2V, V_{CC}- = -28V, V_{CM} = -13V		-2	2	mV	1
				-4	4	mV	2, 3
		V_{CC}+ = 5V, V_{CC}- = Gnd, V_{CM} = +1.4V		-2	2	mV	1
				-4	4	mV	2, 3
		V_{CC}+ = 2.5V, V_{CC}- = -2.5, V_{CM} = -1.1V		-2	2	mV	1
				-4	4	mV	2, 3
I_{IO}	Input Offset Current	V_{CC}+ = 30V, V_{CC}- = Gnd, V_{CM} = +15V		-10	10	nA	1, 2
				-30	30	nA	3
		V_{CC}+ = 2V, V_{CC}- = -28V, V_{CM} = -13V		-10	10	nA	1, 2
				-30	30	nA	3
		V_{CC}+ = 5V, V_{CC}- = Gnd, V_{CM} = +1.4V		-10	10	nA	1, 2
				-30	30	nA	3
		V_{CC}+ = 2.5V, V_{CC}- = -2.5, V_{CM} = -1.1V		-10	10	nA	1, 2
				-30	30	nA	3
$\pm I_{IB}$	Input Bias Current	V_{CC}+ = 30V, V_{CC}- = Gnd, V_{CM} = +15V	(3)	-50	+0.1	nA	1, 2
				-100	+0.1	nA	3
		V_{CC}+ = 2V, V_{CC}- = -28V, V_{CM} = -13V		-50	+0.1	nA	1, 2
				-100	+0.1	nA	3
		V_{CC}+ = 5V, V_{CC}- = Gnd, V_{CM} = +1.4V		-50	+0.1	nA	1, 2
				-100	+0.1	nA	3
		V_{CC}+ = 2.5V, V_{CC}- = -2.5, V_{CM} = -1.1V		-50	+0.1	nA	1, 2
				-100	+0.1	nA	3
+PSRR	Power Supply Rejection Ratio	V_{CC}- = Gnd, V_{CM} = +1.4V, 5V ≤ V_{CC} ≤ 30V		-100	100	uV/V	1, 2, 3
CMRR	Common Mode Rejection Ratio		(4)	76		dB	1, 2, 3
I_{OS}+	Output Short Circiut Current	V_{CC}+ = 30V, V_{CC}- = Gnd, V_O = 25V		-70		mA	1, 2,3
I_{CC}	Power Supply Current	V_{CC}+ = 30V, V_{CC}- = Gnd			3	mA	1, 2
					4	mA	3
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Sensitivity	+25°C ≤ T_A ≤ +125°C, +V_{CC} = 5V, -V_{CC} = 0V, V_{CM} = +1.4V	(5)	-30	30	uV/ °C	2
		-55°C ≤ T_A ≤ +25°C, +V_{CC} = 5V, -V_{CC} = 0V, V_{CM} = +1.4V		-30	30	uV/ °C	3

(1) Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics except as listed in the Post Radiation Limits Table. These parts may be dose rate sensitive in a space environment and demonstrate enhanced low dose rate effect. Radiation end point limits for the noted parameters are ensured only for the conditions as specified in MIL-STD-883, Method 1019

(2) Low dose rate testing has been performed on a wafer-by-wafer basis, per test method 1019 condition D of MIL-STD-883, with no enhanced low dose rate sensitivity (ELDRS) effect.

(3) The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.

(4) The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V (at 25°C). The upper end of the common-mode voltage range is V+ −1.5V (at 25°C), but either or both inputs can go to +32V without damage independent of the magnitude of V+.

(5) Calculated parameters

LM124A RAD HARD Electrical Characteristics SMD: 5962R99504 DC Parameters(1) (2) (continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
All voltages referenced to device ground.

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-Groups
$\Delta_{IO}/\Delta T$	Input Offset Current Temperature Sensitivity	+25°C ≤ T_A ≤ +125°C, +V_{CC} = 5V, -V_{CC} = 0V, V_{CM} = +1.4V	(5)	-400	400	pA/° C	2
		-55°C ≤ T_A ≤ +25°C, +V_{CC} = 5V, -V_{CC} = 0V, V_{CM} = +1.4V		-700	700	pA/ °C	3

LM124A RAD HARD SMD: 5962R99504 AC/DC Parameters(1) (2)

(The following conditions apply to all the following parameters, unless otherwise specified.)
All voltages referenced to device ground.

Symbol	Parameter	Conditions	Notes	Min	Max	UniT	Sub-G roups
V_{OL}	Logical "0" Output Voltage	V_{CC}+ = 30V, V_{CC}- = Gnd, R_L = 10K Ω			35	mV	4, 5, 6
		V_{CC}+ = 30V, V_{CC}- = Gnd, I_{OI} = 5mA			1.5	V	4, 5, 6
		V_{CC}+ = 4.5V, V_{CC}- = Gnd, I_{OI} = 2uA			0.4	V	4, 5, 6
V_{OH}	Logical "1" Output Voltage	V_{CC}+ = 30V, V_{CC}- = Gnd, I_{OH} = -10mA		27		V	4, 5, 6
		V_{CC}+ = 4.5V, V_{CC}- = Gnd, I_{OH} = -10mA		2.4		V	4, 5, 6
A_{VS}+	Voltage Gain	V_{CC}+ = 30V, V_{CC}- = Gnd, 1V ≤ V_O ≤ 26V, R_L = 10K Ω		50		V/mV	4
				25		V/mV	5, 6
		V_{CC}+ = 30V, V_{CC}- = Gnd, 5V ≤ V_O ≤ 20V, R_L = 2K Ω		50		V/mV	4
				25		V/mV	5, 6
A_{VS}	Voltage Gain	V_{CC}+ = 5V, V_{CC}- = Gnd, 1V ≤ V_O ≤ 2.5V, R_L = 10K Ω		10		V/mV	4, 5, 6
		V_{CC}+ = 5V, V_{CC}- = Gnd, 1V ≤ V_O ≤ 2.5V, R_L = 2K Ω		10		V/mV	4, 5, 6
+V_{OP}	Maximum Output Voltage Swing	V_{CC}+ = 30V, V_{CC}- = Gnd, V_O = +30V, R_L = 10K Ω		27		V	4, 5, 6
		V_{CC}+ = 30V, V_{CC}- = Gnd, V_O = +30V, R_L = 2K Ω		26		V	4, 5, 6
TR($_{TR}$)	Transient Response: Rise Time	V_{CC}+ = 30V, V_{CC}- = Gnd			1	uS	7, 8A, 8B
TR($_{OS}$)	Transient Response: Overshoot	V_{CC}+ = 30V, V_{CC}- = Gnd			50	%	7, 8A, 8B
±S_R	Slew Rate: Rise	V_{CC}+ = 30V, V_{CC}- = Gnd		0.1		V/uS	7, 8A, 8B
	Slew Rate: Fall	V_{CC}+ = 30V, V_{CC}- = Gnd		0.1		V/uS	7, 8A, 8B

(1) Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics except as listed in the Post Radiation Limits Table. These parts may be dose rate sensitive in a space environment and demonstrate enhanced low dose rate effect. Radiation end point limits for the noted parameters are ensured only for the conditions as specified in MIL-STD-883, Method 1019
(2) Low dose rate testing has been performed on a wafer-by-wafer basis, per test method 1019 condition D of MIL-STD-883, with no enhanced low dose rate sensitivity (ELDRS) effect.

LM124A RAD HARD SMD: 5962R99504 AC Parameters (1) (2)

(The following conditions apply to all the following parameters, unless otherwise specified.)

AC: $+V_{CC}$ = 30V, $-V_{CC}$ = 0V

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-Groups
NI_{BB}	Noise Broadband	$+V_{CC}$ = 15V, $-V_{CC}$ = -15V, BW = 10Hz to 5KHz			15	uVrm s	7
NI_{PC}	Noise Popcorn	$+V_{CC}$ = 15V, $-V_{CC}$ = -15V, R_S = 20K Ω, BW = 10Hz to 5KHz			50	uVpK	7
C_S	Channel Separation	$+V_{CC}$ = 30V, $-V_{CC}$ = Gnd, R_L = 2K Ω	(3)	80		dB	7
		R_L = 2K Ω, V_{IN} = 1V and 16V, A to B		80		dB	7
		R_L = 2K Ω, V_{IN} = 1V and 16V, A to C		80		dB	7
		R_L = 2K Ω, V_{IN} = 1V and 16V, A to D		80		dB	7
		R_L = 2K Ω, V_{IN} = 1V and 16V, B to A		80		dB	7
		R_L = 2K Ω, V_{IN} = 1V and 16V, B to C		80		dB	7
		R_L = 2K Ω, V_{IN} = 1V and 16V, B to D		80		dB	7
		R_L = 2K Ω, V_{IN} = 1V and 16V, C to A		80		dB	7
		R_L = 2K Ω, V_{IN} = 1V and 16V, C to B		80		dB	7
		R_L = 2K Ω, Vin = 1V and 16V, C to D		80		dB	7
		R_L = 2K Ω, V_{IN} = 1V and 16V, D to A		80		dB	7
		R_L = 2K Ohms, V_{IN} = 1V and 16V, D to B		80		dB	7
		R_L = 2K Ω, Vin = 1V and 16V, D to C		80		dB	7

(1) Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics except as listed in the Post Radiation Limits Table. These parts may be dose rate sensitive in a space environment and demonstrate enhanced low dose rate effect. Radiation end point limits for the noted parameters are ensured only for the conditions as specified in MIL-STD-883, Method 1019

(2) Low dose rate testing has been performed on a wafer-by-wafer basis, per test method 1019 condition D of MIL-STD-883, with no enhanced low dose rate sensitivity (ELDRS) effect.

(3) Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitance increases at higher frequencies.

LM124A RAD HARD - DC Drift Values SMD: 5962R99504 (1) (2)

(The following conditions apply to all the following parameters, unless otherwise specified.)

DC: "Delta calculations performed on QMLV devices at group B, subgroup 5 only"

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-Groups
V_{IO}	Input Offset Voltage	V_{CC}+ = 30V, V_{CC}- = Gnd, V_{CM} = +15V		-0.5	0.5	mV	1
$\pm I_{IB}$	Input Bias Current	V_{CC}+ = 30V, V_{CC}- = Gnd, V_{CM} = +15V		-10	10	nA	1

(1) Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics except as listed in the Post Radiation Limits Table. These parts may be dose rate sensitive in a space environment and demonstrate enhanced low dose rate effect. Radiation end point limits for the noted parameters are ensured only for the conditions as specified in MIL-STD-883, Method 1019

(2) Low dose rate testing has been performed on a wafer-by-wafer basis, per test method 1019 condition D of MIL-STD-883, with no enhanced low dose rate sensitivity (ELDRS) effect.

LM124A - POST RADIATION LIMITS +25°C SMD: 5962R99504 (1) (2)

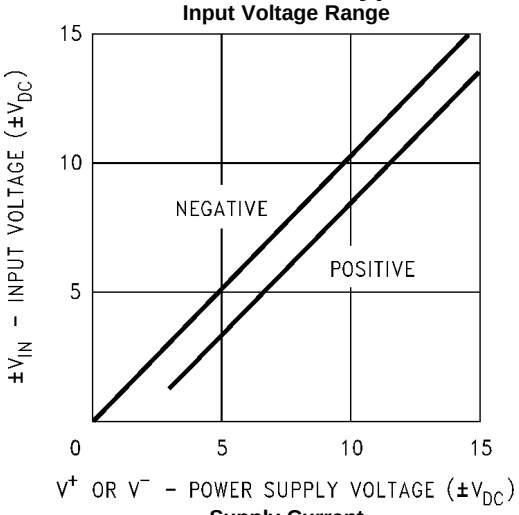
(The following conditions apply to all the following parameters, unless otherwise specified.)
All voltages referenced to device ground.

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-Groups
V_{IO}	Input Offset Voltage	V_{CC}+ = 30V, V_{CC}- = Gnd, V_{CM} = +15V	(1)	-2.5	2.5	mV	1
		V_{CC}+ = 2V, V_{CC}- = -28V, V_{CM} = -13V		-2.5	2.5	mV	1
		V_{CC}+ = 5V, V_{CC}- = Gnd, V_{CM} = +1.4V		-2.5	2.5	mV	1
		V_{CC}+ = 2.5V, V_{CC}- = -2.5, V_{CM} = -1.1V		-2.5	2.5	mV	1
I_{IO}	Input Offset Current	V_{CC}+ = 30V, V_{CC}- = Gnd, V_{CM} = +15V	(1)	-15	15	nA	1
		V_{CC}+ = 2V, V_{CC}- = -28V, V_{CM} = -13V		-15	15	nA	1
		V_{CC}+ = 5V, V_{CC}- = Gnd, V_{CM} = +1.4V		-15	15	nA	1
		V_{CC}+ = 2.5V, V_{CC}- = -2.5V, V_{CM} = -1.1V		-15	15	nA	1
$\pm I_{IB}$	Input Bias Current	V_{CC}+ = 30V, V_{CC}- = Gnd, V_{CM} = +15V	(1)	-75	+0.1	nA	1
		V_{CC}+ = 2V, V_{CC}- = -28V, V_{CM} = -13V		-75	+0.1	nA	1
		V_{CC}+ = 5V, V_{CC}- = Gnd, V_{CM} = +1.4V		-75	+0.1	nA	1
		V_{CC}+ = 2.5V, V_{CC}- = -2.5V, V_{CM} = -1.1V		-75	+0.1	nA	1
A_{VS}+	Voltage Gain	V_{CC}+ = 30V, V_{CC}- = Gnd, 1V ≤ V_O ≤ 26V, R_L = 10K Ω	(1)	40		V/mV	4
		V_{CC}+ = 30V, V_{CC}- = Gnd, 5V ≤ V_O ≤ 20V, R_L = 2K Ω		40		V/mV	4

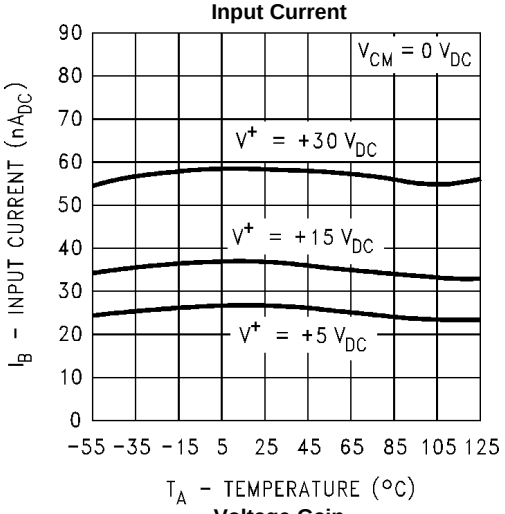
(1) Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics except as listed in the Post Radiation Limits Table. These parts may be dose rate sensitive in a space environment and demonstrate enhanced low dose rate effect. Radiation end point limits for the noted parameters are ensured only for the conditions as specified in MIL-STD-883, Method 1019
(2) Low dose rate testing has been performed on a wafer-by-wafer basis, per test method 1019 condition D of MIL-STD-883, with no enhanced low dose rate sensitivity (ELDRS) effect.

Typical Performance Characteristics

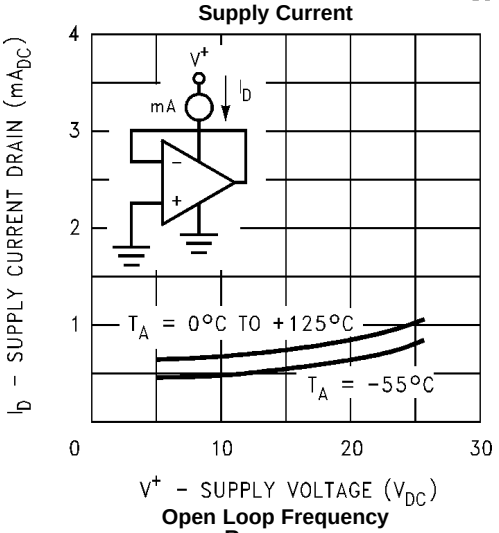
Input Voltage Range



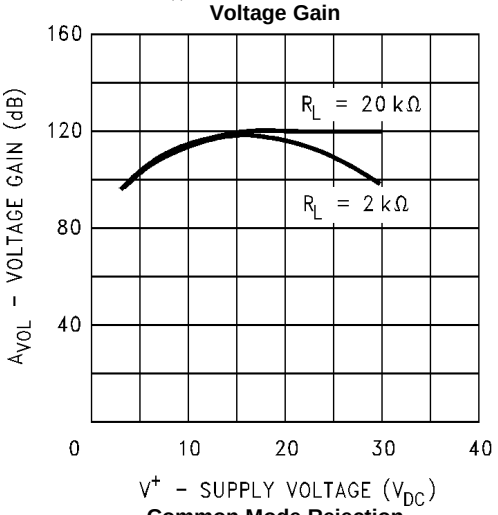
Input Current



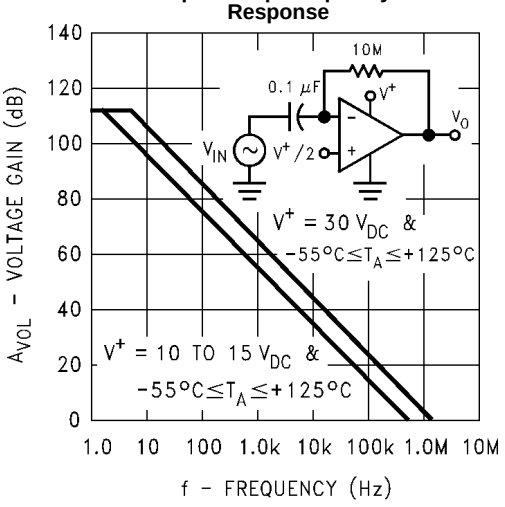
Supply Current



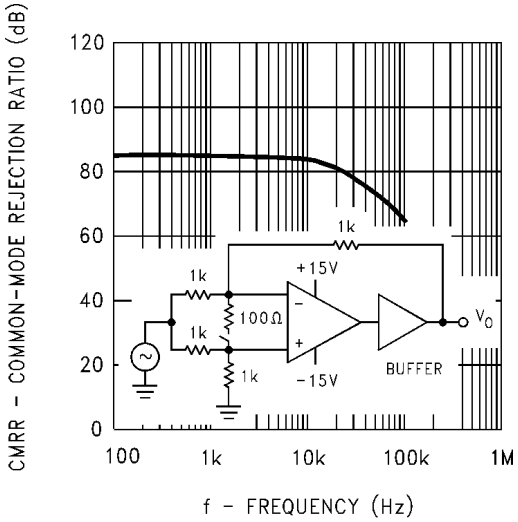
Voltage Gain



Open Loop Frequency Response

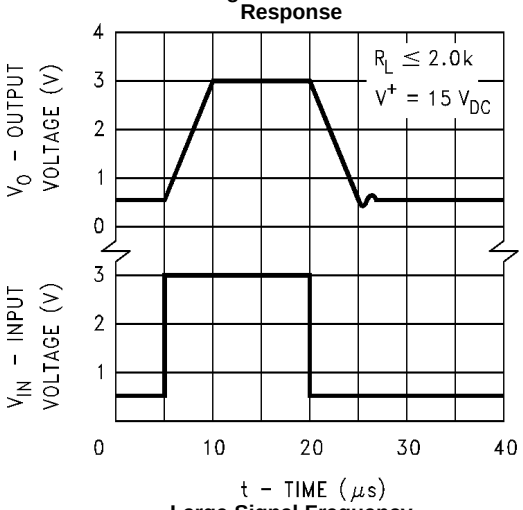


Common Mode Rejection Ratio

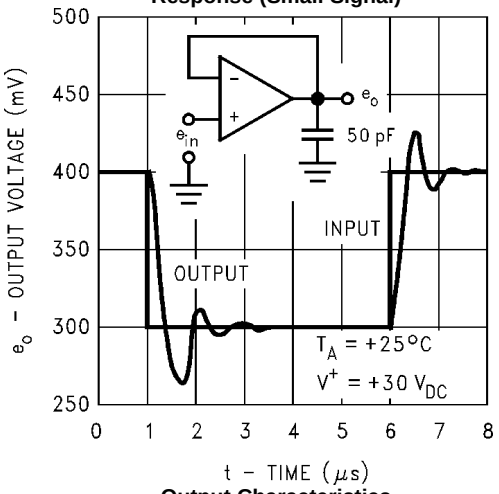


Typical Performance Characteristics (continued)

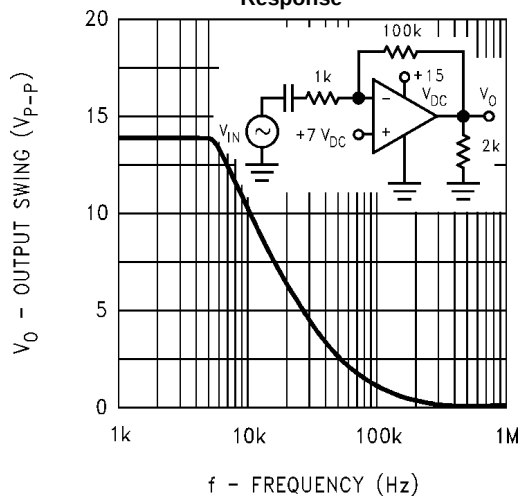
Voltage Follower Pulse Response



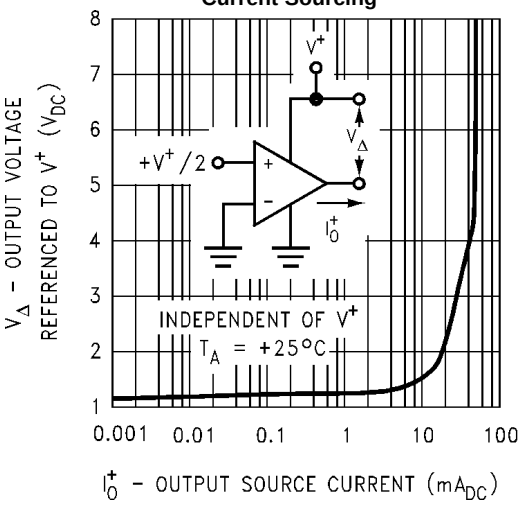
Voltage Follower Pulse Response (Small Signal)



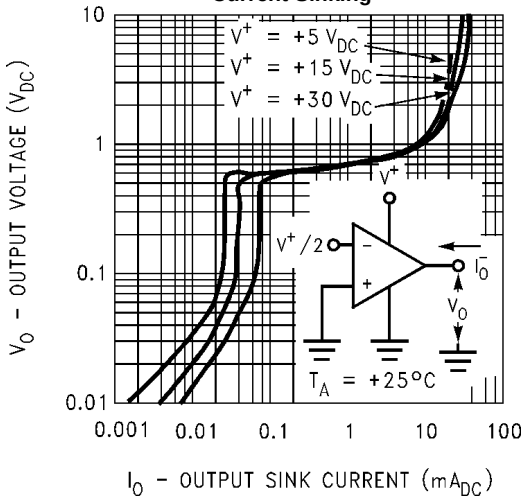
Large Signal Frequency Response



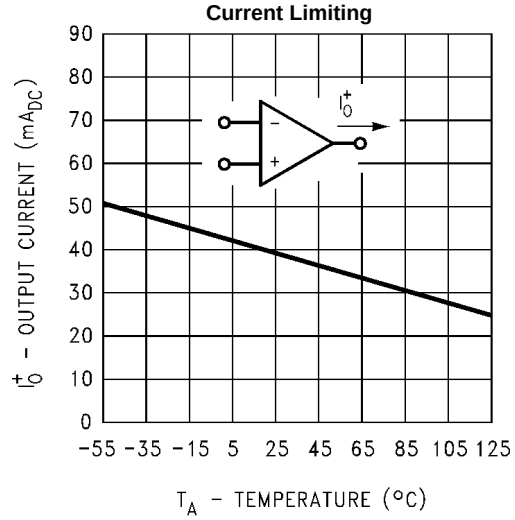
Output Characteristics Current Sourcing



Output Characteristics Current Sinking



Current Limiting



APPLICATION INFORMATION

LM124 Series Operational Amplifiers

The LM124 series are op amps which operate with only a single power supply voltage, have true-differential inputs, and remain in the linear mode with an input common-mode voltage of 0 V_{DC}. These amplifiers operate over a wide range of power supply voltage with little change in performance characteristics. At 25°C amplifier operation is possible down to a minimum supply voltage of 2.3 V_{DC}.

The pinouts of the package have been designed to simplify PC board layouts. Inverting inputs are adjacent to outputs for all of the amplifiers and the outputs have also been placed at the corners of the package (pins 1, 7, 8, and 14).

Precautions should be taken to insure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a test socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Large differential input voltages can be easily accommodated and, as input differential voltage protection diodes are not needed, no large input currents result from large differential input voltages. The differential input voltage may be larger than V^+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than −0.3 V_{DC} (at 25°C). An input clamp diode with a resistor to the IC input terminal can be used.

To reduce the power supply drain, the amplifiers have a class A output stage for small signal levels which converts to class B in a large signal mode. This allows the amplifiers to both source and sink large output currents. Therefore both NPN and PNP external current boost transistors can be used to extend the power capability of the basic amplifiers. The output voltage needs to raise approximately 1 diode drop above ground to bias the on-chip vertical PNP transistor for output current sinking applications.

For ac applications, where the load is capacitively coupled to the output of the amplifier, a resistor should be used, from the output of the amplifier to ground to increase the class A bias current and prevent crossover distortion.

Where the load is directly coupled, as in dc applications, there is no crossover distortion.

Capacitive loads which are applied directly to the output of the amplifier reduce the loop stability margin. Values of 50 pF can be accommodated using the worst-case non-inverting unity gain connection. Large closed loop gains or resistive isolation should be used if larger load capacitance must be driven by the amplifier.

The bias network of the LM124 establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 3 V_{DC} to 30 V_{DC}.

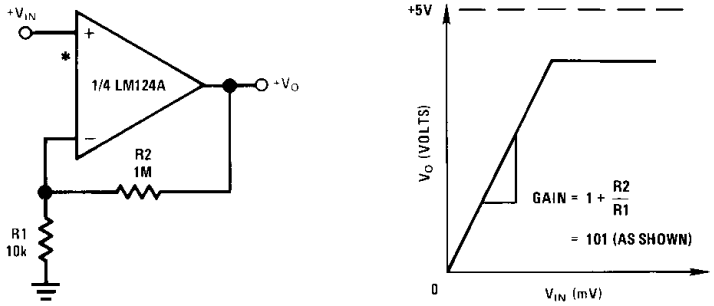
Output short circuits either to ground or to the positive power supply should be of short time duration. Units can be destroyed, not as a result of the short circuit current causing metal fusing, but rather due to the large increase in IC chip dissipation which will cause eventual failure due to excessive junction temperatures. Putting direct short-circuits on more than one amplifier at a time will increase the total IC power dissipation to destructive levels, if not properly protected with external dissipation limiting resistors in series with the output leads of the amplifiers. The larger value of output source current which is available at 25°C provides a larger output current capability at elevated temperatures (see typical performance characteristics) than a standard IC op amp.

The circuits presented in the section on typical applications emphasize operation on only a single power supply voltage. If complementary power supplies are available, all of the standard op amp circuits can be used. In general, introducing a pseudo-ground (a bias voltage reference of $V^+/2$) will allow operation above and below this value in single power supply systems. Many application circuits are shown which take advantage of the wide input common-mode voltage range which includes ground. In most cases, input biasing is not required and input voltages which range to ground can easily be accommodated.

Typical Single-Supply Applications

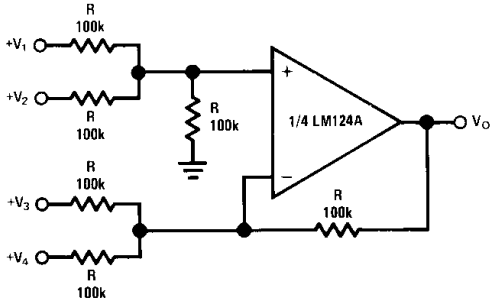
(V^+ = 5.0 V_{DC})

Non-Inverting DC Gain (0V Input = 0V Output)



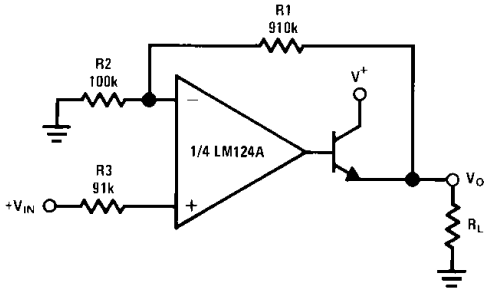
*R not needed due to temperature independent I_{IN}

DC Summing Amplifier
(V_{IN}'S ≥ 0 V_{DC} and V_O ≥ V_{DC})



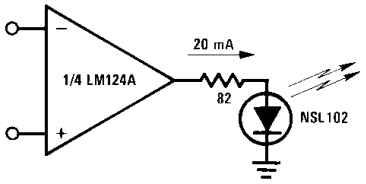
Where: $V_0 = V_1 + V_2 - V_3 - V_4$
$(V_1 + V_2) \geq (V_3 + V_4)$ to keep $V_O > 0$ V_{DC}

Power Amplifier

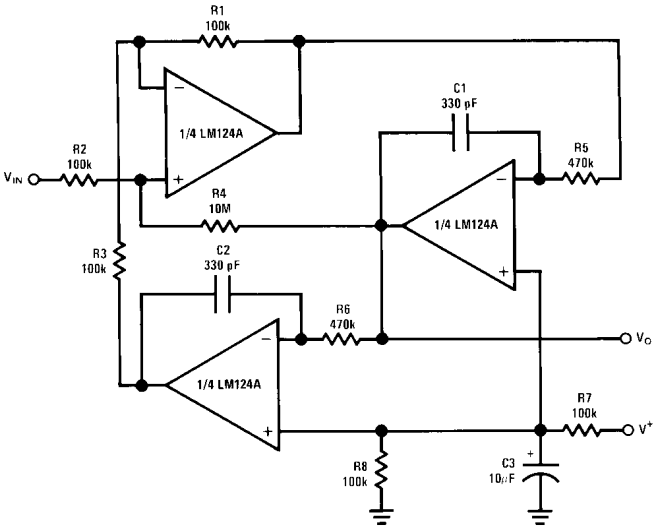


V_0 = 0 V_{DC} for V_{IN} = 0 V_{DC}
A_V = 10

LED Driver



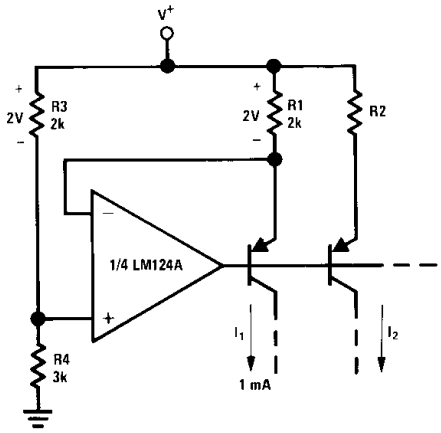
"BI-QUAD" RC Active Bandpass Filter



f_o = 1 kHz
Q = 50
A_V = 100 (40 dB)

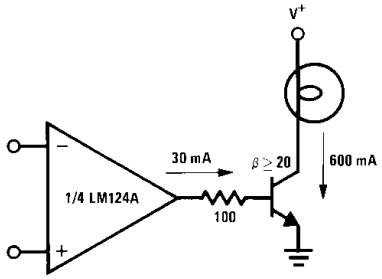
(V^+ = 5.0 V_{DC})

Fixed Current Sources

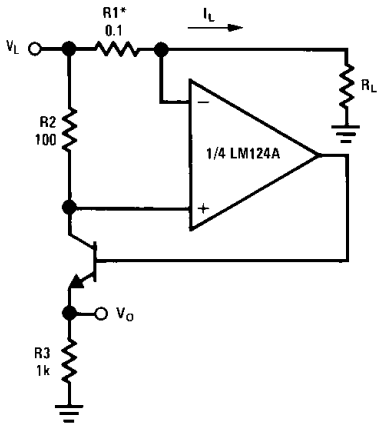


$I_2 = \left(\frac{R1}{R2}\right) I_1$

Lamp Driver



Current Monitor

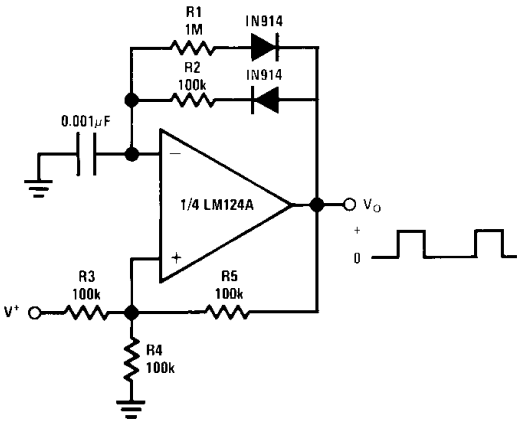


$V_O = \frac{1V(I_L)}{1A}$

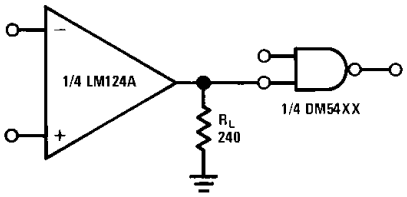
$V_L \leq V^+ - 2V$

*(Increase R1 for I_L small)

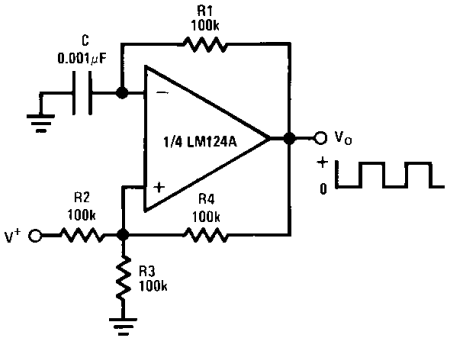
Pulse Generator



Driving TTL

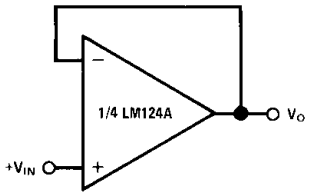


Squarewave Oscillator

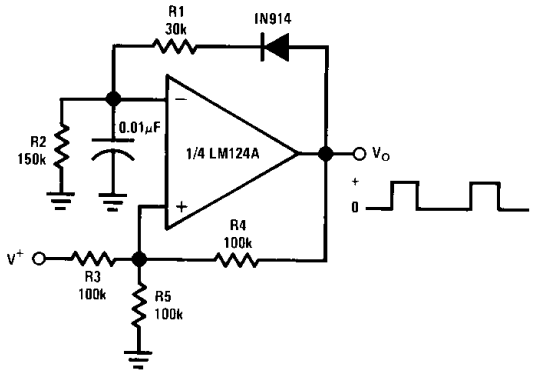


(V^+ = 5.0 V_{DC})

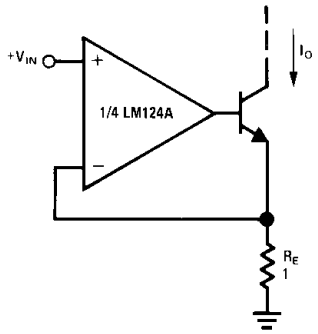
Voltage Follower



Pulse Generator

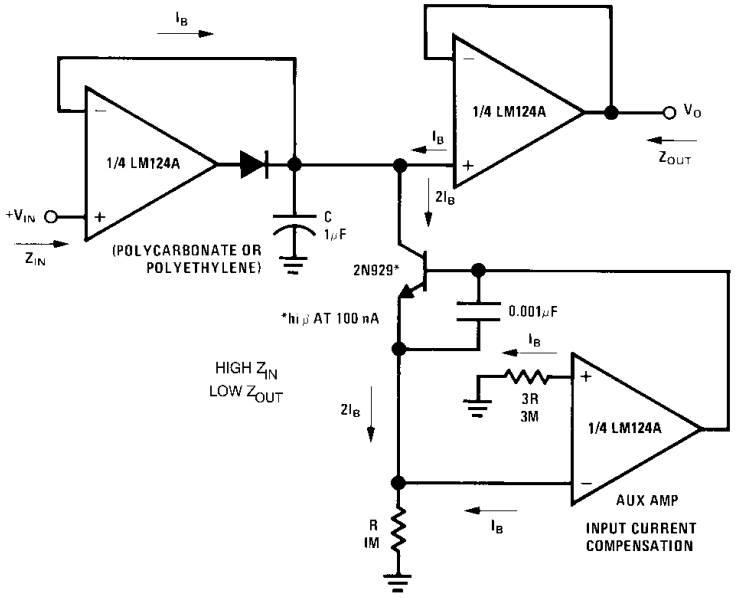


High Compliance Current Sink



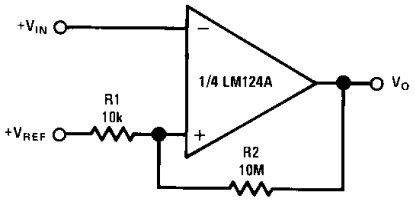
I_O = 1 amp/volt V_{IN}
(Increase R_E for I_o small)

Low Drift Peak Detector

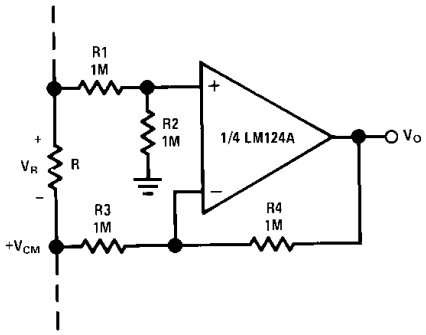


(V^+ = 5.0 V_{DC})

Comparator with Hysteresis

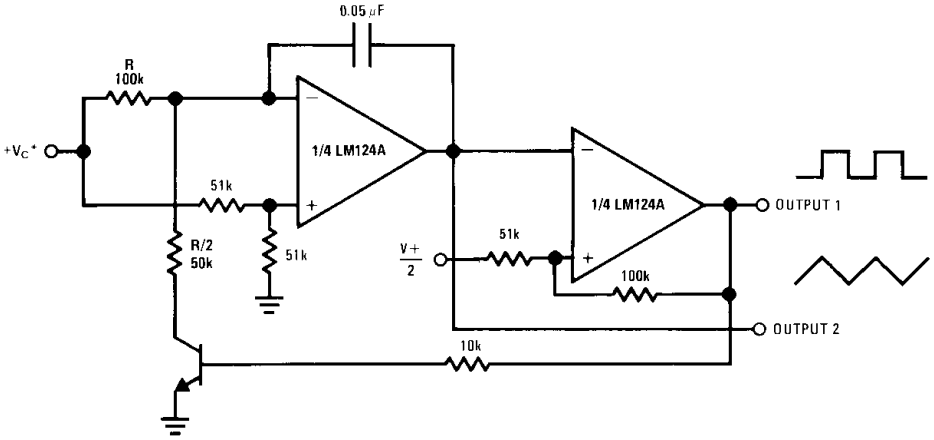


Ground Referencing a Differential Input Signal



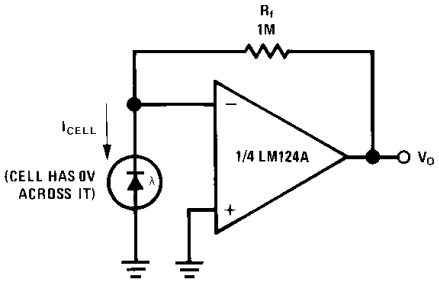
$V_O = V_R$

Voltage Controlled Oscillator Circuit



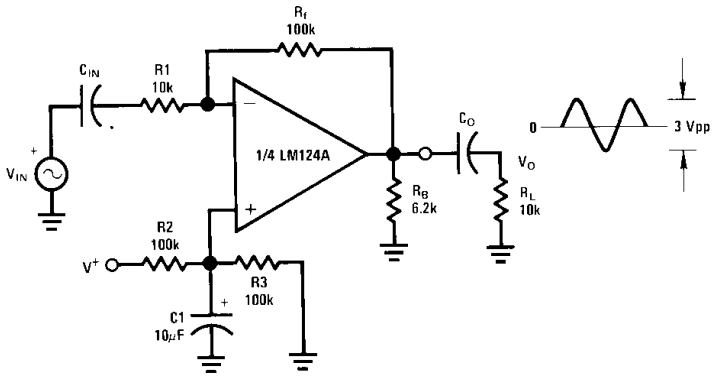
*Wide control voltage range: 0 $V_{DC} \leq V_C \leq 2$ ($V^+ - 1.5$ V_{DC})

Photo Voltaic-Cell Amplifier



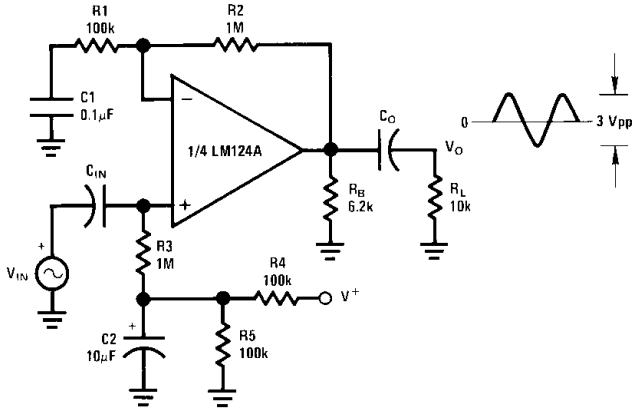
(V^+ = 5.0 V_{DC})

AC Coupled Inverting Amplifier



$A_V = \frac{R_f}{R1}$ (As shown, A_V = 10)

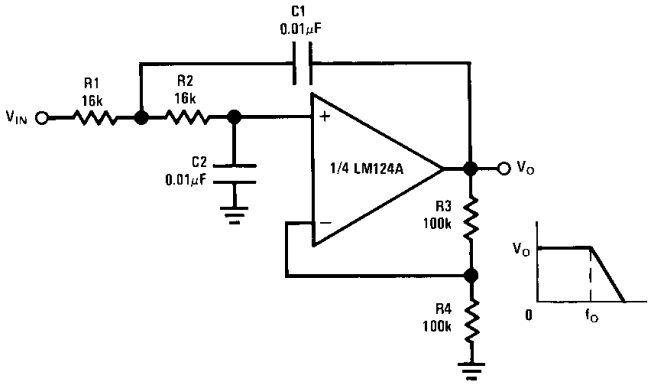
AC Coupled Non-Inverting Amplifier



$A_V = 1 + \frac{R2}{R1}$

A_V = 11 (As shown)

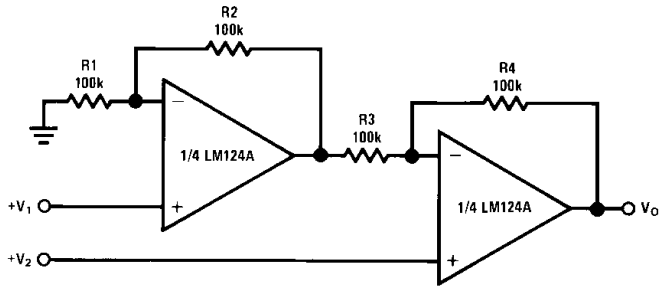
DC Coupled Low-Pass RC Active Filter



f_O = 1 kHz
Q = 1
A_V = 2

(V^+ = 5.0 V_{DC})

High Input Z, DC Differential Amplifier

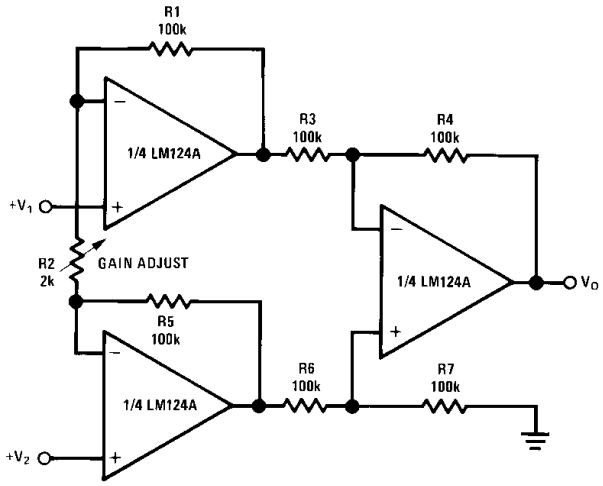


For $\frac{R1}{R2} = \frac{R4}{R3}$ (CMRR depends on this resistor ratio match)

$V_O = 1 + \frac{R4}{R3}(V_2 - V_1)$

As shown: $V_O = 2(V_2 - V_1)$

High Input Z Adjustable-Gain DC Instrumentation Amplifier



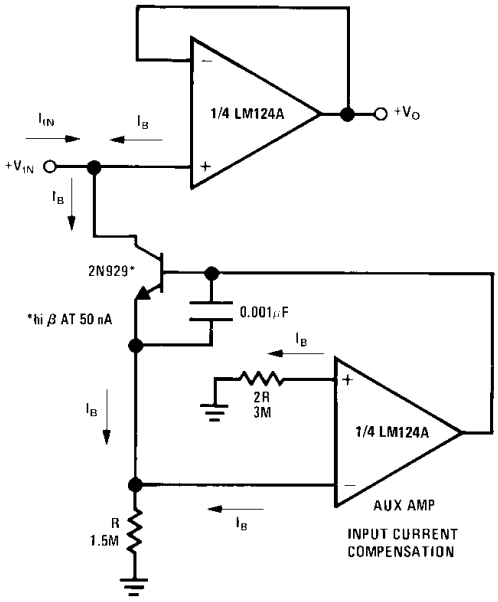
If R1 = R5 & R3 = R4 = R6 = R7 (CMRR depends on match)

$V_O = 1 + \frac{2R1}{R2}(V_2 - V_1)$

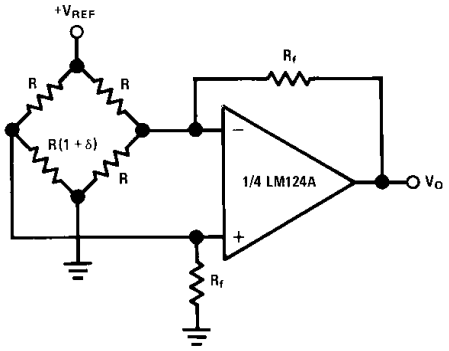
As shown $V_O = 101\,(V_2 - V_1)$

(V^+ = 5.0 V_{DC})

Using Symmetrical Amplifiers to Reduce Input Current (General Concept)



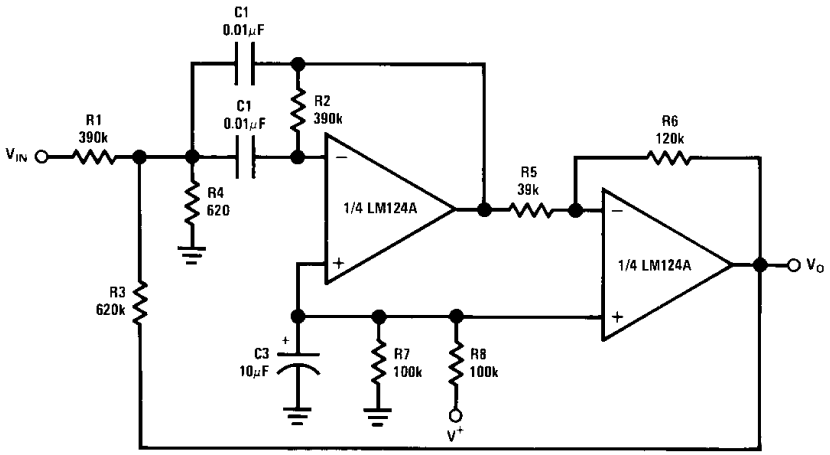
Bridge Current Amplifier



For $\delta << 1$ and $R_f >> R$

$$V_O \cong V_{REF}\left(\frac{\delta}{2}\right)\frac{R_f}{R}$$

Bandpass Active Filter



f_O = 1 kHz
Q = 25

REVISION HISTORY

Date Released	Revision	Section	Changes
9/2/04	A	New Release, Corporate format	3 MDS data sheets converted into one Corp. data sheet format. MNLM124-X, Rev. 1A2, MNLM124A-X, Rev. 1A3 and MRLM124A-X-RH, Rev. 5A0. MDS data sheets will be archived.
01/27/05	B	Connection Diagrams, Quality Conformance Inspection Section, and Physical Dimensions drawings	Added E package Connection Diagram. Changed verbiage under Quality Conformance Title, and Updated Revisions for the Marketing Drawings.
04/18/05	C	Update Absolute Maximum Ratings Section	Corrected typo for Supply Voltage limit From: 32Vdc or +16Vdc TO: 32Vdc or ±16Vdc. Added cerpack, cerdip, LCC package weight.
06/16/06	D	Features, Ordering Information Table, Rad Hard Electrical Section and Notes	Added Available with Radiation Specification, Low Dose NSID's to table 5962R9950402VCA LM124AJRLQMLV, 5962R9950402VDA LM124AWRLQMLV, 5962R9950402VZA LM124AWGRLQMLV, and reference to Note 10 and 11. Deleted code K NSID's LM124AJLQMLV 5962L9950401VCA, LM124AWGLQMLV 5962L9950401VZA, LM124AWLQMLV 5962L9950401VDA, Note 11 to Rad Hard Electrical Heading. Note 11 to Notes.
10/07/2010	E	Data sheet title, Features, Ordering table, Electrical characteristic headings, Rad Hard conditions	Update with current device information and format. Revision D will be Archived
03/26/2013	K	All Sections	Changed layout of National Data Sheet to TI format

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962R9950401V9A	ACTIVE	DIESALE	Y	0	30	RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125		Samples
5962R9950401VCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	LM124AJRQMLV 5962R9950401VCA Q	Samples
5962R9950401VDA	ACTIVE	CFP	NAD	14	19	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	LM124AWR (LQMLV Q, QMLV Q) 5962R99504 01VDA ACO 01VDA >T	Samples
5962R9950401VZA	ACTIVE	CFP	NAC	14	42	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	LM124AWGR QMLV Q 5962R99504 01VZA ACO 01VZA >T	Samples
5962R9950402V9A	ACTIVE	DIESALE	Y	0	30	RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125		Samples
5962R9950402VCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	LM124AJRLQMLV 5962R9950402VCA Q	Samples
5962R9950402VDA	ACTIVE	CFP	NAD	14	19	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	LM124AWR LQMLV Q 5962R99504 02VDA ACO (02VDA >T, 02VDA A CO)	Samples
5962R9950402VZA	ACTIVE	CFP	NAC	14	42	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	LM124AWGR LQMLV Q 5962R99504 02VZA ACO 02VZA >T	Samples
7704302XA	ACTIVE	CFP	NAC	14	42	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	LM124AWG /883 Q 5962-77043 02XA ACO 02XA >T	Samples
LM124 MD8	ACTIVE	DIESALE	Y	0	100	RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125		Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM124 MDE	ACTIVE	DIESALE	Y	0	30	RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125		Samples
LM124 MDR	ACTIVE	DIESALE	Y	0	30	RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125		Samples
LM124AE/883	ACTIVE	LCCC	NAJ	20	50	RoHS-Exempt & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	LM124AE /883 Q 5962-77043 022A ACO 022A >T	Samples
LM124AJ/883	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	LM124AJ/883 (5962-7704302CA Q, 5962-7704302C A Q)	Samples
LM124AJRLQMLV	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	LM124AJRLQMLV 5962R9950402VCA Q	Samples
LM124AJRQMLV	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	LM124AJRQMLV 5962R9950401VCA Q	Samples
LM124AW/883	ACTIVE	CFP	NAD	14	19	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	LM124AW /883 Q ACO /883 Q >T	Samples
LM124AWG/883	ACTIVE	CFP	NAC	14	42	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	LM124AWG /883 Q 5962-77043 02XA ACO 02XA >T	Samples
LM124AWGRLQMLV	ACTIVE	CFP	NAC	14	42	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	LM124AWGR LQMLV Q 5962R99504 02VZA ACO 02VZA >T	Samples
LM124AWGRQMLV	ACTIVE	CFP	NAC	14	42	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	LM124AWGR QMLV Q 5962R99504 01VZA ACO 01VZA >T	Samples
LM124AWRLQMLV	ACTIVE	CFP	NAD	14	19	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	LM124AWR LQMLV Q 5962R99504	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
										02VDA ACO (02VDA >T, 02VDA A CO)	
LM124AWRQMLV	ACTIVE	CFP	NAD	14	19	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	LM124AWR (LQMLV Q, QMLV Q) 5962R99504 01VDA ACO 01VDA >T	Samples
LM124J/883	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	LM124J/883 (5962-7704301CA Q, 5962-7704301C A Q)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

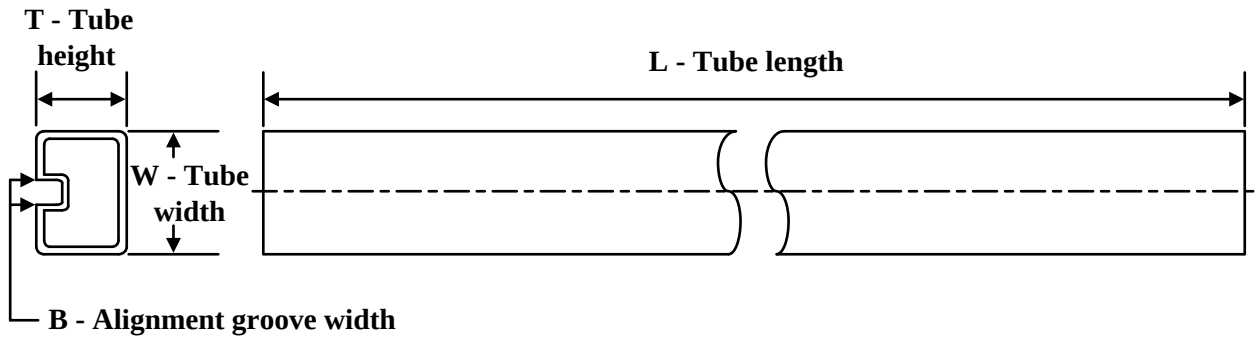
OTHER QUALIFIED VERSIONS OF LM124AQML, LM124AQML-SP :

- Military : LM124AQML
- Space : LM124AQML-SP

NOTE: Qualified Version Definitions:

- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

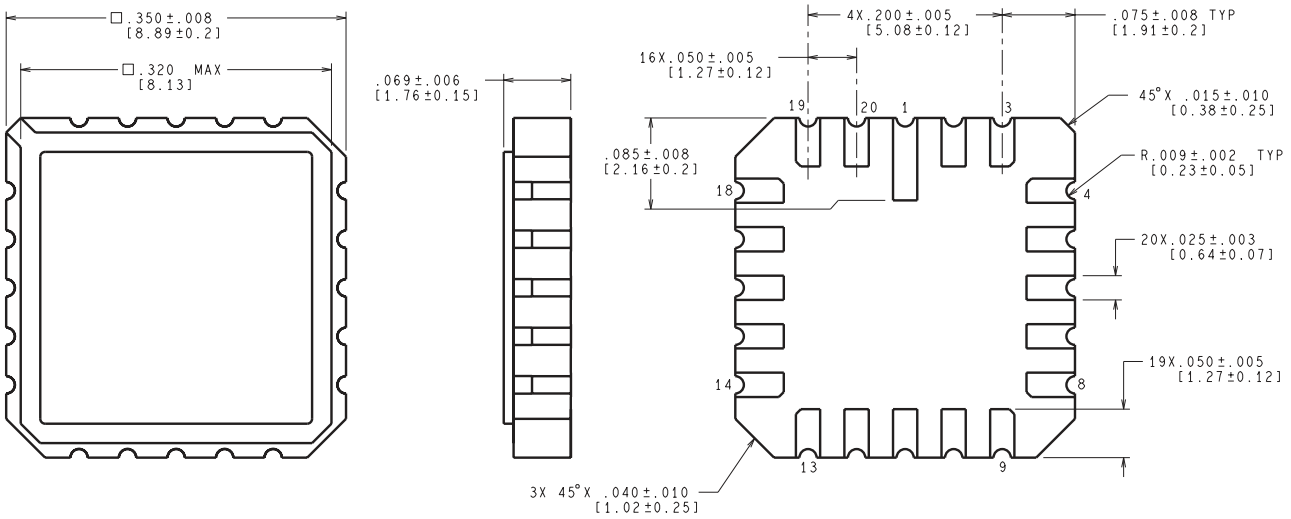
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962R9950401VCA	J	CDIP	14	25	506.98	15.24	13440	NA
5962R9950401VDA	NAD	CFP	14	19	502	23	9398	9.78
5962R9950402VCA	J	CDIP	14	25	506.98	15.24	13440	NA
5962R9950402VDA	NAD	CFP	14	19	502	23	9398	9.78
LM124AE/883	NAJ	LCCC	20	50	470	11	3810	0
LM124AJ/883	J	CDIP	14	25	506.98	15.24	13440	NA
LM124AJRLQMLV	J	CDIP	14	25	506.98	15.24	13440	NA
LM124AJRQMLV	J	CDIP	14	25	506.98	15.24	13440	NA
LM124AW/883	NAD	CFP	14	19	502	23	9398	9.78
LM124AWRLQMLV	NAD	CFP	14	19	502	23	9398	9.78
LM124AWRQMLV	NAD	CFP	14	19	502	23	9398	9.78
LM124J/883	J	CDIP	14	25	506.98	15.24	13440	NA

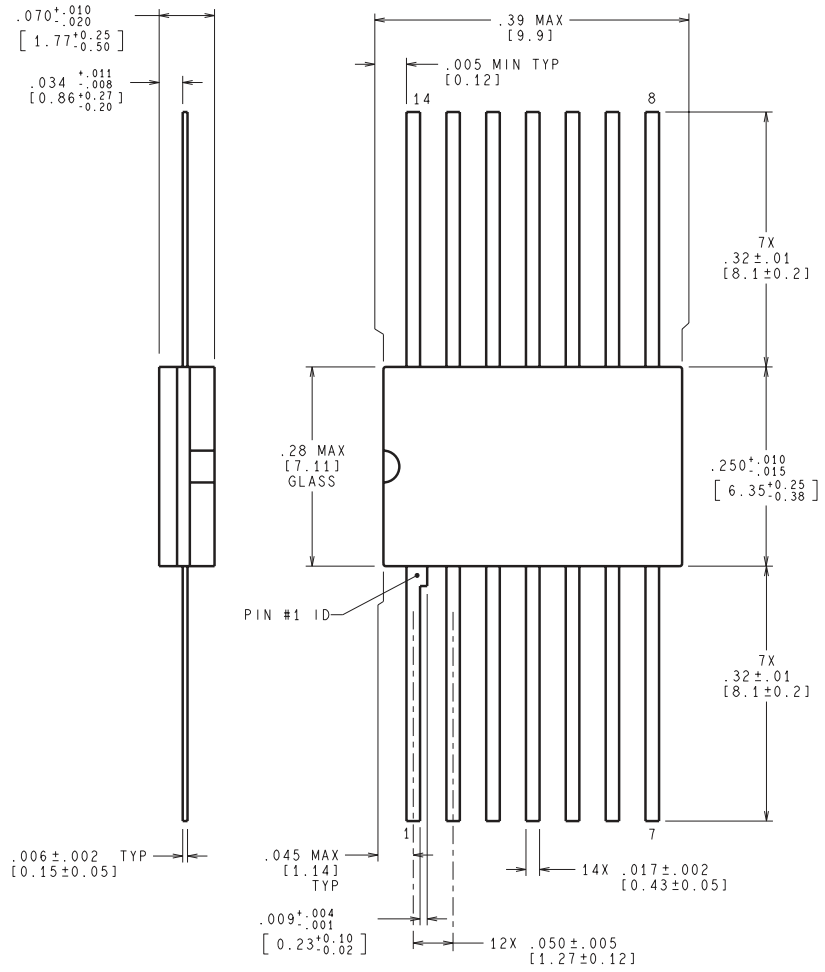
NAJ0020A



CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

E20A (Rev F)

NAD0014B



W14B (Rev P)

MIL-PRF-38535 CONFIGURATION CONTROL

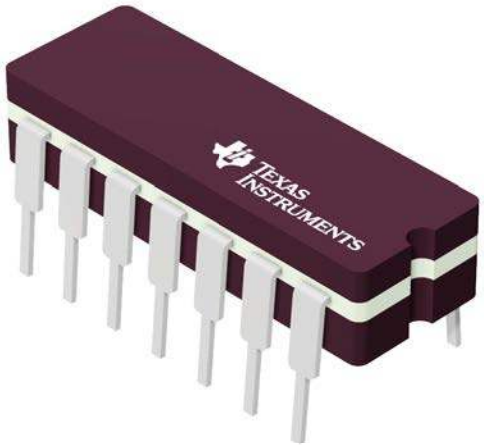
MIL-STD-1835B CONFIGURATION CONTROL

CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

GENERIC PACKAGE VIEW

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

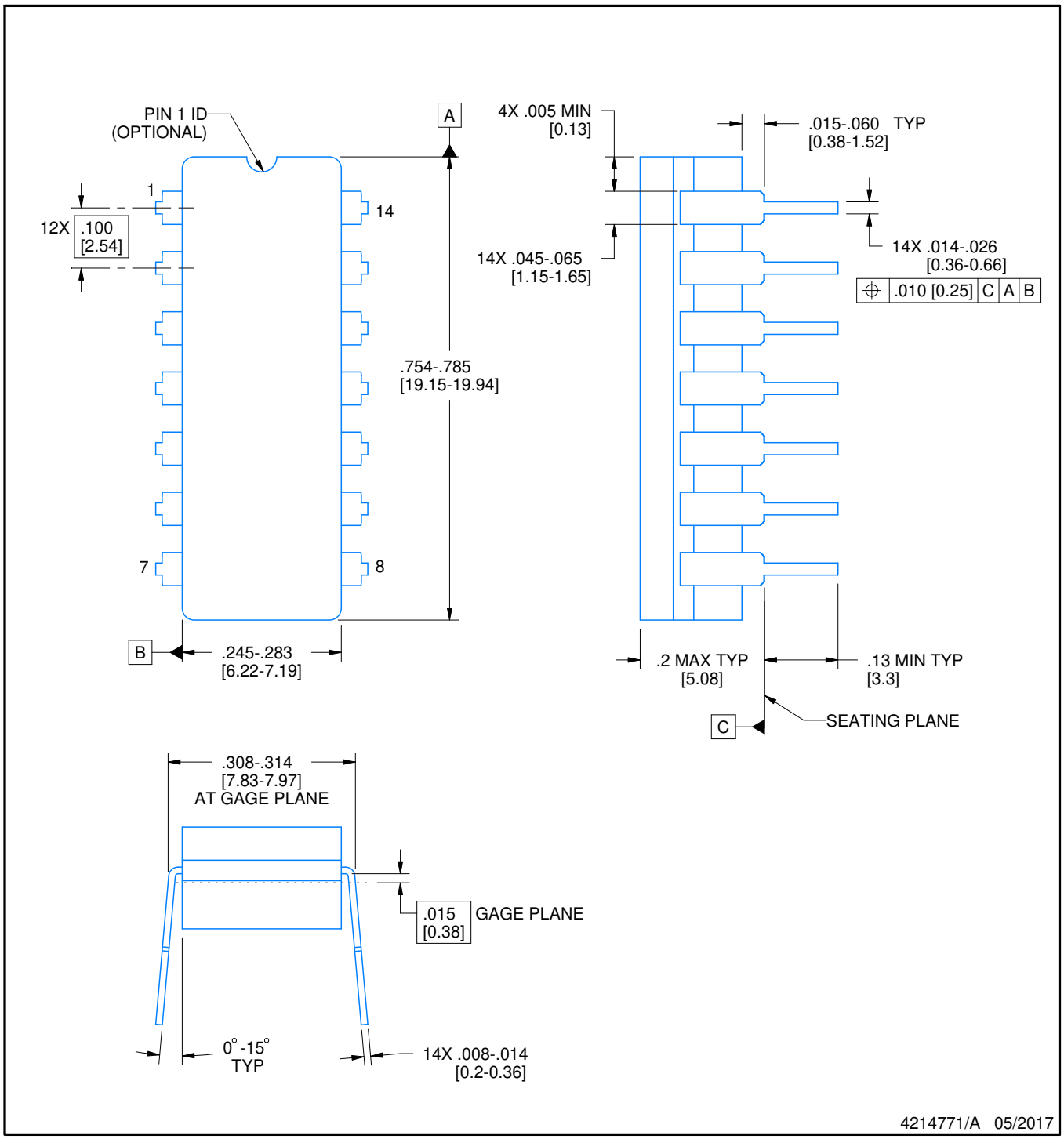
4040083-5/G

PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

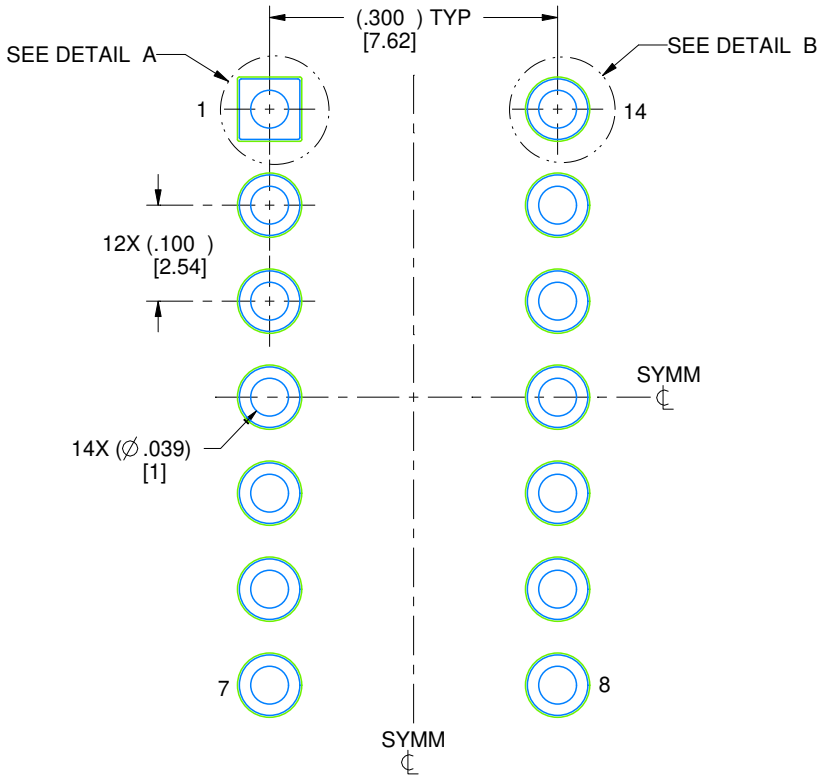
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

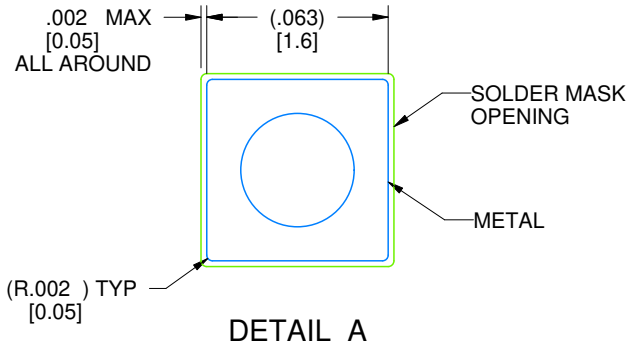
J0014A

CDIP - 5.08 mm max height

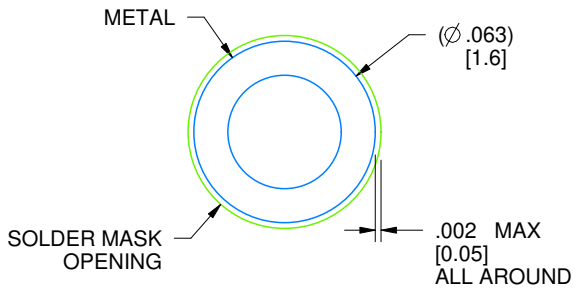
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X

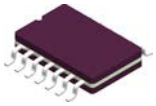


DETAIL A
SCALE: 15X



DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

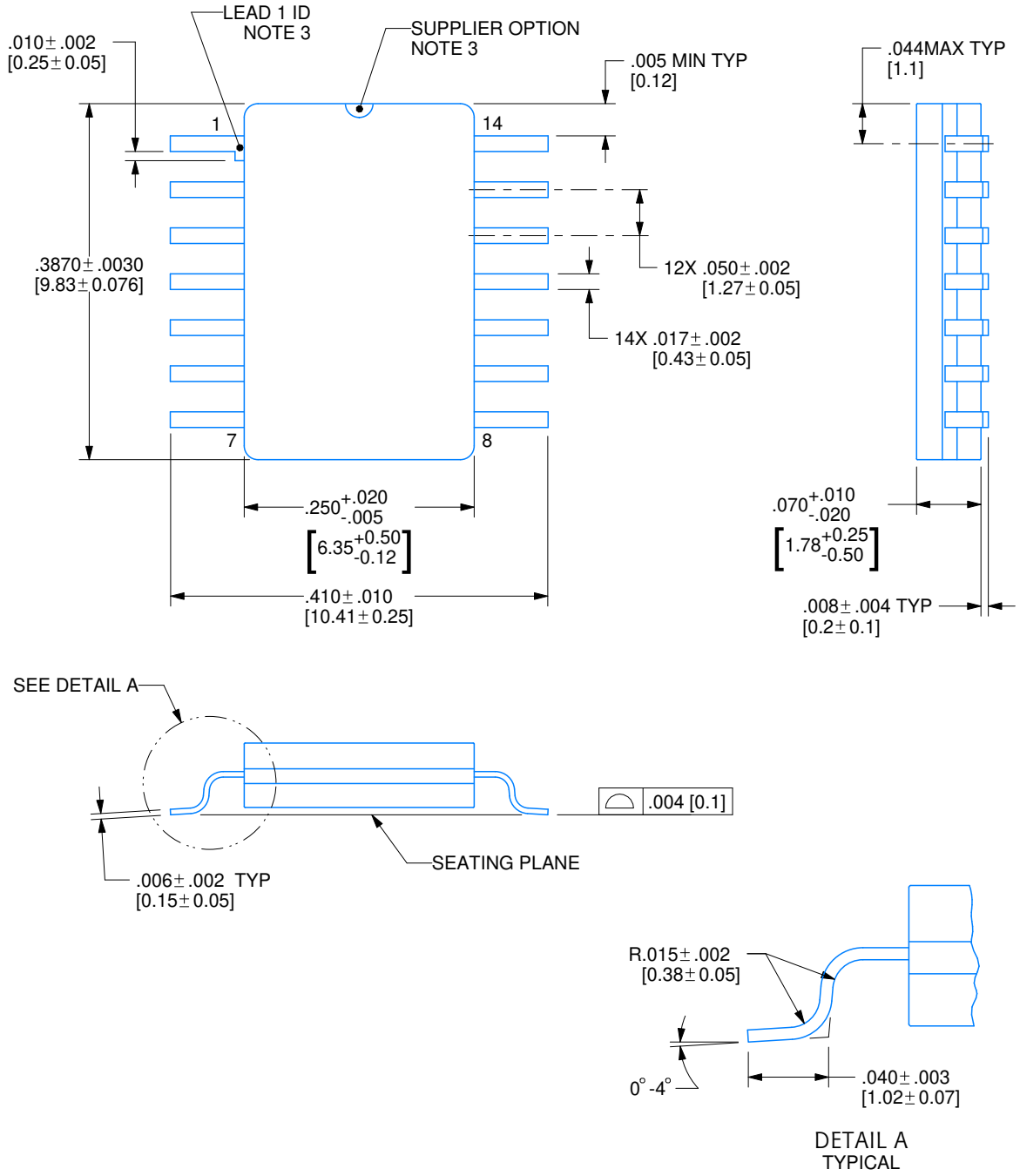


PACKAGE OUTLINE

NAC0014A

CERPACK

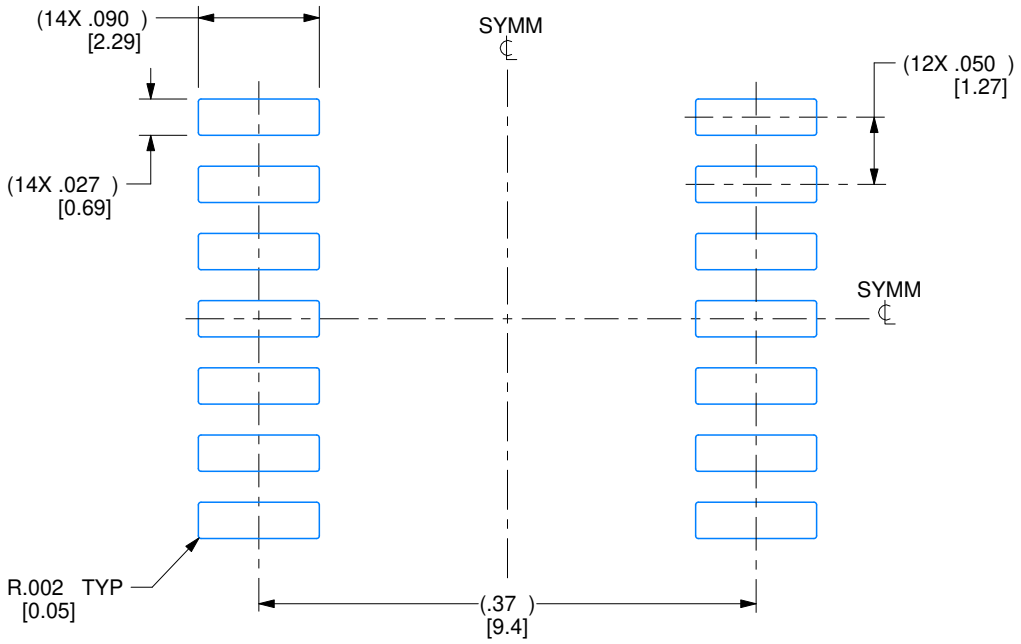
CERAMIC FLATPACK



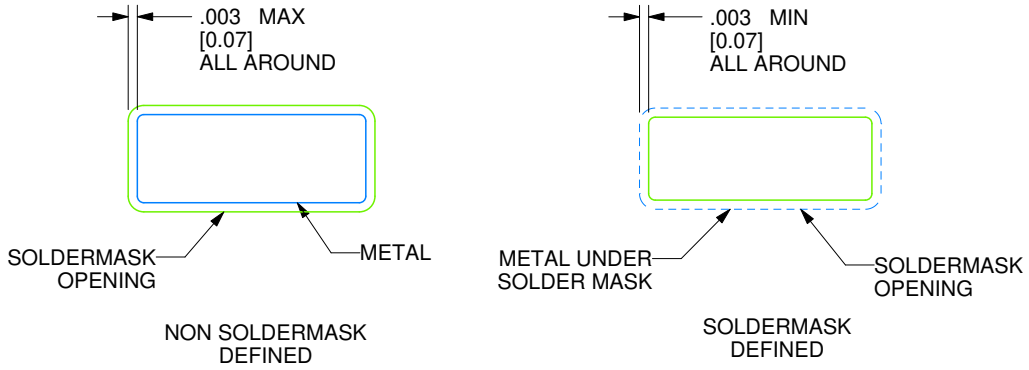
4215197/C 08/2022

NOTES:

1. Controlling dimension is Inch. Values in [ ] are milimeters. Dimensions in ( ) for reference only.
2. For solder thickness and composition, see the "Lead Finish Composition/Thickness" link in the packaging section of the Texas Instruments website
3. Lead 1 identification shall be:
   a) A notch or other mark within this area
   b) A tab on lead 1, either side
4. No JEDEC registration as of December 2021



RECOMMENDED LAND PATTERN



4215197/C 08/2022

REVISIONS

REV	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	2197878	12/30/2021	DAVID CHIN / ANIS FAUZI
B	NO CHANGE TO DRAWING; REVISION FOR YODA RELEASE;	2198833	02/15/2022	K. SINCERBOX
C	.3870± .0030 WAS .39000± .00012;	2200916	08/08/2022	D. CHIN / K. SINCERBOX

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