V_{DS}	1200 V
I_{DS}	480 A

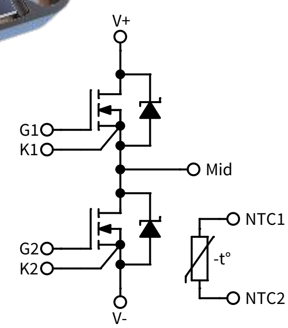
CAS480M12HM3

1200 V, 480 A, Silicon Carbide High-Performance, Switching Optimized, Half-Bridge Module

Technical Features

- Low Inductance, Low Profile 62mm Footprint
- High Junction Temperature (175 °C) Operation
- Implements Switching Optimized Third Generation SiC MOSFET Technology
- Zero Reverse Recovery from Diodes
- Light Weight AlSiC Baseplate
- High Reliability Silicon Nitride Insulator

Package 110mm x 65 mm x 12.2 mm



Applications

- Railway & Traction
- Solar
- EV Chargers
- Industrial Automation & Testing

System Benefits

- Lightweight, Compact Form Factor with 62mm Compatible Baseplate Enables System Retrofit
- Increased System Efficiency, due to Low Switching & Conduction Losses of SiC
- High Reliability Material Selection

Key Parameters (T_C = 25 ˚C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{DS\,max}$	Drain-Source Voltage			1200	V		
$V_{GS\,max}$	Gate-Source Voltage, Maximum Value	-8		+19		Transient, <100 ns	Fig. 33
$V_{GS\,op}$	Gate-Source Voltage, Recommended Op. Value	-4		+15		Static	
I_{DS}	DC Continuous Drain Current		640		A	V_{GS} = 15 V, T_C = 25 ˚C, T_{VJ} ≤ 175 ˚C	Fig. 20
			481			V_{GS} = 15 V, T_C = 90 ˚C, T_{VJ} ≤ 175 ˚C	
I_{SD}	DC Source-Drain Current		640			V_{GS} = 15 V, T_C = 25 ˚C, T_{VJ} ≤ 175 ˚C	
I_F	Schottky Diode DC Forward Current		464			V_{GS} = - 4 V, T_C = 25 ˚C, T_{VJ} ≤ 175 ˚C	
$I_{DS\,(pulsed)}$	Maximum Pulsed Drain-Source Current			960		t_{Pmax} limited by $T_{VJ\,max}$ V_{GS} = 15 V, T_C = 25 ˚C	
$I_{F\,(pulsed)}$	Maximum Pulsed Diode Current			960			
$T_{VJ\,op}$	Maximum Virtual Junction Temperature under Switching Conditions	-40		175	°C		

MOSFET Characteristics (Per Position) (T_{VJ} = 25˚C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	1200			V	V_{GS} = 0 V, T_{VJ} = -40 °C	
$V_{GS(th)}$	Gate Threshold Voltage	1.8	2.5	3.6	V	V_{DS} = V_{GS}, I_D = 160 mA	
			2.0		V	V_{DS} = V_{GS}, I_D = 160 mA, T_{VJ} = 175 °C	
I_{DSS}	Zero Gate Voltage Drain Current		10	280	μA	V_{GS} = 0 V, V_{DS} = 1200 V	
I_{GSS}	Gate-Source Leakage Current		0.1	2	μA	V_{GS} = 15 V, V_{DS} = 0 V	
$R_{DS(on)}$	Drain-Source On-State Resistance (Devices Only)		2.29	2.97	mΩ	V_{GS} = 15 V, I_D = 480 A	Fig. 2 Fig. 3
			3.66		mΩ	V_{GS} = 15 V, I_D = 480 A, T_{VJ} = 175 °C	
g_{fs}	Transconductance		356		S	V_{DS} = 20 V, I_{DS} = 480 A	Fig. 4
			345		S	V_{DS} = 20 V, I_{DS} = 480 A, T_{VJ} = 175 °C	
E_{On}	Turn-On Switching Energy, T_{VJ} = 25 °C T_{VJ} = 125 °C T_{VJ} = 175 °C		11.3 9.6 9.9		mJ	V_{DS} = 600 V, I_D = 500 A, V_{GS} = -4 V/15 V, $R_{G(ext)}$ = 1.0 Ω, L = 13.7 μH	Fig. 11 Fig. 13
E_{Off}	Turn-Off Switching Energy, T_{VJ} = 25 °C T_{VJ} = 125 °C T_{VJ} = 175 °C		7.2 7.3 7.4		mJ		
$R_{G(int)}$	Internal Gate Resistance		0.8		Ω	V_{AC} = 25 mV, f = 100 kHz	
C_{iss}	Input Capacitance		43.1		nF	V_{GS} = 0 V, V_{DS} = 800 V, V_{AC} = 25 mV, f = 100 kHz	Fig. 9
C_{oss}	Output Capacitance		2.76		nF		
C_{rss}	Reverse Transfer Capacitance		70.7		pF		
Q_{GS}	Gate to Source Charge		448		nC	V_{DS} = 800 V, V_{GS} = -4 V/15 V I_D = 480 A Per IEC60747-8-4 pg 21	
Q_{GD}	Gate to Drain Charge		539		nC		
Q_G	Total Gate Charge		1590		nC		
$R_{th\ JC}$	FET Thermal Resistance, Junction to Case		0.1	0.115	°C/W		Fig. 17

Diode Characteristics (Per Position) (T_{VJ} = 25˚C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
V_F	Diode Forward Voltage		1.95		V	V_{GS} = -4 V, I_F = 480 A	Fig. 7
			3.10		V	V_{GS} = -4 V, I_F = 480 A, T_{VJ} = 175 °C	
t_{RR}	Reverse Recovery Time		28		ns	V_{GS} = -4 V, I_{SD} = 500 A, V_R = 600 V di_F/dt = 17 A/ns, T_{VJ} = 175 °C	Fig. 32
Q_{RR}	Reverse Recovery Charge		4.5		μC		
I_{RRM}	Peak Reverse Recovery Current		270		A		
E_{RR}	Diode Energy T_{VJ} = 25 °C T_{VJ} = 125 °C T_{VJ} = 175 °C		1.1 1.3 1.5		mJ	V_{DS} = 600 V, I_D = 500A, V_{GS} = -4 V/15 V, $R_{G(ext)}$ = 1.0 Ω, L = 13.7 μH	Fig. 14 Note 1
$R_{th\ JC}$	Diode Thermal Resistance, Junction to Case		0.11	0.13	°C/W		

Note 1 SiC Schottky diodes do not have reverse recovery energy but still contribute capacitive energy.

Module Physical Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
R_{1-2}	Package Resistance, M1		106.5		µΩ	T_C = 125 °C, Note 2
R_{2-3}	Package Resistance, M2		126.3			T_C = 125 °C, Note 2
L_{Stray}	Stray Inductance		4.8		nH	Between Terminals 1 and 3
T_C	Case Temperature	-40		125	°C	
W	Weight		180		g	
M_S	Mounting Torque	3	4.5	5	N-m	Baseplate, M6 bolts
		0.9	1.1	1.3		Power Terminals, M4 bolts
V_{isol}	Case Isolation Voltage	4			kV	AC, 50 Hz, 1 min
CTI	Comparative Tracking Index	600				
	Clearance Distance	13.07			mm	Terminal to Terminal
		6.00				Terminal to Baseplate
	Creepage Distance	14.27				Terminal to Terminal
		12.34				Terminal to Baseplate

Note 2 Total Effective Resistance (Per Switch Position) = MOSFET $R_{DS(on)}$ + Switch Position Package Resistance.

Temperature Sensor (NTC) Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
R_{25}	Resistance at 25°C		4700		Ω	T_{NTC} = 25 °C
	Tolerance of R_{25}			±1	%	
$B_{25/85}$	Beta Value for 25°C to 85°C		3435		K	
$B_{0/100}$	Beta Value for 0°C to 100°C		3399		K	
	Tolerance of $B_{25/85}$			±1	%	
P_{25}	Maximum Power Dissipation			50	mW	

Steinhart & Hart Coefficients for NTC Resistance & NTC Temperature Computation (T in K)

$$\ln\left(\frac{R}{R_{25}}\right) = A + \frac{B}{T} + \frac{C}{T^2} + \frac{D}{T^3}$$

A	B	C	D
-1.289E+01	4.245E+03	-8.749E+04	-9.588E+06

$$\frac{1}{T} = A_1 + B_1 \ln\left(\frac{R}{R_{25}}\right) + C_1 \ln^2\left(\frac{R}{R_{25}}\right) + D_1 \ln^3\left(\frac{R}{R_{25}}\right)$$

A_1	B_1	C_1	D_1
3.354E-03	3.001E-04	5.085E-06	2.188E-07

Typical Performance

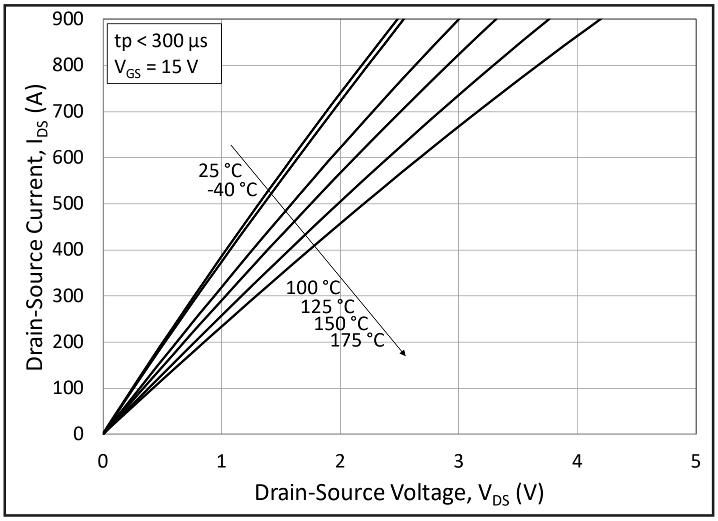


Figure 1. Output Characteristics for Various Junction Temperatures

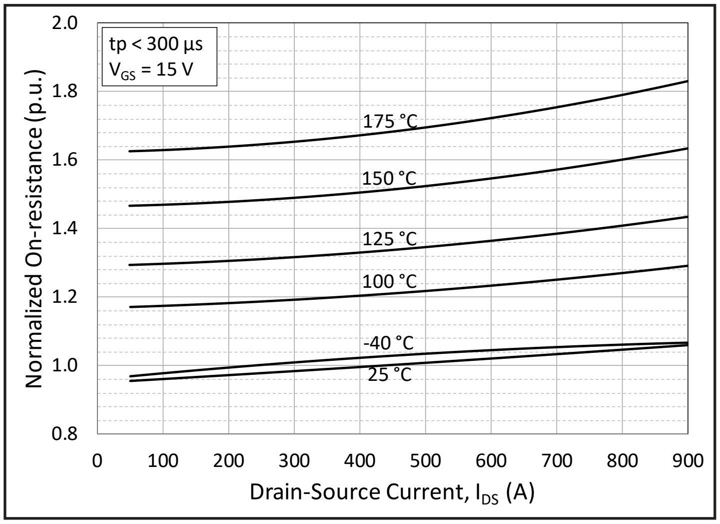


Figure 2. Normalized On-State Resistance vs. Drain Current for Various Junction Temperatures

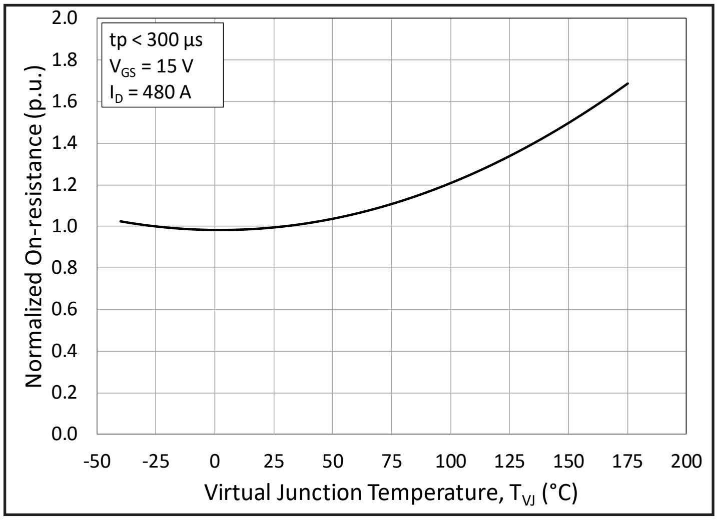


Figure 3. Normalized On-State Resistance vs. Junction Temperature

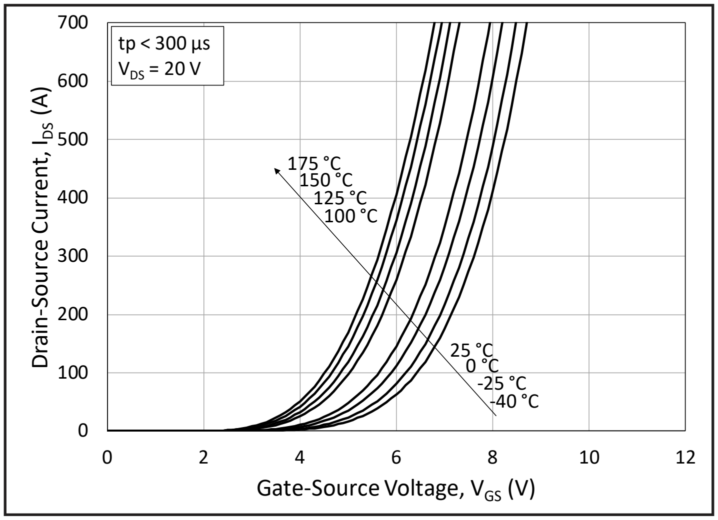


Figure 4. Transfer Characteristic for Various Junction Temperatures

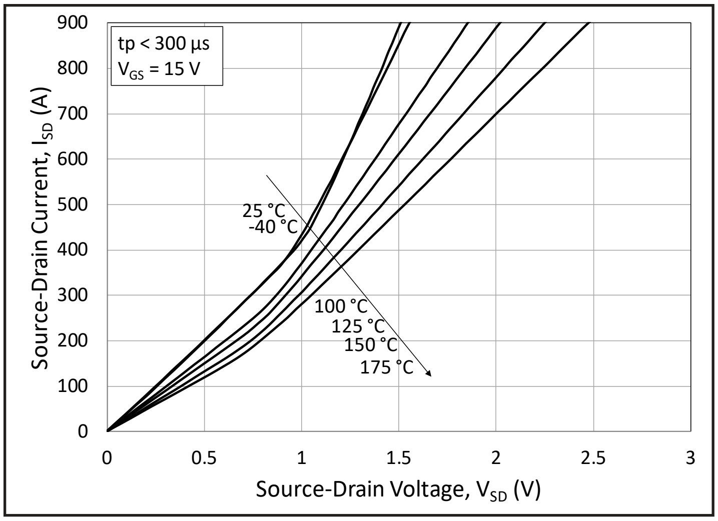


Figure 5. 3rd Quadrant Characteristic vs. Junction Temperatures at V_{GS} = 15 V

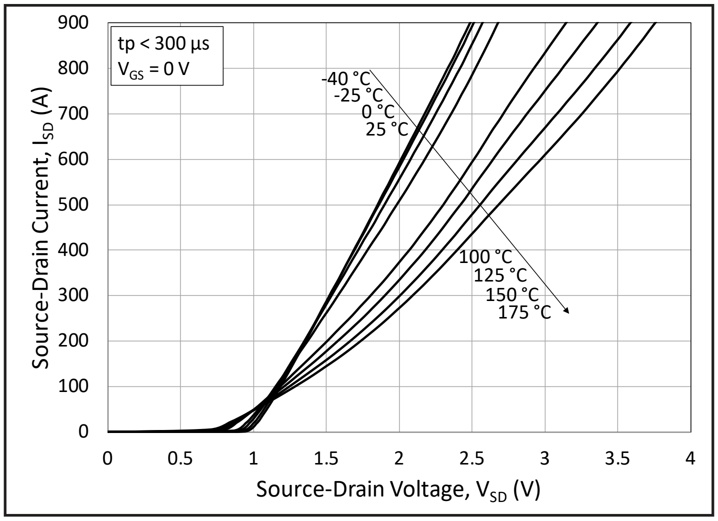


Figure 6. 3rd Quadrant Characteristic vs. Junction Temperatures at V_{GS} = 0V (Diode)

Typical Performance

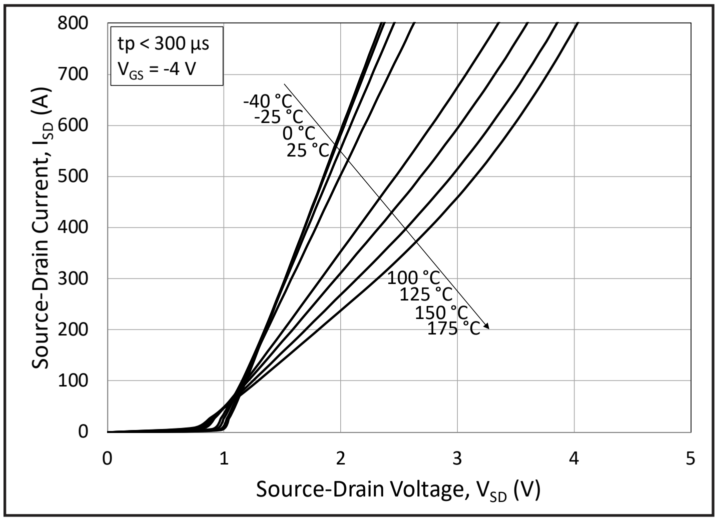


Figure 7. 3rd Quadrant Characteristic vs. Junction Temperatures at V_{GS} = - 4 V (Diode)

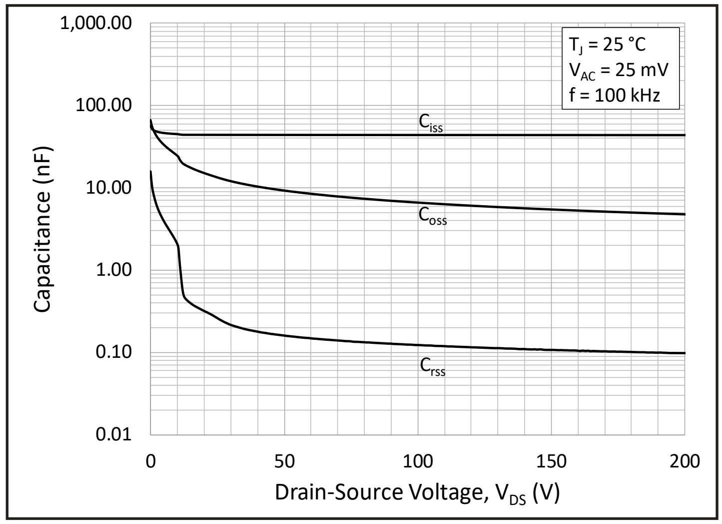


Figure 8. Typical Capacitances vs. Drain to Source Voltage (0 - 200V)

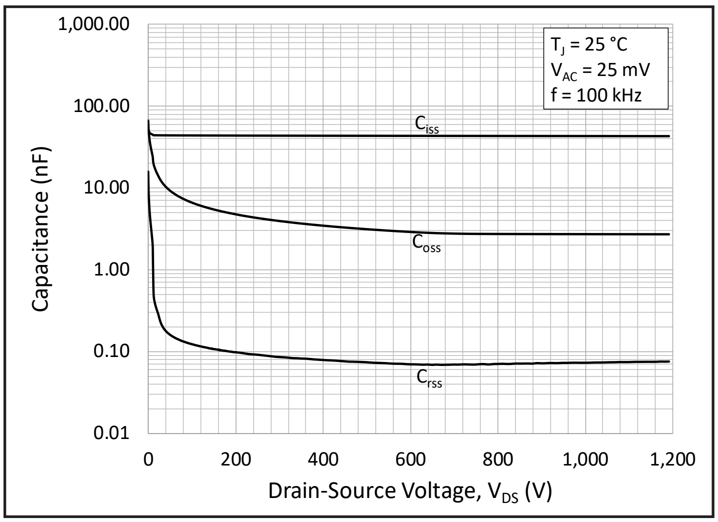


Figure 9. Typical Capacitances vs. Drain to Source Voltage (0 - 1200V)

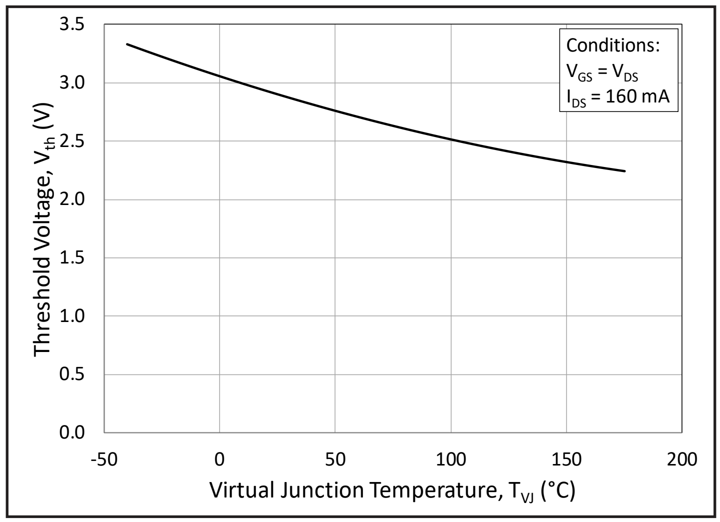


Figure 10. Threshold Voltage vs. Junction Temperature

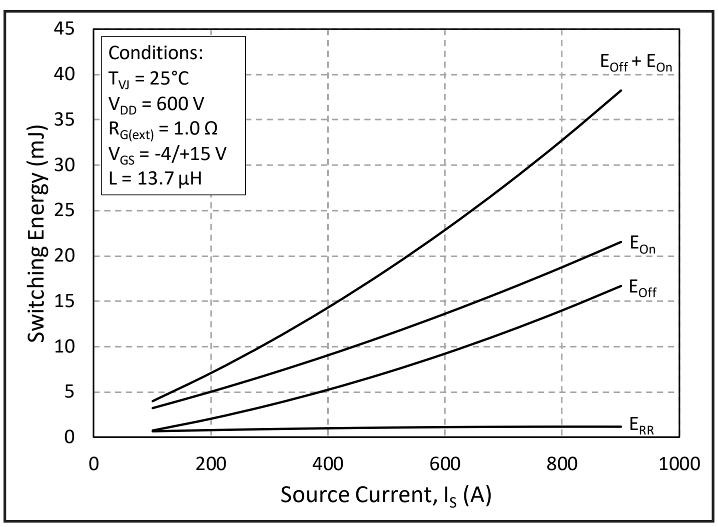


Figure 11. Switching Energy vs. Drain Current (V_{DS} = 600 V)

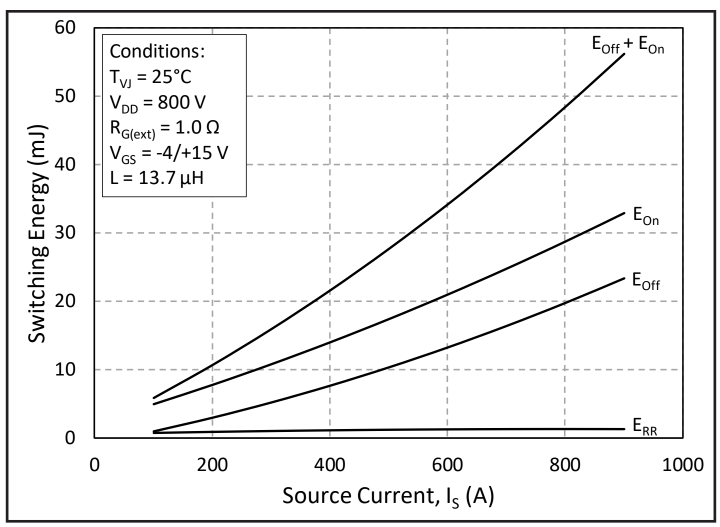


Figure 12. Switching Energy vs. Drain Current (V_{DS} = 800 V)

Typical Performance

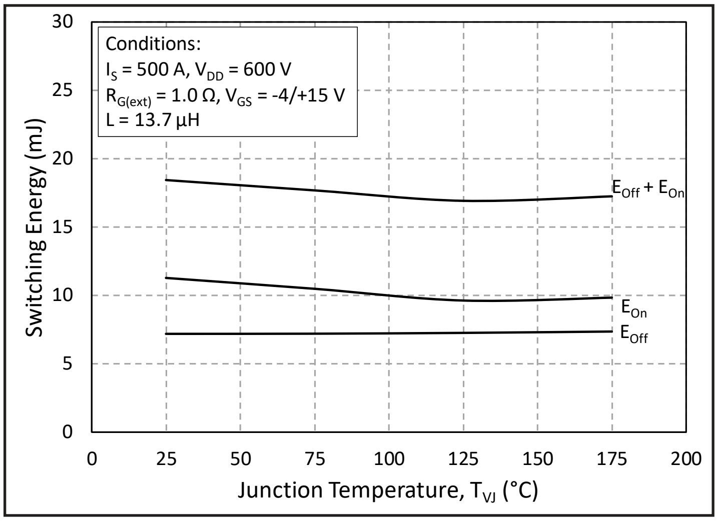


Figure 13. MOSFET Switching Energy vs. Junction Temperature

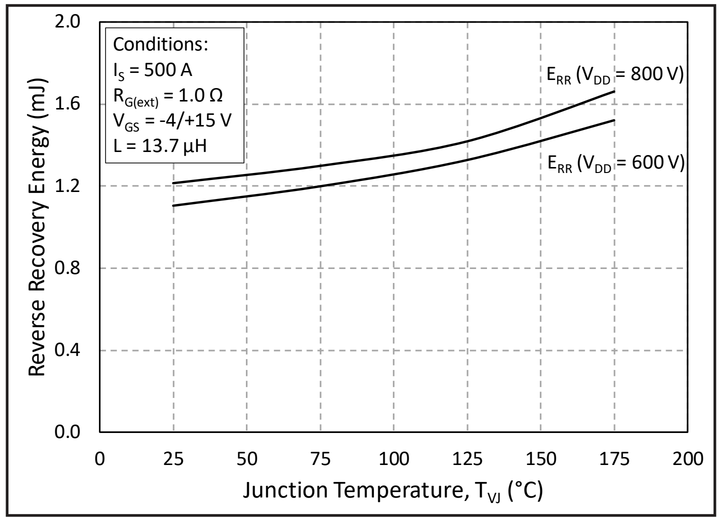


Figure 14. Reverse Recovery Energy vs. Junction Temperature

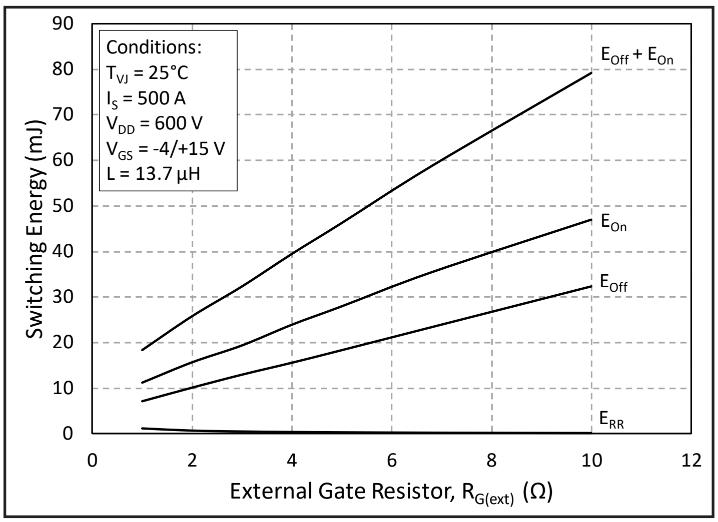


Figure 15. MOSFET Switching Energy vs. External Gate Resistance

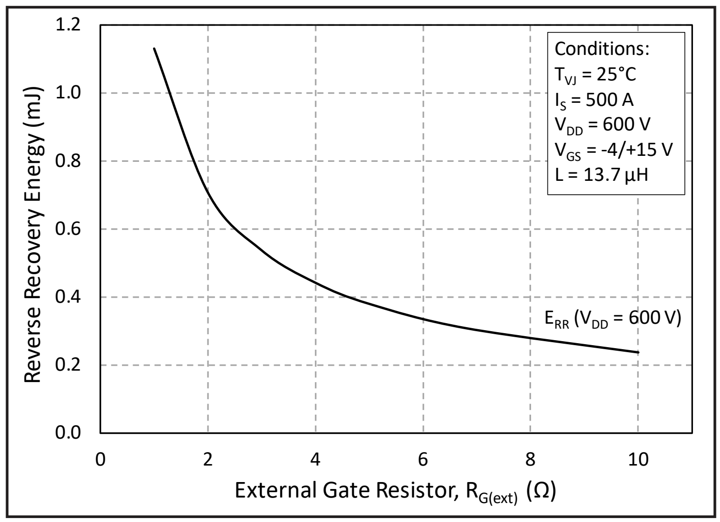


Figure 16. Reverse Recovery Energy vs. External Gate Resistance

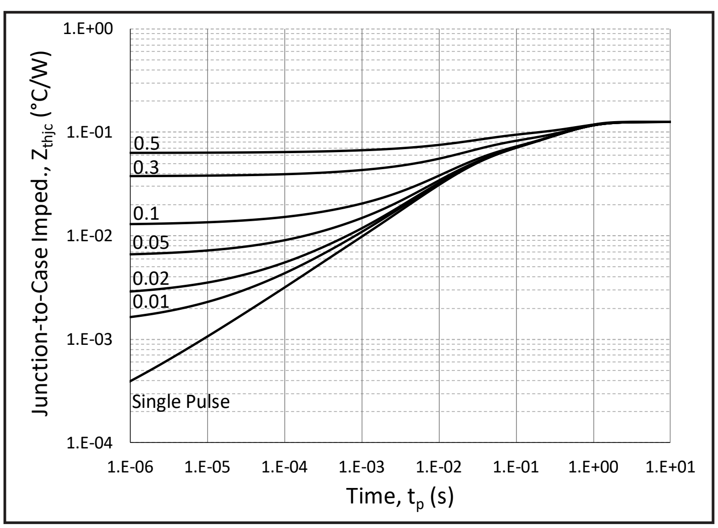


Figure 17. MOSFET Junction to Case Transient Thermal Impedance, $Z_{th\ JC}$ (°C/W)

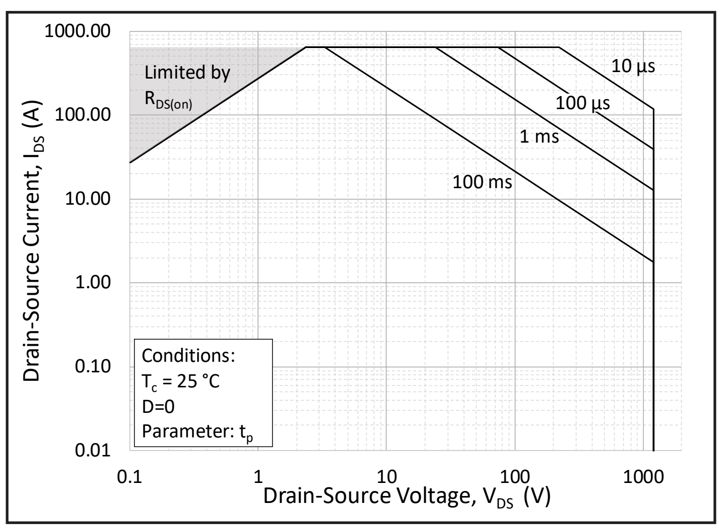


Figure 18. Forward Bias Safe Operating Area (FBSOA)

Typical Performance

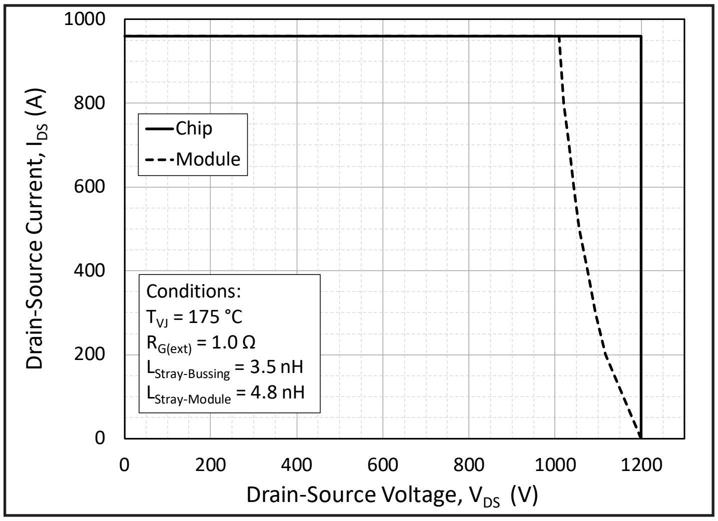


Figure 19. Reverse Bias Safe Operating Area (RBSOA)

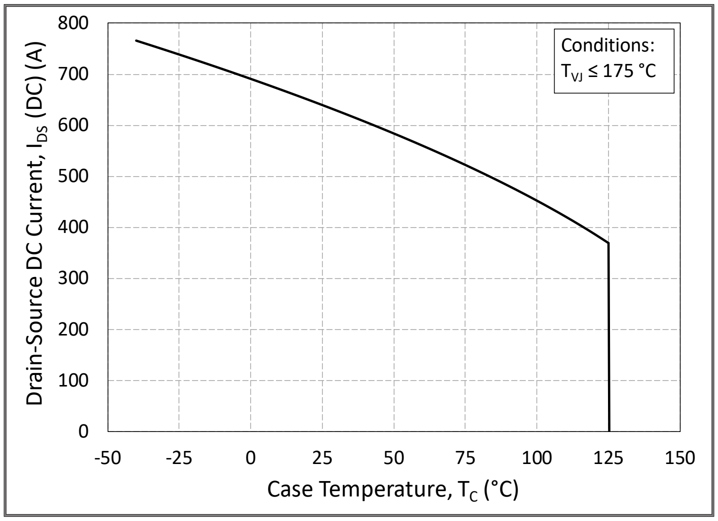


Figure 20. Continuous Drain Current Derating vs. Case Temperature

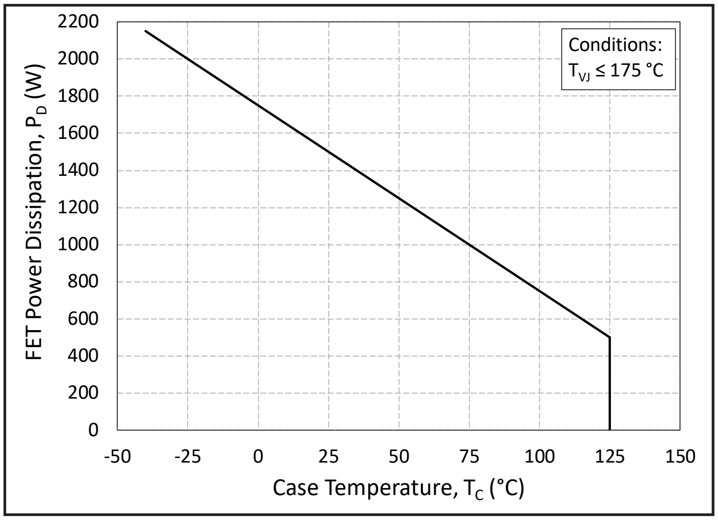


Figure 21. Maximum Power Dissipation Derating vs. Case Temperature

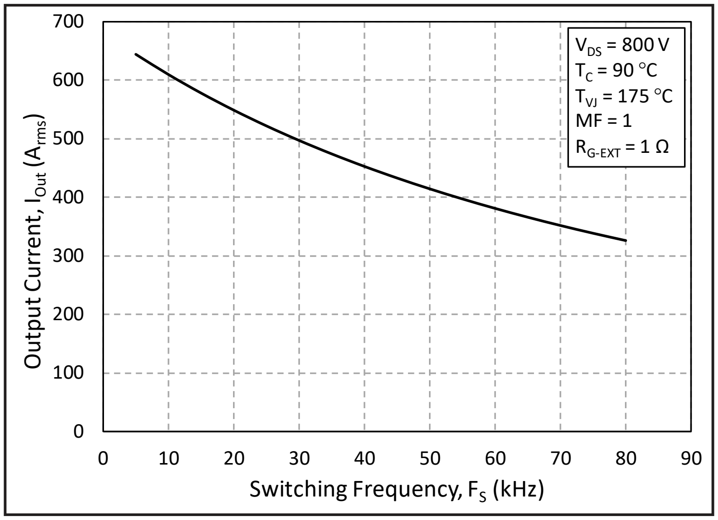


Figure 22. Typical Output Current Capability vs. Switching Frequency (Inverter Application)

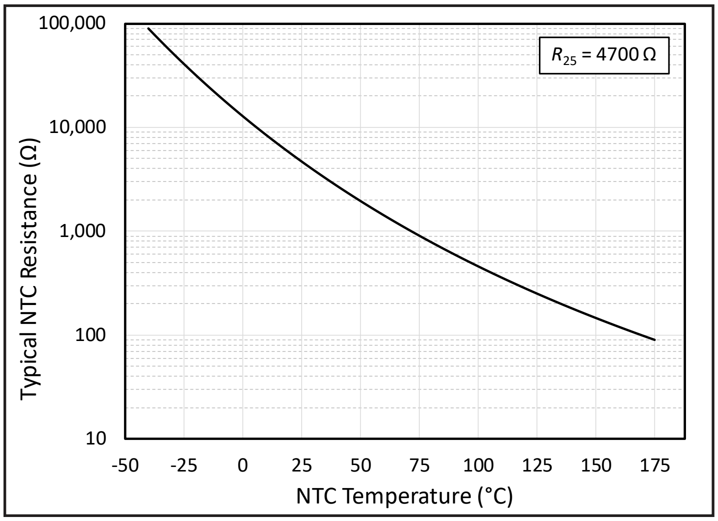


Figure 23. Typical NTC Resistance vs. Temperature

Timing Characteristics

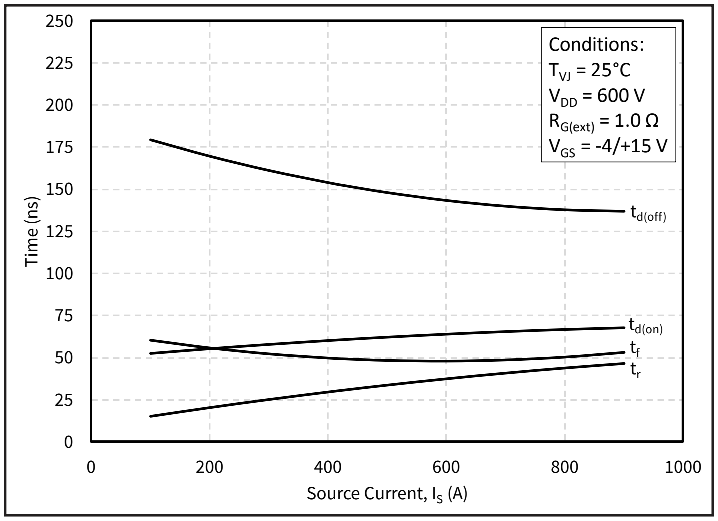


Figure 24. Timing vs. Source Current

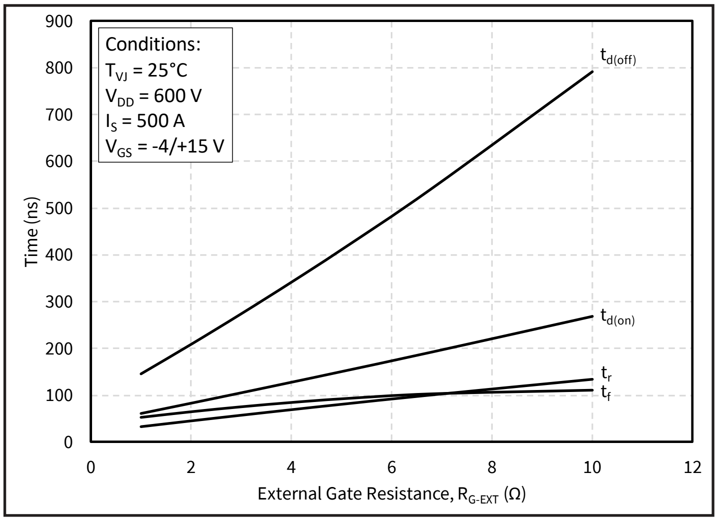


Figure 25. Timing vs. External Gate Resistance

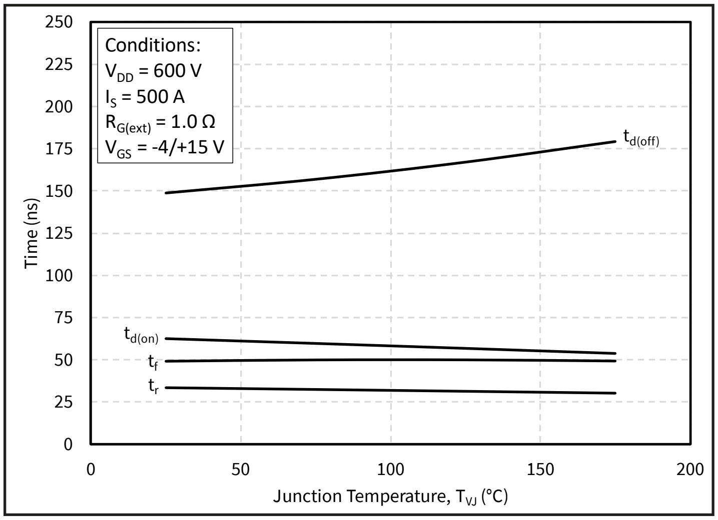


Figure 26. Timing vs. Junction Temperature

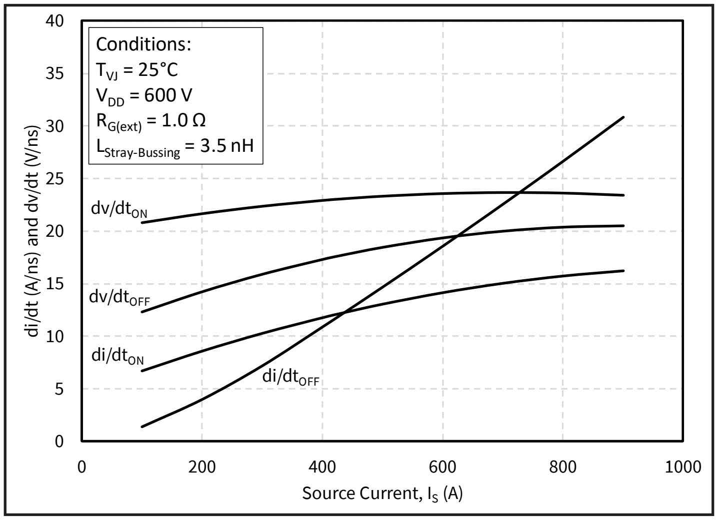


Figure 27. dv/dt and di/dt vs. Source Current

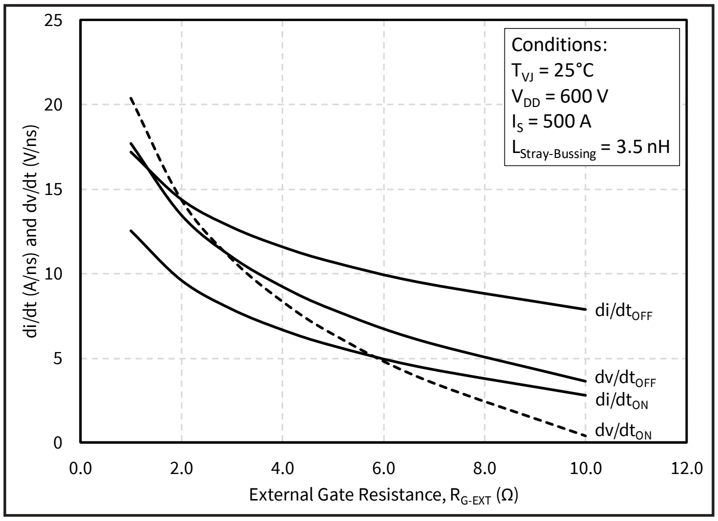


Figure 28. dv/dt and di/dt vs. External Gate Resistance

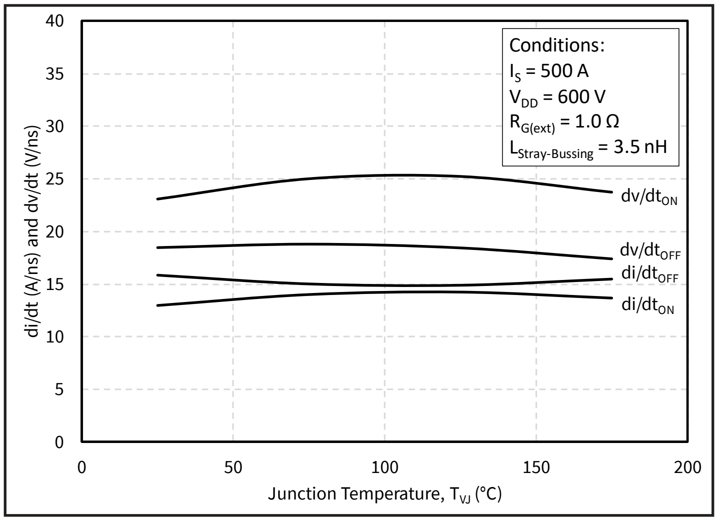


Figure 29. dv/dt and di/dt vs. Junction Temperature

Definitions

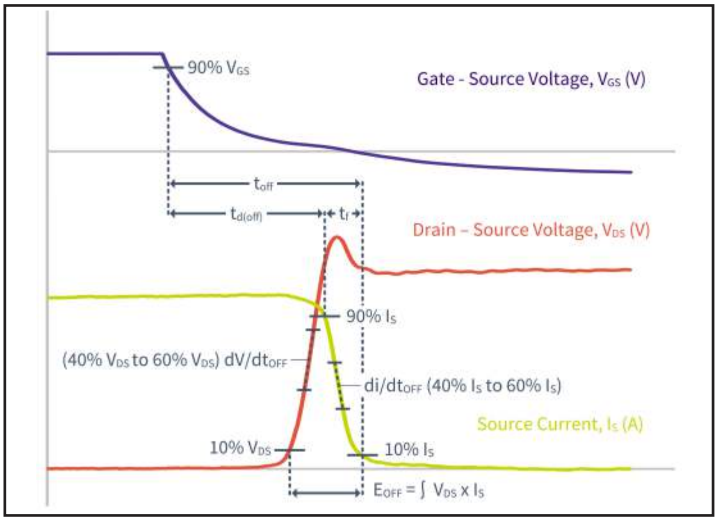


Figure 30. Turn-off Transient Definitions

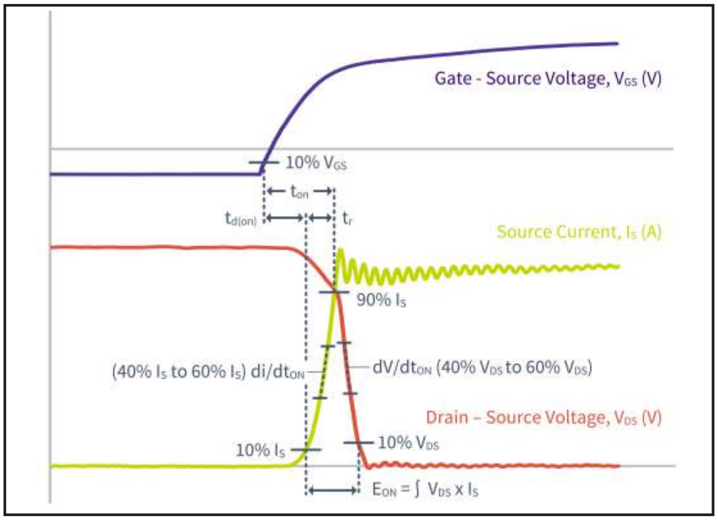


Figure 31. Turn-on Transient Definitions

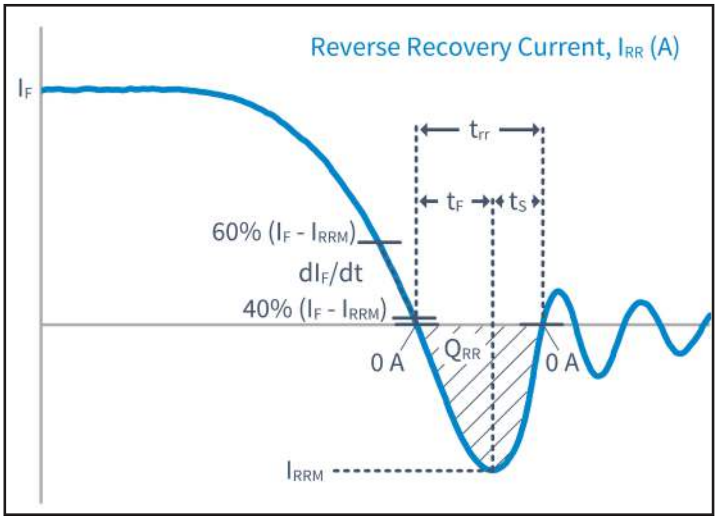


Figure 32. Reverse Recovery Definitions

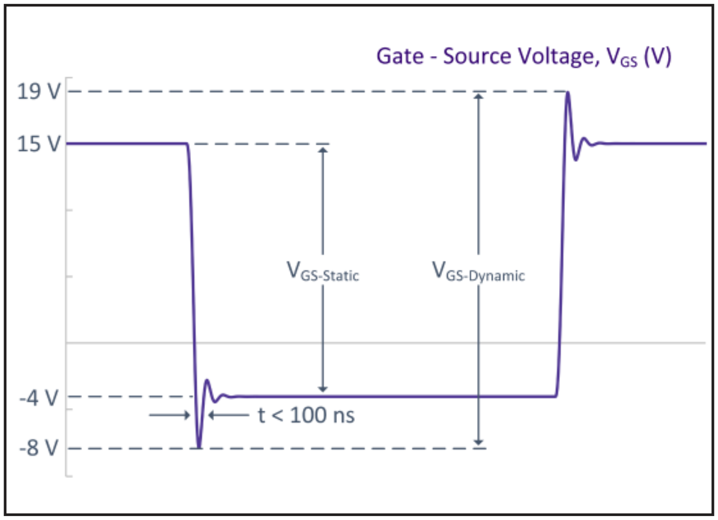
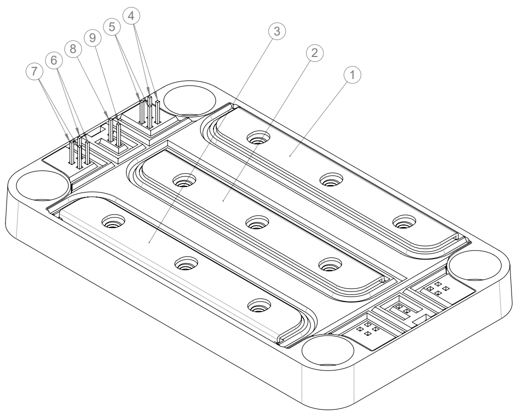
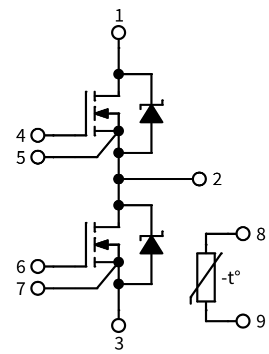


Figure 33. V_{GS} Transient Definitions

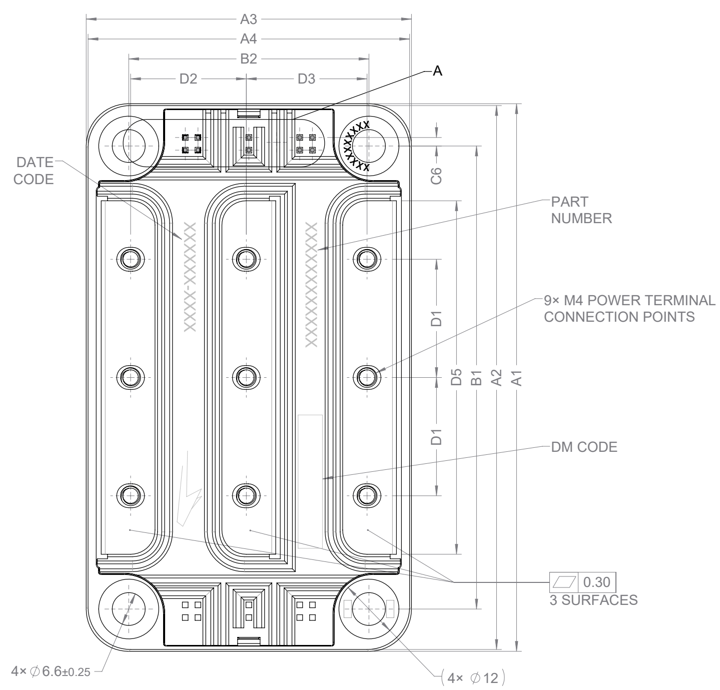
Schematic and Pin Out

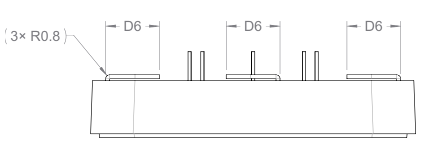


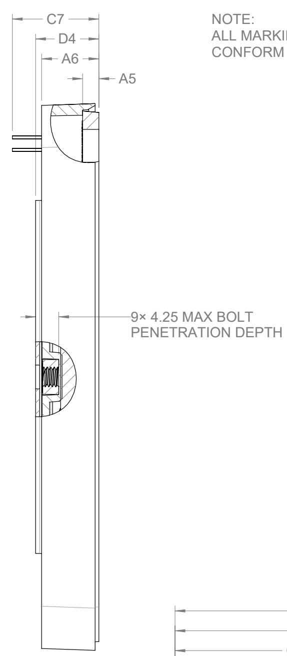
PIN OUT SCHEME	
PIN	LABEL
1	V+
2	Mid
3	V-
4	G1, Top row pins (2)
5	K1, Bottom row pins (2)
6	G2, Top row pins (2)
7	K2, Bottom row pins (2)
8	NTC1
9	NTC2



Package Dimensions (mm)

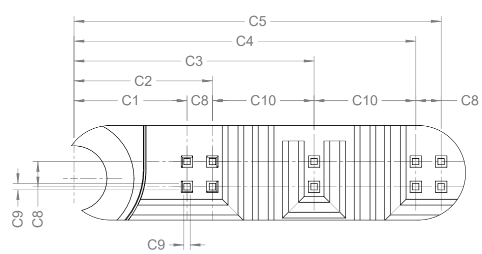






NOTE:
ALL MARKINGS SHALL
CONFORM TO PRC-00786.

DIMENSION TABLE		
SYMBOL	DIMENSION	TOLERANCE
A1	110.00	±0.60
A2	109.25	±0.60
A3	65.00	±0.60
A4	64.25	±0.60
A5	3.25	±0.30
A6	11.45	±0.60
B1	93.00	±0.30
B2	48.00	±0.30
C1	11.30	±0.40
C2	13.84	±0.40
C3	24.00	±0.40
C4	34.16	±0.40
C5	36.70	±0.40
C6	1.71	±0.40
C7	17.30	±0.50
C8	2.54	±0.30
C9	0.64	±0.30
C10	10.16	±0.40
D1	23.75	±0.50
D2	23.13	±0.50
D3	24.13	±0.50
D4	12.20	±0.50
D5	71.00	±0.30
D6	10.75	±0.30



DETAIL A
SCALE: 4:1

Supporting Links & Tools

- CGD1700HB3P-HM3 Evaluation Gate Driver
- CGD12HB00D: Differential Transceiver Board
- CPWR-AN35: Thermal Interface Material Application Note
- CPWR-AN39: KIT-CRD-CIL12N-HM User Guide
- KIT-CRD-CIL12N-HM: Dynamic Performance Evaluation Board for the HM2 and HM3 Module
- CAS480M12HM3 PLECS Models

Notes

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This product has not been designed or tested for use in, and is not intended for use in, applications in which failure of the product would reasonably be expected to cause death, personal injury, or property damage, including but not limited to equipment implanted into the human body, life-support machines, cardiac defibrillators, and similar emergency medical equipment, aircraft navigation, communication, and control systems, aircraft power and propulsion systems, air traffic control systems, and equipment used in the planning, construction, maintenance, or operation of nuclear facilities.

RoHS Compliance

The levels of RoHS restricted materials in this product are below the maximum concentration values (also referred to as the threshold limits) permitted for such substances, or are used in an exempted application, in accordance with EU Directive 2011/65/EC (RoHS2), as implemented January 2, 2013. RoHS Declarations for this product can be obtained from your Cree representative or from the Product Documentation sections of www.cree.com.

REACh Compliance

REACh substances of high concern (SVHCs) information is available for this product. Since the European Chemical Agency (ECHA) has published notice of their intent to frequently revise the SVHC listing for the foreseeable future, please contact your Cree representative to ensure you get the most up-to-date REACh SVHC Declaration. REACh banned substance information (REACh Article 67) is also available upon request.