FAIRCHILD™

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FAN5702
Configurable 180 mA 6-LED Driver with I²C Control

Features

- Six (6) Parallel LEDs (up to 30 mA Each)
- Total Package Load Current Capability: 180 mA
- Group from 2 to 6 LEDs for Flexible Backlighting
- I2C Interface for Easy Programming
- >600:1 Dimming Ratio for 100 Hz PWM Frequency
- Logarithmically Controlled Dimming with 64 Steps
- Secondary Brightness Control Using PWM Dimming up to 20 kHz in Conjunction with I2C Dimming
  - Dynamic Backlight Control (DBC) to Reduce Current Consumption
- Up to 92% Efficiency
- Built-in 1.5x Charge Pump with Low Drop-Out Bypass Switch and automatic switching to 1x mode
- 1.2 MHz Switching Frequency for Small-Sized Capacitors
- 16-Bump 1.6 mm x 1.6 mm WLCSP (0.6 mm Height)
- 16-Lead 3.0 mm x 3.0 mm UMLP (0.55 mm Height)

Applications

- LCD Backlighting
- Mobile Handsets / Smartphones
- Portable Media Players

Description

The FAN5702 is a highly integrated and configurable charge-pump-based multi-LED driver. The device can drive up to six LEDs in parallel with a total output current of 180 mA. Regulated internal current sinks deliver excellent current and brightness matching to all LEDs.

The FAN5702 has an I²C interface that allows the user to independently control the brightness with a default grouping of 2,1,1,1,1 for a maximum of five independent lighting channels. The LED driver can be programmed in a multitude of configurations to address broad lighting requirements for different platforms. Each LED can be configured through I²C as five independent channels (Group A has two LEDs by default) or any additional LEDs can join Group A to increase the backlighting needs as the display size increases. The device offers a second dimming control using the EN/PWM pin. Applying a PWM dimming signal to this pin allows control of the dimming of Group A LEDs so that the average current is the linear value multiplied by the PWM dimming duty-cycle.

The device provides excellent efficiency, without an inductor, by operating the charge pump in 1.5x or pass-through mode.

The FAN5702 can be ordered with default I_{SET} values of 30 mA, 20 mA, 15 mA, or 8 mA. The default I_{SET} is always determined by the I_{SET} ordered *(see Ordering Information)*.

Ordering Information

Part Number	LED Current (I_{SET})	Temperature Range	Package	Packing
FAN5702UC30X	30 mA	-40 to 85°C	WLCSP-16, 0.4 mm Pitch	Tape and Reel
FAN5702UC20X	20 mA			
FAN5702UC15X	15 mA			
FAN5702UC08X	8 mA			
FAN5702UMP30X	30 mA		UMLP-16, 3.0 x 3.0 x 0.55 mm	Tape and Reel
FAN5702UMP20X	20 mA			
FAN5702UMP15X	15 mA			
FAN5702UMP08X	8 mA			

Typical Application
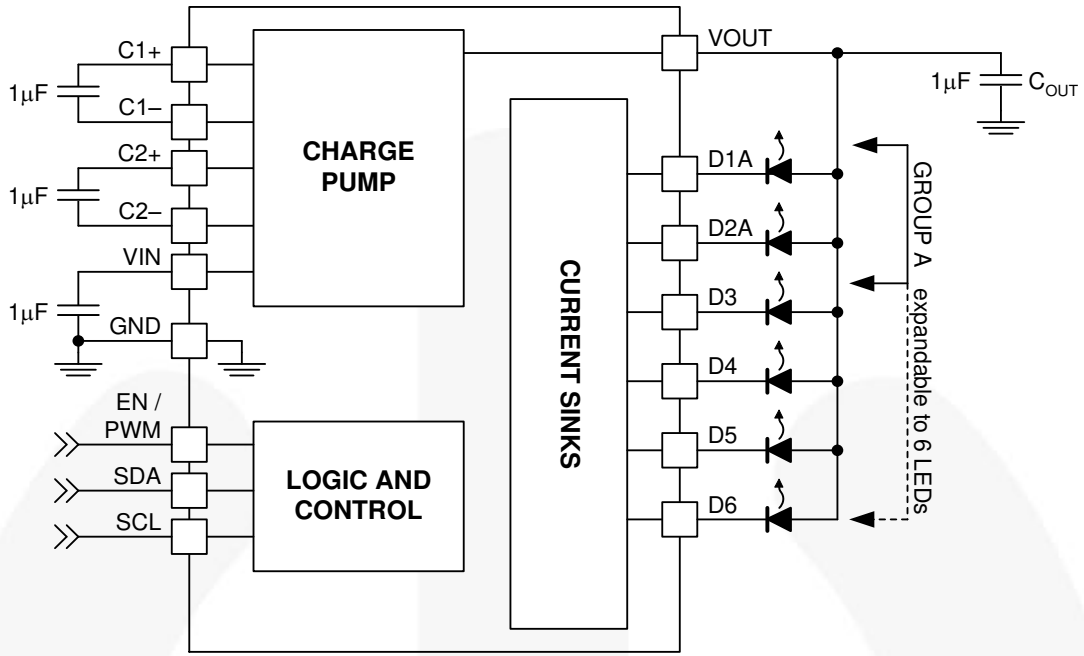
Figure 1.   Typical Application

WLCSP Pin Configuration

Bumps Facing Down

Bumps Facing Up
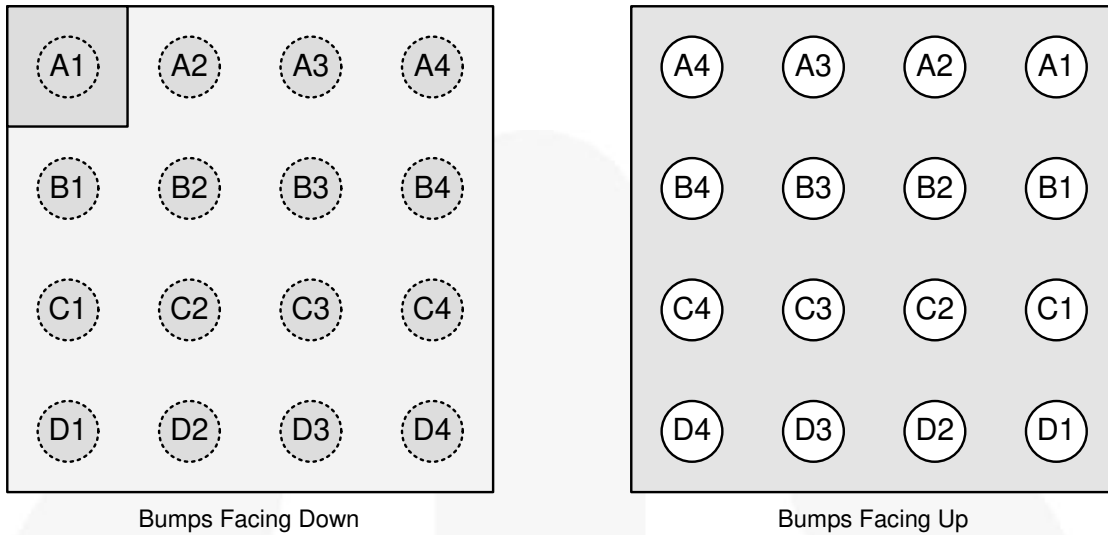
Figure 2.   WLCSP-16, 0.4 mm Pitch, 1.61 x 1.61 mm

Pin Definitions

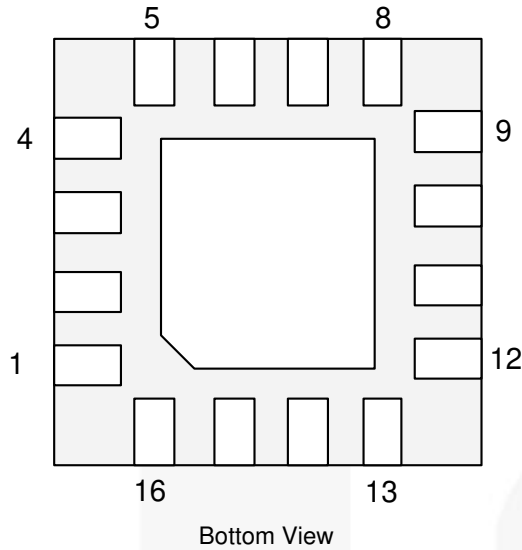| Pin #	Name	Description
D2	VIN	**Input Supply Voltage**. Connect to 2.7 – 5.5 V_{DC} input power source.
B4	GND	**Ground**
D1	VOUT	**Charge Pump Output Voltage**. Connect to LED anodes.
D3 ,D4	C1+, C1–	Charge pump flying capacitor #1
C3, C4	C2+, C2–	Charge pump flying capacitor #2
A1,A2 B1,B2 C1,C2	D2A, D1A D4,D3 D6,D5	**LED Outputs**
A4	EN / PWM	**Enable** / **PWM** dimming input. By default, this pin acts as a simple enable / disable function. When this pin is HIGH, normal operation is enabled. When LOW, the IC is reset and all functions (including I²C communications) are disabled. By setting General Purpose register bit 7 = 1, the pin functions as a PWM dimming input for Group A. To restore the Enable function, the General Purpose register bit 7 must be set LOW.
B3	SDA	I²C interface serial data
A3	SCL	I²C interface serial clock

UMLP Pin Configuration

Bottom View

Figure 3.   UMLP-16, 0.5 mm Pitch, 3 mm x 3 mm

Pin Definitions

Pin #	Name	Description
11	VIN	**Input Supply Voltage**. Connect to 2.7 – 5.5 V$_{DC}$ input power source.
6	GND	**Ground**
12	VOUT	**Charge Pump Output Voltage**. Connect to LED anodes.
10,9	C1+, C1–	Charge pump flying capacitor #1
8,7	C2+, C2–	Charge pump flying capacitor #2
1, 2 15, 16 13, 14	D2A, D1A D4,D3 D6,D5	**LED Outputs**
4	EN / PWM	**Enable** / **PWM** dimming input. By default, this pin acts as a simple enable / disable function. When this pin is HIGH, normal operation is enabled. When LOW, the IC is reset and all functions (including I²C communications) are disabled. By setting General Purpose register bit 7 = 1, the pin functions as a PWM dimming input for Group A. To restore the Enable function, the General Purpose register bit 7 must be set LOW.
5	SDA	I²C interface serial data
3	SCL	I²C interface serial clock

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{CC}	VIN, VOUT Pins		−0.3	6.0	V
	Other Pins[1]		−0.3	V_{IN} + 0.3	V
ESD	Electrostatic Discharge Protection Level	Human Body Model per JESD22-A114	3		kV
		Charged Device Model per JESD22-C101	2		
T_J	Junction Temperature		−40	+150	°C
T_{STG}	Storage Temperature		−65	+150	°C
T_L	Lead Soldering Temperature, 10 Seconds			+260	°C

Note:
1. Lesser of V_{IN} + 0.3 or 6.0 V.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Unit
V_{IN}	Supply Voltage	2.7	5.5	V
V_{LED}	LED Forward Voltage	2	4	V
T_A	Ambient Temperature	−40	+85	°C
T_J	Junction Temperature	−40	+125	°C

Thermal Properties

Symbol	Parameter		Min.	Typ.	Max.	Unit
Θ_{JA}	Junction-to-Ambient Thermal Resistance	WLCSP		80		°C/W
		UMLP		49		

Note:
2. Junction-to-ambient thermal resistance is a function of application and board layout. This data is measured with four-layer 2s2p boards in accordance to JESD51-7 JEDEC standard. Special attention must be paid not to exceed junction temperature $T_{J(max)}$ at a given ambient temperate T_A.

Electrical Specifications

Unless otherwise specified: V_{IN} = 2.7 V to 5.5 V; T_A = -40°C to +85°C; and ENA, EN3, EN4, EN5, and EN6 = 1. Typical values are V_{IN} = 3.6 V, T_A = 25°C, I_{LED} = 20 mA, and LED cathode terminals = 0.4 V. Circuit and components are according to Figure 1.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Power Supplies and Thermal Protection						
I_Q	Quiescent Supply Current	1.5x Mode, No LEDs		4.4		mA
		1x Mode, No LEDs		0.3		
I_{SD}	Shutdown Supply Current	EN = 0, V_{IN} = 4.5V, T_A = -40°C to +85°C		0.1	2.0	µA
V_{UVLO}	Under-Voltage Lockout Threshold	V_{IN} Rising		2.55	2.70	V
		V_{IN} Falling	2.20	2.40		
V_{UVHYST}	Under-Voltage Lockout Hysteresis			150		mV
T_{LIMIT}	Thermal Shutdown			150		°C
T_{HYST}	Thermal Shutdown Hysteresis			20		°C
LED Current Sinks						
I_{LED}	Absolute Current Accuracy	$V_{CATHODE}$ = 0.4 V; *see options for I_{SET}*	−10%	I_{SET}	+10%	mA
$I_{LED(MAX)}$	Maximum Diode Current[3]	I_{LED} = I_{SET}		30		mA
I_{LED_MATCH}	LED Current Matching[4]	$V_{CATHODE}$ = 0.4 V, I_{LED} = I_{SET}		0.4	3.0	%
V_{DTH}	1x to 1.5x Gain Transition Threshold	LED Cathode Voltage Falling		100		mV
V_{HR}	Current Sink Headroom[5]	I_{LED} = 90% $I_{LED(NOMINAL)}$		65		mV
PWM Dimming						
f_{PWM}	PWM Switching Frequency	$t_{ON\_LED(MINIMUM)}$ = 15 µs			20	kHz
D_{PWM}	PWM Duty-Cycle	f_{PWM} = 100 Hz	0.15		100.00	%
Charge Pump						
R_{OUT}	Output Resistance	1.5x Mode		2.4		Ω
		1x Mode		0.9		
f_{SW}	Switching Frequency		0.9	1.2	1.5	MHz
t_{START}	Startup Time	V_{OUT} = 90% of V_{IN}		250		µs
Logic Inputs (EN, SDA, SCL)						
V_{IH}	HIGH-Level Input Voltage		1.2			V
V_{IL}	LOW-Level Input Voltage				0.4	V
V_{IMAX}	Maximum Input Voltage			1.8	5.5	V
I_{IN}	Input Bias Current	Input Tied to GND or V_{IN}		0.01	1.00	µA

Notes:
3. The maximum total output current for the IC should be limited to 180 mA. The total output current can be split between the two groups (IDxA = IDxB = 30 mA maximum). Under maximum output current conditions, special attention must be given to input voltage and LED forward voltage to ensure proper current regulation. *See the Maximum Output Current section of the datasheet for more information.*
4. For the two groups of current sinks on a part (group A and group B), the following are determined: the maximum sink current in the group (MAX), the minimum sink current in the group (MIN), and the average sink current of the group (AVG). For each group, two matching numbers are calculated: (MAX-AVG)/AVG and (AVG-MIN)/AVG. The largest number of the two (worst case) is considered the matching value for the group. The matching value for a given part is considered to be the highest matching value of the two groups. The typical specification provided is the most likely norm of the matching value for all parts.
5. For each Dxx pin, headroom voltage is the voltage across the internal current sink connected to that pin. V_{HRx} = V_{OUT} - V_{LED}. If headroom voltage requirement is not met, LED current regulation is compromised.

Typical Characteristics

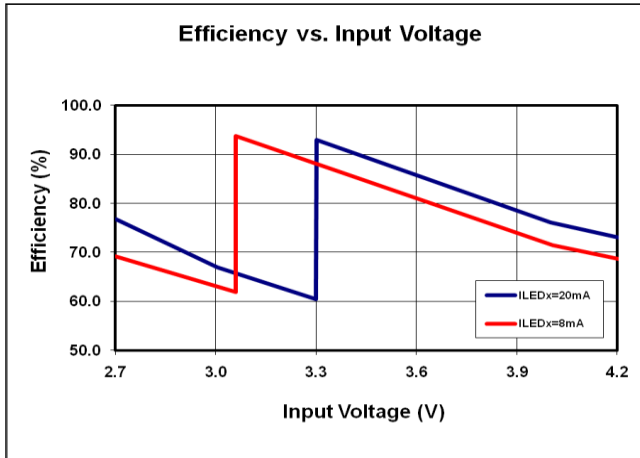V_{IN} = 3.6 V, T_A = 25°C, I_{LED} = 20 mA, and LED cathode terminals = 0.4 V.

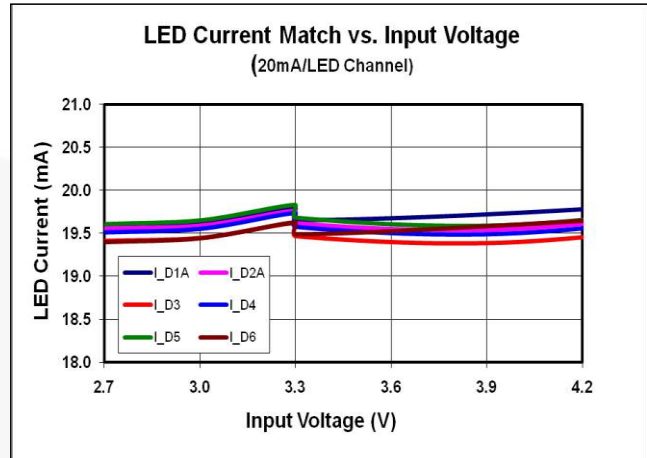Figure 4.   Efficiency with LED Current of 8 mA and 20 mA

Figure 5.   LED Current Match for all 6 LED Channels at I_{LED}=20 mA
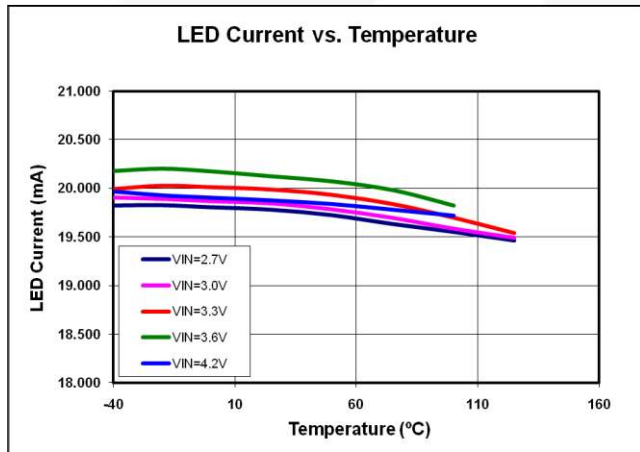

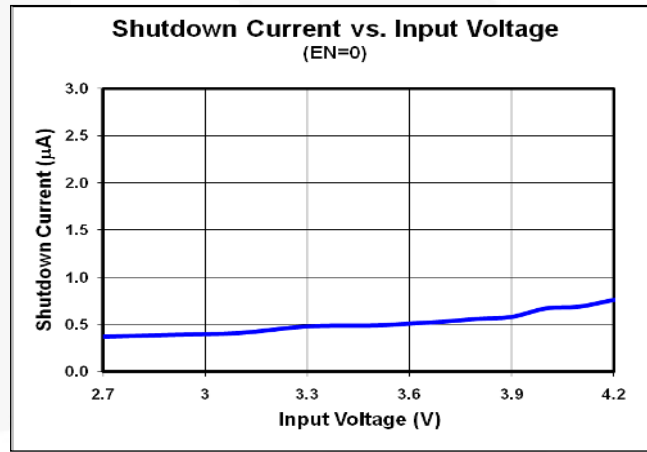Figure 6.   LED Current Variation vs. Temperature
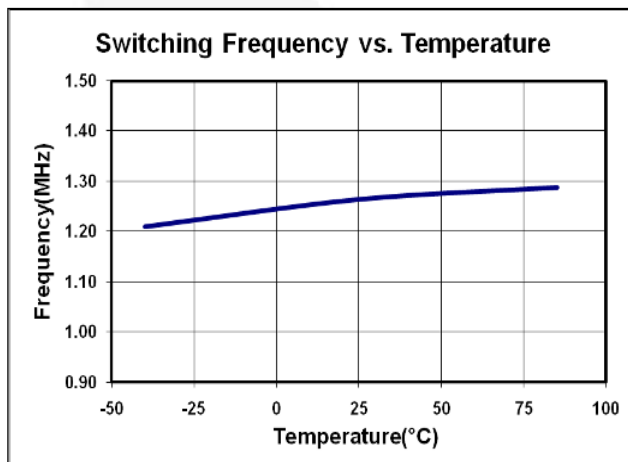

Figure 7.   Shutdown Current vs. Input Voltage

Figure 8.   Switching Frequency Over-Temperature with LED Current at 20 mA
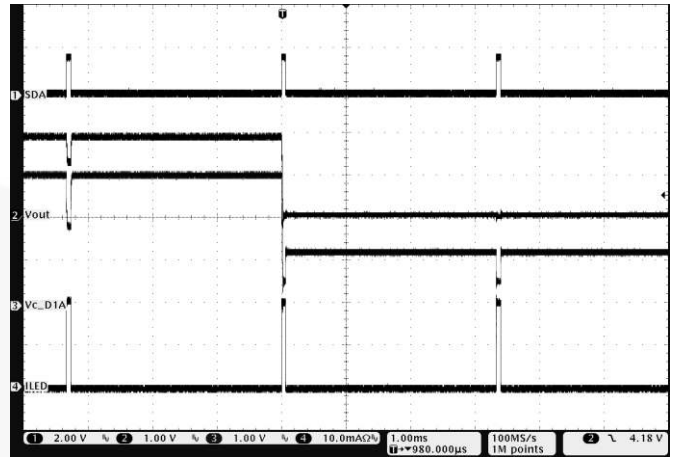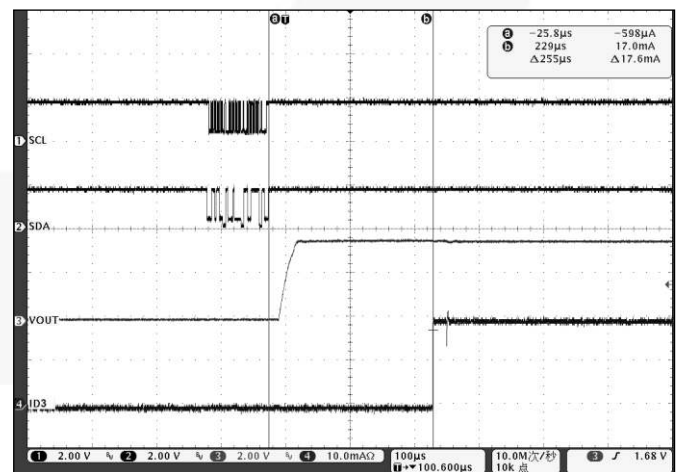
Typical Characteristics

Figure 15.   Linear Dimming via I²C Interface, V_IN=3.6 V, I_LEDx=20 mA, and t_RAMP=6.4 ms

Figure 16.   PWM Dimming, V_IN=3.6 V, I_LEDx=20 mA, and EN=1 kHz with 20% Duty Cycle
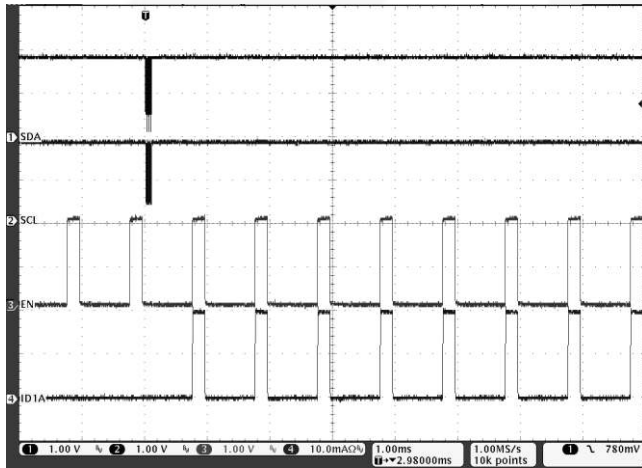
Figure 17.   PWM and Linear (via I²C) Dimming, V_IN=3.6 V, I_LEDx=20 mA, and EN=1 kHz with 20% Duty Cycle

I²C Timing Specifications

Guaranteed by design.

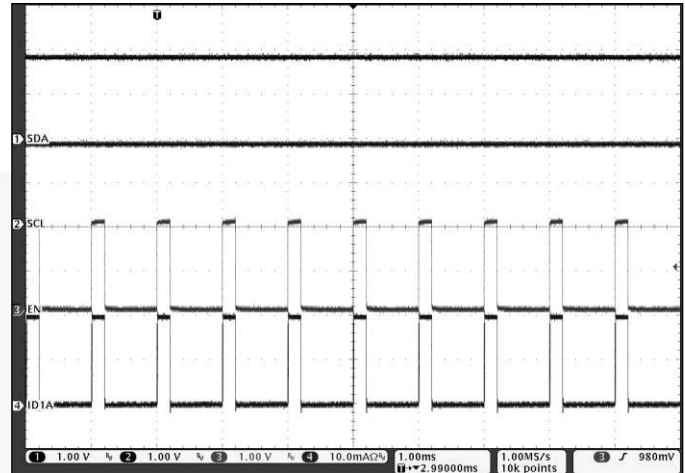| Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{SCL}	SCL Clock Frequency	Standard Mode			100	kHz
		Fast Mode			400	
t_{BUF}	Bus-Free Time between STOP and START Conditions	Standard mode		4.7		µs
		Fast Mode		1.3		
$t_{HD;STA}$	START or Repeated START Hold Time	Standard Mode		4		µs
		Fast Mode		600		ns
t_{LOW}	SCL LOW Period	Standard Mode		4.7		µs
		Fast Mode		1.3		ns
t_{HIGH}	SCL HIGH Period	Standard Mode		4		µs
		Fast Mode		600		ns
$t_{SU;STA}$	Repeated START Setup Time	Standard Mode		4.7		µs
		Fast Mode		600.0		ns
$t_{SU;DAT}$	Data Setup Time	Standard Mode		250		ns
		Fast Mode		100		ns
$t_{HD;DAT}$	Data Hold Time	Standard Mode	0		3.45	µs
		Fast Mode	0		900.00	ns
t_{RCL}	SCL Rise Time	Standard Mode	$20+0.1C_B$		1000	ns
		Fast Mode	$20+0.1C_B$		300	ns
t_{FCL}	SCL Fall Time	Standard Mode	$20+0.1C_B$		300	ns
		Fast Mode	$20+0.1C_B$		300	ns
t_{RDA}	SDA Rise Time[6]	Standard Mode	$20+0.1C_B$		1000	ns
		Fast Mode	$20+0.1C_B$		300	ns
t_{FDA}	SDA Fall Time	Standard Mode	$20+0.1C_B$		300	ns
		Fast Mode	$20+0.1C_B$		300	ns
$t_{SU;STO}$	Stop Condition Setup Time	Standard Mode		4		µs
		Fast Mode		600		ns
C_B	Capacitive Load for SDA and SCL				400	pF

Note:
6. Rise time of SCL after a repeated START condition and after an ACK bit.
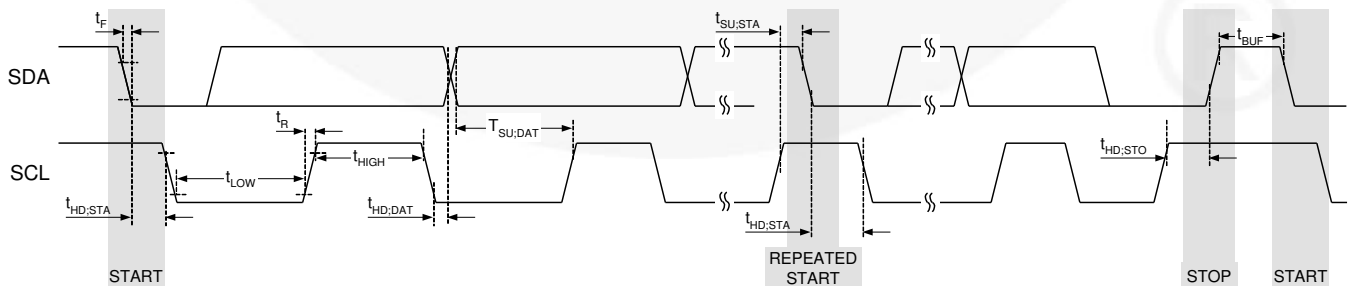
Timing Diagram

Figure 18.   I²C Interface Timing for Fast and Slow Modes

Circuit Description

The FAN5702 is a white LED driver system based on an adaptive 1.5x charge pump capable of supplying up to 180 mA of total output current. The tightly matched current sinks ensure uniform brightness between the LEDs. Each LED has a common anode configuration with its peak drive current set during manufacturing (*see Ordering Information and I_{SET}*). An I²C-compatible interface is used to vary the brightness within the individual current sinks as well as configure the grouping. Each LED is controlled with 64 exponentially spaced analog brightness control levels through I²C, as indicated in Table 1. For maximum flexibility, the FAN5702 can be programmed with five independently controlled LED banks; by default, arranged as 2,1,1,1,1 (first two LEDs represent Group A). Through I²C, the device can be reconfigured to add up to six LEDs to Group A as needed by application requirements.

Charge Pump

The charge pump operates in either 1x mode, where V_{OUT} is connected to V_{IN} through a bypass switch, or in 1.5x mode. The circuit operates in 1x mode until the LED with the highest forward voltage ($V_{LED(MAX)}$) can no longer maintain current regulation. At that point, 1.5x Mode begins. If the lowest active cathode voltage is greater than 1.8 V, the charge pump switches back to 1x Mode.

IC Enable

By default the General Purpose register bit 7 = 0, the EN pin functions as enable/disable. When the EN pin is LOW, all circuit functions, including I²C, are disabled and the registers are set to their default values.

When the EN pin HIGH, I²C interface is enabled. The LEDs can be turned on/off by writing to the General Purpose register. The user can always communicate via I²C with the device to change register settings regardless of whether any LED is on or off.

PWM Dimming

By programming the General Purpose register bit 7 = 1, the EN pin is reappropriated to a PWM dimming input. Applying a PWM signal to this pin controls the LED current waveform to be ON when the PWM dimming pin is HIGH and OFF when the PWM dimming pin is LOW. By using this pin in conjunction with the I²C register dimming, the part can achieve higher dimming resolution. For instance, an 8-bit PWM dimming signal applied along with the 6-bit register dimming yields better than 14 bits of resolution

To change the PWM dimming pin back to the EN function, set the General Purpose register bit 7 to 0.

Register Controlled Brightness

The DC value of the LED current is modulated according to the values in Table 1. Current is expressed as a percentage of the full scale current and is illustrated with a 20 mA I_{SET}.

Table 1.   Brightness Control

Dimming Code (Bx5-Bx0)	Current Level	I_{LED} (mA) (I_{SET}=20 mA)
000000	0.125%	0.025
000001	0.188%	0.038
000010	0.249%	0.050
000011	0.312%	0.063
000100	0.374%	0.075
000101	0.438%	0.088
000110	0.499%	0.100
000111	0.560%	0.113
001000	0.622%	0.125
001001	0.692%	0.138
001010	0.750%	0.150
001011	0.810%	0.163
001100	0.875%	0.175
001101	0.938%	0.188
001110	1.004%	0.200
001111	1.124%	0.225
010000	1.250%	0.250
010001	1.375%	0.275
010010	1.499%	0.300
010011	1.625%	0.325
010100	1.750%	0.350
010101	1.881%	0.375
010110	2.063%	0.413
010111	2.249%	0.450
011000	2.438%	0.488
011001	2.687%	0.538
011010	2.939%	0.588
011011	3.186%	0.638
011100	3.562%	0.713
011101	3.936%	0.788
011110	4.310%	0.863
011111	4.813%	0.963
100000	5.314%	1.063
100001	5.936%	1.188
100010	6.565%	1.313
100011	7.313%	1.463
100100	8.059%	1.613
100101	8.938%	1.788
100110	9.876%	1.975
100111	10.874%	2.175
101000	12.005%	2.400
101001	13.253%	2.650
101010	14.618%	2.925
101011	16.124%	3.225
101100	17.881%	3.575
101101	19.875%	3.975
101110	22.121%	4.425
101111	24.621%	4.925
110000	27.376%	5.475
110001	30.373%	6.075
110010	33.623%	6.725
110011	37.124%	7.425
110100	40.873%	8.175
110101	44.875%	8.975
110110	49.124%	9.825
110111	53.624%	10.725
111000	58.375%	11.675
111001	63.378%	12.675
111010	68.625%	13.725
111011	74.122%	14.825
111100	79.874%	15.975
111101	85.873%	17.175
111110	92.373%	18.475
111111	100.000%	20.000

Brightness Ramp Control

When changing the group A brightness, the IC steps through the brightness table at rate programmed by the RAMP register, indicated in Table 2.

Table 2.   Group A Brightness Ramp Control

RAMP[1:0]	Time per Step	Full-Scale Ramp Time
00	0.1 ms	6.4 ms
01	25 ms	1600 ms
10	50 ms	3200 ms
11	100 ms	6400 ms

V_{OUT} Short-Circuit Protection

The FAN5702 has integrated protection circuitry to prevent the device from being short circuited when the output voltage falls below 2 V. If this occurs, FAN5702 turns off the charge pump and the LED driver outputs, but a small bypass switch is left on. The device monitors the output voltage to determine if it is still in short circuit condition and, once it has passed, soft-starts and returns to normal operation.

V_{OUT} Over-Voltage Protection

If the output voltage goes above 6 V, the FAN5702 shuts down until this condition has passed. The charge pump and LED driver outputs are turned off. Once this condition has passed, the FAN5702 soft-starts into normal operation.

I²C Interface

The FAN5702's serial interface is compatible with standard and fast I²C bus specifications. The FAN5702's SCL line is an input and its SDA line is a bi-directional open-drain output, meaning that it can only pull down the bus when active. The SDA line only pulls LOW during data reads and when signaling ACK. All data is shifted in MSB (bit 7) first.

Slave Address

The FAN5702's slave address is 6CH.

Table 3.   I²C Slave Address

7	6	5	4	3	2	1	0
0	1	1	0	1	1	0	R/$\overline{\text{W}}$

Register Addressing

The FAN5702 has six user-accessible registers.

Table 4.   I²C Register Addresses

	Default Value								Address
	7	6	5	4	3	2	1	0	HEX
GENERAL	0	0	0	0	0	0	0	0	10
CONFIG	0	0	0	0	0	0	0	0	20
CHA	**1**	**1**	1	1	1	1	1	1	A0
CH3	**1**	**1**	1	1	1	1	1	1	30
CH4	**1**	**1**	1	1	1	1	1	1	40
CH5	**1**	**1**	1	1	1	1	1	1	50
CH6	**1**	**1**	1	1	1	1	1	1	60

Note:

7.   Bold identifies bits that cannot be overwritten.

Bus Timing

As shown in Figure 19 data is normally transferred when SCL is LOW. Data is clocked in to the FAN5702 on the rising edge of SCL. Typically, data transitions shortly at or after the falling edge of SCL to allow ample time for the data to set up before the next SCL rising edge.
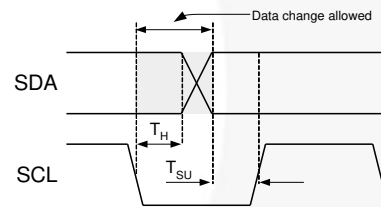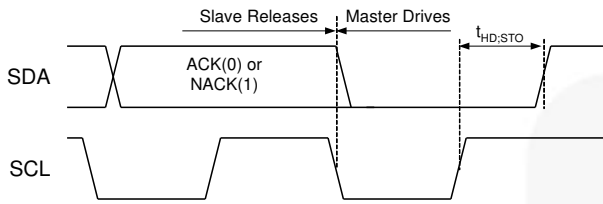

Figure 19.   Data Transfer Timing

Each bus transaction begins and ends with SDA and SCL HIGH. A transaction begins with a START condition, which is defined as SDA transitioning from 1 to 0 with SCL HIGH, as shown in Figure 20.
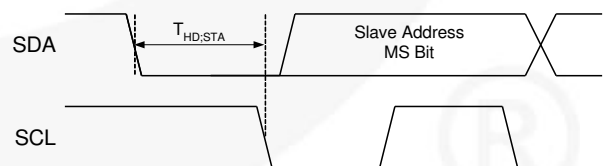

Figure 20.   Start Bit

A transaction ends with a STOP condition, which is defined as SDA transitioning from 0 to 1 with SCL HIGH, as shown in Figure 21.

Figure 21.   Stop Bit

During a read from the FAN5702 (Figure 24, the master issues a "Repeated Start" after sending the register address and before resending the slave address. The "Repeated Start" is a 1-to-0 transition on SDA while SCL is HIGH, as shown in Figure 22.
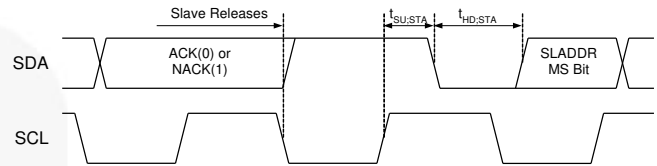


Figure 22.   Repeated Start Timing

Read and Write Transactions

The following figures outline the sequences for data read and write. Bus control is signified by the shading of the packet, defined as Master Drives Bus and Slave Drives Bus. All addresses and data are MSB first.

Table 5.   I²C bit Definitions for Figure 23 and Figure 24.

Symbol	Definition
S	START. *See Figure 20.*
A	ACK. The slave drives SDA to 0 to acknowledge the preceding packet.
$\overline{A}$	NACK. The slave sends a 1 to NACK the preceding packet.
R	Repeated START. *See Figure 22*
P	STOP. *See Figure 21.*
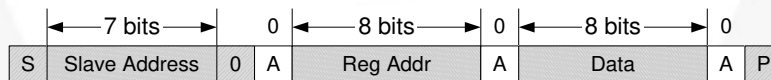
Figure 23.   Write Transaction

Figure 24.   Read Transaction

Register Descriptions

The following tables define the operation of each register bit. **Bold** values are power-up defaults. These values apply only to I²C version of the part.
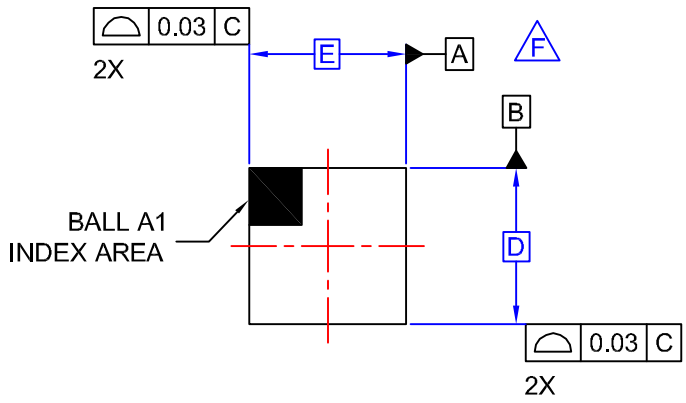
Bit	Name	Default Value	Description
GENERAL	**Default: 00H**	**General Purpose Register**	**ADDR = 10H**
7	PWM	**0**	Setting this bit=1 changes the EN pin to function as a PWM dimming input for group A LEDs. This bit must be set to zero for the chip to be disabled.
6,5	FS1, FS2	**00**	00=20 mA (default), 01=30 mA, 10=15 mA, 11=8 mA when I²C is used.
4	EN6	**0**	Default=0 (Off), LED Channel Active=1
3	EN5	**0**	Default=0 (Off), LED Channel Active=1
2	EN4	**0**	Default=0 (Off), LED Channel Active=1
1	EN3	**0**	Default=0 (Off), LED Channel Active=1
0	ENA	**0**	Default=0 (Off), LED Channel Active=1
CONFIG	**Default: 00H**	**Configuration Register**	**ADDR = 20H**
7	T56	**0**	Tie channel 5 and 6 together. Default=0 (Separate). Group 5&6 =1. Both currents are set by CH5 register. T56 is overwritten by either S5A or S6A.
6	T34	**0**	Tie channel 3 and 4 together. Default=0 (Separate). Group 3&4 =1. Both currents are set by the CH3 register. T34 is overwritten by either S3A or S4A.
5	S6A	**0**	CH6 group configuration. Independent=0 (default); part of group A=1.
4	S5A	**0**	CH5 group configuration. Independent=0 (default); part of group A=1.
3	S4A	**0**	CH4 group configuration. Independent=0 (default); part of group A=1.
2	S3A	**0**	CH3 group configuration. Independent=0 (default); part of group A=1.
1,0	RS1, RS0	**00**	Sets current ramp rate for group A channels
CHA	**Default: FFH**	**Group A Brightness Control**	**ADDR = A0H**
7:6	Reserved	**11**	Vendor ID bits. These bits can be used to distinguish between vendors via I²C. Writing to these bits does not change their value.
5:0	Brightness A	**0 – 63** **00 – 3FH**	6-bit value that controls group A brightness per values in Table 1
CH3	**Default:**	**Channel 3 Brightness Control**	**ADDR=30H**
7:6	Reserved	**11**	Writing to these bits does not change their value.
5:0	Brightness 3	**0 – 63** **00 – 3FH**	6-bit value that controls channel 3 brightness per values in Table 1
CH4	**Default: FFH**	**Channel 4 Brightness Control**	**ADDR = 40H**
7:6	Reserved	**11**	Writing to these bits does not change their value.
5:0	Brightness 4	**0 – 63** **00 – 3FH**	6-bit value that controls channel 3 brightness per values in Table 1
CH5	**Default: FFH**	**Channel 5 Brightness Control**	**ADDR = 50H**
7:6	Reserved	**11**	Writing to these bits does not change their value.
5:0	Brightness 5	**0 – 63** **00 – 3FH**	6-bit value that controls channel 3 brightness per values in Table 1
CH6	**Default: FFH**	**Channel 6 Brightness Control**	**ADDR = 60H**
7:6	Reserved	**11**	Writing to these bits does not change their value.
5:0	Brightness 6	**0 – 63** **00 – 3FH**	6-bit value that controls channel 3 brightness per values in Table 1

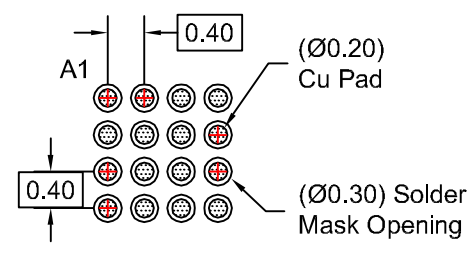The table below pertains to the Marketing Outline drawing on the following page…

Product-Specific Dimensions

Product	D	E	X	Y
FAN5702UCxx	1.610 mm	1.610 mm	0.205 mm	0.205 mm

⌒ 0.03 C
2X

E → ▶ A   △F

B

BALL A1 INDEX AREA

D

⌒ 0.03 C
2X

TOP VIEW

0.40

A1   (Ø0.20) Cu Pad

0.40   (Ø0.30) Solder Mask Opening

RECOMMENDED LAND PATTERN
(NSMD PAD TYPE)

// 0.06 C

0.625
0.547   △E

⌒ 0.05 C

C

SEATING PLANE   △D

SIDE VIEWS

0.378±0.018
0.208±0.021

⊕ 0.005Ⓜ C A B

0.40   Ø0.260±0.02 16X

D
C
B
A   (Y) ±0.018

0.40

1 2 3 4   △F

(X) ±0.018
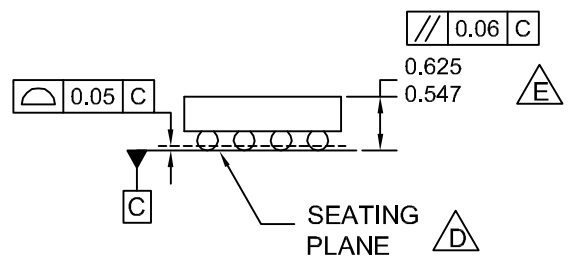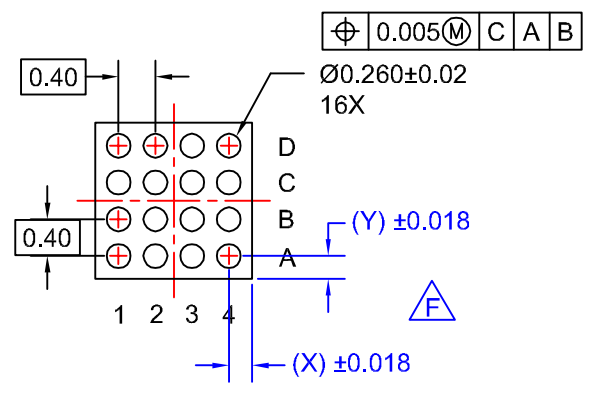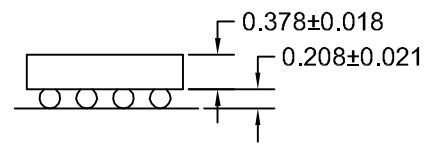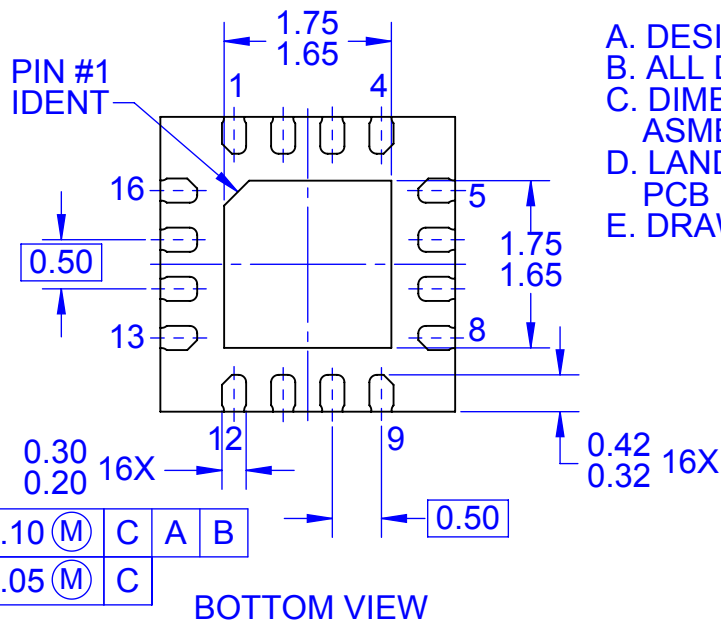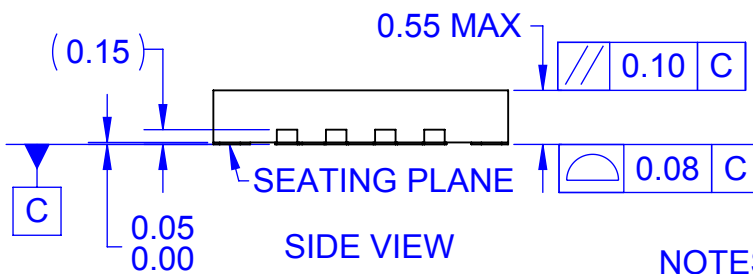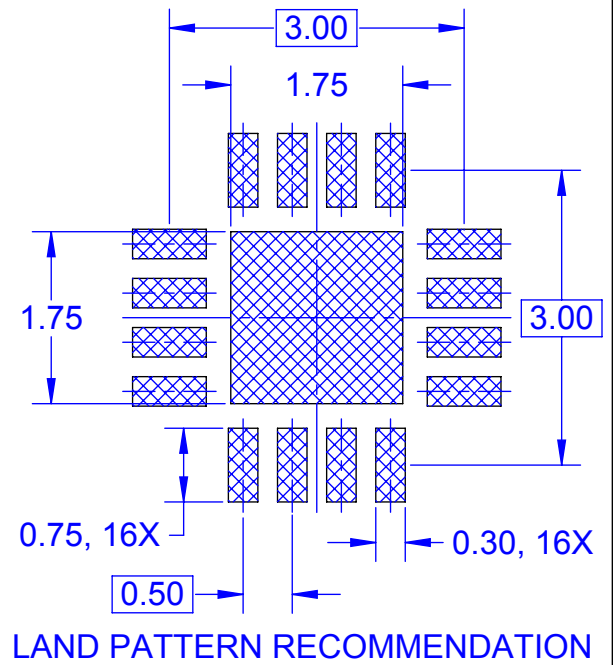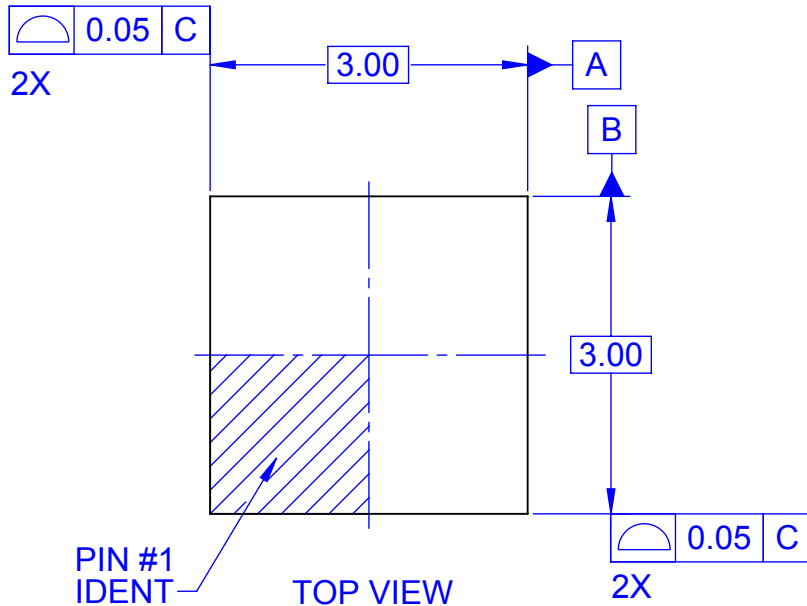
BOTTOM VIEW

NOTES:

A. NO JEDEC REGISTRATION APPLIES.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCE PER ASME Y14.5M, 1994.

△D DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.

△E PACKAGE NOMINAL HEIGHT IS 586 MICRONS ±39 MICRONS (547-625 MICRONS).

△F FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.

G. DRAWING FILNAME: MKT-UC016AArev2.

APPROVALS	DATE	FAIRCHILD SEMICONDUCTOR™		
DRAWN L. England	10-26-09			
DFTG. CHK. E. Shacham	10-26-09	16BALL WLCSP, 4X4 ARRAY 0.4MM PITCH, 250UM BALL		
ENGR. CHK.				
		SCALE N/A	SIZE N/A	DRAWING NUMBER MKT-UC016AA	REV 2
PROJECTION INCH [MM]		DO NOT SCALE DRAWING		SHEET 1 of 1

⌒ | 0.05 | C

2X

3.00 → A

B

3.00

PIN #1 IDENT

⌒ | 0.05 | C

2X

TOP VIEW

3.00

1.75

1.75

3.00

0.75, 16X

0.30, 16X

0.50

LAND PATTERN RECOMMENDATION

(0.15)

0.55 MAX

∥ | 0.10 | C

⌒ | 0.08 | C

SEATING PLANE

C

0.05
0.00

SIDE VIEW

NOTES:

A. DESIGN CONFORMS TO JEDEC MO-248
B. ALL DIMENSIONS ARE IN MILLIMETERS
C. DIMENSIONS AND TOLERANCES PER
   ASME Y14.5M, 2009
D. LAND PATTERN RECOMMENDATION FROM
   PCB MATRIX IPC LP CALCULATOR (V2009)
E. DRAWING FILENAME: MKT-UMLP16Brev2

1.75
1.65

PIN #1 IDENT

1   4

16   5

0.50

13   8

1.75
1.65

12   9

0.30
0.20   16X

0.50

0.42   16X
0.32

⊕ | 0.10 Ⓜ | C | A | B
  | 0.05 Ⓜ | C

BOTTOM VIEW

FAIRCHILD ™

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