

## 74LCX821

# Low Voltage 10-Bit D-Type Flip-Flop with 5V Tolerant Inputs and Outputs

### General Description

The LCX821 consists of ten D-type Flip-Flops with 3-STATE outputs for bus organized system applications. The device is designed for low voltage (2.5V or 3.3V)  $V_{CC}$  applications with capability of interfacing to a 5V signal environment.

The LCX821 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

### Features

- 5V tolerant inputs and outputs
- 2.3V–3.6V  $V_{CC}$  specifications provided
- 7.0 ns  $t_{PD}$  max ( $V_{CC} = 3.3V$ ), 10  $\mu A$   $I_{CC}$  max
- Power-down high impedance inputs and outputs
- Supports live insertion/withdrawal (Note 1)
- $\pm 24$  mA output drive ( $V_{CC} = 3.0V$ )
- Implements patented noise/EMI reduction circuitry
- Latch-up performance exceeds 500 mA
- ESD performance:
  - Human Body Model > 2000V
  - Machine Model > 200V

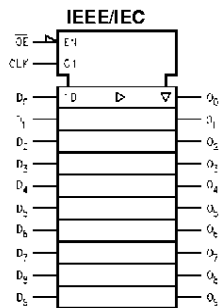
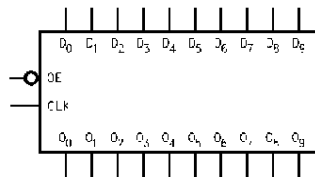
**Note 1:** To ensure the high-impedance state during power up or down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pull-up resistor. The minimum value of the resistor is determined by the current-sourcing capability of the driver.

### Ordering Code:

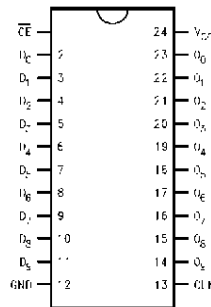
Order Number	Package Number	Package Description
74LCX821WM	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74LCX821MSA	MSA24	24-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
74LCX821MTC	MTC24	24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix 'X' to the ordering code.

### Logic Symbols



### Connection Diagram



## Pin Descriptions

Pin Names	Description
D <sub>0</sub> –D <sub>9</sub>	Data Inputs
CLK	Clock Input
$\overline{OE}$	Output Enable Input
O <sub>0</sub> –O <sub>9</sub>	3-STATE Latch Outputs

## Function Table

Inputs			Internal	Outputs	Function
$\overline{OE}$	CLK	D	Q	O <sub>n</sub>	
H	H	L	NC	Z	Hold
H	H	H	NC	Z	Hold
H	$\nearrow$	L	L	Z	Load
H	$\nearrow$	H	H	Z	Load
L	$\nearrow$	L	L	L	Data Available
L	$\nearrow$	H	H	H	Data Available
L	H	L	NC	NC	No Change in Data
L	H	H	NC	NC	No Change in Data

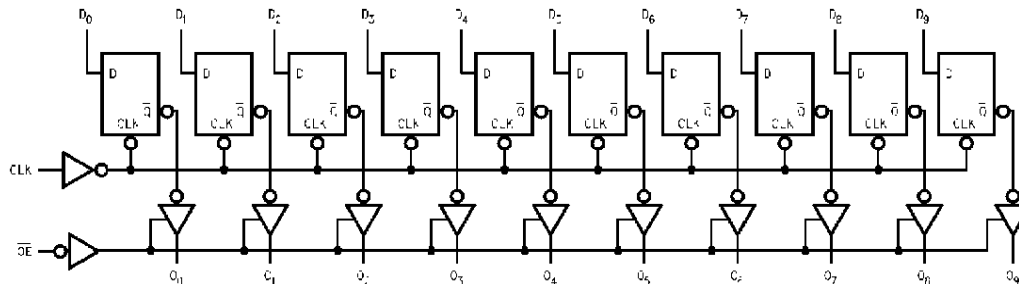
H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 Z = High Impedance  
 $\nearrow$  = LOW-to-HIGH Transition  
 NC = No Change

## Functional Description

The LCX821 consists of ten edge-triggered flip-flops with individual D-type inputs with 3-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The ten flip-flops will store the state of their individual D inputs that meet the setup and hold time

requirements on the LOW-to-HIGH Clock (CLK) transition. With the Output Enable ( $\overline{OE}$ ) LOW, the contents of the ten flip-flops are available at the outputs. When  $\overline{OE}$  is HIGH, the outputs go to the high impedance state. Operation of the  $\overline{OE}$  input does not affect the state of the flip-flops.

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays

Absolute Maximum Ratings (Note 2)				
Symbol	Parameter	Value	Conditions	Units
$V_{CC}$	Supply Voltage	-0.5 to +7.0		V
$V_I$	DC Input Voltage	-0.5 to +7.0		V
$V_O$	DC Output Voltage	-0.5 to +7.0 -0.5 to $V_{CC} + 0.5$	Output in 3-STATE Output in HIGH or LOW State (Note 3)	V
$I_{IK}$	DC Input Diode Current	-50	$V_I < GND$	mA
$I_{OK}$	DC Output Diode Current	-50 +50	$V_O < GND$ $V_O > V_{CC}$	mA
$I_O$	DC Output Source/Sink Current	$\pm 50$		mA
$I_{CC}$	DC Supply Current per Supply Pin	$\pm 100$		mA
$I_{GND}$	DC Ground Current per Ground Pin	$\pm 100$		mA
$T_{STG}$	Storage Temperature	-65 to +150		$^{\circ}C$

Recommended Operating Conditions (Note 4)					
Symbol	Parameter	Min	Max	Units	
$V_{CC}$	Supply Voltage	Operating	2.0	3.6	V
		Data Retention	1.5	3.6	
$V_I$	Input Voltage	0	5.5	V	
$V_O$	Output Voltage	HIGH or LOW State	0	$V_{CC}$	V
		3-STATE	0	5.5	
$I_{OH}/I_{OL}$	Output Current	$V_{CC} = 3.0V - 3.6V$		$\pm 24$	mA
		$V_{CC} = 2.7V - 3.0V$		$\pm 12$	
		$V_{CC} = 2.3V - 2.7V$		$\pm 8$	
$T_A$	Free-Air Operating Temperature	-40	85	$^{\circ}C$	
$\Delta t/\Delta V$	Input Edge Rate, $V_{IN} = 0.8V - 2.0V$ , $V_{CC} = 3.0V$	0	10	ns/V	

**Note 2:** The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The 'Recommended Operating Conditions' table will define the conditions for actual device operation.

**Note 3:**  $I_O$  Absolute Maximum Rating must be observed.

**Note 4:** Unused inputs must be held HIGH or LOW. They may not float.

### DC Electrical Characteristics

Symbol	Parameter	Conditions	$V_{CC}$ (V)	$T_A = -40^{\circ}C$ to $+85^{\circ}C$		Units
				Min	Max	
$V_{IH}$	HIGH Level Input Voltage		2.3 - 2.7	1.7		V
			2.7 - 3.6	2.0		
$V_{IL}$	LOW Level Input Voltage		2.3 - 2.7		0.7	V
			2.7 - 3.6		0.8	
$V_{OH}$	HIGH Level Output Voltage	$I_{OH} = -100 \mu A$	2.3 - 3.6	$V_{CC} - 0.2$		V
		$I_{OH} = -8 mA$	2.3	1.8		
		$I_{OH} = -12 mA$	2.7	2.2		
		$I_{OH} = -18 mA$	3.0	2.4		
		$I_{OH} = -24 mA$	3.0	2.2		
$V_{OL}$	LOW Level Output Voltage	$I_{OL} = 100 \mu A$	2.3 - 3.6	0.2		V
		$I_{OL} = 8 mA$	2.3	0.6		
		$I_{OL} = 12 mA$	2.7	0.4		
		$I_{OL} = 16 mA$	3.0	0.4		
		$I_{OL} = 24 mA$	3.0	0.55		
$I_I$	Input Leakage Current	$0 \leq V_I \leq 5.5V$	2.3 - 3.6	$\pm 5.0$		$\mu A$
$I_{OZ}$	3-STATE Output Leakage	$0 \leq V_O \leq 5.5V$ $V_I = V_{IH}$ or $V_{IL}$	2.3 - 3.6	$\pm 5.0$		$\mu A$
$I_{OFF}$	Power-Off Leakage Current	$V_I$ or $V_O = 5.5V$	0	10		$\mu A$

## DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = -40°C to +85°C		Units
				Min	Max	
I <sub>CC</sub>	Quiescent Supply Current	V <sub>I</sub> = V <sub>CC</sub> or GND	2.3 – 3.6		10	μA
		3.6V ≤ V <sub>I</sub> , V <sub>O</sub> ≤ 5.5V (Note 5)	2.3 – 3.6		±10	
ΔI <sub>CC</sub>	Increase in I <sub>CC</sub> per Input	V <sub>IH</sub> = V <sub>CC</sub> - 0.6V	2.3 – 3.6		500	μA

**Note 5:** Outputs disabled or 3-STATE only

## AC Electrical Characteristics

Symbol	Parameter	T <sub>A</sub> = -40°C to +85°C, R <sub>L</sub> = 500Ω						Units
		V <sub>CC</sub> = 3.3V ± 0.3V		V <sub>CC</sub> = 2.7V		V <sub>CC</sub> = 2.5V ± 0.2V		
		C <sub>L</sub> = 50 pF		C <sub>L</sub> = 50 pF		C <sub>L</sub> = 30 pF		
		Min	Max	Min	Max	Min	Max	
f <sub>MAX</sub>	Maximum Clock Frequency	150						MHz
t <sub>PHL</sub>	Propagation Delay	1.5	7.0	1.5	7.5	1.5	8.4	ns
t <sub>PLH</sub>	CLK to O <sub>n</sub>	1.5	7.0	1.5	7.5	1.5	8.4	
t <sub>PZL</sub>	Output Enable Time	1.5	7.5	1.5	8.0	1.5	9.8	ns
t <sub>PZH</sub>		1.5	7.5	1.5	8.0	1.5	9.8	
t <sub>PLZ</sub>	Output Disable Time	1.5	6.5	1.5	7.0	1.5	7.8	ns
t <sub>PHZ</sub>		1.5	6.5	1.5	7.0	1.5	7.8	
t <sub>OSSL</sub>	Output to Output Skew		1.0					ns
t <sub>OSLH</sub>	(Note 6)		1.0					
t <sub>S</sub>	Setup Time, D <sub>n</sub> to CLK	2.5		2.5		4.0		ns
t <sub>H</sub>	Hold Time, D <sub>n</sub> to CLK	1.5		1.5		2.0		ns
t <sub>w</sub>	CLK Pulse Width	3.3		3.3		4.0		ns

**Note 6:** Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction either HIGH-to-LOW (t<sub>OSSL</sub>) or LOW-to-HIGH (t<sub>OSLH</sub>).

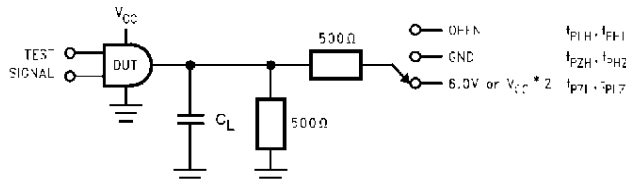
## Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C	Units
				Typical	
V <sub>OLP</sub>	Quiet Output Dynamic Peak V <sub>OL</sub>	C <sub>L</sub> = 50 pF, V <sub>IH</sub> = 3.3V, V <sub>IL</sub> = 0V	3.3	0.8	V
		C <sub>L</sub> = 30 pF, V <sub>IH</sub> = 2.5V, V <sub>IL</sub> = 0V	2.5	0.6	
V <sub>OLV</sub>	Quiet Output Dynamic Valley V <sub>OL</sub>	C <sub>L</sub> = 50 pF, V <sub>IH</sub> = 3.3V, V <sub>IL</sub> = 0V	3.3	-0.8	V
		C <sub>L</sub> = 30 pF, V <sub>IH</sub> = 2.5V, V <sub>IL</sub> = 0V	2.5	-0.6	

## Capacitance

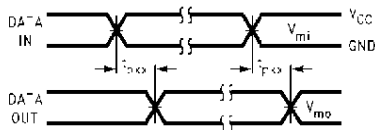
Symbol	Parameter	Conditions	Typical	Units
C <sub>IN</sub>	Input Capacitance	V <sub>CC</sub> = Open, V <sub>I</sub> = 0V or V <sub>CC</sub>	7	pF
C <sub>O</sub>	Output Capacitance	V <sub>CC</sub> = 3.3V, V <sub>I</sub> = 0V or V <sub>CC</sub>	8	pF
C <sub>PD</sub>	Power Dissipation Capacitance	V <sub>CC</sub> = 3.3V, V <sub>I</sub> = 0V or V <sub>CC</sub> , f = 10 MHz	20	pF

**AC LOADING and WAVEFORMS** Generic for LCX Family

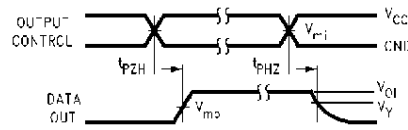


**FIGURE 1. AC Test Circuit ( $C_L$  includes probe and jig capacitance)**

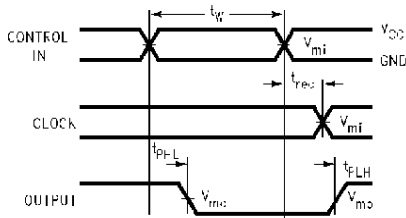
Test	Switch
$t_{PLH}, t_{PHL}$	Open
$t_{PZL}, t_{PLZ}$	6V at $V_{CC} = 3.3 \pm 0.3V$ $V_{CC} \times 2$ at $V_{CC} = 2.5 \pm 0.2V$
$t_{PZH}, t_{PHZ}$	GND



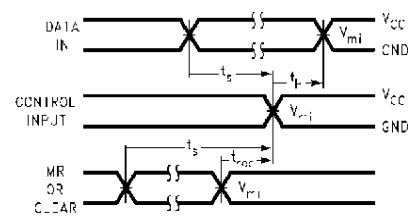
**Waveform for Inverting and Non-Inverting Functions**



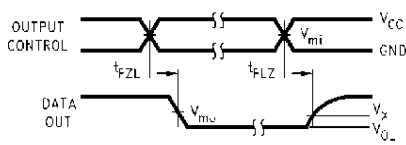
**3-STATE Output High Enable and Disable Times for Logic**



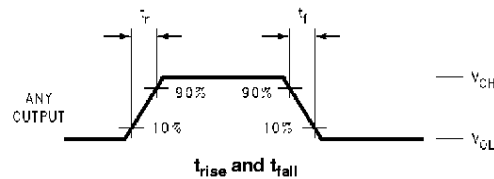
**Propagation Delay, Pulse Width and  $t_{rec}$  Waveforms**



**Setup Time, Hold Time and Recovery Time for Logic**



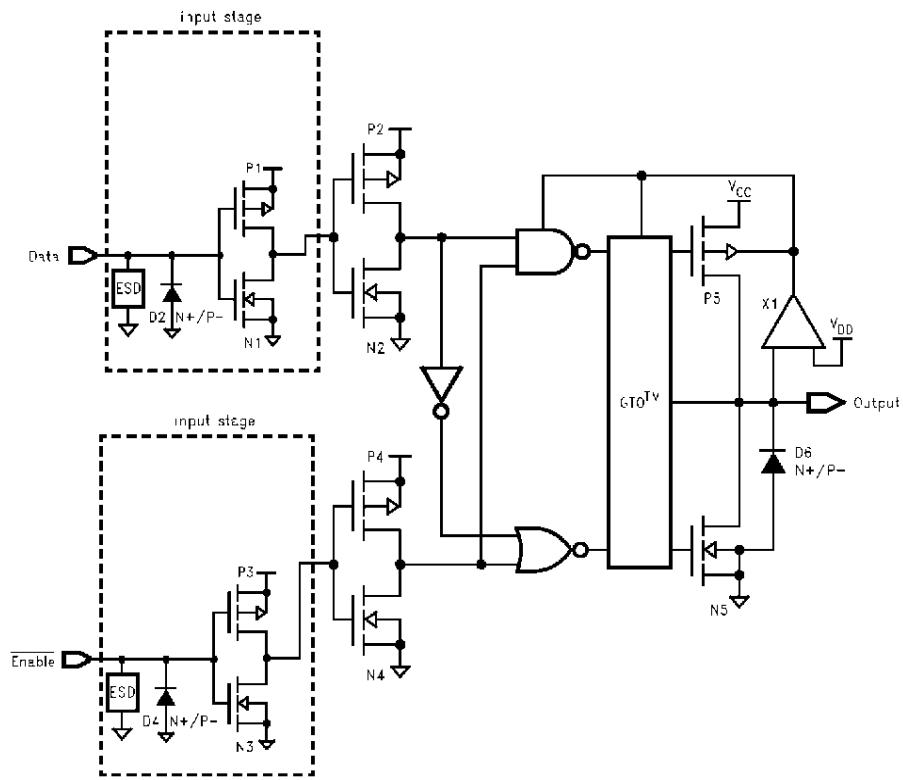
**3-STATE Output Low Enable and Disable Times for Logic**



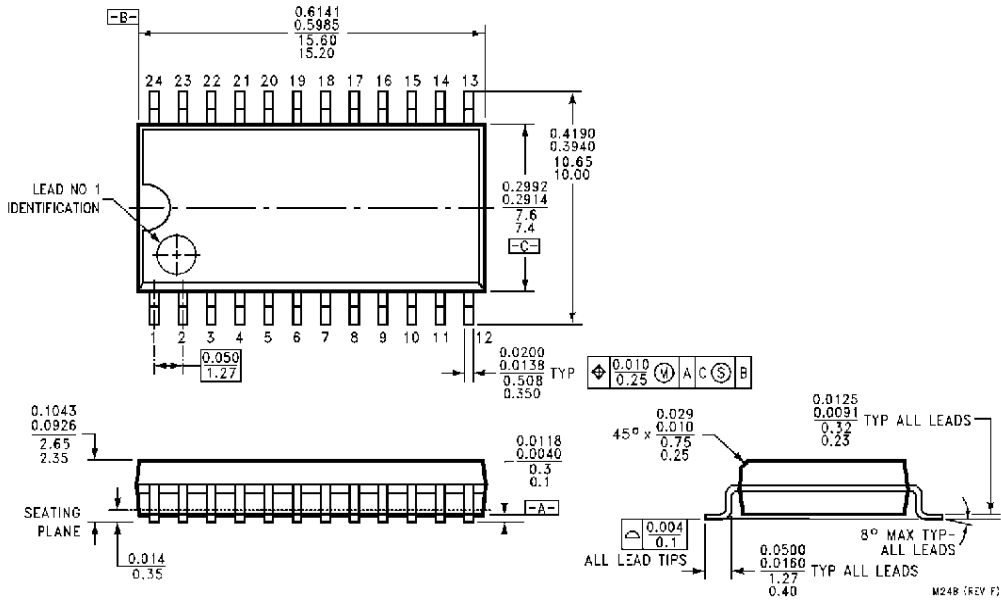
**FIGURE 2. Waveforms (Input Characteristics;  $f = 1MHz, t_R = t_F = 3ns$ )**

Symbol	$V_{CC}$		
	$3.3V \pm 0.3V$	2.7V	$2.5V \pm 0.2V$
$V_{mi}$	1.5V	1.5V	$V_{CC}/2$
$V_{mo}$	1.5V	1.5V	$V_{CC}/2$
$V_x$	$V_{OL} + 0.3V$	$V_{OL} + 0.3V$	$V_{OL} + 0.15V$
$V_y$	$V_{OH} - 0.3V$	$V_{OH} - 0.3V$	$V_{OH} - 0.15V$

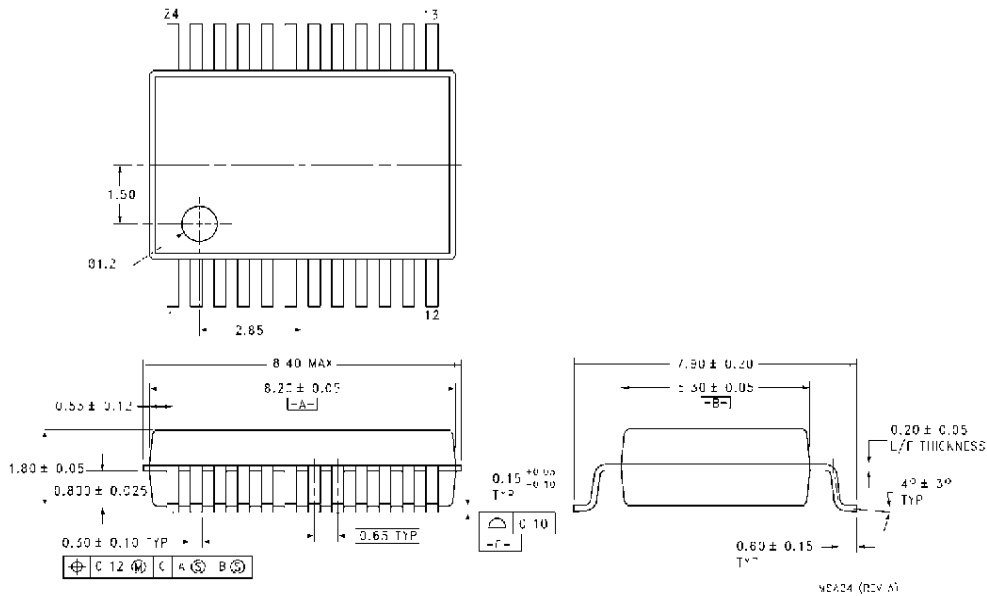
Schematic Diagram Generic for LCX Family



**Physical Dimensions** inches (millimeters) unless otherwise noted

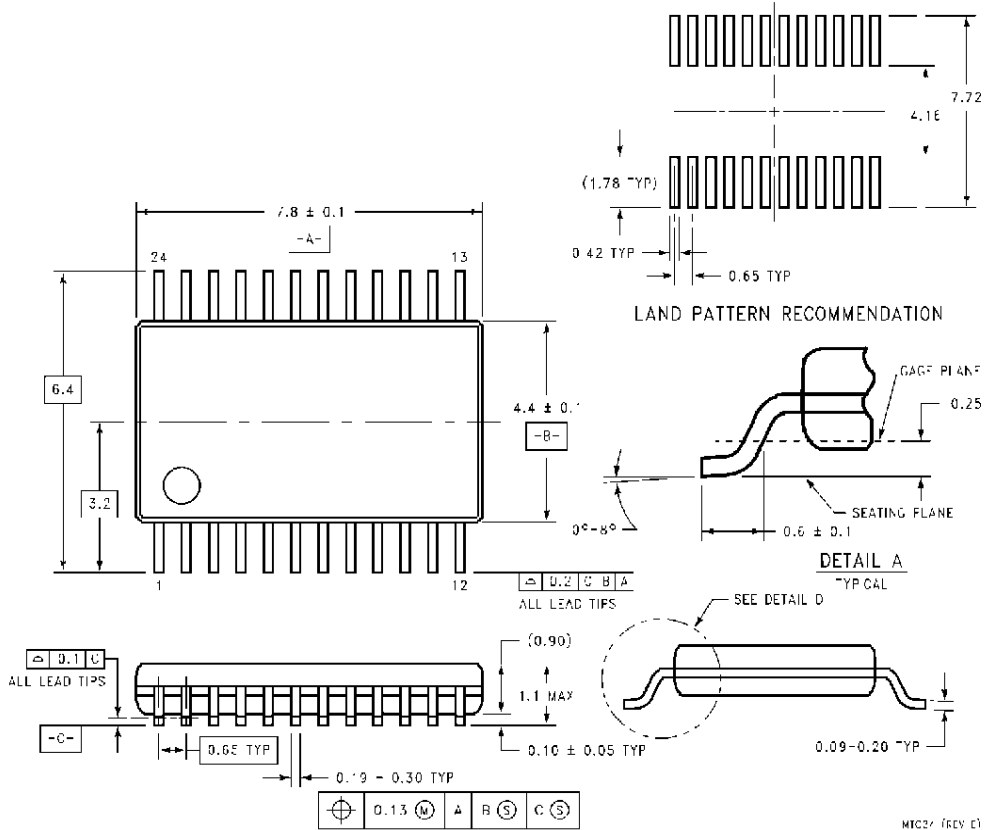


**24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide  
Package Number M24B**



**24-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide  
Package Number MSA24**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide  
Package Number MTC24

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