User Guide
EVB-ATEK356P3-01

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Revisions

Revision No	Revision Date	Revision Reason	Section / Page No
1.0	29.07.2021	Initial Version	
1.1	10.01.2022	Format and Content Fixed	
1.2	16.04.2022	Format and Content Fixed	

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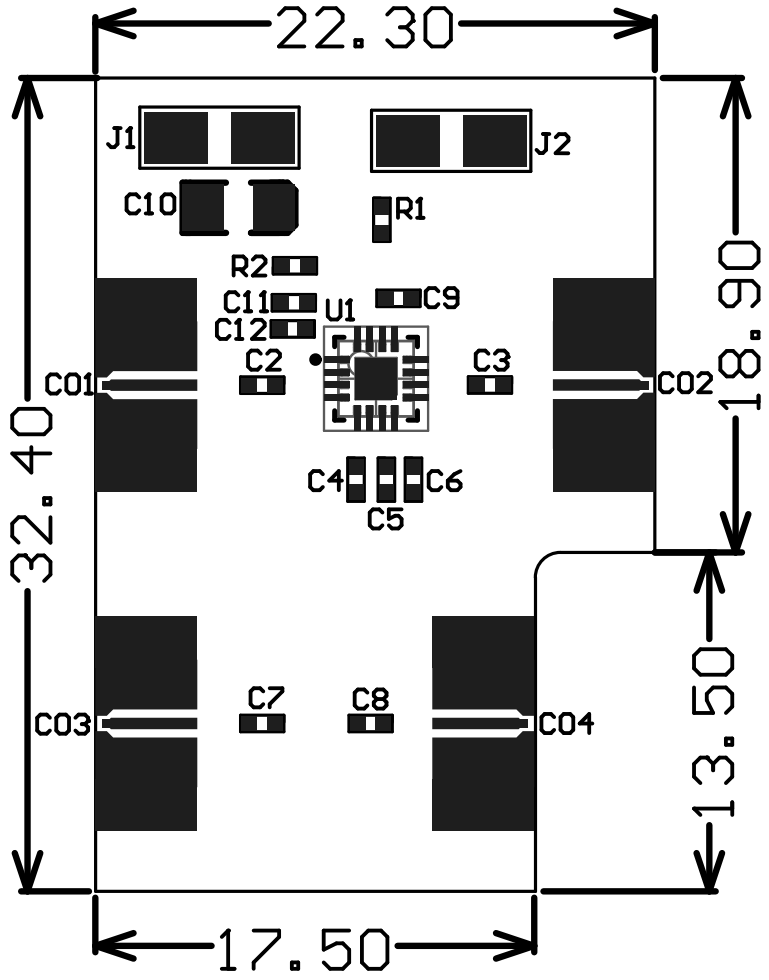
1 GENERAL INFORMATION



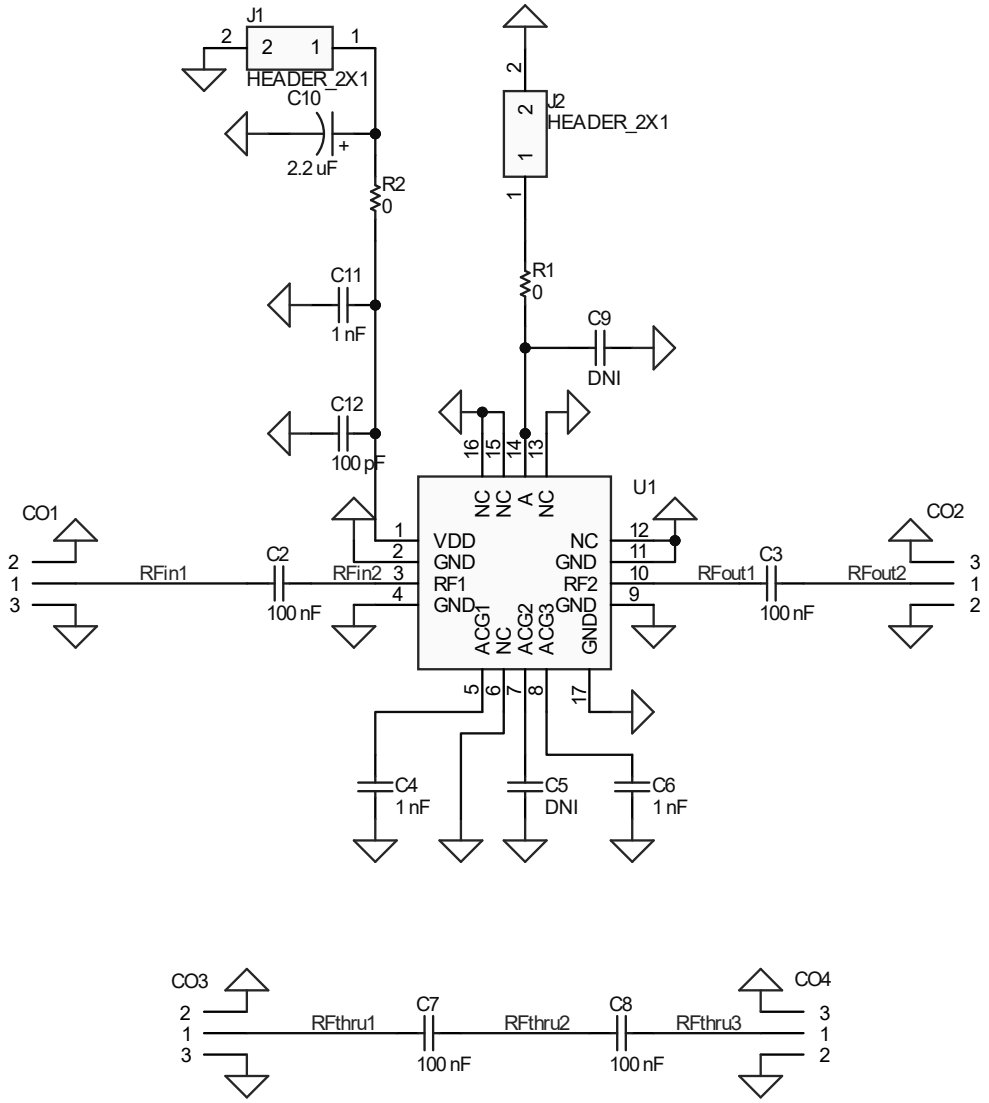
PIN Name	Definition	Comment
CO1	RF IN	SMA Connector
CO2	RF OUT	SMA Connector
CO3, CO4	RF Thru Line IO	SMA Connector
J1 Right	VDD	2.54mm Header
J1 Left, J2 Right	GND	2.54mm Header
J2 Left	P1 – CTRLA	2.54mm Header

Notes:

1. VDD Voltage is detailed in Datasheet.
2. Control Voltage is detailed in Datasheet.
3. The definition of up, down, right, and left is valid for this view of PCB.

2 DESIGN INFORMATION

2.1 SCHEMATIC



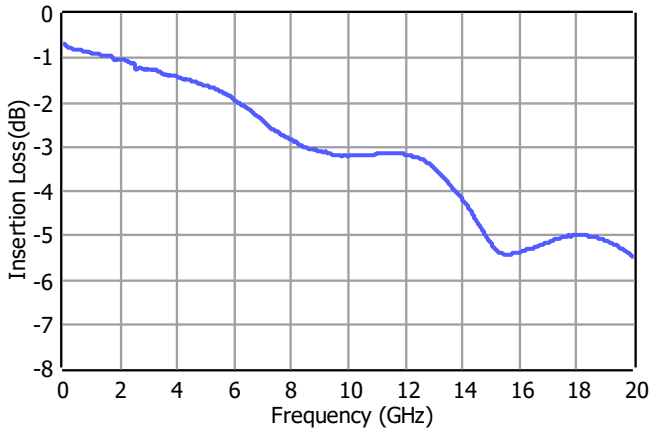
2.2 BOM

Designator	Footprint	Qty	Comment	PN
C2, C3, C7, C8	0402	4	100nF	
C4, C6, C11	0402	3	1nF	
C5, C9	0402	2	DNP	
C10	CASEA	1	2.2uF	
C12	0402	1	100pF	
CO1, CO2, CO3, CO4	SMA Connector	4	SMA Connector	
J1, J2	2x1 Header	2	2x1 Header	
R1, R2	0402	2	0R	
U1	ATEKQ3316	1	DSA 1 Bit	ATEK356P3

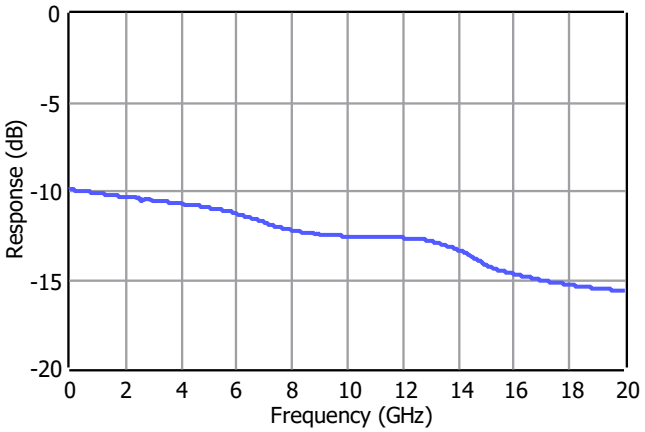
3 TYPICAL PERFORMANCE PLOTS

Conditions unless otherwise specified: Typical, V_{DD} = 5 V, T = 25 C, CW. For details, please refer to the datasheet.

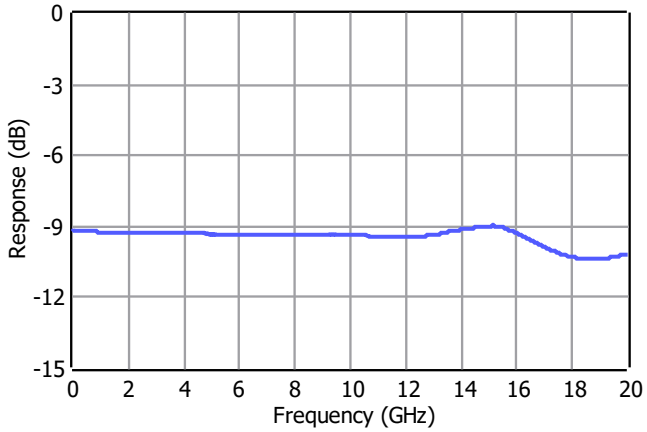
Insertion Loss



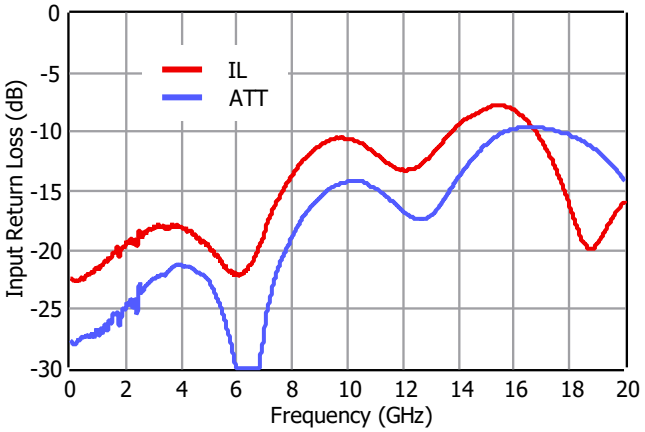
Insertion Loss vs. Attenuation State



Relative Attenuation



Input Return Loss



Output Return Loss