

# 64-Mbit (4 M × 16) Static RAM

## Features

- High speed
  - $t_{AA} = 12 \text{ ns}$
- Low active power
  - $I_{CC} = 300 \text{ mA}$  at 12 ns
- Low complementary metal oxide semiconductor (CMOS) standby power
  - $I_{SB2} = 100 \text{ mA}$
- Operating voltages of  $3.3 \pm 0.3 \text{ V}$
- 2.0-V data retention
- Automatic power-down when deselected
- Transistor-transistor logic (TTL)-compatible inputs and outputs
- Easy memory expansion with  $\overline{CE}_1$  and  $CE_2$  features
- Available in Pb-free 48-ball fine ball grid array (FBGA) package

## Functional Description

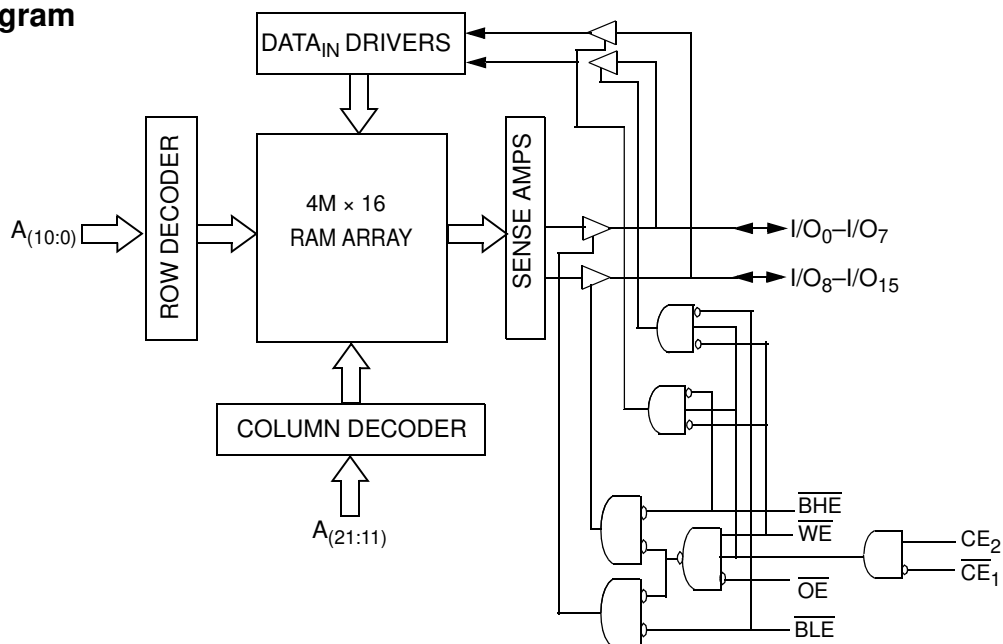
The CY7C1081DV33 is a high-performance CMOS static RAM organized as 4,194,304 words by 16 bits.

To write to the device, take Chip Enables ( $\overline{CE}_1$  LOW and  $CE_2$  HIGH) and Write Enable (WE) inputs LOW. If Byte Low Enable (BLE) is LOW, then data from I/O pins (I/O<sub>0</sub> through I/O<sub>7</sub>) is written into the location specified on the address pins (A<sub>0</sub> through A<sub>21</sub>). If Byte High Enable (BHE) is LOW, then data from I/O pins (I/O<sub>8</sub> through I/O<sub>15</sub>) is written into the location specified on the address pins (A<sub>0</sub> through A<sub>21</sub>).

To read from the device, take Chip Enables ( $\overline{CE}_1$  LOW and  $CE_2$  HIGH) and Output Enable (OE) LOW while forcing the Write Enable (WE) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins appears on I/O<sub>0</sub> to I/O<sub>7</sub>. If Byte High Enable (BHE) is LOW, then data from memory appears on I/O<sub>8</sub> to I/O<sub>15</sub>. See the [Truth Table on page 9](#) for a complete description of read and write modes.

The input and output pins (I/O<sub>0</sub> through I/O<sub>15</sub>) are placed in a high impedance state when the device is deselected ( $\overline{CE}_1$  HIGH or  $CE_2$  LOW), the outputs are disabled ( $\overline{OE}$  HIGH), both byte high enable and byte low enable are disabled ( $\overline{BHE}$ ,  $\overline{BLE}$  HIGH), or during a write operation ( $\overline{CE}_1$  LOW,  $CE_2$  HIGH, and  $\overline{WE}$  LOW).

## Logic Block Diagram



## Contents

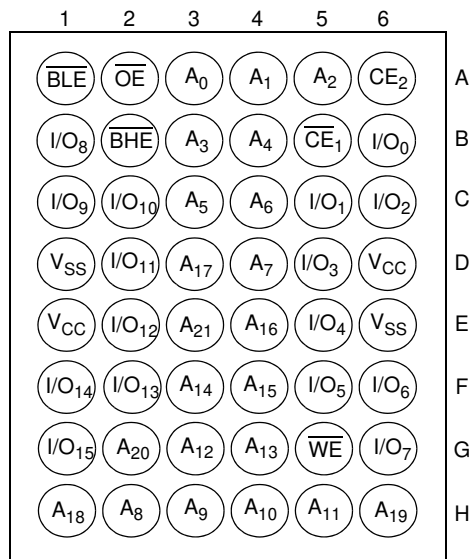
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**Selection Guide**

Description	-12	Unit
Maximum access time	12	ns
Maximum operating current	300	mA
Maximum CMOS standby current	100	mA

**Pin Configuration**

**Figure 1. 48-Ball FBGA (Top View)**



## Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

Storage temperature ..... -65 °C to +150 °C  
 Ambient temperature with power applied ..... -55 °C to +125 °C  
 Supply voltage on V<sub>CC</sub> relative to GND <sup>[1]</sup> ..... -0.5 V to +4.6 V  
 DC voltage applied to outputs in high-Z state <sup>[1]</sup> ..... -0.5 V to V<sub>CC</sub> + 0.5 V  
 DC input voltage <sup>[1]</sup> ..... -0.5 V to V<sub>CC</sub> + 0.5 V

Current into outputs (LOW) ..... 20 mA  
 Static discharge voltage ..... >2001 V (MIL-STD-883, Method 3015)  
 Latch-up current ..... >140 mA

## Operating Range

Range	Ambient Temperature	V <sub>CC</sub>	Speed
Industrial	-40 °C to +85 °C	3.3 V ± 0.3 V	12 ns

## DC Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	-12		Unit
			Min	Max	
V <sub>OH</sub>	Output HIGH voltage	V <sub>CC</sub> = Min, I <sub>OH</sub> = -4.0 mA	2.4	-	V
V <sub>OL</sub>	Output LOW voltage	V <sub>CC</sub> = Min, I <sub>OL</sub> = 8.0 mA	-	0.4	V
V <sub>IH</sub>	Input HIGH voltage		2.0	V <sub>CC</sub> + 0.3	V
V <sub>IL</sub>	Input LOW voltage <sup>[1]</sup>		-0.3	0.8	V
I <sub>Ix</sub>	Input leakage current	GND ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>	-1	+1	μA
I <sub>OZ</sub>	Output leakage current	GND ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> , Output Disabled	-1	+1	μA
I <sub>CC</sub>	V <sub>CC</sub> operating supply current	V <sub>CC</sub> = Max, f = f <sub>max</sub> = 1/t <sub>RC</sub> , I <sub>OUT</sub> = 0 mA CMOS levels	-	300	mA
I <sub>SB1</sub>	Automatic CE power-down current – TTL inputs	Max V <sub>CC</sub> , $\overline{CE}_1 \geq V_{IH}$ , CE <sub>2</sub> ≤ V <sub>IL</sub> , V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>max</sub>	-	120	mA
I <sub>SB2</sub>	Automatic CE power-down current – CMOS inputs	Max V <sub>CC</sub> , $\overline{CE}_1 \geq V_{CC} - 0.3$ V, CE <sub>2</sub> ≤ 0.3 V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3 V, or V <sub>IN</sub> ≤ 0.3 V, f = 0,	-	100	mA

## Capacitance

Tested initially and after any design or process changes that may affect these parameters.

Parameter	Description	Test Conditions	Max	Unit
C <sub>IN</sub>	Input capacitance	T <sub>A</sub> = 25 °C, f = 1 MHz, V <sub>CC</sub> = 3.3 V	32	pF
C <sub>OUT</sub>	I/O capacitance		40	pF

## Thermal Resistance

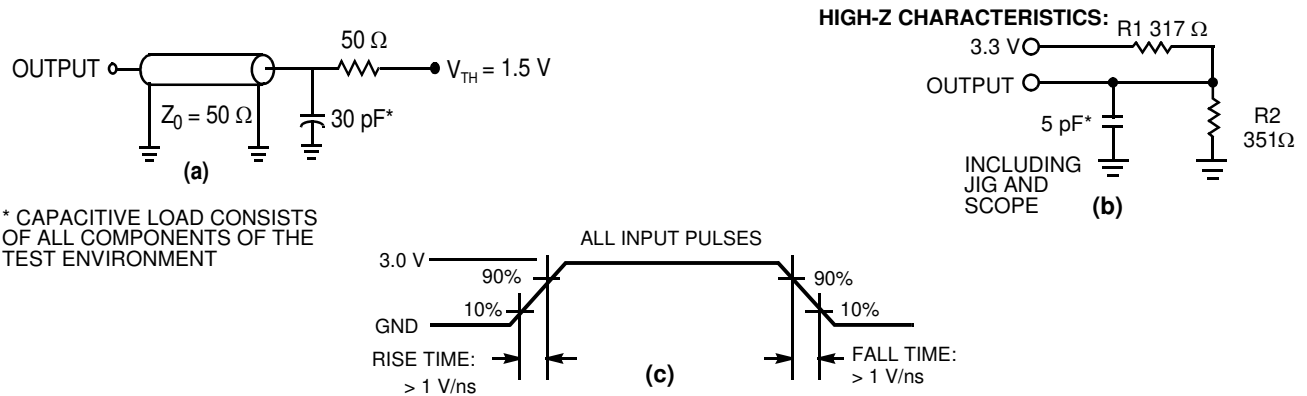
Tested initially and after any design or process changes that may affect these parameters.

Parameter	Description	Test Conditions	FBGA	Unit
θ <sub>JA</sub>	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	55	°C/W
θ <sub>JC</sub>	Thermal resistance (junction to case)		23.04	°C/W

### Note

1. V<sub>IL</sub> (min) = -2.0 V and V<sub>IH</sub> (max) = V<sub>CC</sub> + 2 V for pulse durations of less than 20 ns.

Figure 2. AC Test Loads and Waveforms<sup>[2]</sup>

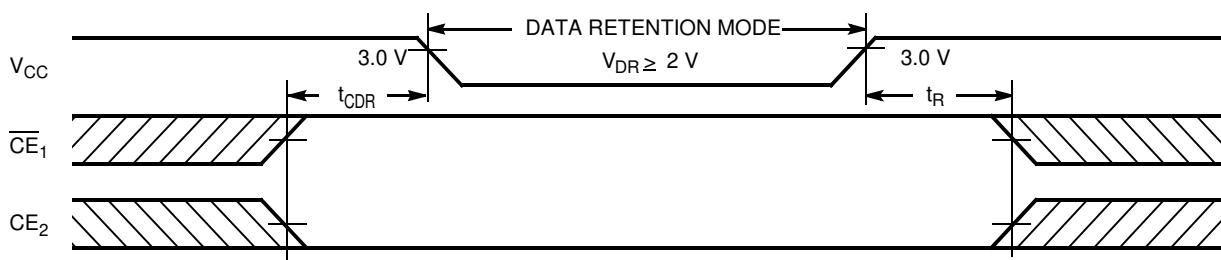


### Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ	Max	Unit
$V_{DR}$	$V_{CC}$ for data retention		2	—	—	V
$I_{CCDR}$	Data retention current	$V_{CC} = 2V, \overline{CE}_1 \geq V_{CC} - 0.2V, CE_2 \leq 0.2V, V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	—	—	100	mA
$t_{CDR}^{[3]}$	Chip deselect to data retention time		0	—	—	ns
$t_R^{[4]}$	Operation recovery time		12	—	—	ns

Figure 3. Data Retention Waveform



**Notes**

- Valid SRAM operation does not occur until the power supplies reach the minimum operating  $V_{DD}$  (3.0 V). 100  $\mu$ s ( $t_{power}$ ) after reaching the minimum operating  $V_{DD}$ , normal SRAM operation begins to include reduction in  $V_{DD}$  to the data retention ( $V_{CCDR}$ ; 2.0 V) voltage.
- Tested initially and after any design or process changes that may affect these parameters.
- Full device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC}(\min) \geq 50 \mu$ s or stable at  $V_{CC}(\min) \geq 50 \mu$ s.

## AC Switching Characteristics

Over the Operating Range <sup>[5]</sup>

Parameter	Description	-12		Unit
		Min	Max	
<b>Read Cycle</b>				
$t_{power}$	$V_{CC}(typ)$ to the first access <sup>[6]</sup>	100	–	$\mu s$
$t_{RC}$	Read cycle time	12	–	ns
$t_{AA}$	Address to data valid	–	12	ns
$t_{OHA}$	Data hold from address change	3	–	ns
$t_{ACE}$	$\overline{CE}_1$ LOW and $CE_2$ HIGH to Data Valid	–	12	ns
$t_{DOE}$	$\overline{OE}$ LOW to data valid	–	7	ns
$t_{LZOE}$	$\overline{OE}$ LOW to low-Z	1	–	ns
$t_{HZOE}$	$\overline{OE}$ HIGH to high-Z <sup>[7]</sup>	–	7	ns
$t_{LZCE}$	$\overline{CE}_1$ LOW and $CE_2$ HIGH to low-Z <sup>[7]</sup>	3	–	ns
$t_{HZCE}$	$\overline{CE}_1$ HIGH and $CE_2$ LOW to high-Z <sup>[7]</sup>	–	7	ns
$t_{PU}$	$\overline{CE}_1$ LOW and $CE_2$ HIGH to power-up <sup>[8]</sup>	0	–	ns
$t_{PD}$	$\overline{CE}_1$ HIGH and $CE_2$ LOW to power-down <sup>[8]</sup>	–	12	ns
$t_{DBE}$	Byte enable to data valid	–	7	ns
$t_{LZBE}$	Byte enable to low-Z	1	–	ns
$t_{HZBE}$	Byte disable to high-Z	–	7	ns
<b>Write Cycle</b> <sup>[9, 10]</sup>				
$t_{WC}$	Write cycle time	12	–	ns
$t_{SCE}$	$\overline{CE}_1$ LOW and $CE_2$ HIGH to write end	9	–	ns
$t_{AW}$	Address setup to write end	9	–	ns
$t_{HA}$	Address hold from write end	0	–	ns
$t_{SA}$	Address setup to write start	0	–	ns
$t_{PWE}$	$\overline{WE}$ pulse width	9	–	ns
$t_{SD}$	Data setup to write end	7	–	ns
$t_{HD}$	Data hold from write end	0	–	ns
$t_{LZWE}$	$\overline{WE}$ HIGH to low-Z <sup>[7]</sup>	3	–	ns
$t_{HZWE}$	$\overline{WE}$ LOW to high-Z <sup>[7]</sup>	–	7	ns
$t_{BW}$	Byte enable to end of write	9	–	ns

### Notes

- Test conditions are based on signal transition time of 3 ns or less and timing reference levels of 1.5 V and input pulse levels of 0 to 3.0 V. Test conditions for the read cycle use output loading shown in part a) of [AC Test Loads and Waveforms](#)<sup>[2]</sup>, unless specified otherwise.
- $t_{power}$  is the minimum amount of time that the power supply must be at typical  $V_{CC}$  values until the first memory access can be performed.
- $t_{HZOE}$ ,  $t_{HZCE}$ ,  $t_{HZWE}$ ,  $t_{HZBE}$  and  $t_{LZOE}$ ,  $t_{LZCE}$ ,  $t_{LZWE}$ ,  $t_{LZBE}$  are specified with a load capacitance of 5 pF as in (b) of [AC Test Loads and Waveforms](#)<sup>[2]</sup>.
- These parameters are guaranteed by design and are not tested.
- The internal memory write time is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE}_1 = V_{IL}$ , and  $CE_2 = V_{IH}$ . Chip enables must be active and  $\overline{WE}$  and byte enables must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data setup and hold timing must be referenced to the leading edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle 2 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .

### Switching Waveforms

Figure 4. Read Cycle 1 (Address Transition Controlled) [11, 12]

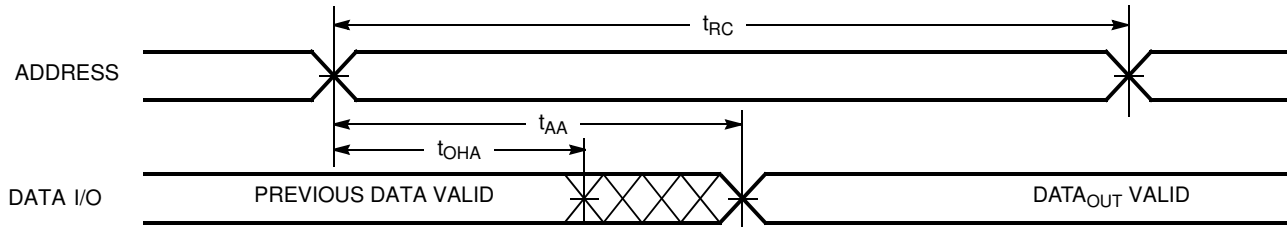
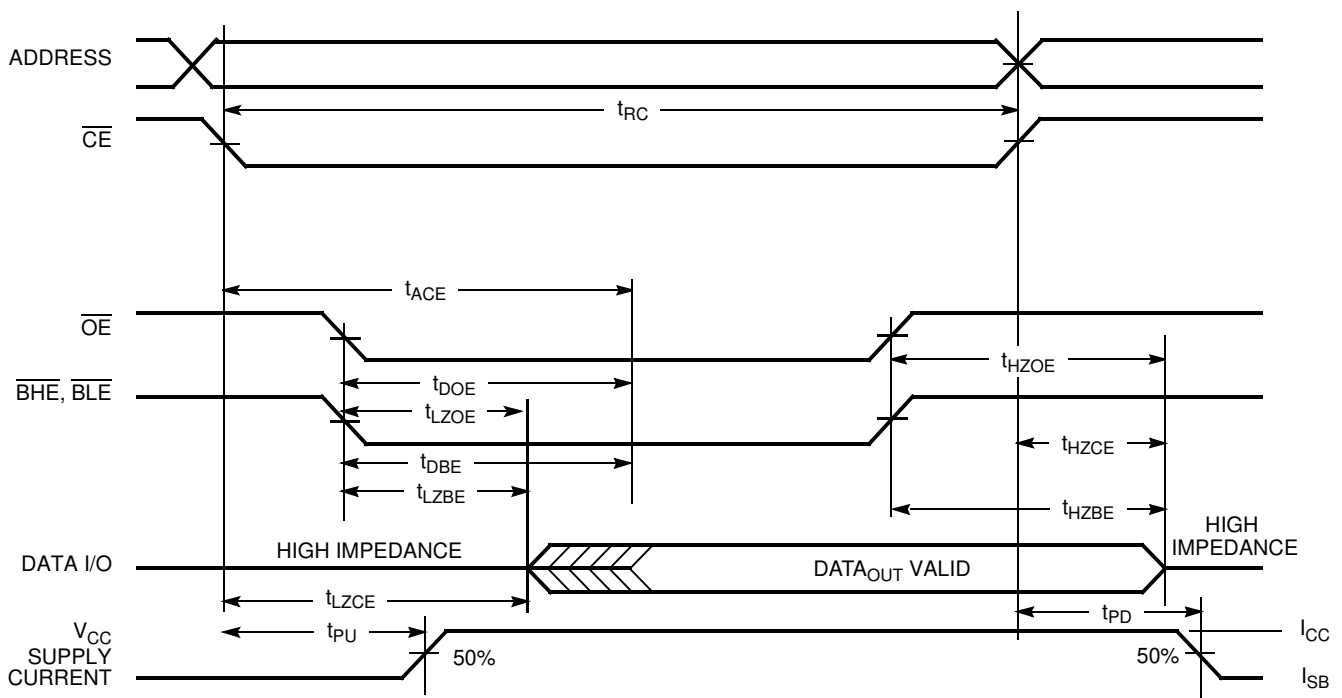


Figure 5. Read Cycle 2 ( $\overline{OE}$  Controlled) [12, 13, 14]



**Notes**

- 11. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}_1 = V_{IL}$ ,  $\overline{BHE}$  or  $\overline{BLE}$  or both =  $V_{IL}$ , and  $CE_2 = V_{IH}$ .
- 12.  $\overline{WE}$  is HIGH for read cycle.
- 13. Address valid before or similar to  $\overline{CE}_1$  transition LOW and  $CE_2$  transition HIGH.
- 14.  $\overline{CE}$  refers to the internal logical combination of  $\overline{CE}_1$  and  $CE_2$  such that when  $\overline{CE}_1$  is LOW and  $CE_2$  is HIGH,  $\overline{CE}$  is LOW. For all other combinations,  $\overline{CE}$  is HIGH.

Switching Waveforms (continued)

Figure 6. Write Cycle 1 ( $\overline{CE}$  Controlled) [15, 16, 17]

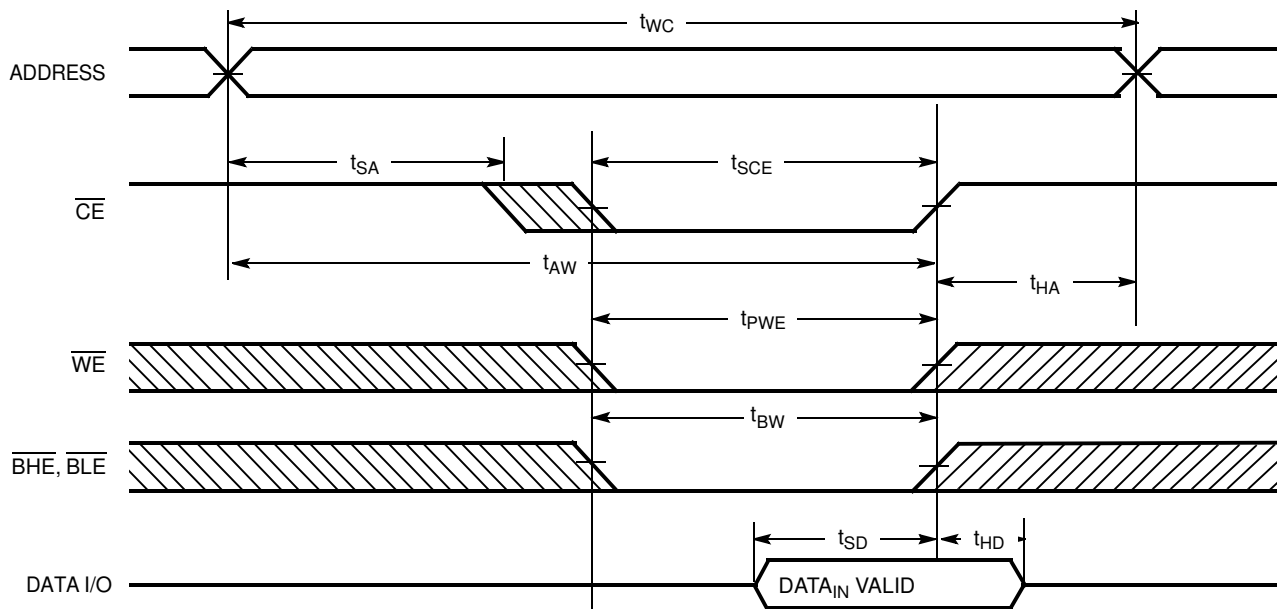
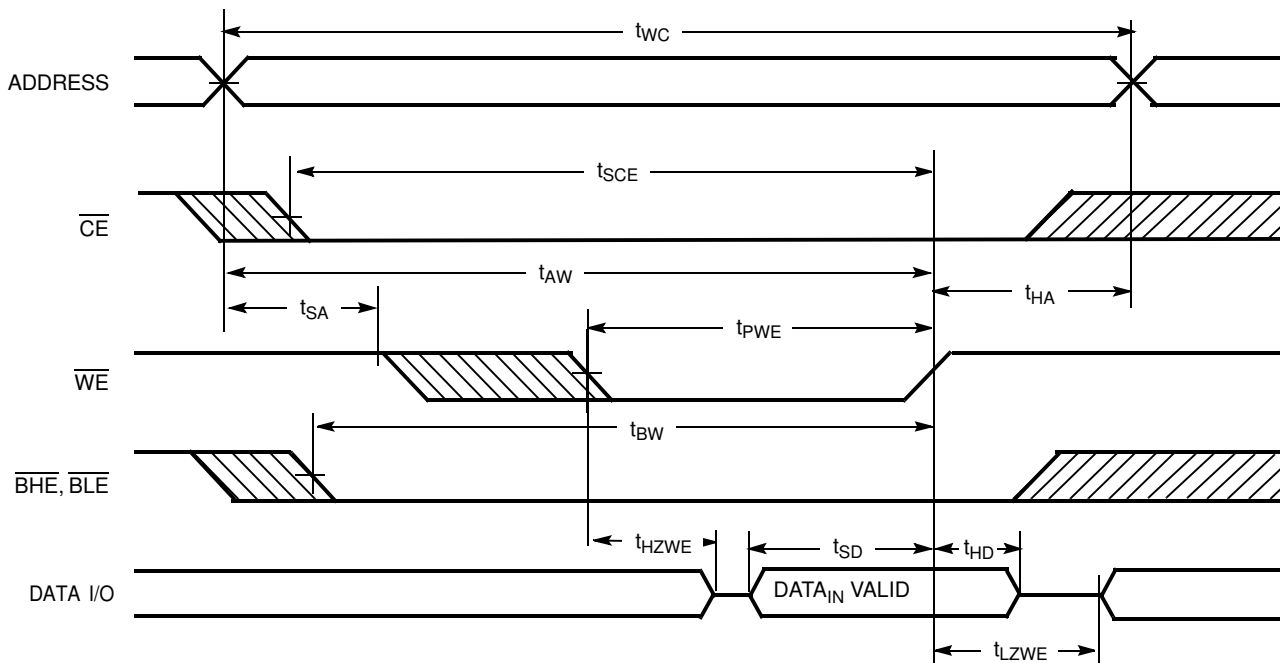


Figure 7. Write Cycle 2 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) [15, 16, 17]



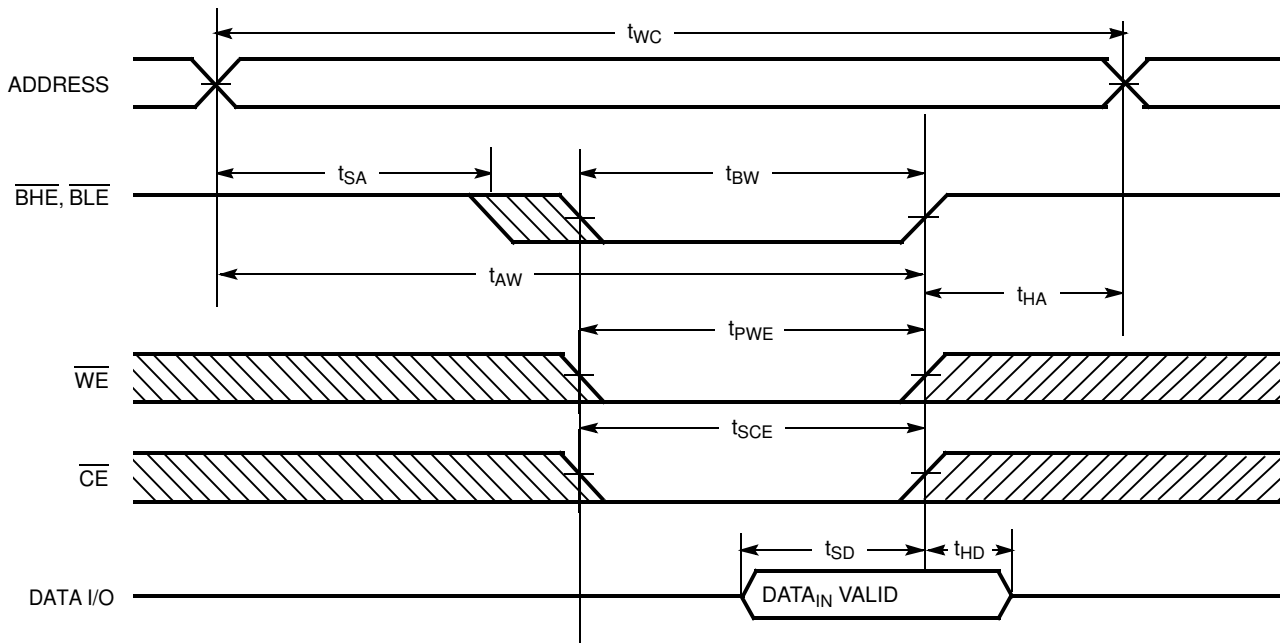
Notes

- 15.  $\overline{CE}$  refers to the internal logical combination of  $\overline{CE}_1$  and  $CE_2$  such that when  $\overline{CE}_1$  is LOW and  $CE_2$  is HIGH,  $\overline{CE}$  is LOW. For all other combinations,  $\overline{CE}$  is HIGH.
- 16. Data I/O is high impedance if  $\overline{OE}$  or  $\overline{BHE}$ ,  $\overline{BLE}$  or both =  $V_{IH}$ .
- 17. If  $\overline{CE}$  goes HIGH simultaneously with WE going HIGH, the output remains in a high impedance state.



Switching Waveforms (continued)

Figure 8. Write Cycle 3 ( $\overline{\text{BLE}}$  or  $\overline{\text{BHE}}$  Controlled) [18]



Truth Table

$\overline{\text{CE}}_1$	$\overline{\text{CE}}_2$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	$\overline{\text{BLE}}$	$\overline{\text{BHE}}$	I/O <sub>0</sub> - I/O <sub>7</sub>	I/O <sub>8</sub> - I/O <sub>15</sub>	Mode	Power
H	X	X	X	X	X	High-Z	High-Z	Power down	Standby ( $I_{SB}$ )
X	L	X	X	X	X	High-Z	High-Z	Power down	Standby ( $I_{SB}$ )
L	H	L	H	L	L	Data Out	Data Out	Read all bits	Active ( $I_{CC}$ )
L	H	L	H	L	H	Data Out	High-Z	Read lower bits only	Active ( $I_{CC}$ )
L	H	L	H	H	L	High-Z	Data Out	Read upper bits only	Active ( $I_{CC}$ )
L	H	X	L	L	L	Data In	Data In	Write all bits	Active ( $I_{CC}$ )
L	H	X	L	L	H	Data In	High-Z	Write lower bits only	Active ( $I_{CC}$ )
L	H	X	L	H	L	High-Z	Data In	Write upper bits only	Active ( $I_{CC}$ )
L	H	H	H	X	X	High-Z	High-Z	Selected, Outputs disabled	Active ( $I_{CC}$ )

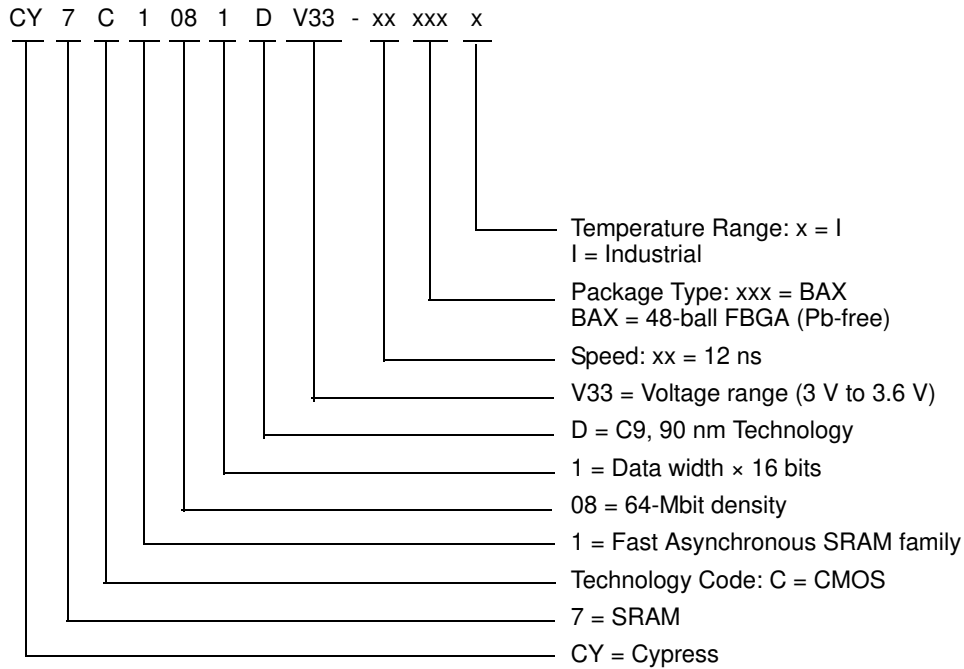
Note

18.  $\overline{\text{CE}}$  refers to the internal logical combination of  $\overline{\text{CE}}_1$  and  $\overline{\text{CE}}_2$  such that when  $\overline{\text{CE}}_1$  is LOW and  $\overline{\text{CE}}_2$  is HIGH,  $\overline{\text{CE}}$  is LOW. For all other combinations,  $\overline{\text{CE}}$  is HIGH.

**Ordering Information**

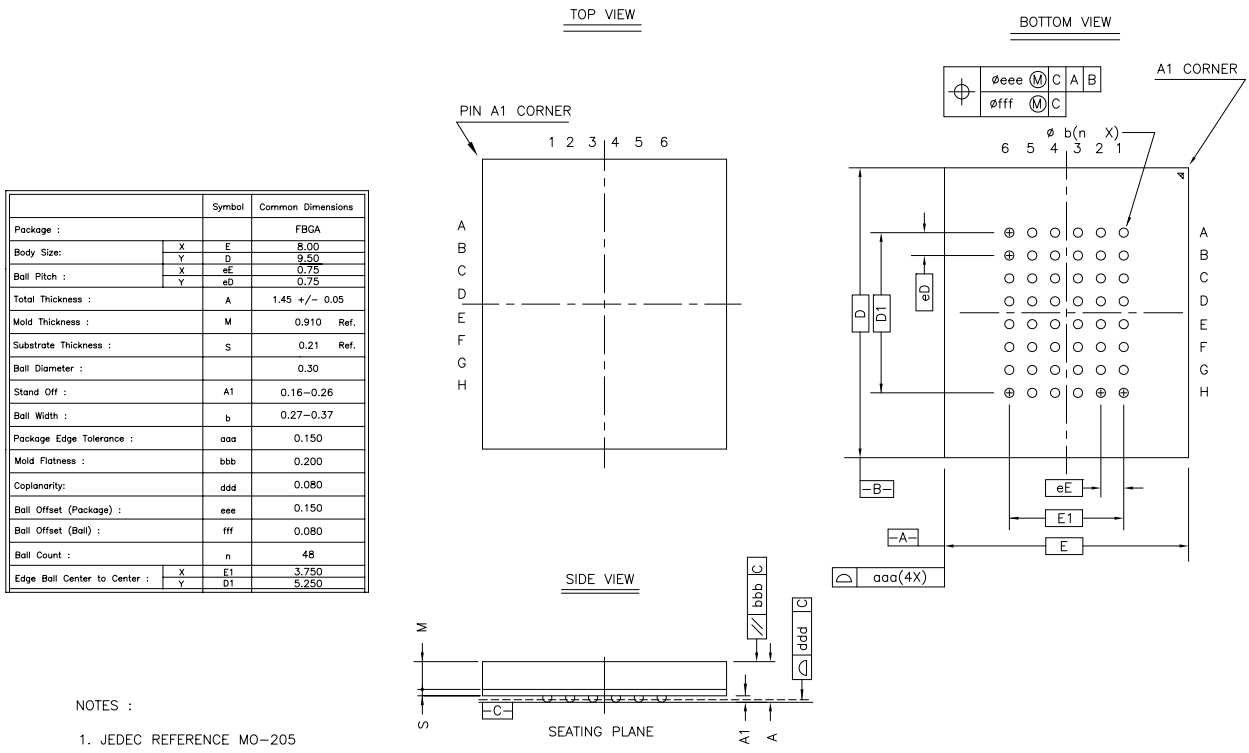
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
12	CY7C1081DV33-12BAXI	001-50044	48-Ball FBGA (8 × 9.5 × 1.4 mm) (Pb-free)	Industrial

**Ordering Code Definition**



### Package Diagram

Figure 9. 48-Ball FBGA (8 x 9.5 x 1.4 mm) (001-50044)



NOTES :

1. JEDEC REFERENCE MO-205
2. PACKAGE WEIGHT : 0.2409g
3. DIMENSIONS IN MILLIMETERS

001-50044 \*C

### Acronyms

Acronym	Description
CMOS	complementary metal oxide semiconductor
FBGA	fine ball grid array
I/O	input/output
SRAM	static random access memory
TTL	transistor-transistor logic

### Document Conventions

#### Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
μA	microampere
mA	milliampere
MHz	megahertz
ns	nanosecond
pF	picofarad
V	volt
Ω	ohm
W	watt

## Document History Page

Document Title: CY7C1081DV33, 64-Mbit (4 M × 16) Static RAM				
Document Number: 001-53992				
Revision	ECN	Submission Date	Orig. of Change	Description of Change
**	2746867	07/31/2009	VKN/AESA	New datasheet
*A	3100499	12/02/2010	PRAS	Updated Note 14. Changed datasheet status from Preliminary to Final. Updated <a href="#">Package Diagram</a> and <a href="#">Sales, Solutions, and Legal Information</a> . Added <a href="#">Acronyms</a> , <a href="#">Document Conventions</a> and <a href="#">Ordering Code Definition</a> .
*B	3178249	21/02/2011	PRAS	Post to external web
*C	3246293	05/04/2011	PRAS	Modified Figure 44-B all FBGA pin configuration.
*D	3720094	08/22/2012	TAVA	Minor Text edits.

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