

HGTP10N40F1D, HGTP10N50F1D

10A, 400V and 500V N-Channel IGBTs
with Anti-Parallel Ultrafast Diodes

April 1995

Features

- 10A, 400V and 500V
- Latch Free Operation
- Typical Fall Time < 1.4 μ s
- High Input Impedance
- Low Conduction Loss
- Anti-Parallel Diode
- $t_{RR} < 60$ ns

Description

The IGBT is a MOS gated high voltage switching device combining the best features of MOSFETs and bipolar transistors. The device has the high input impedance of a MOSFET and the low on-state conduction loss of a bipolar transistor. The much lower on-state voltage drop varies only moderately between +25°C and +150°C. The diode used in parallel with the IGBT is an ultrafast ($t_{RR} < 60$ ns) with soft recovery characteristic.

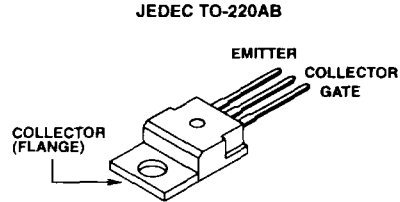
IGBTs are ideal for many high voltage switching applications operating at frequencies where low conduction losses are essential, such as: AC and DC motor controls, power supplies and drivers for solenoids, relays and contactors.

PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
HGTP10N40F1D	TO-220AB	10N40F1D
HGTP10N50F1D	TO-220AB	10N50F1D

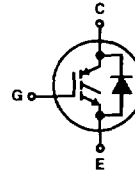
NOTE: When ordering, use the entire part number

Package



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings $T_C = +25^\circ\text{C}$, Unless Otherwise Specified

	HGTP10N40F1D	HGTP10N50F1D	UNITS
Collector-Emitter Voltage	400	500	V
Collector-Gate Voltage $R_{GE} = 1\text{M}\Omega$	400	500	V
Collector Current Continuous at $T_C = +25^\circ\text{C}$	12	12	A
at $T_C = +90^\circ\text{C}$	10	10	A
Collector Current Pulsed (Note 1)	12	12	A
Gate-Emitter Voltage Continuous	± 20	± 20	V
Diode Forward Current at $T_C = +25^\circ\text{C}$	16	16	A
at $T_C = +90^\circ\text{C}$	10	10	A
Power Dissipation Total at $T_C = +25^\circ\text{C}$	75	75	W
Power Dissipation Derating $T_C > +25^\circ\text{C}$	0.6	0.6	W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	-55 to +150	-55 to +150	$^\circ\text{C}$
Maximum Lead Temperature for Soldering	260	260	$^\circ\text{C}$

NOTE:

1. $T_J = +150^\circ\text{C}$, Min. $R_{GE} = 25\Omega$ without latch.

HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951
4,969,027							

Specifications HGTP10N40F1D, HGTP10N50F1D

Electrical Specifications $T_C = +25^\circ\text{C}$, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS				UNITS	
			HGTP10N40F1D		HGTP10N50F1D			
			MIN	MAX	MIN	MAX		
Collector-Emitter Breakdown Voltage	BV_{CES}	$I_C = 1.25\text{mA}, V_{GE} = 0\text{V}$	400	-	500	-	V	
Gate Threshold Voltage	$V_{GE(TH)}$	$V_{GE} = V_{CE}, I_C = 1\text{mA}$	2.0	4.5	2.0	4.5	V	
Zero Gate Voltage Collector Current	I_{CES}	$T_J = +150^\circ\text{C}, V_{CE} = 400\text{V}$	-	1.25	-	-	mA	
		$T_J = +150^\circ\text{C}, V_{CE} = 500\text{V}$	-	-	-	1.25	mA	
Gate-Emitter Leakage Current	I_{GES}	$V_{GE} = \pm 20\text{V}, V_{CE} = 0\text{V}$	-	100	-	100	nA	
Collector-Emitter On-Voltage	$V_{CE(ON)}$	$T_J = +150^\circ\text{C}, I_C = 5\text{A}, V_{GE} = 10\text{V}$	-	2.5	-	2.5	V	
		$T_J = +150^\circ\text{C}, I_C = 5\text{A}, V_{GE} = 15\text{V}$	-	2.2	-	2.2	V	
		$T_J = +25^\circ\text{C}, I_C = 5\text{A}, V_{GE} = 10\text{V}$	-	2.5	-	2.5	V	
		$T_J = +25^\circ\text{C}, I_C = 5\text{A}, V_{GE} = 15\text{V}$	-	2.2	-	2.2	V	
Gate-Emitter Plateau Voltage	V_{GEP}	$I_C = 5\text{A}, V_{CE} = 10\text{V}$	5.3 (Typ)				V	
On-State Gate Charge	$Q_{G(ON)}$	$I_C = 5\text{A}, V_{CE} = 10\text{V}$	13.4 (Typ)				nC	
Turn-On Delay Time	$t_{D(ON)}$	Resistive Load, $I_C = 5\text{A}$, $V_{CE} = 400\text{V}, R_L = 80\Omega$, $T_J = +150^\circ\text{C}, V_{GE} = 10\text{V}$, $R_G = 25\Omega$	45 (Typ)				ns	
Rise Time	t_{RI}		35 (Typ)				ns	
Turn-Off Delay Time	$t_{D(OFF)}$		130 (Typ)				ns	
Fall Time	t_{FI}		1400 (Typ)				ns	
Turn-Off Energy Loss Per Cycle (Off Switching Dissipation = $W_{OFF} \times$ Frequency)	W_{OFF}		0.64 (Typ)				mJ	
Turn-Off Delay Time	$t_{D(OFF)I}$		Inductive Load (See Figure 13), $I_C = 5\text{A}, V_{CE(CLIP)} = 400\text{V}, R_L =$ $80\Omega, L = 50\mu\text{H}, T_J = +150^\circ\text{C}, V_{GE} =$ $10\text{V}, R_G = 25\Omega$	-	375	-	375	ns
Fall Time	t_{FI}			-	1200	-	1200	ns
Turn-Off Energy Loss Per Cycle (Off Switching Dissipation = $W_{OFF} \times$ Frequency)	W_{OFF}		-	1.2	-	1.2	mJ	
Thermal Resistance Junction-to-Case (IGBT)	$R_{\theta JC}$		-	1.67	-	1.67	$^\circ\text{C/W}$	
Thermal Resistance of Diode	$R_{\theta JC}$		-	2.0	-	2.0	$^\circ\text{C/W}$	
Diode Forward Voltage	V_{EC}	$I_{EC} = 10\text{A}$	-	1.7	-	1.7	V	
Diode Reverse Recovery Time	t_{RR}	$I_{EC} = 10\text{A}, dI_{EC}/dt = 100\text{A}/\mu\text{s}$	-	60	-	60	ns	

Typical Performance Curves

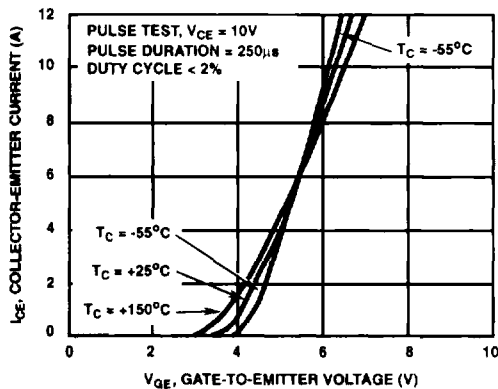


FIGURE 1. TYPICAL TRANSFER CHARACTERISTICS

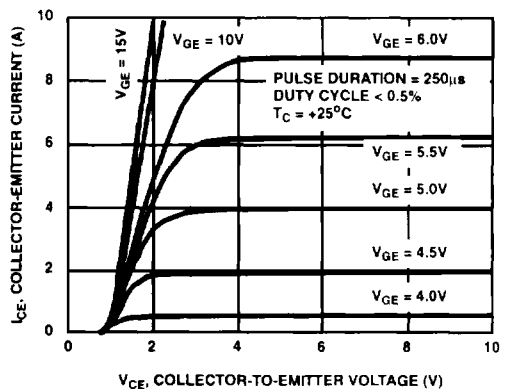


FIGURE 2. TYPICAL SATURATION CHARACTERISTICS

Typical Performance Curves (Continued)

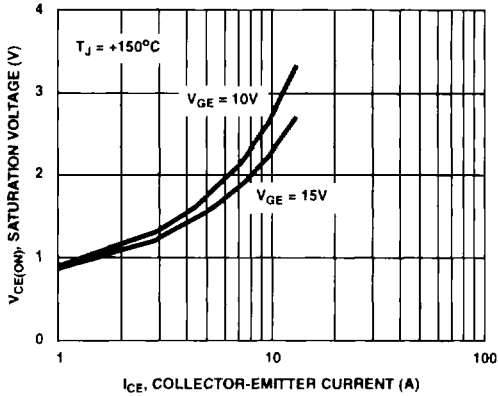


FIGURE 3. SATURATION VOLTAGE vs COLLECTOR-EMITTER CURRENT (TYPICAL)

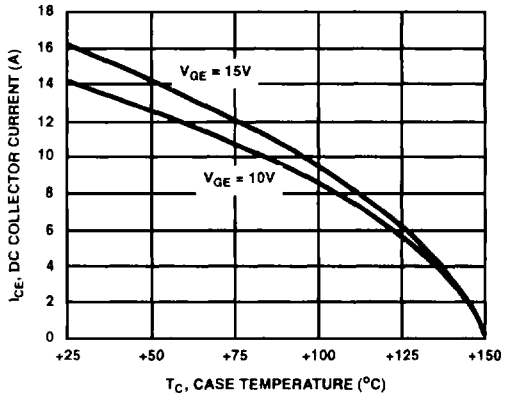


FIGURE 4. DC COLLECTOR CURRENT vs CASE TEMPERATURE

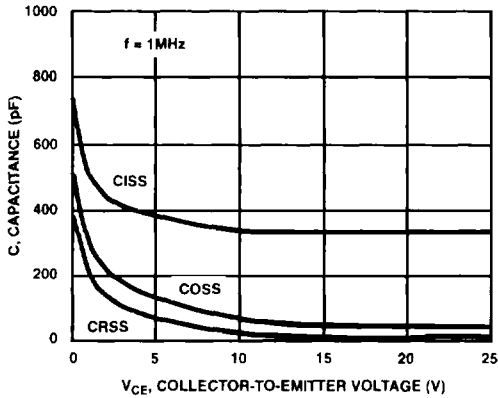


FIGURE 5. CAPACITANCE vs COLLECTOR-TO-EMITTER VOLTAGE (TYPICAL)

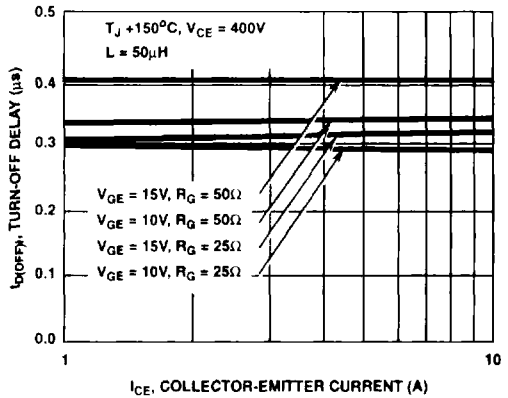


FIGURE 6. TURN-OFF DELAY vs COLLECTOR-TO-EMITTER CURRENT (TYPICAL)

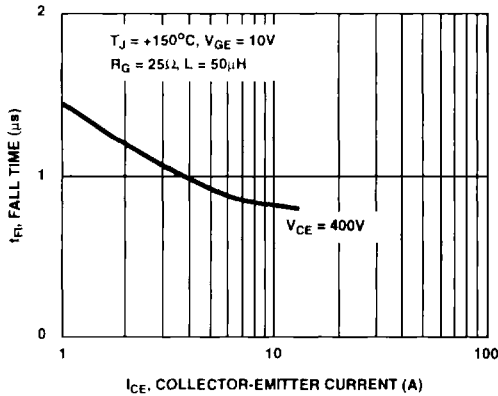


FIGURE 7. FALL TIME vs COLLECTOR-TO-EMITTER CURRENT (TYPICAL)

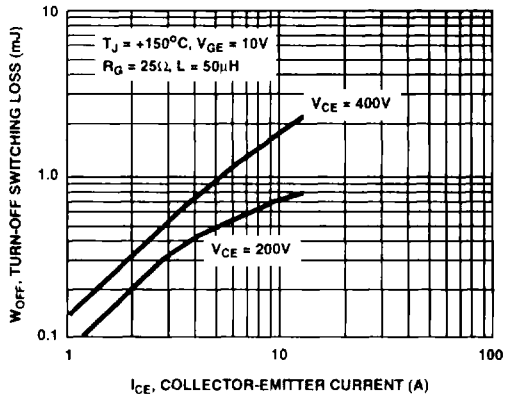
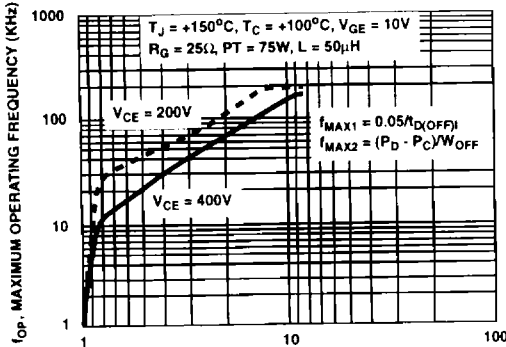


FIGURE 8. TURN-OFF SWITCHING LOSS vs COLLECTOR-EMITTER CURRENT (TYPICAL)

3
IGBTs

Typical Performance Curves (Continued)



NOTE:
 I_{CE} = COLLECTOR-EMITTER CURRENT (A)
 P_D = ALLOWABLE DISSIPATION P_C = CONDUCTION DISSIPATION

FIGURE 9. MAXIMUM OPERATING FREQUENCY vs COLLECTOR CURRENT AND VOLTAGE (TYPICAL)

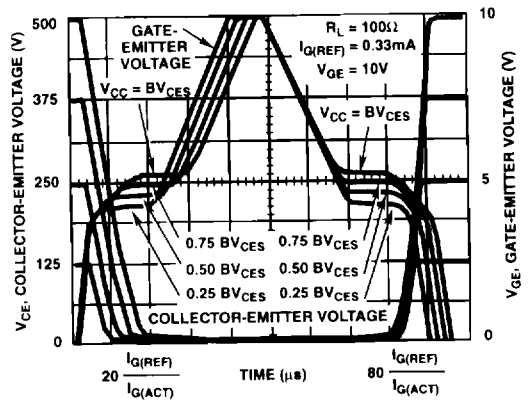


FIGURE 10. NORMALIZED SWITCHING WAVEFORMS AT CONSTANT GATE CURRENT

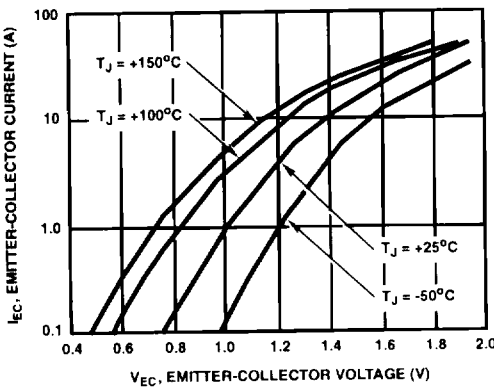


FIGURE 11. TYPICAL FORWARD VOLTAGE

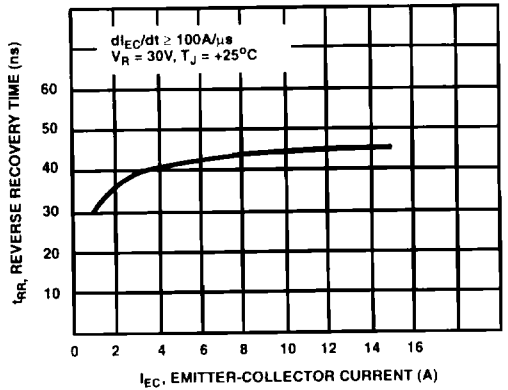


FIGURE 12. TYPICAL REVERSE RECOVERY TIME

Test Circuit

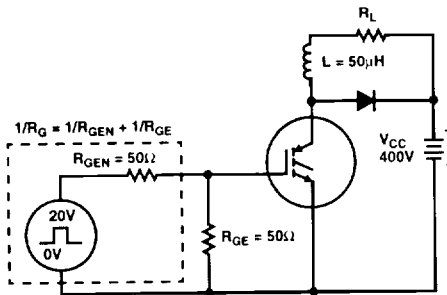


FIGURE 13. INDUCTIVE SWITCHING TEST CIRCUIT