

## SRAM Nonvolatile Controller Unit

### Features

- ▶ Power monitoring and switching for 3-volt battery-backup applications
- ▶ Write-protect control
- ▶ 3-volt primary cell inputs
- ▶ Less than 10ns chip-enable propagation delay
- ▶ 5% or 10% supply operation

### General Description

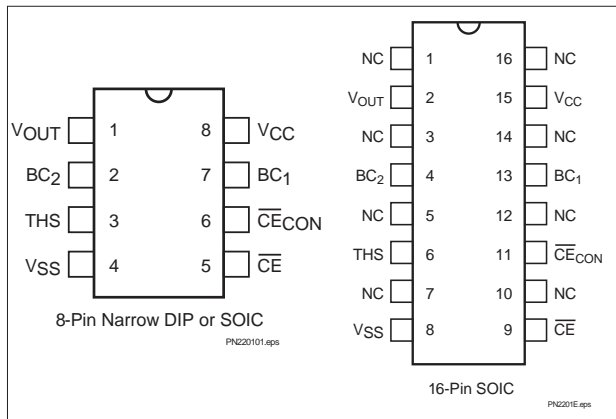
The CMOS bq2201 SRAM Nonvolatile Controller Unit provides all necessary functions for converting a standard CMOS SRAM into nonvolatile read/write memory.

A precision comparator monitors the 5V  $V_{CC}$  input for an out-of-tolerance condition. When out of tolerance is detected, a conditioned chip-enable output is forced inactive to write-protect any standard CMOS SRAM.

During a power failure, the external SRAM is switched from the  $V_{CC}$  supply to one of two 3V backup supplies. On a subsequent power-up, the SRAM is write-protected until a power-valid condition exists.

The bq2201 is footprint- and timing-compatible with industry standards with the added benefit of a chip-enable propagation delay of less than 10ns.

### Pin Connections



### Pin Names

$V_{OUT}$	Supply output
$BC_1$ — $BC_2$	3-volt primary backup cell inputs
THS	Threshold select input
$\overline{CE}$	chip-enable active low input
$\overline{CE}_{CON}$	Conditioned chip-enable output
$V_{CC}$	+5-volt supply input
$V_{SS}$	Ground
NC	No Connect

### Functional Description

An external CMOS static RAM can be battery-backed using the  $V_{OUT}$  and the conditioned chip-enable output pin from the bq2201. As  $V_{CC}$  slews down during a power failure, the conditioned chip-enable output  $\overline{CE}_{CON}$  is forced inactive independent of the chip-enable input  $\overline{CE}$ .

This activity unconditionally write-protects external SRAM as  $V_{CC}$  falls to an out-of-tolerance threshold  $V_{PFD}$ .  $V_{PFD}$  is selected by the threshold select input pin, THS.

If THS is tied to  $V_{SS}$ , power-fail detection occurs at 4.62V typical for 5% supply operation. If THS is tied to  $V_{CC}$ , power-fail detection occurs at 4.37V typical for 10% supply operation. The THS pin must be tied to  $V_{SS}$  or  $V_{CC}$  for proper operation.

If a memory access is in process during power-fail detection, that memory cycle continues to completion before the memory is write-protected. If the memory cycle is not terminated within time  $t_{WPT}$ , the  $\overline{CE}_{CON}$  output is unconditionally driven high, write-protecting the memory.

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As the supply continues to fall past  $V_{PFD}$ , an internal switching device forces  $V_{OUT}$  to one of the two external backup energy sources.  $\overline{CE}_{CON}$  is held high by the  $V_{OUT}$  energy source.

During power-up,  $V_{OUT}$  is switched back to the  $V_{CC}$  supply as  $V_{CC}$  rises above the backup cell input voltage sourcing  $V_{OUT}$ . The  $\overline{CE}_{CON}$  output is held inactive for time  $t_{CER}$  (120 ms maximum) after the supply has reached  $V_{PFD}$ , independent of the  $\overline{CE}$  input, to allow for processor stabilization.

During power-valid operation, the  $\overline{CE}$  input is fed through to the  $\overline{CE}_{CON}$  output with a propagation delay of less than 10ns. Nonvolatility is achieved by hardware hookup, as shown in Figure 1.

## Energy Cell Inputs—BC<sub>1</sub>, BC<sub>2</sub>

Two primary backup energy source inputs are provided on the bq2201. The BC<sub>1</sub> and BC<sub>2</sub> inputs accept a 3V primary battery, typically some type of lithium chemistry. If no primary cell is to be used on either BC<sub>1</sub> or BC<sub>2</sub>, the unused input should be tied to  $V_{SS}$ .

If both inputs are used, during power failure the  $V_{OUT}$  output is fed only by BC<sub>1</sub> as long as it is greater than 2.5V. If the voltage at BC<sub>1</sub> falls below 2.5V, an internal isolation switch automatically switches  $V_{OUT}$  from BC<sub>1</sub> to BC<sub>2</sub>.

To prevent battery drain when there is no valid data to retain,  $V_{OUT}$  and  $\overline{CE}_{CON}$  are internally isolated from BC<sub>1</sub> and BC<sub>2</sub> by either of the following:

- Initial connection of a battery to BC<sub>1</sub> or BC<sub>2</sub>, or
- Presentation of an isolation signal on  $\overline{CE}$ .

A valid isolation signal requires  $\overline{CE}$  low as  $V_{CC}$  crosses both  $V_{PFD}$  and  $V_{SO}$  during a power-down. See Figure 2. Between these two points in time,  $\overline{CE}$  must be brought to the point of  $(0.48 \text{ to } 0.52) \cdot V_{CC}$  and held for at least 700ns. The isolation signal is invalid if  $\overline{CE}$  exceeds  $0.54 \cdot V_{CC}$  at any point between  $V_{CC}$  crossing  $V_{PFD}$  and  $V_{SO}$ .

The appropriate battery is connected to  $V_{OUT}$  and  $\overline{CE}_{CON}$  immediately on subsequent application and removal of  $V_{CC}$ .

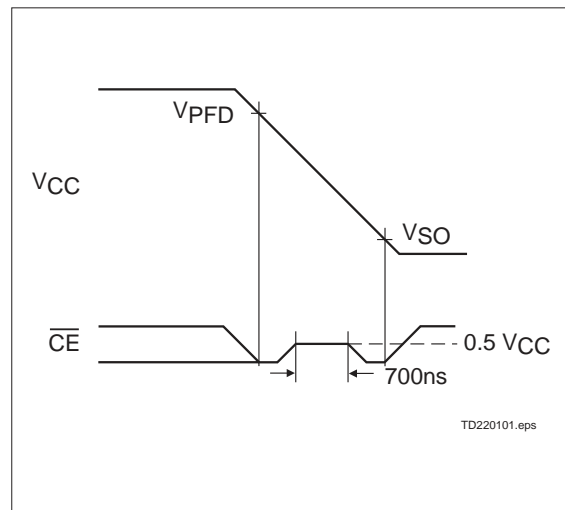


Figure 2. Battery Isolation Signal

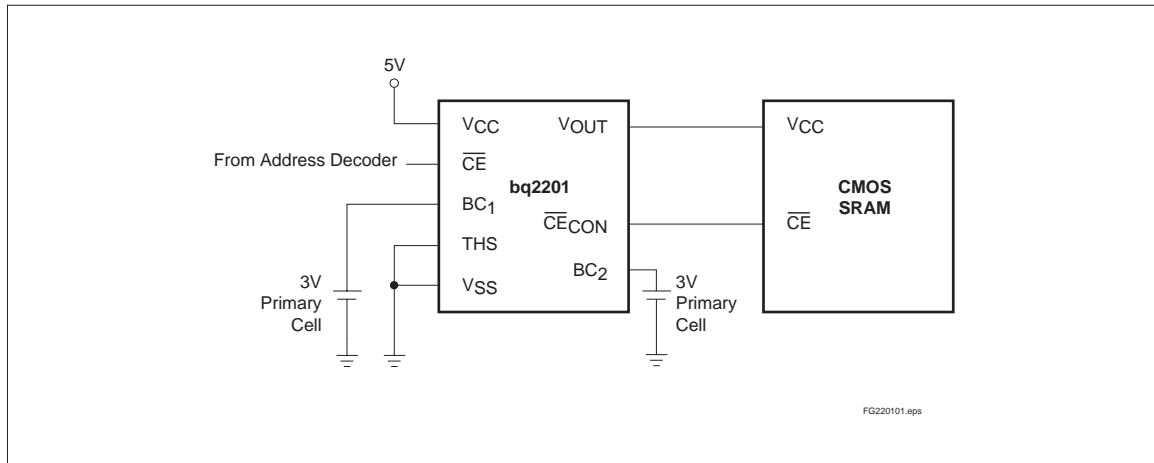


Figure 1. Hardware Hookup (5% Supply Operation)

## Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V <sub>CC</sub>	DC voltage applied on V <sub>CC</sub> relative to V <sub>SS</sub>	-0.3 to 7.0	V	
V <sub>T</sub>	DC voltage applied on any pin excluding V <sub>CC</sub> relative to V <sub>SS</sub>	-0.3 to 7.0	V	V <sub>T</sub> ≤ V <sub>CC</sub> + 0.3
T <sub>OPR</sub>	Operating temperature	0 to +70	°C	Commercial
		-40 to +85	°C	Industrial "N"
T <sub>STG</sub>	Storage temperature	-55 to +125	°C	
T <sub>BIAS</sub>	Temperature under bias	-40 to +85	°C	
T <sub>SOLDER</sub>	Soldering temperature	260	°C	For 10 seconds
I <sub>OUT</sub>	V <sub>OUT</sub> current	200	mA	

**Note:** Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

## Recommended DC Operating Conditions (T<sub>A</sub> = T<sub>OPR</sub>)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V <sub>CC</sub>	Supply voltage	4.75	5.0	5.5	V	THS = V <sub>SS</sub>
		4.50	5.0	5.5	V	THS = V <sub>CC</sub>
V <sub>SS</sub>	Supply voltage	0	0	0	V	
V <sub>IL</sub>	Input low voltage	-0.3	-	0.8	V	
V <sub>IH</sub>	Input high voltage	2.2	-	V <sub>CC</sub> + 0.3	V	
V <sub>BC1</sub> , V <sub>BC2</sub>	Backup cell voltage	2.0	-	4.0	V	
THS	Threshold select	-0.3	-	V <sub>CC</sub> + 0.3	V	

**Note:** Typical values indicate operation at T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5V or V<sub>BC</sub>.

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## DC Electrical Characteristics ( $T_A = T_{OPR}$ , $V_{CC} = 5V \pm 10\%$ )

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
$I_{LI}$	Input leakage current	-	-	$\pm 1$	$\mu A$	$V_{IN} = V_{SS}$ to $V_{CC}$
$V_{OH}$	Output high voltage	2.4	-	-	V	$I_{OH} = -2.0mA$
$V_{OHB}$	$V_{OH}$ , BC supply	$V_{BC} - 0.3$	-	-	V	$V_{BC} > V_{CC}$ , $I_{OH} = -10\mu A$
$V_{OL}$	Output low voltage	-	-	0.4	V	$I_{OL} = 4.0mA$
$I_{CC}$	Operating supply current	-	3	5	mA	No load on $V_{OUT}$ and $\overline{CE}_{CON}$ .
$V_{PFD}$	Power-fail detect voltage	4.55	4.62	4.75	V	$THS = V_{SS}$
		4.30	4.37	4.50	V	$THS = V_{CC}$
$V_{SO}$	Supply switch-over voltage	-	$V_{BC}$	-	V	
$I_{CCDR}$	Data-retention mode current	-	-	100	nA	$V_{OUT}$ data-retention current to additional memory not included.
$V_{OUT1}$	$V_{OUT}$ voltage	$V_{CC} - 0.2$	-	-	V	$V_{CC} > V_{BC}$ , $I_{OUT} = 100mA$
		$V_{CC} - 0.3$	-	-	V	$V_{CC} > V_{BC}$ , $I_{OUT} = 160mA$
$V_{OUT2}$	$V_{OUT}$ voltage	$V_{BC} - 0.3$	-	-	V	$V_{CC} < V_{BC}$ , $I_{OUT} = 100\mu A$
$V_{BC}$	Active backup cell voltage	-	$V_{BC2}$	-	V	$V_{BC1} < 2.5V$
		-	$V_{BC1}$	-	V	$V_{BC1} > 2.5V$
$I_{OUT1}$	$V_{OUT}$ current	-	-	160	mA	$V_{OUT} > V_{CC} - 0.3V$
$I_{OUT2}$	$V_{OUT}$ current	-	100	-	$\mu A$	$V_{OUT} > V_{BC} - 0.2V$

**Note:** Typical values indicate operation at  $T_A = 25^\circ C$ ,  $V_{CC} = 5V$  or  $V_{BC}$ .

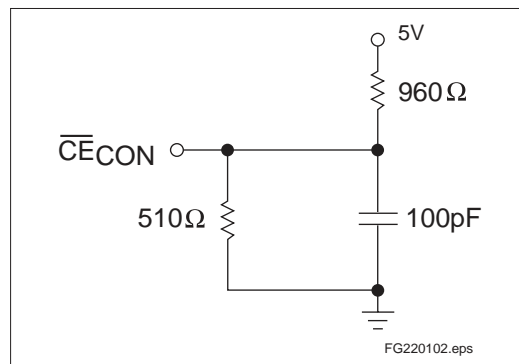
**Capacitance** ( $T_A = 25^\circ\text{C}$ ,  $F = 1\text{MHz}$ ,  $V_{CC} = 5.0\text{V}$ )

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
$C_{IN}$	Input capacitance	-	-	8	pF	Input voltage = 0V
$C_{OUT}$	Output capacitance	-	-	10	pF	Output voltage = 0V

**Note:** This parameter is sampled and not 100% tested.

**AC Test Conditions**

Parameter	Test Conditions
Input pulse levels	0V to 3.0V
Input rise and fall times	5ns
Input and output timing reference levels	1.5V (unless otherwise specified)
Output load (including scope and jig)	See Figure 3



**Figure 3. Output Load**

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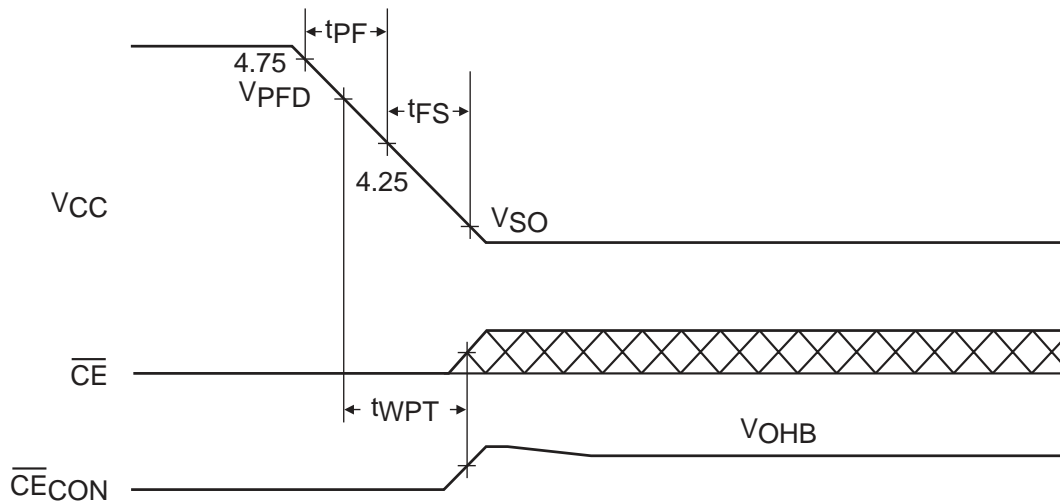
## Power-Fail Control ( $T_A = T_{OPR}$ )

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
$t_{PF}$	$V_{CC}$ slew, 4.75V to 4.25V	300	-	-	$\mu s$	
$t_{FS}$	$V_{CC}$ slew, 4.25V to $V_{SO}$	10	-	-	$\mu s$	
$t_{PU}$	$V_{CC}$ slew, 4.25V to 4.75V	0	-	-	$\mu s$	
$t_{CED}$	Chip-enable propagation delay	-	7	10	ns	
$t_{CER}$	Chip-enable recovery	40	80	120	ms	Time during which SRAM is write-protected after $V_{CC}$ passes $V_{PFD}$ on power-up.
$t_{WPT}$	Write-protect time	40	100	150	$\mu s$	Delay after $V_{CC}$ slews down past $V_{PFD}$ before SRAM is write-protected.

**Note:** Typical values indicate operation at  $T_A = 25^\circ C$ .

**Caution:** Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.

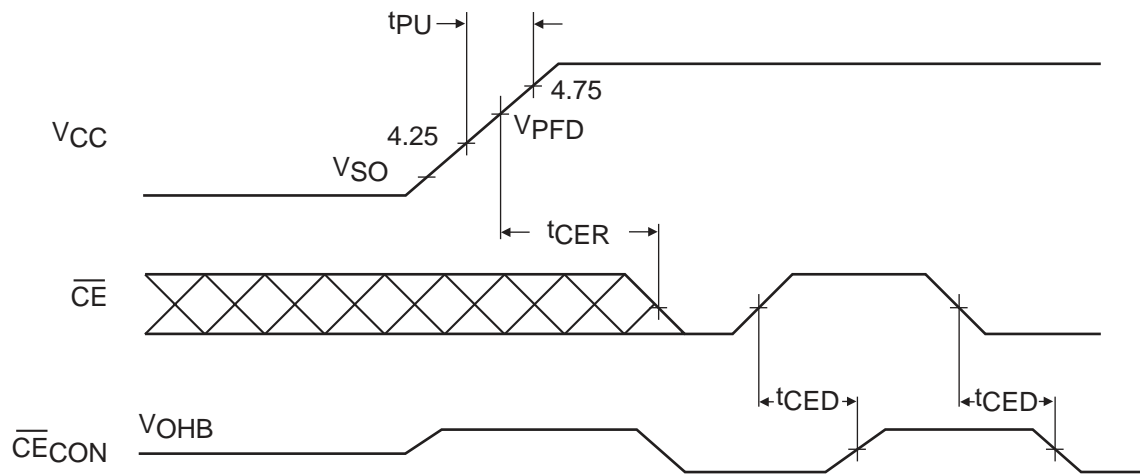
## Power-Down Timing



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Oct. 1998 D

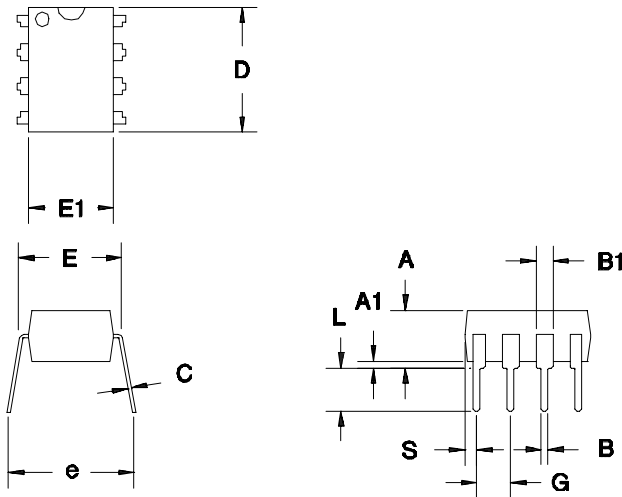
### Power-Up Timing



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## 8-Pin DIP Narrow (PN)

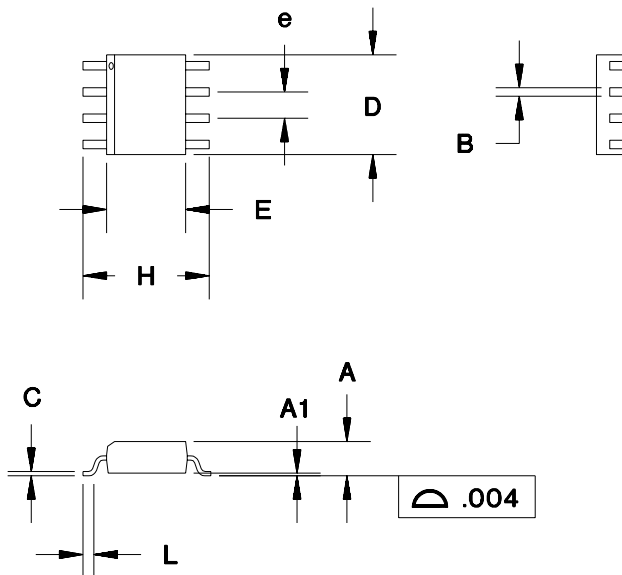


### 8-Pin DIP Narrow (PN)

Dimension	Minimum	Maximum
A	0.160	0.180
A1	0.015	0.040
B	0.015	0.022
B1	0.055	0.065
C	0.008	0.013
D	0.350	0.380
E	0.300	0.325
E1	0.230	0.280
e	0.300	0.370
G	0.090	0.110
L	0.115	0.150
S	0.020	0.040

All dimensions are in inches.

## 8-Pin SOIC Narrow (SN)



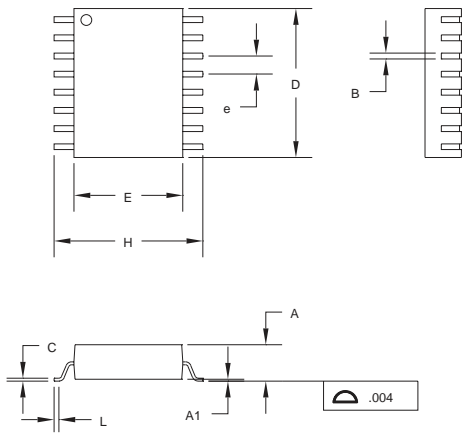
### 8-Pin SOIC Narrow (SN)

Dimension	Minimum	Maximum
A	0.060	0.070
A1	0.004	0.010
B	0.013	0.020
C	0.007	0.010
D	0.185	0.200
E	0.150	0.160
e	0.045	0.055
H	0.225	0.245
L	0.015	0.035

All dimensions are in inches.



**S: 16-Pin SOIC**



**16-Pin S (SOIC)**

Dimension	Minimum	Maximum
A	0.095	0.105
A1	0.004	0.012
B	0.013	0.020
C	0.008	0.013
D	0.400	0.415
E	0.290	0.305
e	0.045	0.055
H	0.395	0.415
L	0.020	0.040

All dimensions are in inches.

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## Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
1		Added industrial temperature range	
2	1, 3, 4	10% supply operation	Was: THS tied to $V_{OUT}$ Is: THS tied to $V_{CC}$
3	1, 9, 11	Added 16-pin package option	

**Note:** Change 1 = Sept. 1991 B changes from Sept. 1990 A.  
Change 2 = Aug. 1997 C changes from Sept. 1991 B.  
Change 3 = Oct. 1998 D changes from Aug. 1997 C.

## Ordering Information

**bq2201**

**Temperature Range:**

blank = Commercial (0 to +70°C)

N = Industrial (-40 to +85°C)

**Package Option:**

PN = 8-pin narrow plastic DIP



SN = 8-pin narrow SOIC

S = 16-pin SOIC

**Device:**

bq2201 Nonvolatile SRAM Controller

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ2201SN-N	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2201 -N	
BQ2201SN-NTR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2201 -N	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

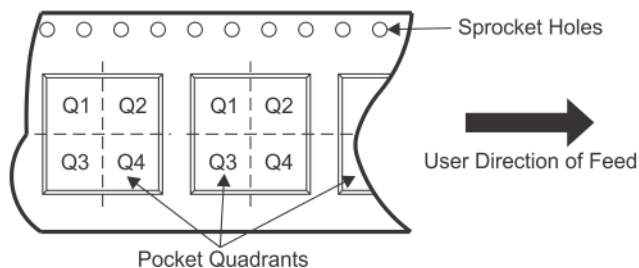
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ2201SN-NTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ2201SN-NTR	SOIC	D	8	2500	367.0	367.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
BQ2201SN-N	D	SOIC	8	75	506.6	8	3940	4.32



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